Hi3516C V300 Professional HD IP Camera SoC

Data Sheet

Issue 00B03

Date 2016-09-28

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About This Document

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module of Hi3516C V300. This document also describes the interface timings and related parameters in diagrams. In addition, this document describes the pins, pin usages, performance parameters, and package dimension of Hi3516C V300 in detail.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3516C	V300

Intended Audience

This document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 DANGER	Indicates a hazard with a high level of risk which, if not avoided, will result in death or serious injury.

Symbol	Description
 WARNING	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
 CAUTION	Indicates a potentially hazardous situation, which if not avoided, could result in equipment damage, data loss, performance degradation, or unexpected results.
TIP	Indicates a tip that may help you solve a problem or save time.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

General Conventions

The general conventions that may be found in this document are defined as follows.

Convention	Description
Times New Roman	Normal paragraphs are in Times New Roman.
Boldface	Names of files, directories, folders, and users are in **boldface**. For example, log in as user **root**.
Italic	Book titles are in *italics*.
`Courier New`	Examples of information displayed on the screen are in `Courier New`.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Content	Description
–	The cell is blank.
*	The content in this cell is configurable.

Notes

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description	Symbol	Description
RO	The register is read-only.	RW	The register is read/write.
RC	The register is cleared on a read.	WC	The register can be read. The register is cleared when 1 is written. The register keeps unchanged when 0 is written.

Reset Value Conventions

In the register definition tables:

- If the reset value (for the Reset row) of a bit is "?", the reset value is undefined.
- If the reset values of one or multiple bits are "?", the total reset value of a register is undefined and is marked as "-".

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity (such as the RAM capacity)	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0xFE04, 0x18	Address or data in hexadecimal
0b	0b000, 0b00 00000000	Data or sequence in binary (register description is excluded.)
X	00X, 1XX	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and 1XX indicates 100, 101, 110, or 111.

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B03 (2016-09-28)

This issue is the third draft release, which incorporates the following changes:

Chapter 1 Product Description

Section 1.3.10 is modified.

Chapter 2 Hardware

In section 2.3.3, table 2-6 is modified.

Chapter 3 System

In section 3.10.2.4, PWR_CTRL0 is modified.

Chapter 9 Video Interfaces

Section 9.1.2 is modified.

Chapter 10 ISP

Section 10.1, section 10.2, and section 10.4 are modified.

Chapter 11 Audio Interfaces

Section 11.2.1 is modified.

In section 11.2.5, AUDIO_ANA_CTRL_1 is modified.

Issue 00B02 (2016-08-25)

This issue is the second draft release, which incorporates the following changes:

Chapter 2 Hardware

Section 2.3.3 and section 2.5.2 are modified.

Section 2.5.3.2, table 2-29 is modified.

Section 2.5.10, table 2-38 is modified.

Chapter 3 System

In section 3.2.7, PERI_CRG_PLL1, PERI_CRG_PLL5, and PERI_CRG_PLL9 are modified.

Section 3.8.3, section 3.8.4, and section 3.10.7 are modified.

In section 3.10.2, PWR_STATUS is modified.

Chapter 5 ETH

In section 5.6.1, MDIO_RWCTRL is modified.

Chapter 10 ISP

In section 10.6, the description of the ISP_DCG_MODE register is modified.

Appendix A Ordering Information

Ordering information is added.

Issue 00B01 (2016-07-27)

This issue is the first draft release.

Contents

Figures

Tables

1 Product Description

1.1 Description

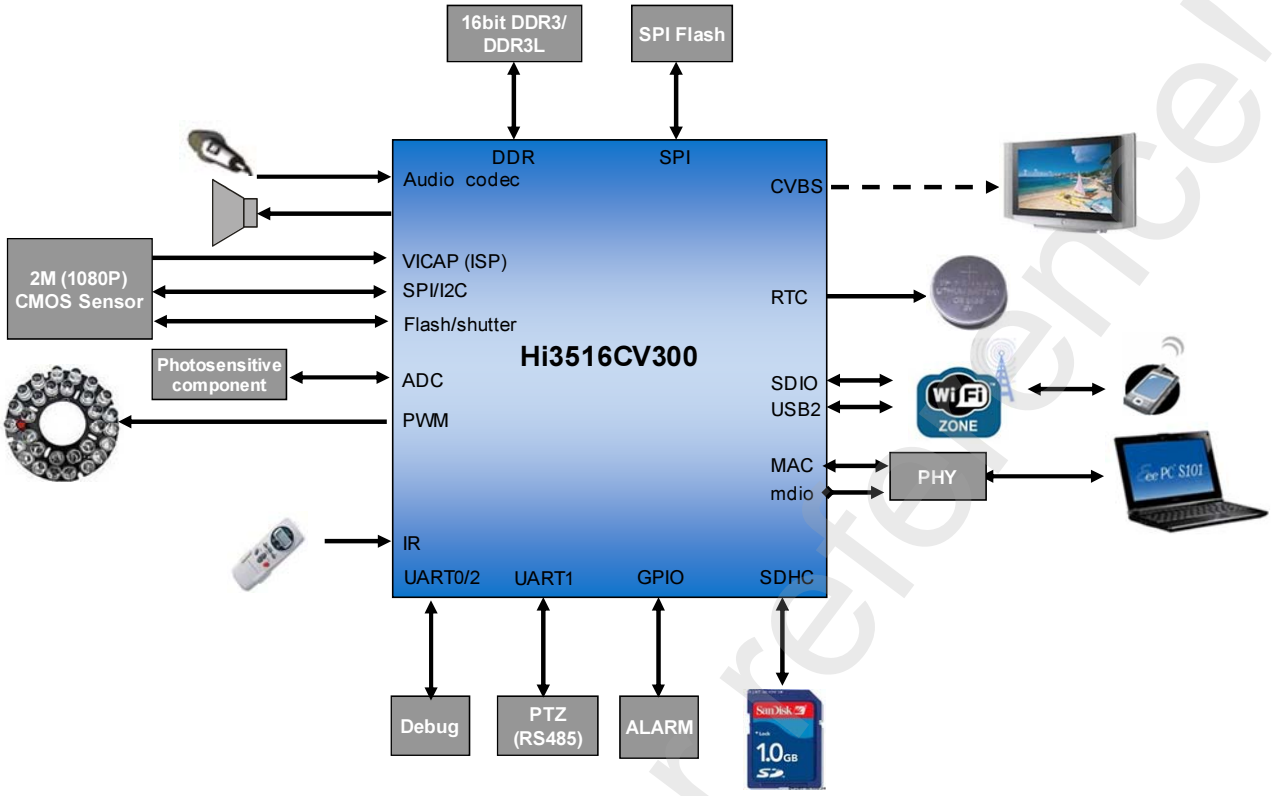
Hi3516C V300 is a new-generation SoC designed for the industry-dedicated HD IP camera. It has an integrated new-generation ISP and the latest H.265 video compression encoder in the industry. It uses the advanced low-power technology and architecture design. All of these features enable Hi3516C V300 to lead the industry in the low bit rate, high profile, and low power consumption. Hi3516C V300 integrates the POR, RTC, audio CODEC, and standby wakeup circuit, which significantly reduces customers' EBOM cost. In addition, the interface design similar to that of other HiSilicon DVR and NVR chips facilitate development and mass production of customer's products.

1.2 Application Scenarios

1.2.1 Hi3516C V300 HD IP Camera Solution

Figure 1-1 shows the typical application scenario of the Hi3516C V300.

Figure 1-1 Application block diagram of Hi3516C V300

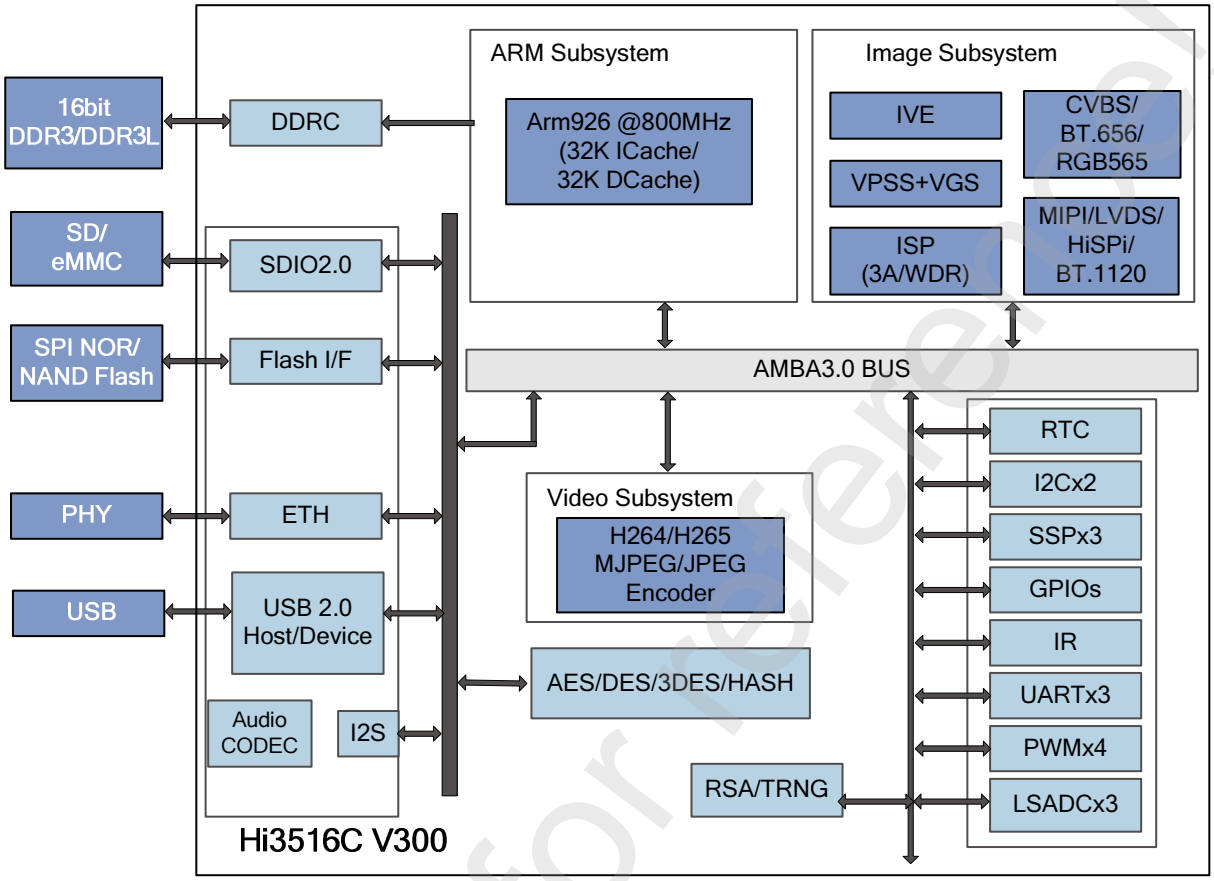


1.3 Architecture

1.3.1 Overview

Figure 1-2 shows the logic block diagram of the Hi3516C V300.

Figure 1-2 Logic block diagram of the Hi3516C V300



1.3.2 Processor Core

ARM926@800 MHz with 32 KB I-cache and 32 KB D-cache

1.3.3 Video Encoding

- H.264 BP/MP/HP
- H.265 Main Profile
- MJPEG/JPEG baseline

1.3.4 Video Encoding Performance

- Maximum 2-megapixel resolution for H.264/H.265 encoding
- Real-time multi-stream H.264/H.265 encoding capabilities
  - 1920x1080@45 fps
  - 1920x1080@30 fps+720x480@30 fps+360x240@30 fps
- JPEG snapshot at 2 megapixels@5 fps
- CBR/VBR control, ranging from 16 kbit/s to 30 Mbit/s
- Encoding frame rate ranging from 1/16 fps to 60 fps
- Encoding of eight ROIs

1.3.5 Intelligent Video Analysis

Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis.

1.3.6 Video and Graphics Processing

- 3DNR, image enhancement, and DCI
- Anti-flicker for output videos and graphics
- 1/15x to 16x video and graphic scaling
- Overlaying of video and graphics
- Picture rotation by 90°, 180° or 270°
- Picture mirroring and flipping
- OSD overlaying of eight regions before encoding

1.3.7 ISP

- 3A (AE, AF, and AWB) function. The third-party 3A algorithms are supported.
- FPN removal and DPC
- LSC, LDC, and purple edge correction
- Direction-adaptive demosaic
- Gamma correction, DCI, and color management and enhancement
- Adaptive region de-fog
- Multi-level NR (BayerNR and 3DNR) and sharpening enhancement
- Local tone mapping
- Sensor built-in WDR and 2F WDR (line-base/frame-base/DCG)
- DIS
- ISP tuning tools for the PC

1.3.8 Audio Encoding/Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, G.726, and ADPCM protocols
- Audio 3A functions (AEC, ANR, and AGC)

1.3.9 Security Engine

- Various encryption and decryption algorithms implemented by using hardware, including AES, DES, 3DES, and RSA
- HASH (SHA1/SHA256/HMAC_SHA/HMAC_SHA256) algorithms implemented by using hardware
- Integrated 512-bit OTP storage space and random number generator

1.3.10 Video Interfaces

- VI interfaces
  - 8-/10-/12-/14-bit RGB Bayer DC timing VI

  - BT.601, BT.656, and BT.1120 VI interfaces
  - MIPI, LVDS/sub-LVDS, and HiSPi
  - Compatibility with mainstream HD CMOS sensors provided by Sony, ON, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
  - Maximum input resolution of 2048 x 2048, up to 198 megapixels/s
- VO interfaces
  - One PAL/NTSC output for automatic load detection
  - One BT.656 VO interface
  - 6-bit RGB565 serial LCD output

1.3.11 Audio Interfaces

- Integrated audio CODEC supporting 16-bit audio inputs and outputs
- Mono-channel differential MIC inputs for reducing the background noises
- Single-ended dual-channel input
- I^2S interface for connecting to the external audio CODEC

1.3.12 Peripheral Interfaces

- POR
- One integrated high-precision RTC
- Integrated 3-channel LSADC
- Three UART interfaces (including one 4-wire interface)
- IR, I^2C, SPI, and GPIO interfaces
- Four PWM interfaces
- Two SDIO 2.0 interfaces, supporting the 3.3 V level and 1.8 V level
- One USB 2.0 host/device port
- RMII in 10/100 Mbit/s full-duplex or half-duplex mode, TSO network acceleration, and PHY clock output

1.3.13 External Memory Interfaces

- SDRAM interface

  16-bit DDR3/DDR3L interface with the maximum capacity of 4 Gbits
- SPI NOR flash interface
  - 1-/2-/4-wire mode
  - Maximum capacity of 32 MB
- SPI NAND flash interface with maximum 4 Gbits capacity
- SD card interface supporting the maximum capacity of 2 TB
- eMMC 4.5 interface with 4-bit data width

1.3.14 SDK

- Linux-3.18-based SDK
- High-performance H.264 PC decoding library
- High-performance H.265 PC/Android/iOS decoding library

1.3.15 Physical Specifications

- Power consumption
  - 1080p30, typical power consumption of 550 mW
  - Deep standby wakeup
- Operating voltages
  - 0.9 V core voltage
  - 3.3 V±10% I/O voltage
  - 1.35 V or 1.5 V DDR3/3L SDRAM interface voltage
- Package

  Body size of 12 mm x 12 mm (0.47 in. x 0.47 in.), 0.65 mm (0.03 in.) ball pitch, TFBGA RoHS package with 273 pins

1.4 Boot and Upgrade Modes

The mode that the chip enters after boot is determined by the latch values of the BOOT_SEL1, BOOT_SEL0, and UPDATE_MODE signals during POR. Table 1-1 is the truth table.

Table 1-1 Boot modes

UPDATE_MODE	BOOT_SEL1	BOOT_SEL0	Boot Mode
1	0	0	The chip boots from an off-chip SPI NAND/NOR flash memory.
1	0	1	The chip boots from the off-chip eMMC storage space.
1	1	0	The chip enters the fastboot mode. For details, see section 1.4.3 "Fastboot Mode."
1	1	1	
0	x	x	The chip enters the mode of upgrading the U-boot program by using the SD card or USB port.

NOTE

- BOOT_SEL1 signal is multiplexed with the external pin MDCK.
- BOOT_SEL0 signal is multiplexed with the external pin EPHY_RSTN.
- UPDATE_MODE signal is multiplexed with the external pin GPIO0_3.

- If the chip enters the mode of upgrading the U-boot program by using the SD card or USB port, do not connect the HiBurn by using the serial port.

1.4.1 Booting from an Off-Chip SPI NAND/NOR Flash Memory

When the chip boots from an SPI flash memory, the externally connected memory is the SPI NAND/NOR flash. The pull-up and pull-down levels of BOOT_SEL1 and BOOT_SEL0 need to be configured to select the boot medium. When BOOT_SEL1 and BOOT_SEL0 are 0, the chip boots from the SPI NAND/NOR flash connected to the SFC interface.

When the chip boots from the SPI NAND/NOR flash, the latch values of SFC_DEVICE_MODE and SFC_BOOT_MODE during POR need to be configured based on the boot medium, as shown in Table 1-2.

Table 1-2 Mapping between signal values and SPI flash boot modes

SFC_DEVICE_MODE	SFC_BOOT_MODE	SPI Flash Boot Mode
0	0	SPI NOR flash, 3-byte address mode
0	1	SPI NOR flash, 4-byte address mode
1	0	SPI NAND flash, 1-line boot mode
1	1	SPI NAND flash, 4-line boot mode

NOTE

- SFC_DEVICE_MODE signal is multiplexed with the external pin SENSOR_RSTN.
- SFC_ BOOT_MODE signal is multiplexed with the external pin SFC_CLK.

1.4.2 Booting from the off-chip eMMC

When the chip boots from the eMMC, the externally connected memory is an eMMC. In this case, the pull-up and pull-down levels of BOOT_SEL1 (multiplexed with the external pin MDCK) and BOOT_SEL0 (multiplexed with the external pin EPHY_RSTN) need to be configured to select the boot medium. When BOOT_SEL1 is 0 and BOOT_SEL0 is 1, the chip can boot from the eMMC connected to the eMMC interface.

NOTE

Hi3516C V300 supports only the 4-bit eMMC mode.

1.4.3 Fastboot Mode

When the fastboot mode is used, the serial port communication mechanism will be started. The communication between the serial port and the related software running on the PC is set up, and then the boot program is downloaded. By then the boot process is complete (for details, see the *HiBurn User Guide*). If the serial port communication times out during the fastboot process, check the value of BOOT_SEL0 and do as follows:

- When BOOT_SEL0 is 0, the chip jumps to and boots from the off-chip SPI NAND/NOR flash.
- When BOOT_SEL0 is 1, the chip jumps to and boots from the off-chip eMMC storage space.

1.4.4 Upgrading the U-boot Program by Using the SD Card or USB Port

If UPDATE_MODE is 0, the chip enters the mode of upgrading the U-boot program by using the SD card or USB port after being powered on. That is, the chip can upgrade the U-boot program in the SPI flash (when BOOT_SEL0 is 0) or eMMC (when BOOT_SEL0 is 1) by using the SD card or USB port.

NOTE

If Hi3516C V300 uses the mode of upgrading the U-boot program by using the SD card, it can only use the SD card on the SDIO0 interface.

1.5 Address Space Mapping

Table 1-3 describes the address space mapping.

Table 1-3 Address space mapping

Start Address	End Address	Function	Size	Description
0x0000_0000	0x03FF_FFFF	During remapping: deassert the start address space; after remapping: point to the on-chip RAM	64 MB	-
0x0400_0000	0x0400_FFFF	BOOTROM address space	64 KB	The actual capacity of the BOOTROM is 32 KB.
0x0401_0000	0x0401_FFFF	Address space of the on-chip RAM	64 KB	The actual capacity of the BOOTROM is 32 KB.
0x0402_0000	0x0FFF_FFFF	Reserved	-	-
0x1000_0000	0x1000_FFFF	FMC register	64 KB	-
0x1001_0000	0x1002_FFFF	Reserved	-	-
0x1003_0000	0x1003_FFFF	DMAC register	64 KB	-
0x1004_0000	0x1004_FFFF	VIC register	64 KB	-
0x1005_0000	0x1005_FFFF	ETH register	64 KB	-
0x1006_0000	0x1007_FFFF	Reserved	-	-
0x1008_0000	0x1008_FFFF	Cipher register	64 KB	-
0x1009_0000	0x1009_FFFF	HASH register	64 KB	-
0x100A_0000	0x100B_FFFF	Reserved	-	-
0x100C_0000	0x100C_FFFF	MMC0 register	64 KB	-
0x100D_0000	0x100D_FFFF	MMC1 register	64 KB	-
0x100E_0000	0x100E_FFFF	MMC2 register	64 KB	-

Start Address	End Address	Function	Size	Description
0x100F_0000	0x100F_0000	MMC3 register	64 KB	-
0x1010_0000	0x1010_FFFF	Reserved	-	-
0x1011_0000	0x1011_FFFF	Host OHCI register	64 KB	-
0x1012_0000	0x1012_FFFF	Host EHCI register	64 KB	-
0x1013_0000	0x1013_FFFF	USB 2.0 device register	64 KB	-
0x1014_0000	0x111F_FFFF	Reserved	-	-
0x1120_0000	0x1120_FFFF	DDRT register	64 KB	-
0x1121_0000	0x1121_FFFF	GZIP register	64 KB	-
0x1122_0000	0x1122_FFFF	JPGE register	64 KB	-
0x1123_0000	0x1123_FFFF	IVE register	64 KB	-
0x1124_0000	0x1124_FFFF	VGS register	64 KB	-
0x1125_0000	0x1125_FFFF	VPSS register	64 KB	-
0x1126_0000	0x1126_FFFF	VEDU register	64 KB	-
0x1127_0000	0x112F_FFFF	Reserved	-	-
0x1130_0000	0x1130_FFFF	MIPI register	64 KB	-
0x1131_0000	0x1131_FFFF	AIAO register	64 KB	-
0x1132_0000	0x1132_FFFF	Audio codec register	-	-
0x1133_0000	0x1137_FFFF	Reserved	-	-
0x1138_0000	0x113E_FFFF	VICAP register	448 KB	-
0x113F_0000	0x113F_FFFF	Reserved	-	-
0x1140_0000	0x1140_FFFF	VDP register	64 KB	-
0x1141_0000	0x11FF_FFFF	Reserved	-	-
0x1200_0000	0x1200_0FFF	Timer0/Timer1 register	4 KB	-
0x1200_1000	0x1200_1FFF	Timer2/Timer3 register	4 KB	-
0x1200_2000	0x1200_FFFF	Reserved	-	-
0x1201_0000	0x1201_FFFF	CRG register	64 KB	-
0x1202_0000	0x1202_FFFF	System control register	64 KB	-
0x1203_0000	0x1203_FFFF	Peripheral control register	64 KB	-
0x1204_0000	0x1204_07FF	I/O multiplexing register	2 KB	-
0x1204_0800	0x1204_0FFF	I/O control register	2 KB	-
0x1205_0000	0x1205_FFFF	Reserved	-	-

Start Address	End Address	Function	Size	Description
0x1206_0000	0x1206_FFFF	MDDRC register	64 KB	-
0x1207_0000	0x1207_7FFF	OTP key control register	32 KB	-
0x1207_8000	0x1207_FFFF	Reserved	32 KB	-
0x1208_0000	0x1208_FFFF	WDG register	64 KB	-
0x1209_0000	0x1209_7FFF	RTC register	32 KB	-
0x1209_8000	0x1209_FFFF	Power control register	32 KB	-
0x120A_0000	0x120A_FFFF	EFUSE_USER_IF register	-	-
0x120B_0000	0x120B_7FFF	RSA register	32 KB	-
0x120B_8000	0x120B_FFFF	KLAD register	32 KB	-
0x120C_0000	0x120C_FFFF	TRNG register	64 KB	-
0x120D_0000	0x120D_FFFF	Reserved	64 KB	-
0x120E_0000	0x120E_FFFF	LSADC register	64 KB	-
0x120F_0000	0x120F_FFFF	IR register	-	-
0x1210_0000	0x1210_0FFF	UART0 register	4 KB	-
0x1210_1000	0x1210_1FFF	UART1 register	4 KB	-
0x1210_2000	0x1210_2FFF	UART2 register	4 KB	-
0x1210_3000	0x1210_FFFF	Reserved	-	-
0x1211_0000	0x1211_0FFF	I^2C0 register	4 KB	-
0x1211_2000	0x1211_2FFF	I^2C1 register	4 KB	-
0x1211_3000	0x1211_FFFF	Reserved	-	-
0x1212_0000	0x1212_0FFF	SSP0 register	4 KB	-
0x1212_1000	0x1212_1FFF	SSP1 register	4 KB	-
0x1212_2000	0x1212_2FFF	3-line SPI register	4 KB	-
0x1212_3000	0x1212_FFFF	Reserved	-	-
0x1213_0000	0x1213_FFFF	PWM register	64 KB	-
0x1214_0000	0x1214_0FFF	GPIO0 register	4 KB	-
0x1214_1000	0x1214_1FFF	GPIO1 register	4 KB	-
0x1214_2000	0x1214_2FFF	GPIO2 register	4 KB	-
0x1214_3000	0x1214_3FFF	GPIO3 register	4 KB	-
0x1214_4000	0x1214_4FFF	GPIO4 register	4 KB	-
0x1214_5000	0x1214_5FFF	GPIO5 register	4 KB	-

Start Address	End Address	Function	Size	Description
0x1214_6000	0x1214_6FFF	GPIO6 register	4 KB	-
0x1214_7000	0x1214_7FFF	GPIO7 register	4 KB	-
0x1214_8000	0x1214_8FFF	GPIO8 register	4 KB	-
0x1214_9000	0x13FF_FFFF	Reserved	-	-
0x1400_0000	0x14FF_FFFF	FMC storage space	16 MB	-
0x1500_0000	0x3FFF_FFFF	Reserved	-	-
0x8000_0000	0x9FFF_FFFF	DDR storage space	512 MB	-
0x5000_0000	0xFFFF_FFFF	Reserved	-	-

Contents

Figures

Tables

2 Hardware

2.1 Package and Pinout

2.1.1 Package

Hi3516C V300 uses the thin & fine ball grid array (TFBGA) package. It has 273 pins, its body size is 12 mm x 12 mm (0.47 in. x 0.47 in.), and its ball pitch is 0.65 mm (0.03 in.). Figure 2-1 to Figure 2-4 show package views. Figure 2-5 shows package dimensions.

Figure 2-1 Top view

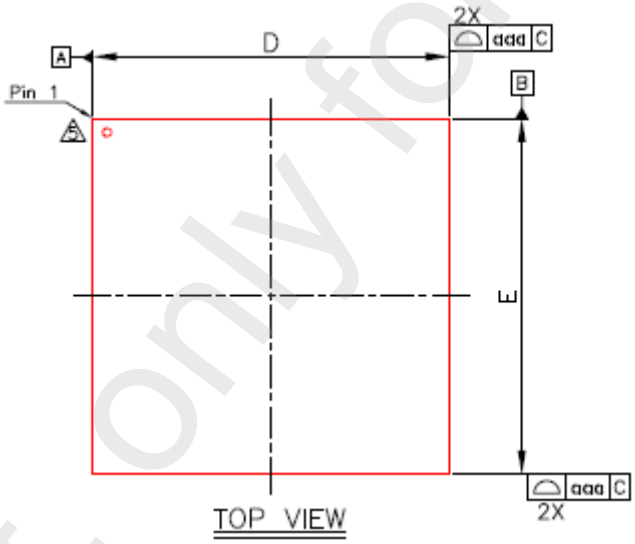


Figure 2-2 Bottom view

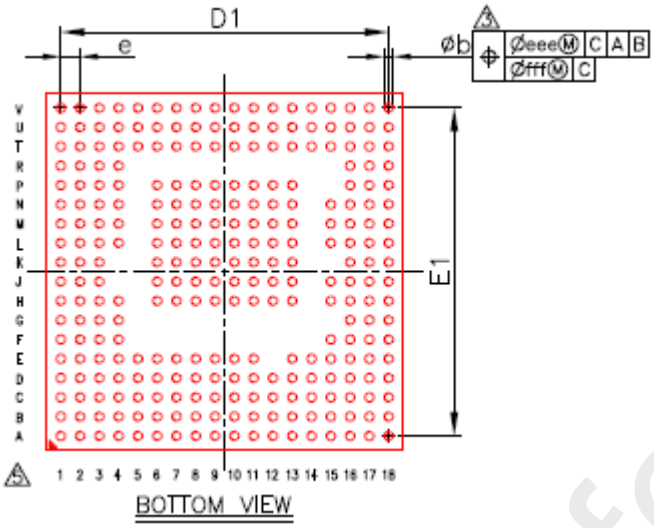


Figure 2-3 Side view

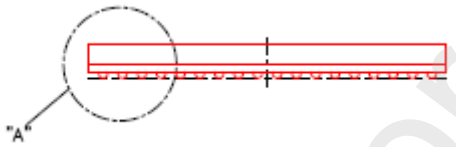


Figure 2-4 Enlarged view of detail "A"

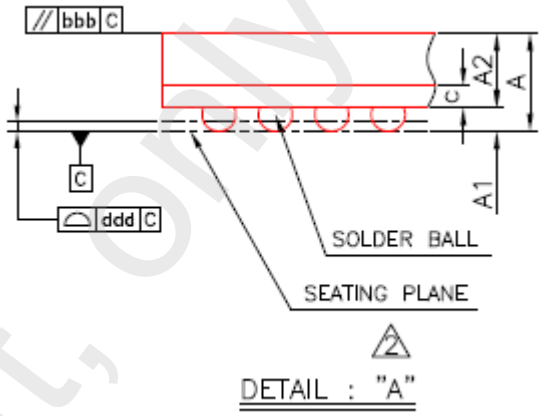


Figure 2-5 Package dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	11.05	---	---	0.435	---
E1	---	11.05	---	---	0.435	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	18 / 18					

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
6. REFERENCE DOCUMENT : JEDC PUBLICATION 95 DESIGN GUIDE 4.5

2.1.2 Pinout

Hi3516C V300 has 273 pins. Table 2-1 lists the pin quantity of Hi3516C V300 by type.

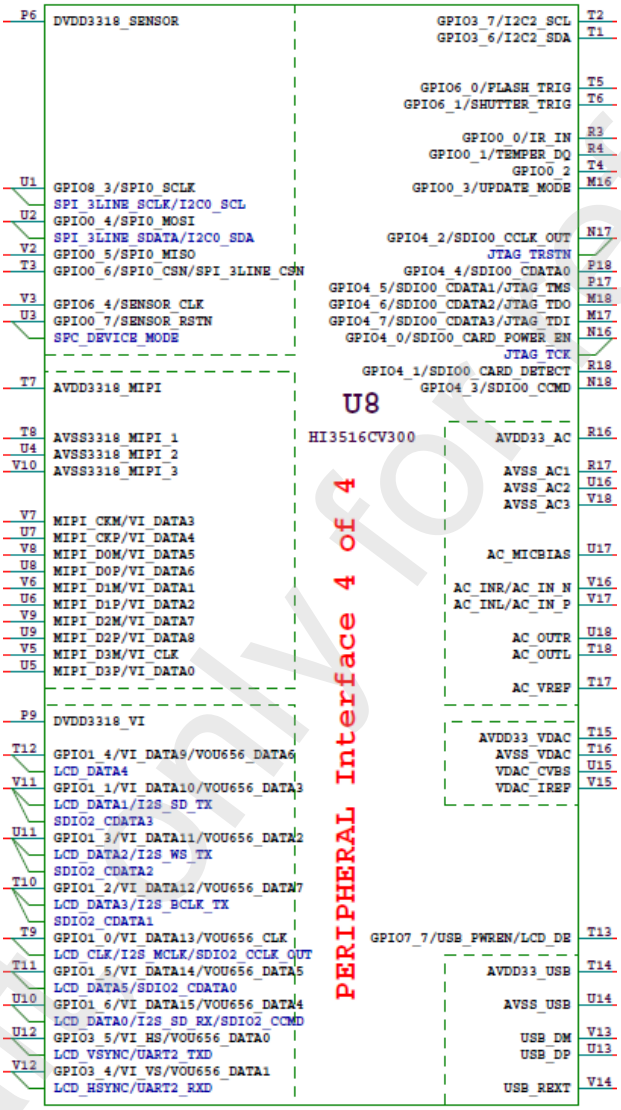
Table 2-1 Pin quantity

Pin Type	Quantity
I/O	151
Digital power	21
Digital GND	69
Others/Analog power	18
Others/Analog GND	12
NC	2
Total	273

2.2 Pin Description

- For details about the pin description and default states of digital pins, see the *HI3516C V300_PINOUT_EN*.
- For details about the distribution of power domains corresponding to the pins, see the schematic diagram of the demo board. In the Hi3516C V300 SYMBOL, the pins in the same dashed box belong to the same power domain. As shown in Figure 2-6, the SENSOR_CLK pin, SPI0 pin, and the power pin DVDD3318_SENSOR are in the same power domain.

Figure 2-6 Part of the Hi3516C V300 SYMBOL



2.3 Electrical Specifications

2.3.1 Power Consumption Parameters

Table 2-2 describes power consumption parameters.

CAUTION

- The values of power consumption parameters are provided based on typical application scenarios.
- The maximum values are the tested maximum average power consumption within a specific time period, and cannot reflect the transient maximum power consumption when the system is working. Therefore, design board power supplies by following the *Hi3516C V300 Hardware Design User Guide*.

Table 2-2 Power consumption parameters

Symbol	Parameter	Typ	Max	Unit
0.9 V power	Power consumption of the VDD core power domain	TBD	TBD	mW
3.3 V power	Power consumption of the 3.3 V I/O interface	TBD	TBD	mW
1.8 V power	Power consumption of the 1.8 V I/O interface	TBD	TBD	mW
1.5 V power	Power consumption of the DDR interface	TBD	TBD	mW

NOTE

The typical scenario of Hi3516C V300 is as follows: 1080p@30 fps+D1@30 fps+CIF@30 fps+1080p@1 fps snapshot.

2.3.2 Temperature and Thermal Resistance Parameters

Table 2-3 describes temperature and thermal resistance parameters.

NOTE

- The thermal resistance is provided in compliance with the JEDEC JESD51 series of standards. The actual system design and environment may be different.
  - ✓ For details about θ_{JA}, see the JEDEC Standard No.51-2.
  - ✓ For details about θ_{JB}, see the JEDEC Standard No.51-8.
  - ✓ For details about θ_{JC}, see the following standards:
    - *MIL-STD-883 1012.1 Thermal characteristics*
    - *SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages*

- The chip junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.
- The chip can be stored in the sealed packaging bag for up to 12 months when the temperature is below 40ºC (104ºF) and the relative humidity (RH) is below 90%.
- After the packaging bag is opened, the following conditions must be met before the component is used in the reflow soldering process or other high-temperature processes:

  a. The process is complete within 168 hours at 30ºC (86ºF) or lower and at most 60% RH.

  b. The component is stored at the RH lower than 10%.
- The soldering temperature curve is based on the J-STD-020D.1 standard.

Table 2-3 Operating environment parameters

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_A	0	70	ºC

CAUTION

- The maximum value of the rated junction temperature for the Hi3516C V300 is TBD. The chip junction temperature cannot be greater than this value in any condition. The Hi3516C V300 may be physically damaged when the parameter values in the rated working environment are exceeded.
- The maximum value of the long-term junction temperature for the Hi3516C V300 is TBD. The chip junction temperature should be less than this value in normal working conditions.
- In the short-term working condition (According to the GR-63-CORE standard, the definition is that the work duration does not exceed 96 hours each time and the accumulated annual working time does not exceed 15 days), the Hi3516C V300 can tolerate the high temperatures which are above TBD and below TBD. However, if the Hi3516C V300 works at the junction temperature above TBD for a long time, the chip life is shortened or the chip works unstably.

Table 2-4 lists the junction temperature parameters of the Hi3516C V300.

Table 2-4 Junction temperature parameters of the Hi3516C V300

Package	Maximum Power Consumption (W)	Lower Limit of the Junction Temperature for Normal Working (°C)	Maximum Junction Temperature for Long-Term Working (°C)	Upper Limit of the Junction Temperature for Short-Term Working (°C)	Maximum Destructive Junction Temperature (°C)	Life Cycle (Year)
TFBGA	TBD	TBD	TBD	TBD	TBD	TBD

Table 2-5 lists the thermal resistance parameters of Hi3516C V300.

Table 2-5 Thermal resistance parameters

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-ambient thermal resistance	θ_{JA}	-	29.8	-	℃/W
Junction-to-board thermal resistance	θ_{JB}	-	17.7	-	℃/W
Junction-to-case thermal resistance	θ_{JC}	-	12.1	-	℃/W

2.3.3 Operating Conditions

Table 2-6 and Table 2-7 describe operating conditions.

CAUTION

- The prerequisite for using the VDD voltage range (when SVB is used) is as follows: the customer's board must use the SVB circuit, and the impedance and capacitance parameters of the SVB circuit must completely copy the related RC parameters of Hi3516C V300 DMEB VER.A.
- For a specific chip and specific SVB circuit, the operating voltage value of the chip is a fixed value instead of a fluctuation range.

Table 2-6 Operating conditions for the SVB related power supply

Symbol	Description	Chip Voltage Range			Power Noise Vpp	Unit
		Min	Typ	Max	Max	
VDD	Internal core power (when SVB is not used)	TBD	0.9	TBD	TBD	V
	Internal core power (when SVB is used)	TBD	0.9	TBD	TBD	V
AVDD09_PLL	PLL core analog power (when SVB is not used)	TBD	0.9	TBD	TBD	V
	PLL core analog power (when SVB is used)	TBD	0.9	TBD	TBD	V

Table 2-7 Operating conditions for the power supply under normal voltage

Symbol	Description	Min	Typ	Max	Unit
DVDD33_1/2	I/O power	2.97	3.3	3.63	V

Symbol	Description	Min	Typ	Max	Unit
DVDD3318_VI	VI I/O power	1.62	1.8	1.98	V
	VI I/O power	2.97	3.3	3.63	V
DVDD3318_SENSOR	SENSOR, SPI0 I/O power	1.62	1.8	1.98	V
	SENSOR, SPI0 I/O power	2.97	3.3	3.63	V
DVDD3318_FLASH	SFC, I/O power	1.62	1.8	1.98	V
	SFC, I/O power	2.97	3.3	3.63	V
DVDD3318_RMII	RMII I/O power	1.62	1.8	1.98	V
	RMII I/O power	2.97	3.3	3.63	V
DVDD3318_UART1	UART1 I/O power	1.62	1.8	1.98	V
	UART1 I/O power	2.97	3.3	3.63	V
DVDD3318_PC	PC I/O power	1.62	1.8	1.98	V
	PC I/O power	2.97	3.3	3.63	V
DVDD3318_SARADC	LSADC I/O power	1.62	1.8	1.98	V
	LSADC I/O power	2.97	3.3	3.63	V
VDDIO_DDR	DDR3 interface power	1.425	1.5	1.575	V
	DDR3L interface power	1.323	1.35	1.425	V
VDDIO_CK_DDR	DDR3 clock interface power	1.425	1.5	1.575	V
	DDR3L clock interface power	1.323	1.35	1.425	V
AVDD_DDRPLL1/2	DDR3/3L PLL3.3 V analog power	2.97	3.3	3.63	V
AVDD33_PLL	PLL 3.3 V analog power	2.97	3.3	3.63	V
AVDD33_AC	Audio codec 3.3 V analog power	3	3.3	3.6	V
AVDD33_VDAC	VDAC 3.3 V analog power	2.97	3.3	3.63	V
AVDD33_USB	USB 3.3 V analog power	3	3.3	3.6	V
AVDD3318_MIPI	MIPI analog power	1.71	1.8	1.89	V

Symbol	Description	Min	Typ	Max	Unit
	3.3 V power when the MIPI signal is multiplexed as a single-ended digital signal	2.97	3.3	3.63	V
	1.8 V power when the MIPI signal is multiplexed as a single-ended digital signal	1.62	1.8	1.98	V
AVDD_BAT	RTC battery power	1.6	3.3	3.6	V
AVDD18_EFUSE	EFUSE 1.8 V analog power	1.71	1.8	1.89	V

2.3.4 Power-On and Power-Off Sequences

For details about power-on and power-off sequences, see section 1.2.5 "Requirements on the Power-on and Power-off Timing" in the *Hi3516C V300 Hardware Design User Guide*.

2.3.5 DC and AC Electrical Parameters

Table 2-8 and Table 2-9 describe direct current (DC) electrical specifications.

Table 2-8 DC electrical parameters (DVDD33_1/DVDD33_2/DVDD3318_VI/DVDD3318_SENSOR/DVDD3318_FLASH /DVDD3318_RMII/DVDD3318_UART1/DVDD3318_PC/DVDD3318_SARADC = 3.3 V, incompatible with the 5 V input)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD33_1/2	Interface voltage	2.97	3.3	3.63	V	-
V_{IH}	High-level input voltage	2.0	-	DVDD33_1/2 + 0.3	V	Incompatible with the 5 V input
V_{IL}	Low-level input voltage	–0.3	-	0.8	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	2.4	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.4	V	-
R_{PU1}	Internal pull-up resistor	17	19	21	kΩ	-
R_{PU2}	Internal pull-up resistor	18	20	22	kΩ	-

Symbol	Description	Min	Typ	Max	Unit	Remarks
R_{PU3}	Internal pull-up resistor	29	32	35	kΩ	-
R_{PU4}	Internal pull-up resistor	7	8	9	kΩ	-
R_{PD1}	Internal pull-down resistor	76	84	92	kΩ	-
R_{PD2}	Internal pull-down resistor	22	24	26	kΩ	-
R_{PD3}	Internal pull-down resistor	28	31	34	kΩ	-
R_{PD4}	Internal pull-down resistor	22	24	26	kΩ	-

Table 2-9 DC electrical parameters (DVDD3318_VI/DVDD3318_SENSOR/ DVDD3318_FLASH /DVDD3318_RMII/ DVDD3318_UART1/ DVDD3318_PC/ DVDD3318_SARADC=1.8 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
DVDD18	Interface voltage	1.62	1.8	1.98	V	-
V_{IH}	High-level input voltage	1.17	-	DVDD3318+0.3	V	-
V_{IL}	Low-level input voltage	–0.3	-	0.63	V	-
I_L	Input leakage current	-	-	±10	μA	-
I_{OZ}	Tristate output leakage current	-	-	±10	μA	-
V_{OH}	High-level output voltage	1.35	-	-	V	-
V_{OL}	Low-level output voltage	-	-	0.45	V	-
R_{PU1}	Internal pull-up resistor	39	43	47	kΩ	-
R_{PU2}	Internal pull-up resistor	40	44	48	kΩ	-
R_{PU3}	Internal pull-up resistor	32	36	40	kΩ	-
R_{PU4}	Internal pull-up resistor	7	8	9	kΩ	-
R_{PD1}	Internal pull-down resistor	212	236	260	kΩ	-
R_{PD2}	Internal pull-down resistor	50	56	62	kΩ	-
R_{PD3}	Internal pull-down resistor	77	86	95	kΩ	-
R_{PD4}	Internal pull-down resistor	46	51	56	kΩ	

Table 2-10 describes DC electrical parameters in DDR3 mode.

Table 2-10 DC electrical parameters in DDR3 mode (VDDIO_DDR = 1.5 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.425	1.5	1.575	V	-
Vref	Reference voltage	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	-	(0.49 to 0.51) x VDDIO_DDR
$V_{IH(DC)}$	High-level input voltage	Vref + 0.1	-	VDDIO_DDR + 0.3	V	-
$V_{IL(DC)}$	Low-level input voltage	–0.3	-	Vref − 0.1	V	-
V_{OH}	High-level output voltage	0.8 x VDDIO_DDR	-	(1 + 0.1) x VDDIO_DDR	V	The drive impedance is configurable.
V_{OL}	Low-level output voltage	0	-	0.2 x VDDIO_DDR	V	The drive impedance is configurable.
I_{OH}	High-level output current	-	10.50	10.83	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
I_{OL}	Low-level output current	-	10.50	10.83	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
Output impedance	-	34	-	80	Ω	-

Table 2-11 describes AC electrical parameters in DDR3 mode.

Table 2-11 AC electrical parameters in DDR3 mode (VDDIO_DDR = 1.5 V)

Symbol	Description	Min	Max	Unit	Remarks
$V_{IH(AC)}$	High-level input voltage	Vref + 0.15	VDDIO_DDR + 0.3	V	-
$V_{IL(AC)}$	Low-level input voltage	-	Vref − 0.15	V	-

Table 2-12 describes DC electrical parameters in DDR3L mode.

Table 2-12 DC electrical parameters in DDR3L mode (VDDIO_DDR =1.35 V)

Symbol	Description	Min	Typ	Max	Unit	Remarks
VDDIO_DDR	Interface voltage	1.283	1.35	1.45	V	-
VREF	Reference voltage of the DDR interface	0.49 x VDDIO_DDR	0.5 x VDDIO_DDR	0.51 x VDDIO_DDR	V	-
$V_{IH(DC)}$	High-level input voltage	0.49 x VDDIO_DDR + 0.125	-	VDDIO_DDR + 0.3	V	-
$V_{IL(DC)}$	Low-level input voltage	–0.3	-	0.51 x VDDIO_DDR -0.125	V	-
V_{OH}	High-level output voltage	VDDIO_DDR -0.28	-	-	V	-
V_{OL}	Low-level output voltage	-	-	VDDIO_DDR +0.28	V	-
I_{OH}	Low-level output current	-	9.42	9.85	mA	The DDR drive impedance is 34 Ω, and RTT is 60.
I_{OL}	Low-level output current	-	9.42	9.85	mA	The DDR drive impedance is 34 Ω, and RTT is 60.

Table 2-13 describes AC electrical parameters in DDR3L mode.

Table 2-13 AC electrical parameters in DDR3L mode (VDDIO_DDR = 1.35 V)

Symbol	Description	533−1600 Mbit/s		Unit	Remarks
		Min	Max		
$V_{IH(AC)}$	AC high-level input voltage	0.49 x VDDIO_DDR + 0.25	N/A	V	N/A
$V_{IL(AC)}$	AC low-level input voltage	N/A	0.51 x VDDIO_DDR– 0.25	V	N/A

2.3.6 MIPI/LVDS RX Electrical Parameters

Table 2-14 describes low-voltage differential signaling (LVDS) differential DC electrical parameters.

Table 2-14 LVDS differential DC electrical parameters

Symbol	Description		Min	Typ	Max	Unit
VIDTH (SL)	Differential input threshold voltage (VP-VM)	Sub-LVDS	–70	-	70	mV
VIDTH (HS)		HiSPi	–70	-	70	
VIDTH(HiVCM)		HiSPi(HiVCM)	–100		100	
VIDTH (DP)		D-PHY HS	–70	-	70	
VIDTH (LV)		LVDS	–100	-	100	
VIDTH (ML)		Mini-LVDS	–100	-	100	
VCM (SL)	Common mode voltage range (VP+VM)/2	Sub-LVDS	0.5	0.9	1.3	V
VCM (HS)		HiSPi(SLVS)	0.07	0.2	0.35	
VCM(HiVCM)		HiSPi(HiVCM)	0.66	0.90	1.17	
VCM (DP)		D-PHY HS	0.07	0.2	0.33	
VCM (LV)		LVDS	0.925	1.2	1.475	
VCM (ML)		Mini-LVDS	1.025	1.2	1.375	
VISVR (SL)	Single-ended input voltage range VP, VM	Sub-LVDS	0.4	-	1.4	V
VCM (HS)		HiSPi	-0.165	-	0.575	
VCM (DP)		D-PHY HS	-0.04	-	0.46	
VCM (LV)		LVDS	0	-	1.8	
VCM (ML)		Mini-LVDS	0.825	-	1.575	
ZID (SL)	Internal termination resister value	Sub-LVDS	80	100	120	Ω
ZID (HS)		HiSPi			125	
ZID (LV)		LVDS			120	
ZID (ML)		Mini-LVDS			120	
ZID (DP)		D-PHY HS			125	

Table 2-15 to Table 2-17 describe the MIPI parameters.

Table 2-15 MIPI high-speed (HS) DC parameters

Symbol	Description	Min	Typ	Max	Unit
VTERM-EN	Single-ended threshold for HS termination enable	-	-	450	mV

Table 2-16 MIPI HS AC parameters

Symbol	Description	Min	Typ	Max	Unit
ΔVCMRX (HF)	Common-mode interface beyond 450 MHz	-	-	100	-
ΔVCMRX (LF)	Common-mode interface 50−450 MHz	–50	-	50	mV
CCM	Common-mode termination	-	-	60	pF

Table 2-17 MIPI low-power (LP) DC parameters

Symbol	Description	Min	Typ	Max	Unit
VIHLP	Logic 1 input voltage	880	-	-	mV
VILLP	Logic 0 input voltage	-	-	550	
VHYST	Input hysteresis	25	-	-	

2.3.7 Audio CODEC Electrical Parameters

Table 2-18 to Table 2-22 describe the electrical parameters of the audio CODEC.

Table 2-18 Overall specifications

Description	Min	Typ	Max	Unit	Remarks
Analog circuit power AVDD33_AC	3	3.3	3.6	V	Relative to AVSS_AC
AC_VREF	-	AVDD33_AC /2	-	V	Relative to AVSS_AC

Table 2-19 Major DAC specifications

Description	Min	Typ	Max	Unit	Remarks
Output amplitude at full scale	-	0.875	-	Vrms	Maximum output signal swing

Table 2-20 Major ADC specifications

Description	Min	Typ	Max	Unit	Remarks
Maximum input amplitude	-	1	-	Vrms	Maximum input signal swing of the ADC

Table 2-21 Major MICBIAS specifications

Description	Min	Typ	Max	Unit	Remarks
Bias voltage	-	2.1 x AVDD33_AC/3.3	-	V	MIC bias voltage
Maximum output current	-	-	3	mA	-

Table 2-22 Major MICPGA specifications

Description	Min	Typ	Max	Unit	Remarks
Input voltage range	-	1	-	Vrms	Maximum input signal swing
Input impedance	-	10	12	kΩ	MICPGA input impedance

2.4 PCB Design Recommendations

For details about printed circuit board (PCB) design recommendations, see the *Hi3516C V300 Hardware Design User Guide*.

2.5 Interface Timings

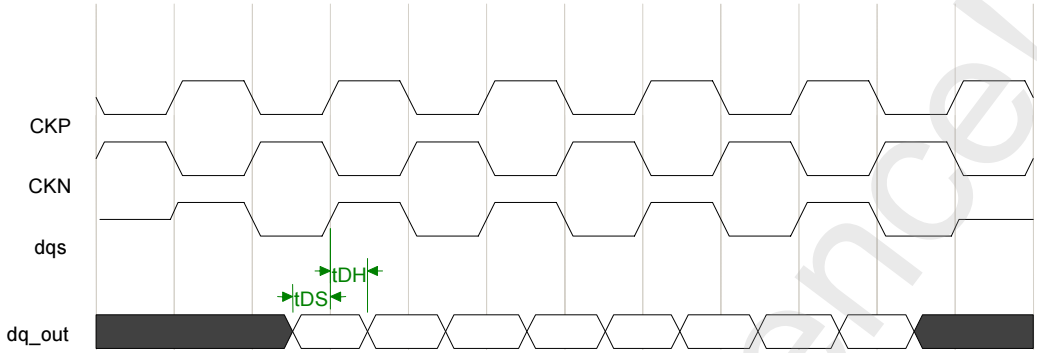
2.5.1 DDR Interface Timings

2.5.1.1 Write Timings

Write Timings of dqs_out Relative to dq_out

In the write timing of dqs_out relative to dq_out, the major parameters are tDS and tDH.

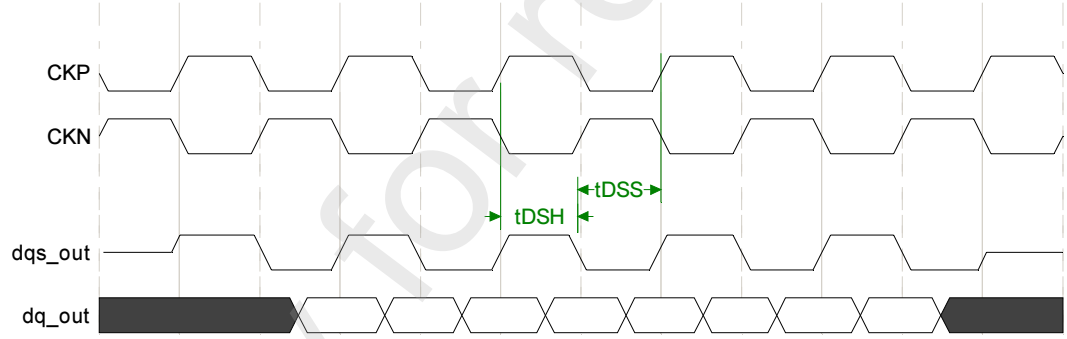
Figure 2-7 Write timing of dqs_out relative to dq_out for the DDR3



Write Timings of dqs_out Relative to CK

Figure 2-8 shows the write timing of dqs_out relative to CK for the DDR3.

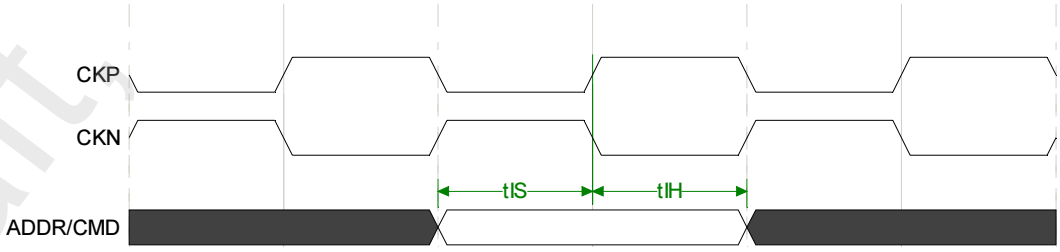
Figure 2-8 Write timing of dqs_out relative to CK for the DDR3



Write Timing of CMD/ADDR Relative to CK

Figure 2-9 shows the write timing of CMD/ADDR relative to CK.

Figure 2-9 Write timing of CMD/ADDR relative to CK



2.5.1.2 Read Timings

Read Timing of CMD/ADDR Relative to CK

The read timing of CMD/ADDR relative to CK is the same as the "Write Timing of CMD/ADDR Relative to CK".

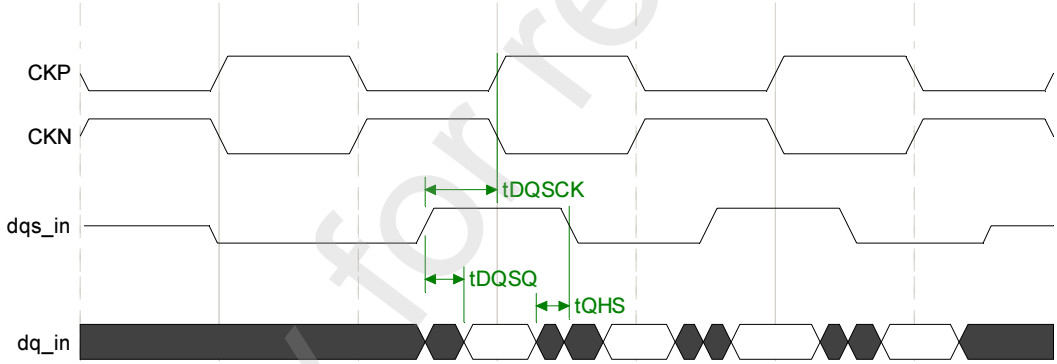
Read Timings of dqs_in Relative to dq_in

The read timings of dqs_in relative to dq_in are classified into the DDR3 SDRAM output timing, dqs_in timing on the DDR PHY side, and dq_in timing on the DDR PHY side.

For the DDR3 SDRAM output timing, the phases of DQS and CK are the same in the ideal condition; however, there is a tDQSCK skew between DQS and CK. The value of tDQSCK is 0.35 ns. tDQSQ is the jitter of the last valid DQ relative to DQS and its value is 0.2 ns; tQHS is the jitter of the first valid DQ relative to DQS and its value is 0.3 ns.

Figure 2-10 shows the output timing of the DDR3 SDRAM.

Figure 2-10 Output timing of the DDR3 SDRAM



2.5.1.3 Timing Parameters

The timings of the DDR interface comply with the JEDEC standards including JESD79 -3B standards. All the timings in this document are output on the DDR PHY side.

Table 2-23 describe the parameters of the DDR3-1600 SDRAM.

Table 2-23 Parameters of the DDR3-1600 SDRAM

Parameter	Symbol	Typ	Unit
Setup time, DQS falling edge to DDR clock	tDSS	0.18	tCK
Hold time, DQS falling edge to DDR clock	tDSH	0.18	tCK
Setup time, DQ/DM to DQS	tDS	0.010	ns
Hold time, DQ/DM to DQS	tDH	0.045	ns
Skew between DQS and DQ	tDQSQ	0.100	ns
Setup time, ADDR/CMD to DDR clock	tIS	0.170	ns

Parameter	Symbol	Typ	Unit
Hold time, ADDR/CMD to DDR clock	tIH	0.120	ns
Skew of DQS (output) to DDR clock	tDQSCK	0.225	ns

2.5.2 SFC Interface Timings

Figure 2-11 shows the SFC-SDR input timing.

Figure 2-11 SFC input timing (in SDR mode)

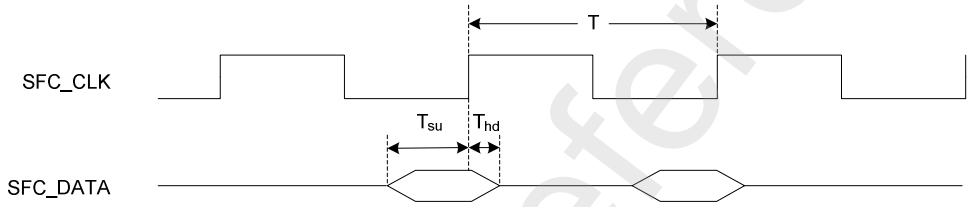


Table 2-24 describes the parameters of the SFC-SDR input timing.

Table 2-24 Parameters of the SFC-SDR input timing

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK (SDR mode)	T_{clk}	13.47	-	83.2	ns
Input signal setup time	T_{su}	2	-	-	ns
Input signal hold time	T_{hd}	1.2	-	-	ns

Figure 2-12 shows the SFC-SDR output timing.

Figure 2-12 SFC output timing (in SDR mode)

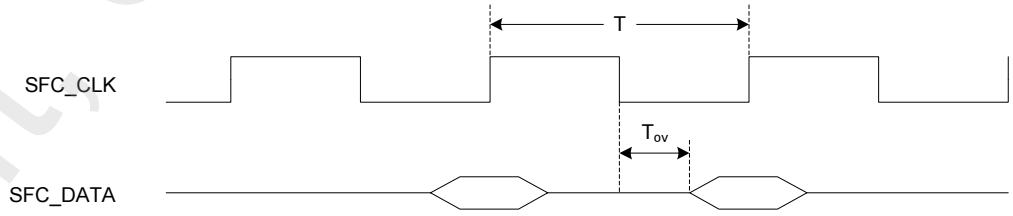


Table 2-25 describes the parameters of the SFC-SDR output timing.

Table 2-25 Parameters of the SFC-SDR output timing

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK (SDR)	T	13.47	-	83.2	ns
Output data signal delay	T_{ov}	-3	-	3	ns
Output CS signal delay	T_{ov}	-3	-	3	ns

Figure 2-13 shows the SFC-DDR input timing.

Figure 2-13 SFC input timing (in DDR mode)

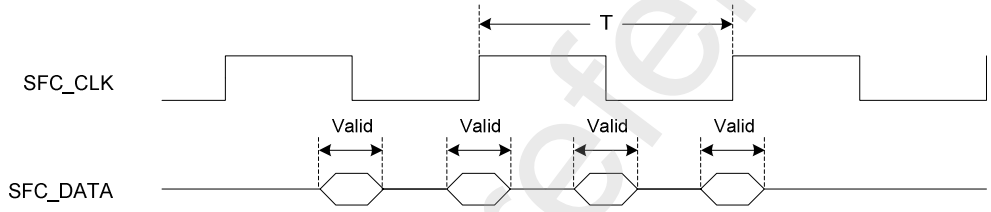


Table 2-26 describes the parameters of the SFC-DDR input timing.

Table 2-26 Parameters of the SFC-DDR input timing

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFC_CLK (DDR)	T_{clk}	13.47	-	83.2	ns
Valid time of the input signal	Valid	3	-	-	ns
Duty cycle of the input clock	Duty	56%	-	-	%

Figure 2-14 shows the SFC-DDR output timing.

Figure 2-14 SFC output timing (in DDR mode)

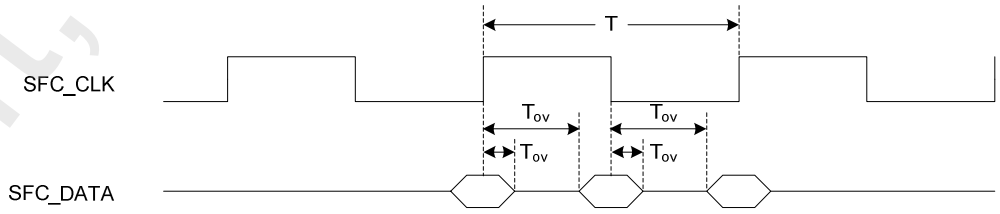


Table 2-27 describes the parameters of the SFC-DDR output timing.

Table 2-27 Parameters of the SFC-DDR output timing

Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle of SFCCLK (DDR)	T	13.47	-	83.2	ns
Output data signal delay	T_{ov}	1.25	-	3/8*T	ns
Output CS signal delay	T_{ov}	1.25	-	3/8*T	ns

2.5.3 Ethernet MAC Interface Timings

2.5.3.1 RMII Timings

Figure 2-15 shows the 100 Mbit/s RX timing of the RMII.

Figure 2-15 100 Mbit/s RX timing of the RMII

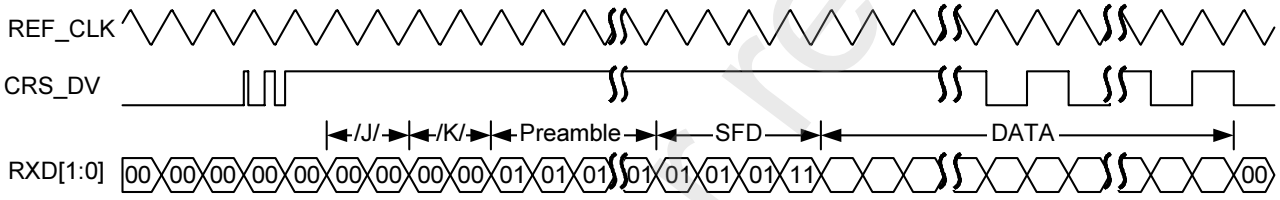


Figure 2-16 shows the 100 Mbit/s TX timing of the RMII.

Figure 2-16 100 Mbit/s TX timing of the RMII

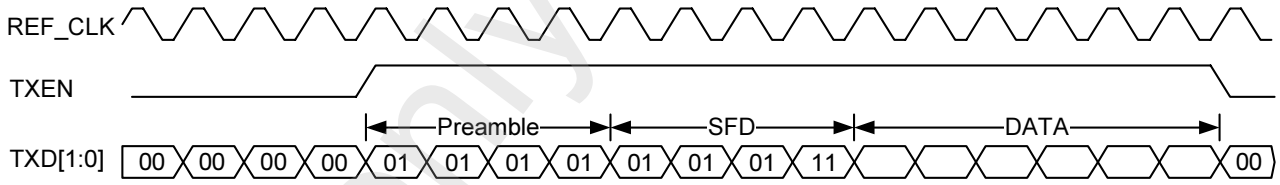


Figure 2-17 shows the 10 Mbit/s RX timing of the RMII.

Figure 2-17 10 Mbit/s RX timing of the RMII

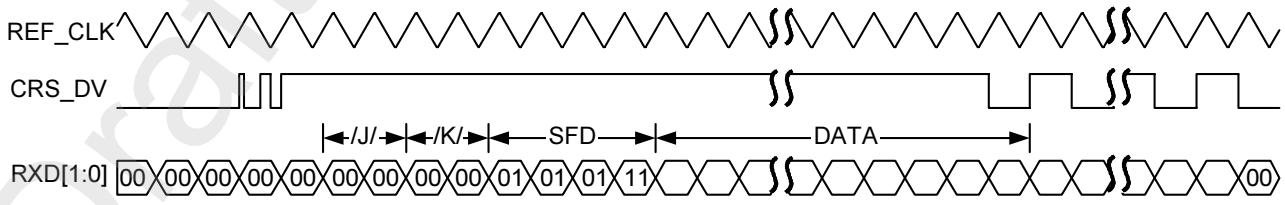


Figure 2-18 shows the 10 Mbit/s TX timing of the RMII.

Figure 2-18 10 Mbit/s TX timing of the RMII

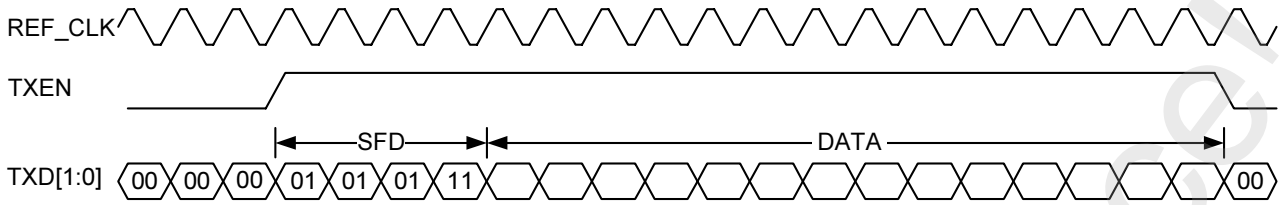


Figure 2-19 shows the RMII timing parameters.

Figure 2-19 RMII timing parameters

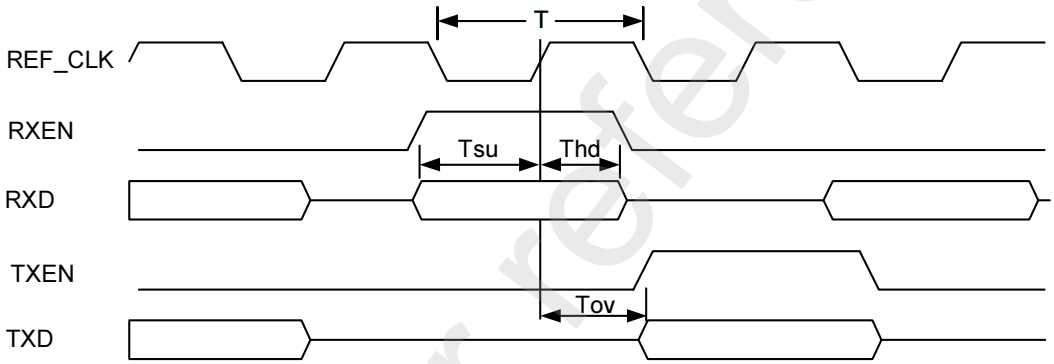


Table 2-28 describes the RMII timing parameters.

Table 2-28 RMII timing parameters

Parameter	Symbol	Signal	Min	Max	Unit
RMII clock cycle	T	REF_CLK	20	20	ns
RMII signal setup time	Tsu (RX)	CRS_DV/RXD[1:0]	4	N/A	ns
RMII signal hold time	Thd (RX)	CRS_DV/RXD[1:0]	2	N/A	ns
RMII output signal delay	Tov (TX)	TXEN/TXD[1:0]	3	16	ns

2.5.3.2 MDIO Interface Timings

Figure 2-20 shows the read timing of the MDIO interface.

Figure 2-20 Read timing of the MDIO interface

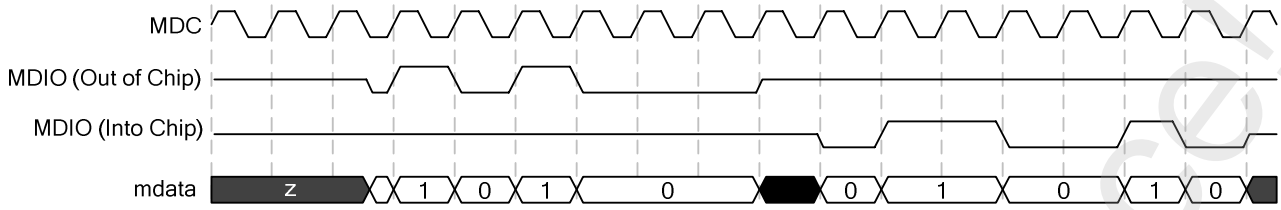


Figure 2-21 shows the write timing of the MDIO interface.

Figure 2-21 Write timing of the MDIO interface

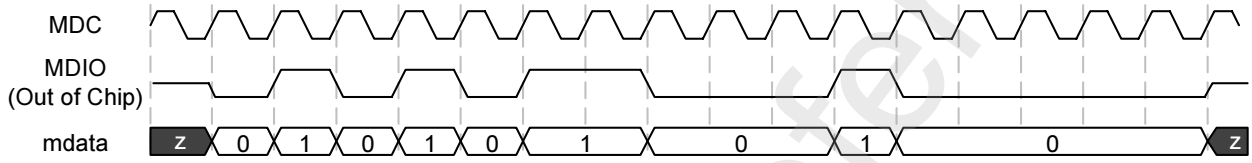


Figure 2-22 shows the RX timing parameters of the MDIO interface.

Figure 2-22 RX timing parameters of the MDIO interface

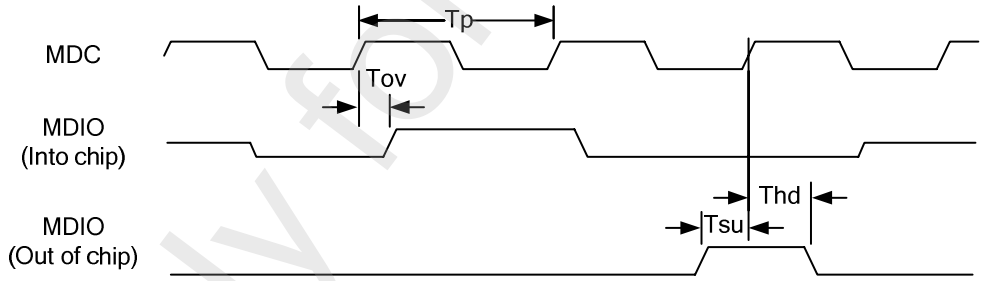


Table 2-29 describes the timing parameters of the MDIO interface.

Table 2-29 Timing parameters of the MDIO interface

Parameter	Symbol	Signal	Min	Max	Unit
MDIO data RX delay	Tov	MDIO	0	375	ns
MDIO clock cycle	Tp	MDCK	500	64000	ns
MDIO data TX setup time	Tsu	MDIO	10	N/A	ns
MDIO data TX hold time	Thd	MDIO	10	N/A	ns

2.5.4 VI Interface Timing

Figure 2-23 shows the VI interface timing in CMOS mode.

Figure 2-23 VI interface timing in CMOS mode

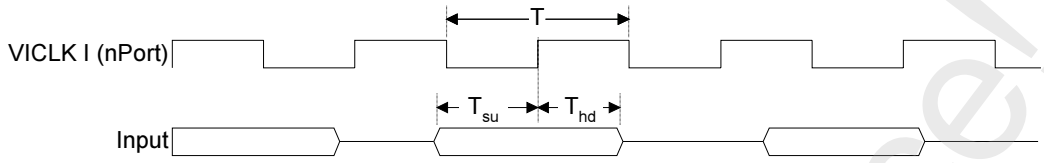


Table 2-30 describes the VI interface timing parameters.

Table 2-30 VI interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
VICLK clock cycle	T	6.73	N/A	N/A	ns
Input signal setup time	T_{su}	2.5	N/A	N/A	ns
Input signal hold time	T_{hd}	2.0	N/A	N/A	ns

2.5.5 VO Interface Timings

Figure 2-24 shows the BT.656 interface timing.

Figure 2-24 BT.656 interface timing

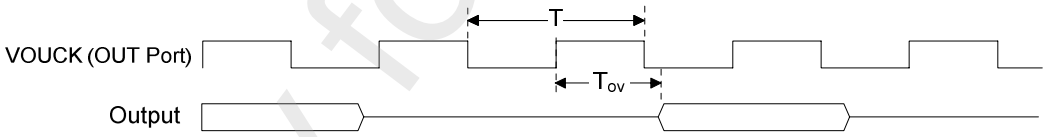


Table 2-31 describes the timing parameters of the BT.656 interface.

Table 2-31 Timing parameters of the BT.656 interface

Parameter	Symbol	Min	Typ	Max	Unit
VOUCLK clock cycle	T	13.46	13.48	37	ns
Output signal delay	T_{ov}	T/2-1.5	N/A	T/2+1.5	ns

Figure 2-25 shows the liquid crystal display (LCD) interface timing.

Figure 2-25 LCD interface timing

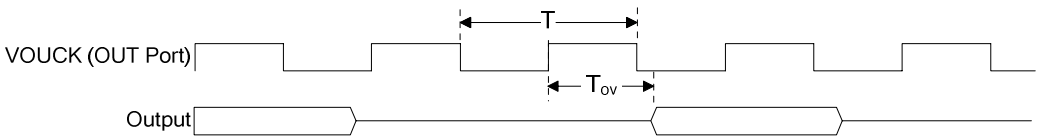


Table 2-32 describes the timing parameters of the LCD interface.

Table 2-32 Timing parameters of the LCD interface

Parameter	Symbol	Min	Typ	Max	Unit
VOUCLK clock cycle	T	37	N/A	500	ns
Output signal delay	T_{ov}	T/2 − 1.5	N/A	T/2 + 1.5	ns

2.5.6 AIAO Interface Timings

2.5.6.1 I²S Interface Timing

Figure 2-26 shows the RX timing of the I²S interface.

Figure 2-26 RX timing of the I²S interface

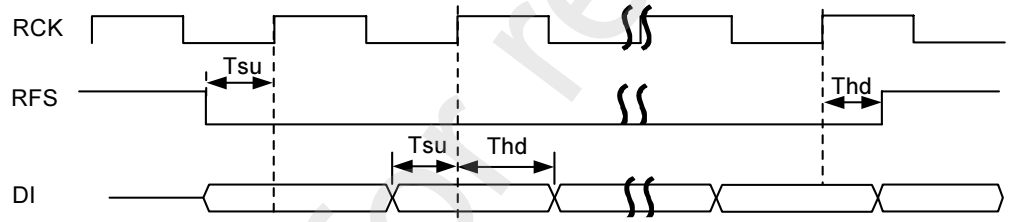


Figure 2-27 shows the TX timing of the I²S interface.

Figure 2-27 TX timing of the I²S interface

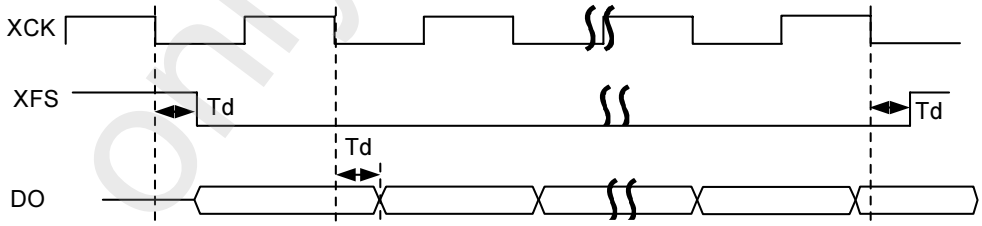


Table 2-33 describes the timing parameters of the I²S interface.

Table 2-33 Timing parameters of the I²S interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	N/A	N/A	ns
Input signal hold time	T_{hd}	10	N/A	N/A	ns
Output signal delay	T_d	0	N/A	8	ns

2.5.6.2 PCM Interface Timings

Figure 2-28 shows the RX timing of the PCM interface.

Figure 2-28 RX timing of the PCM interface

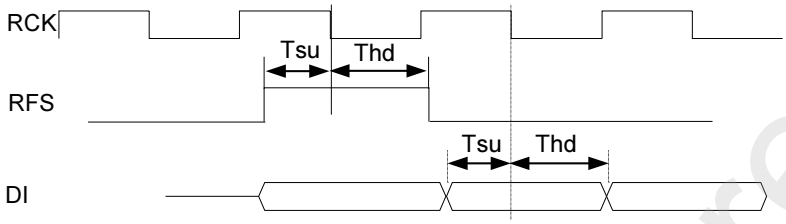


Figure 2-29 shows the TX timing of the PCM interface

Figure 2-29 TX timing of the PCM interface

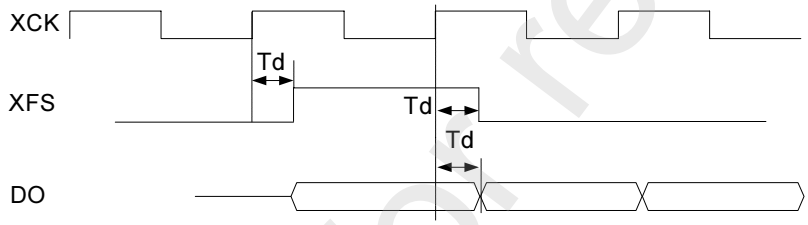


Table 2-34 describes the timing parameters of the PCM interface.

Table 2-34 Timing parameters of the PCM interface

Parameter	Symbol	Min	Typ	Max	Unit
Input signal setup time	T_{su}	10	N/A	N/A	ns
Input signal hold time	T_{hd}	10	N/A	N/A	ns
Output signal delay	T_d	0	N/A	8	ns

2.5.7 I²C Interface Timing

Figure 2-30 shows the I²C transfer timing.

Figure 2-30 I²C transfer timing

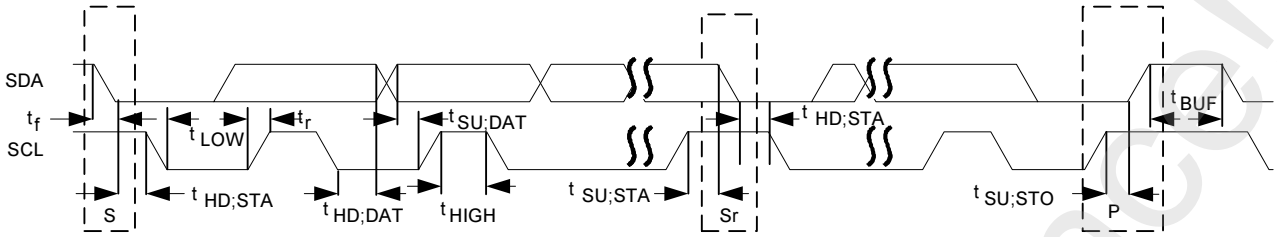


Table 2-35 describes the timing parameters of the I²C interface.

Table 2-35 Timing parameters of the I²C interface

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Serial clock (SCL) frequency	f_{SCL}	0	100	0	400	kHz
Start hold time	$t_{HD;STA}$	4.0	N/A	0.6	N/A	µs
SCL low-level cycle	t_{LOW}	4.7	N/A	1.3	N/A	µs
SCL high-level cycle	t_{HIGH}	4.0	N/A	0.6	N/A	µs
Start setup time	$t_{SU;STA}$	4.7	N/A	0.6	N/A	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU;DAT}$	250	N/A	100	N/A	ns
Serial data (SDA) and SCL rising time	t_r	N/A	1000	$20 + 0.1C_b$	300	ns
SDA and SCL falling time	t_f	N/A	300	$20 + 0.1C_b$	300	ns
End setup time	$t_{SU;STO}$	4.0	N/A	0.6	N/A	µs
Bus release time from start to end	t_{BUF}	4.7	N/A	1.3	N/A	µs
Bus load	C_b	N/A	400	N/A	400	pF
Low-level noise tolerance	V_{nL}	$0.1V_{DD}$	N/A	$0.1V_{DD}$	N/A	V
High-level noise tolerance	V_{nH}	$0.2V_{DD}$	N/A	$0.2V_{DD}$	N/A	V

2.5.8 SPI Timings

NOTE

In Figure Figure 2-31 to Figure 2-33, the conventions are as follows:

- MSB = most significant bit
- LSB = least significant bit

- SPI_CK(0):spo = 0
- SPI_CK(1):spo = 1

Figure 2-31 shows the SPI clock (SPICK) timing.

Figure 2-31 SPICK timing

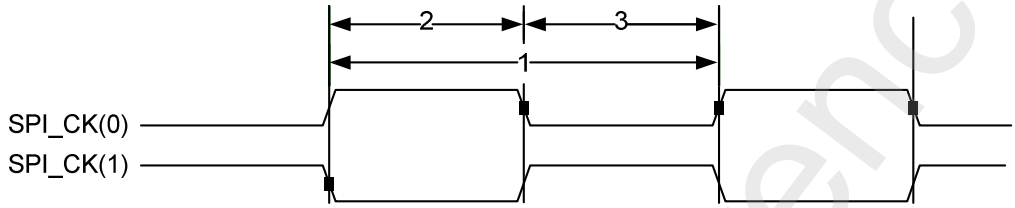


Figure 2-32 and Figure 2-33 show the SPI timings in master mode.

Figure 2-32 SPI timing in master mode (sph = 1)

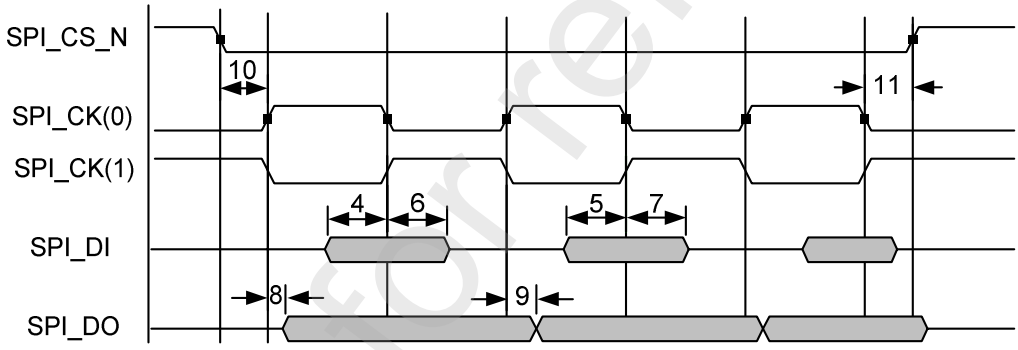


Figure 2-33 SPI timing in master mode (sph = 0)

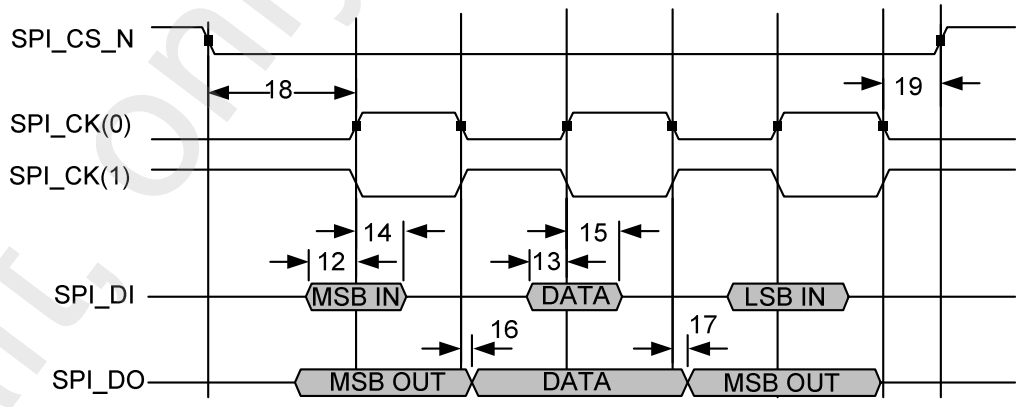


Table 2-36 describes the SPI timing parameters.

Table 2-36 SPI timing parameters

No.	Parameter	Symbol	Min	Typ	Max	Unit	Remark
1	Cycle time, SPI_CK	tc	2000/Fsspclk	N/A	65024000/Fsspclk	ns	Fsspclk unit: MHz
2	Pulse duration, SPI_CK high (all master modes)	tw1	N/A	1/2 tc	N/A	ns	N/A
3	Pulse duration. SPI_CK low (all master modes)	tw2	N/A	1/2 tc	N/A	ns	N/A
4	Setup time, SPI_DI (input) valid before SPI_CK (output) falling edge	tsu1	N/A	1/2 tc	N/A	ns	N/A
5	Setup time, SPI_DI (in put) valid before SPICK (output) rising edge	tsu2	N/A	1/2 tc	N/A	ns	N/A
6	Hold time, SPI_DI (input) valid after SPI_CK (output) falling edge	th1	N/A	1/2 tc	N/A	ns	N/A
7	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th2	N/A	1/2 tc	N/A	ns	N/A
8	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td1	0	N/A	N/A	ns	N/A
9	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td2	0	N/A	N/A	ns	N/A
10	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td3	N/A	tc	N/A	ns	N/A
11	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td4	N/A	1/2 tc	N/A	ns	N/A
12	Setup time, SPI_DI (input) valid before SPI_CK (output) rising edge	tsu3	N/A	1/2 tc	N/A	ns	N/A
13	Setup time, SPI_DI (in put) valid before SPI_CK (output) falling edge	tsu4	N/A	1/2 tc	N/A	ns	N/A
14	Hold time, SPI_DI (input) valid after SPI_CK (output) rising edge	th3	N/A	1/2 tc	N/A	ns	N/A
15	Hold time, SPI_DI (input) valid	th4	N/A	1/2 tc	N/A	ns	N/A

No.	Parameter	Symbol	Min	Typ	Max	Unit	Remark
	after SPI_CK (output) falling edge						
16	Delay time, SPI_CK (output) falling edge to SPI_DO (output) transition	td5	0	N/A	N/A	ns	N/A
17	Delay time, SPI_CK (output) rising edge to SPI_DO (output) transition	td6	0	N/A	N/A	ns	N/A
18	Delay time, SPI_CS_N (output) falling edge to first SPI_CK (output) rising or falling edge	td7	N/A	1/2 tc	N/A	ns	N/A
19	Delay time, SPI_CK (output) rising or falling edge to SPI_CS_N (output) rising edge	td8	N/A	tc	N/A	ns	N/A

2.5.9 MIPI RX Timings

Table 2-37 describes the MIPI RX timing parameters.

Table 2-37 MIPI RX timing parameters

Symbol	Description	Min	Tye	Max	Unit
F_{MAX}	Data rate	N/A	N/A	1 G	bit/s
T_{PERIOD}	Differential clock cycle	2	T	N/A	ns
T_{DUTY}	Differential clock duty cycle	0.45 T	N/A	0.55T	ns
T_{SET}	Differential clock setup time	0.15 x UI	N/A	N/A	ns
T_{HD}	Differential clock hold time	0.15 x UI	N/A	N/A	ns
T_{RISE}	Differential clock rising time (20%−80%)	0.15	N/A	N/A	ns
T_{FALL}	Differential clock falling time (20%−80%)	0.15	N/A	0.3 x UI	ns

NOTE

UI = T/2

2.5.10 SDIO/MMC Interface Timings

Figure 2-34 shows the single-edge data input and output timings of the SDIO/MMC interface.

Figure 2-34 Single-edge data input and output timings of the SDIO/MMC interface

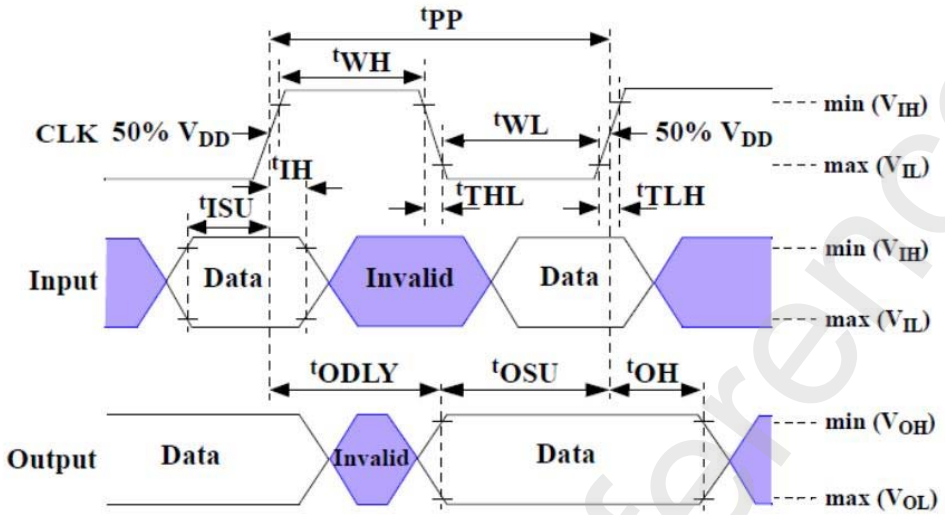


Figure 2-35 shows the dual-edge data input and output timings of the SDIO/MMC interface.

Figure 2-35 Dual-edge data input and output timings of the SDIO/MMC interface

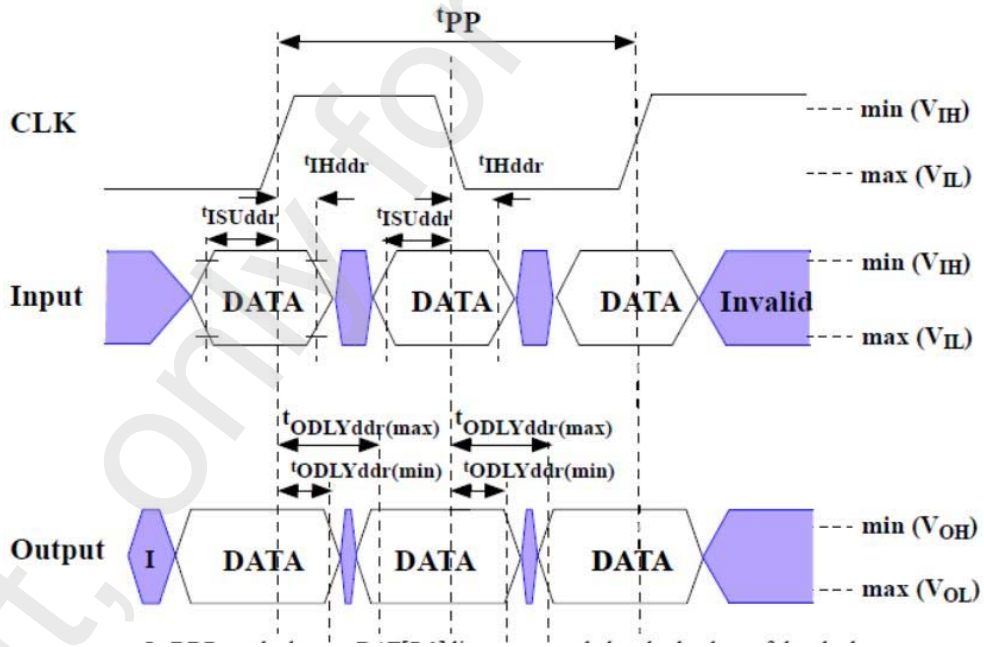


Table 2-38 describes the timing parameters of the SDIO/MMC interface.

Table 2-38 Timing parameters of the SDIO/MMC interface

Speed Mode	Maximum Frequency (MHz)/Cycle (ns)		Minimum Hold Time	Minimum Setup Time	Maximum Output Delay of the Card	High Level Duration of the Card Clock
MMC_HS200	100 MHz	10 ns	1.4 ns	0.8 ns	N/A	(0.45−0.55) clock cycle
MMC DDR (CMD line)	50 MHz	20 ns	3.0 ns	3.0 ns	13.7 ns	
MMC DDR (DAT line)	50 MHz	20 ns	2.5 ns	2.5 ns	7.0 ns	
MMC_HS	50 MHz	20 ns	3.0 ns	3.0 ns	13.7 ns	
SD_HS	50 MHz	20 ns	2.0 ns	6.0 ns	14 ns	
SD_DS	25 MHz	40 ns	5.0 ns	5.0 ns	14 ns	
Identification mode	400 kHz	2.5 μs	5.0 ns	5.0 ns	50 ns	

Contents

Figures

Tables

3 System

3.1 Reset

3.1.1 Overview

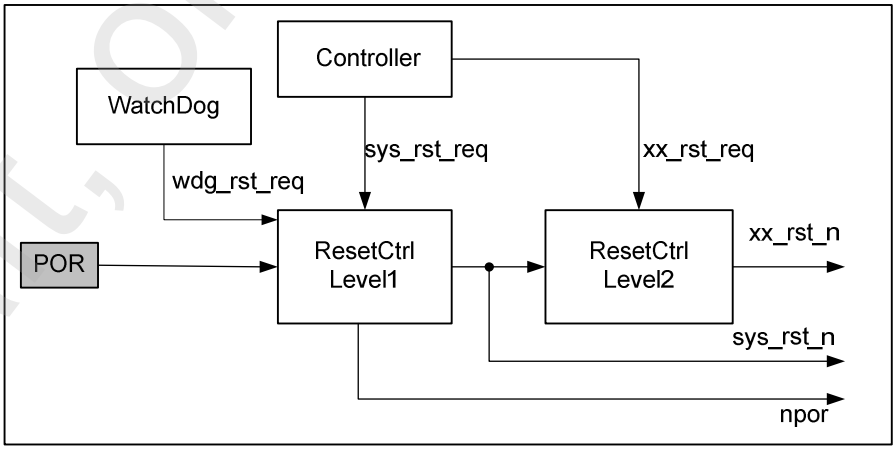
The reset management module resets the entire chip and all functional modules in a unified manner as follows:

- Manages and controls power-on reset.
- Manages and controls the watchdog.
- Controls the system soft reset and the separate soft reset of each functional module.
- Synchronizes reset signals to the clock domain corresponding to each module.
- Generates reset signals for internal functional modules of the chip.

3.1.2 Reset Control

Figure 3-1 shows the diagram of controlling reset signals.

Figure 3-1 Diagram of controlling reset signals



NOTE

- POR: internal power-on reset (POR) module
- wdg_rst_req: watchdog reset request
- sys_rst_req: global soft reset request signal. This signal is derived from the system controller.
- xx_rst_req: separate soft reset request signal of each submodule. This signal is derived from the clock and reset generator (CRG) system controller.
- xx_rst_n, sys_rst_n, and npor: reset signals.

Table 3-1 Types of reset signals

Type	Generation Mode	Function
Global hard reset signal (npor)	Derived from the internal POR module	Globally resets the entire.
Global soft reset signal (syn_rst_n)	Derived from the global soft reset register of the software configuration system controller.	Globally resets all the modules of the Hi3516C V300, excluding the clock reset circuits, test circuits, and registers that do not support soft reset
Submodule reset signal (xx_rst_n)	Derived from the submodule reset control register of the CRG system controller.	Separately resets each submodule of the Hi3516C V300.

3.1.3 Reset Configuration

Power-On Reset

To implement power-on reset, the following conditions must be met:

- The internal POR module generates a low-level pulse, and the low pulse duration is greater than 12 XIN crystal clock cycles.
- The clock input by the XIN pin of the crystal oscillator clock works properly.

System Reset

The system is reset in either of the following ways:

- Power-on reset
- Watchdog reset
- Global soft reset, controlled by the system controller

Soft Reset

Soft reset control is implemented by configuring the corresponding CRG controller. For details about configurations, see the description of the reset register for each module.

CAUTION

- After a system soft reset request is sent, the reset is deasserted only after at least 64 ms.
- The separate soft reset of each module is not automatically deasserted. For example, if a module is reset after 1 is written to the related bit, the reset of this module is deasserted only when the related bit is set to 0.

3.2 Clock

3.2.1 Overview

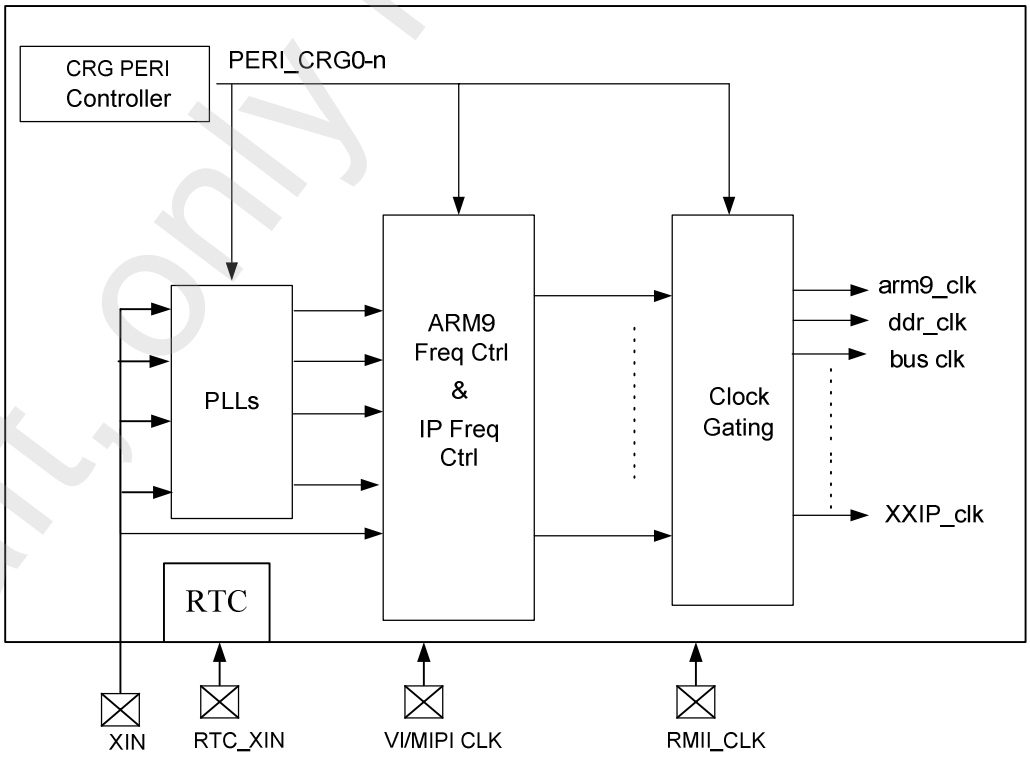
The clock and reset generator (CRG) manages clock input, clock generation, and clock control in a unified manner as follows:

- Manages and controls clock inputs
- Divides and controls clock frequencies
- Generates working clocks for each module

3.2.2 Clock Control Block Diagram

Figure 3-2 shows the functional block diagram of the CRG.

Figure 3-2 Functional block diagram of the CRG



NOTE

XIN is the PLL input clock and is always connected to a 24 MHz crystal, whereas RTC_XIN is the RTC input clock and is always connected to a 32.768 kHz crystal.

3.2.3 Clock Distribution

The CRG configures, controls, and manages the internal PLLs and the input clocks from pins. It also generates the clocks required by each module. Figure 3-3 shows the clock distribution diagram.

NOTE

The APLL in gray can be configured by programming, and the configurations of other PLLs are fixed.

Figure 3-3 Clock distribution diagram 1

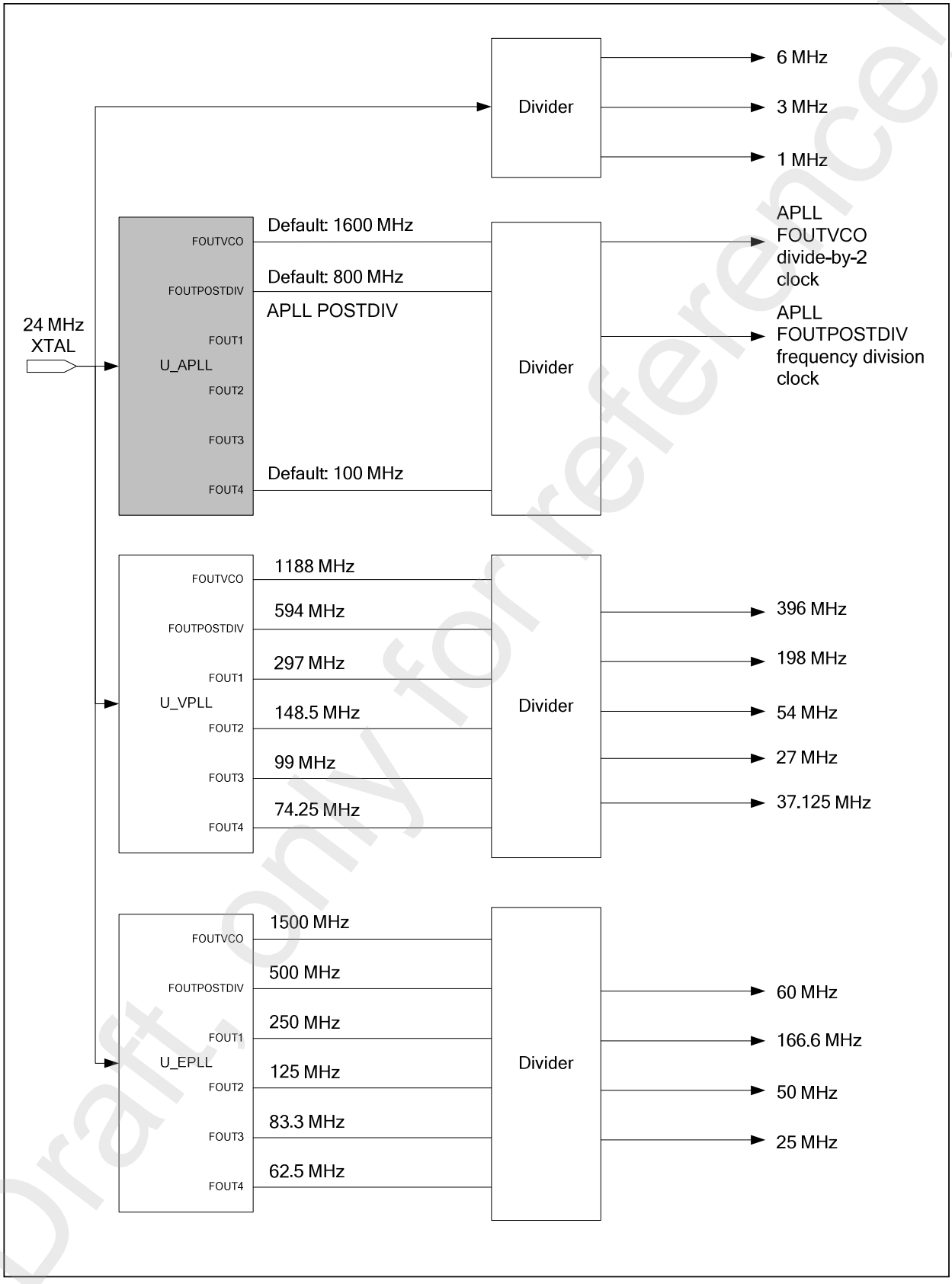


Figure 3-4 Clock distribution diagram 2

Table 3-2 shows the optional clocks for major modules. (For details about the configuration, see the description of the corresponding clock select register of each module.)

Table 3-2 Optional clocks of major modules

Module	Default Frequency	All Frequencies	Remarks
ARM9	24 MHz	24 MHz APLL POSTDIV APLL FOUTVCO divide-by-2 clock 594 MHz	-
DDR	24 MHz	24 MHz APLL FOUTPOSTDIV frequency division clock 250 MHz 198 MHz	DDR controller clock
SYSAPB	24 MHz	24 MHz 50 MHz	-
ISP	83.3 MHz	VICAP VICAP_DIV2	The VICAP clock or VICAP divide-by-2 clock can be selected.
VICAP	83.3 MHz	83.3 MHz 125 MHz 148.5 MHz 198 MHz	-
VDP CLKOUT	27 MHz	74.25 MHz 27 MHz	Chip output clock

Module	Default Frequency	All Frequencies	Remarks
		CLK_LCD	
VPSS	148.5 MHz	Offline mode: • 148.5 MHz • 198 MHz • 250 MHz Online mode: • VICAP • VICAP_DIV2	-
VEDU	166.6 MHz	166.6 MHz 198 MHz	-
VGS	198 MHz	198 MHz 250 MHz 297 MHz 396 MHz	-
AIAO	1188 MHz	1188 MHz	The actual working frequency is the divided frequency of this clock.
IVE	198 MHz	198 MHz 250 MHz 297 MHz	-
JPGE	198 MHz	198 MHz	-
GZIP	198 MHz	198 MHz	-
FMC	24 MHz	24 MHz 83.3 MHz 148.5 MHz 198 MHz 297 MHz	The chip output clock is the frequency division clock of this clock.
Sensor	74.25 MHz	74.25 MHz 37.125 MHz 54 MHz 27 MHz 24 MHz 25 MHz	Reference clock to the sensor from the chip

3.2.4 PLL Configuration

The Hi3516C V300 has three internal PLLs. Each PLL uses two configuration registers. See Table 3-3.

Table 3-3 Configuration registers corresponding to PLLs

PLL	Configuration Register 0	Configuration Register 1
APLL	PERI_CRG_PLL0	PERI_CRG_PLL1
VPLL	PERI_CRG_PLL4	PERI_CRG_PLL5
EPLL	PERI_CRG_PLL8	PERI_CRG_PLL9

All PLLs use the input crystal oscillator clock of the XIN pin as the input clock. For details on how to calculate PLL output frequencies, see Table 3-4.

Table 3-4 Methods of calculating PLL output frequencies

PLL Pin	Formula	Remarks
FREF	PLL input reference clock	The input clock must be 24 MHz.
FOUTVCO	FREF x (fbdiv + frac/2^24)/refdiv	PLL working frequency. It must be greater than 800 MHz but less than or equal to 2.3 GHz.
FOUTVCO2X	FOUTVCO x 2	None
FOUTPOSTDIV	FOUTVCO/(pstdiv1 x pstdiv2)	None
FOUT1ph0	FOUTVCO/(pstdiv1 x pstdiv2 x 2)	None
FOUT2	FOUTVCO/(pstdiv1 x pstdiv2 x 4)	None
FOUT3	FOUTVCO/(pstdiv1 x pstdiv2 x 6)	None
FOUT4	FOUTVCO/(pstdiv1 x pstdiv2 x 8)	None

NOTE

- fbdiv: integral part of the frequency multiplier
- frac: decimal part of the frequency multiplier
- refdiv: frequency divider of the reference clock
- pstdiv1: level-1 output frequency divider
- pstdiv2: level-2 output frequency divider

For details about the frequency multiplier and divider of each PLL, see Table 3-3.

For example, to set the APLL FOUTVCO output frequency to 1600 MHz and the FOUTPOSTDIV output frequency to half of the FOUTVCO frequency, calculate as follows:

- Set the FOUTPOSTDIV output frequency to half of the FOUTVCO frequency. According to the formula FOUTPOSTDIV = FOUTVCO/(pstdiv1 x pstdiv2), **postdiv2** is **1** and **postdiv1** is **2**.
- Set the FOUTVCO output frequency to 1600 MHz. FREF x (fbdiv + frac/2^{24})/refdiv = 1600 MHz, and **FREF** is 24 MHz. If **refdiv** is **3**, then **fbdiv** is **200** and **frac** is **0**.

3.2.5 Frequency Configurations

3.2.5.1 Frequency Configurations of ARM9/DDR/Bus Clocks

Table 3-5 describes the frequency configurations of ARM9/DDR/bus clocks.

Table 3-5 Frequency configurations of ARM9/DDR/bus clocks

Signal	Configuration Register
cpu_sc_sel	PERI_CRG12 bit[5:4]
cpuclk_loaden	PERI_CRG10 bit[17]
cpuclk_skipcfg	PERI_CRG10 bit[16:12]
ddr_clk_div	PERI_CRG12 bit[9:8]
ddr_sc_sel	PERI_CRG12 bit[3:2]
apb_sc_sel	PERI_CRG12 bit[0]

3.2.5.2 Frequency Configurations of Module Clocks

Table 3-6 describes the frequency configurations of module clocks.

Table 3-6 Frequency configurations of module clocks

Signal	Configuration Register
VDP clock configurations	
dac_pctrl	PERI_CRG13 bit[21]
lcd_clksel	PERI_CRG13 bit[20]
hd_lcd_clksel	PERI_CRG13 bit[17]
vo_out_clksel	PERI_CRG13 bit[14]
hd_clksel	PERI_CRG13 bit[13:12]
vo_out_pctrl	PERI_CRG13 bit[2]
VI_MIPI clock configurations	
sensor_clksel	PERI_CRG11 bit[25:23]
phy_cmos_lat	PERI_CRG11 bit[22:21]
phy_hs_lat	PERI_CRG11 bit[20:19]

Signal	Configuration Register
isp_clksel	PERI_CRG11 bit[17]
vi0_sc_sel	PERI_CRG11 bit[4:2]
vi0_pctrl	PERI_CRG11 bit[1]
viclk_loaden	PERI_CRG28 bit[5]
vicclk_skipcfg	PERI_CRG28 bit[4:0]
Video encoding/decoding unit (VEDU) clock configurations	
vedu_clksel	PERI_CRG16 bit[11:10]
veduclk_loaden	PERI_CRG16 bit[9]
veduclk_skipcfg	PERI_CRG16 bit[8:4]
VPSS clock configurations	
vps_clksel	PERI_CRG18 bit[11:10]
vpsclk_loaden	PERI_CRG18 bit[9]
vpsclk_skipcfg	PERI_CRG18 bit[8:4]
VGS clock configurations	
vgs_clksel	PERI_CRG23 bit[11:10]
tdeclk_loaden	PERI_CRG23 bit[9]
tdeclk_skipcfg	PERI_CRG23 bit[8:4]
JPGE clock configurations	
jpgeclk_loaden	PERI_CRG24 bit[9]
tdeclk_skipcfg	PERI_CRG24 bit[8:4]
LCD clock configurations	
lcd_mclk_div	PERI_CRG26 bit[26:0]
IVE clock configurations	
ive_clksel	PERI_CRG27 bit[3:2]
USB 2.0 clock configurations	
usb2_phy_clksel	PERI_CRG46 bit[15]
FMC clock configurations	
fmc_clksel	PERI_CRG48 bit[4:2]
SDIO0/SDIO1/SDIO2/EMMC clock configurations	
sdio0_clksel	PERI_CRG49 bit[5:4]
sdio1_clksel	PERI_CRG49 bit[13:12]

Signal	Configuration Register
sdio2_clksel	PERI_CRG50 bit[5:4]
emmc_clksel	PERI_CRG49 bit[21:20]
Pulse-width modulation (PWM)/UART clock configurations	
pwm_clksel	PERI_CRG14 bit[3:2]
uart_clksel	PERI_CRG57 bit[19]
ETH clock configurations	
ethcore_clksel	PERI_CRG59 bit[7]
ethphy_clksel	PERI_CRG59 bit[5:4]
ethrmii_clksel	PERI_CRG59 bit[2]

3.2.5.3 Precautions

Take the following precautions when configuring clocks:

- By default, the ARM9 working clock is in crystal oscillator mode after power-on. That is, the crystal oscillator clock input by the XIN pin is selected.
- If the frequency of the PLL is changed, the PLL can output a stable clock 0.1 ms later. The PLL frequency can be changed only when the system working clock is in crystal oscillator mode.
- If the PLL output clock is not stable, the system mode cannot be switched to PLL mode. You can wait for 0.1 ms and then view the PLL lock bit to check whether the PLL is locked. The status of the PLL lock bit can be obtained by reading PERI_CRG58 bit[2:0].

3.2.6 Register Summary

Table 3-7 describes CRG registers.

Table 3-7 Summary of CRG registers (base address: 0x1201_0000)

Offset Address	Register	Description	Page
0x0000	PERI_CRG_PLL0	APLL configuration register 0	3-13
0x0004	PERI_CRG_PLL1	APLL configuration register 1	3-13
0x0010	PERI_CRG_PLL4	VPLL configuration register 0	3-15
0x0014	PERI_CRG_PLL5	VPLL configuration register 1	3-15
0x0020	PERI_CRG_PLL8	EPLL configuration register 0	3-17
0x0024	PERI_CRG_PLL9	EPLL configuration register 1	3-17
0x0028	PERI_CRG10	ARM9 frequency mode and reset configuration register	3-19

Offset Address	Register	Description	Page
0x0030	PERI_CRG12	System-on-chip (SoC) clock selection register	3-22
0x0034	PERI_CRG13	VDP clock and reset control register	3-23
0x0038	PERI_CRG14	PWM clock and reset control register	3-25
0x0040	PERI_CRG16	VEDU clock and soft reset control register	3-25
0x0048	PERI_CRG18	VPSS clock and reset control register	3-26
0x005C	PERI_CRG23	VGS clock and soft reset control register	3-27
0x0060	PERI_CRG24	JPGE clock and soft reset control register	3-28
0x0068	PERI_CRG26	LCD clock control register	3-29
0x006C	PERI_CRG27	IVE&HASH clock and soft reset control register	3-29
0x0070	PERI_CRG28	VICAP/VPSS online mode clock configuration register	3-30
0x007C	PERI_CRG31	LSADC & cipher clock and soft reset control register	3-31
0x008C	PERI_CRG35	AIAO clock and soft reset control register	3-32
0x00B8	PERI_CRG46	USB2.0 clock and soft reset control register	3-33
0x00C0	PERI_CRG48	FMC clock and soft reset control register	3-34
0x00C4	PERI_CRG49	eMMC/SDIO0/SDIO1 clock and soft reset control register	3-35
0x00C8	PERI_CRG50	SDIO2 clock and soft reset control register	3-37
0x00D4	PERI_CRG53	GZIP clock and soft reset control register	3-38
0x00D8	PERI_CRG54	DMAC/DDR TEST clock and soft reset control register	3-39
0x00DC	PERI_CRG55	SoC SW feedback indicator register	3-40
0x00E0	PERI_CRG_PLL56	GZIP reset status register	3-41
0x00E4	PERI_CRG57	Soft reset control register for other CRG interface modules	3-41
0x00E8	PERI_CRG58	CRG status register	3-43

Offset Address	Register	Description	Page
0x00EC	PERI_CRG59	ETH clock and soft reset control register	3-44
0x0100	PERI_CRG64	RSA clock and soft reset control register	3-45
0x0108	PERI_CRG66	APLL spread spectrum configuration register	3-46
0x0110	PERI_CRG68	VPLL spread spectrum configuration register	3-47
0x0118	PERI_CRG70	EPLL spread spectrum configuration register	3-48

3.2.7 Register Description

PERI_CRG_PLL0

PERI_CRG_PLL0 is APLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	PERI_CRG_PLL0	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	apll_postdiv2			reserved	apll_postdiv1			apll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved
[30:28]	RW	apll_postdiv2	Level-2 output divider of the APLL
[27]	RW	reserved	Reserved
[26:24]	RW	apll_postdiv1	Level-1 output divider of the APLL
[23:0]	RW	apll_frac	Decimal part of the APLL frequency multiplication coefficient

PERI_CRG_PLL1

PERI_CRG_PLL1 is APLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	PERI_CRG_PLL1	0x0900_30C8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				apll_foutvco2xpd	apll_bypass	apll_dacpd	apll_dsmpd	apll_pd	apll_foutvcopd	apll_postdivpd	apll_fout4phasepd	reserved				apll_refdiv				apll_fbdiv											
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved
[27]	RW	apll_foutvco2xpd	APLL VCO2X output power-down control 0: normal output clock 1: no output clock
[26]	RW	apll_bypass	APLL clock frequency division bypass 0: not bypassed 1: bypassed
[25]	RW	apll_dacpd	APLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	apll_dsmpd	APLL decimal division control 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	apll_pd	APLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	apll_foutvcopd	APLL VCO output power-down control 0: normal output clock 1: no output clock
[21]	RW	apll_postdivpd	APLL POSTDIV output power-down control 0: normal output clock 1: no output clock
[20]	RW	apll_fout4phasepd	APLL FOUT output power-down control 0: normal output clock 1: no output clock
[19:18]	RW	reserved	Reserved

[17:12]	RW	apll_refdiv	Frequency divider of the APLL reference clock
[11:0]	RW	apll_fbdiv	Integral part of the APLL frequency multiplication coefficient

PERI_CRG_PLL4

PERI_CRG_PLL 4 is VPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0010	PERI_CRG_PLL 4	0x1200_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	vpll_postdiv2			reserved	vpll_postdiv1			vpll_frac																							
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved
[30:28]	RW	vpll_postdiv2	Level-2 output divider of VPLL
[27]	RW	reserved	Reserved
[26:24]	RW	vpll_postdiv1	Level-1 output divider of VPLL
[23:0]	RW	vpll_frac	Decimal part of the VPLL frequency multiplication coefficient

PERI_CRG_PLL5

PERI_CRG_PLL 5 is VPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0014	PERI_CRG_PLL 5	0x0900_2063

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vpll_foutvco2xpd	vpll0_bypass	vpll0_dacpd	vpll0_dsmpd	vpll0_pd	vpll0_foutvcopd	vpll0_postdivpd	vpll0_fout4phasepd	reserved		vpll0_refdiv						vpll0_fbdiv											
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	1	1

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved
[27]	RW	vpll_foutvco2xpd	VPLL VCO2X output power-down control 0: normal output clock 1: no output clock
[26]	RW	vpll_bypass	VPLL clock frequency division bypass 0: not bypassed 1: bypassed
[25]	RW	vpll_dacpd	VPLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	vpll_dsmpd	VPLL decimal division control 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	vpll_pd	VPLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	vpll_foutvcopd	VPLL VCO output power-down control 0: normal output clock 1: no output clock
[21]	RW	vpll_postdivpd	VPLL POSTDIV output power-down control 0: normal output clock 1: no output clock
[20]	RW	vpll_fout4phasepd	VPLL FOUT output power-down control 0: normal output clock 1: no output clock
[19:18]	RW	reserved	Reserved

[17:12]	RW	vpll_refdiv	Frequency divider of the VPLL reference clock
[11:0]	RW	vpll_fbdiv	Integral part of the VPLL frequency multiplication coefficient

PERI_CRG_PLL8

PERI_CRG_PLL 8 is EPLL configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0020	PERI_CRG_PLL 8	0x1300_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		epll_postdiv2		reserved		epll_postdiv1		epll_frac																							
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	reserved	Reserved
[30:28]	RW	epll_postdiv2	Level-2 output divider of the EPLL
[27]	RW	reserved	Reserved
[26:24]	RW	epll_postdiv1	Level-1 output divider of the EPLL
[23:0]	RW	epll_frac	Decimal part of the EPLL frequency multiplication coefficient

PERI_CRG_PLL9

PERI_CRG_PLL 9 is EPLL configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0024	PERI_CRG_PLL 9	0x0900_207D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				epll_foutvco2xpd	epll_bypass	epll_dacpd	epll_dsmpd	epll_pd	epll_foutvcopd	epll_postdivpd	epll_fout4phasepd	reserved				epll_refdiv				epll_fbdiv											
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved
[27]	RW	epll_foutvco2xpd	EPLL VCO2X output power-down control 0: normal output clock 1: no output clock
[26]	RW	epll_bypass	EPLL clock frequency division bypass 0: not bypassed 1: bypassed
[25]	RW	epll_dacpd	EPLL test signal control 0: normal operating mode 1: power-down mode
[24]	RW	epll_dsmpd	EPLL decimal division control 0: decimal frequency-division mode 1: integral frequency-division mode
[23]	RW	epll_pd	EPLL power-down control 0: normal operating mode 1: power-down mode
[22]	RW	epll_foutvcopd	EPLL VCO output power-down control 0: normal output clock 1: no output clock
[21]	RW	epll_postdivpd	EPLL POSTDIV output power-down control 0: normal output clock 1: no output clock
[20]	RW	epll_fout4phasepd	EPLL FOUT output power-down control 0: normal output clock 1: no output clock
[19:18]	RW	reserved	Reserved

[17:12]	RW	epll_refdiv	Frequency divider of the EPLL reference clock
[11:0]	RW	epll_fbdiv	Integral part of the EPLL frequency multiplication coefficient

PERI_CRG10

PERI_CRG10 is an ARM9 frequency mode and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	PERI_CRG10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved		cpuclk_loaden		cpuclk_skipcfg				reserved				arm_core_srst_req		reserved					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved
[19:18]	RW	reserved	Reserved
[17]	RW	cpuclk_loaden	Skip configuration enable for the CPU clock To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[16:12]	RW	cpuclk_skipcfg	Skip configuration of the CPU clock N: *N*-beat clocks are disabled for every 32-beat CPU clocks.
[11:6]	RW	reserved	Reserved
[5]	RW	arm_core_srst_req	ARM core soft reset request 0: deassert reset 1: reset
[4:0]	RW	reserved	Reserved

PERI_CRG11

PERI_CRG11 is a VICAP&MIPI CTRL and sensor clock and reset configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	PERI_CRG11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				sensor_srst_req	sensor_cken	sensor_clksel		phy_cmos_lat				phy_hs_lat				isp_cken	isp_clksel	mipi_core_srst_req		mipi_cken	isp_cfg_srst_req	isp_core_srst_req	mipi_hrst_req	mipi_srst_req	vi_ch0_srst_req	vi_hrst_req	vi0_srst_req	reserved				vi0_sc_sel				vi0_pctrl	vi0_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved
[27]	RW	sensor_srst_req	Sensor soft reset request 0: deassert reset 1: reset
[26]	RW	sensor_cken	Sensor clock (reference clock output to the sensor from the chip) gating 0: disabled 1: enabled
[25:23]	RW	sensor_clksel	Sensor clock (reference clock output to the sensor from the chip) select 000: 74.25 MHz 001: 37.125 MHz 010: 54 MHz 011: 27 MHz 1X0: 24 MHz 1X1: 25 MHz
[22:21]	RW	phy_cmos_lat	Latency of the MIPI PHY CMOS mode interface clock N: N steps are added on the basis of the default steps (500 ps/step).
[20:19]	RW	phy_hs_lat	Latency of the MIPI PHY HS mode interface clock N: N steps are added on the basis of the default steps (500 ps/step).
[18]	RW	isp_cken	ISP clock gating 0: disabled 1: enabled
[17]	RW	isp_clksel	ISP clock select 0: VI working clock 1: divide-by-2 clock of the VI working clock

[16]	RW	mipi_core_srst_req	MIPI Ctrl core soft reset 0: deassert reset 1: reset
[15]	RW	mipi_cken	MIPI PIX clock gating 0: The clock is disabled. 1: The clock is enabled.
[14]	RW	isp_cfg_srst_req	ISP CFG soft reset request 0: deassert reset 1: reset
[13]	RW	isp_core_srst_req	ISP core soft reset request 0: deassert reset 1: reset
[12]	RO	reserved	Reserved
[11]	RW	mipi_srst_req	MIPI Ctrl (core&CFG) soft reset request 0: deassert reset 1: reset
[10]	RW	vi_ch0_srst_req	VI port soft reset request 0: deassert reset 1: reset
[9]	RW	vi_hrst_req	VI bus soft reset request 0: deassert reset 1: reset
[8]	RW	vi0_srst_req	VI soft reset request 0: deassert reset 1: reset
[7:5]	RW	reserved	Reserved
[4:2]	RW	vi0_sc_sel	VI clock select 000: 83.3 MHz 001: 125 MHz 010: 148.5 MHz 011: 198 MHz 100: reserved 101: reserved 110: reserved 111: reserved
[1]	RW	vi0_pctrl	Phase of the VI interface clock 0 (default): normal phase 1: inverted phase

[0]	RW	vi0_cken	VI clock gating 0: disabled 1: enabled

PERI_CRG12

PERI_CRG12 is an SoC clock selection register.

Offset Address	Register Name	Total Reset Value
0x0030	PERI_CRG12	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9 8	7 6	5 4	3 2	1	0
Name	reserved						ddr_clk_div	reserved	cpu_clk_div	ddr_sc_sel	reserved	apb_sc_sel
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0 0	0 0	0 0	0 0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved
[9:8]	RW	ddr_clk_div	DDR APLL FOUTPOSTDIV frequency division configuration 00: divided by 1 01: divided by 2 10: divided by 3 11: divided by 4
[7:6]	RO	reserved	Reserved
[5:4]	RW	cpu_sc_sel	CPU clock select 00: crystal oscillator clock 01: APLL FOUTPOSTDIV clock 10: APLL FOUTVCO divide-by-2 clock 11: 594 MHz
[3:2]	RW	ddr_sc_sel	DDR clock select 00: crystal oscillator clock 01: APLL FOUTPOSTDIV frequency-division clock 10: 250 MHz 11: 198 MHz
[1]	RW	reserved	Reserved

[0]	RW	apb_sc_sel	SYSAPB clock select 0: crystal oscillator clock 1: 50 MHz

PERI_CRG13

PERI_CRG13 is a VDP clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0034	PERI_CRG13	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									dac_cken	dac_pctrl	lcd_clksel	reserved	lcd_cken	hd_lcd_clksel	reserved	vo_out_clksel		hd_clksel		reserved	vou_sd_cken	vou_hd_cken	vou_acken	vo_out_cken	vou_pcken	vou_ppc_cken	vou_cfg_cken	reserved	vo_out_pctrl	reserved	vo_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved
[22]	RW	dac_cken	DAC clock gating 0: disabled 1: enabled
[21]	RW	dac_pctrl	DAC clock phase 0: normal 1: reversed
[20]	RW	lcd_clksel	LCD frequency division clock select 0: LCD clock after being divided by 3 1: LCD clock after being divided by 4
[19]	RW	reserved	Reserved
[18]	RW	lcd_cken	LCD working clock gating 0: disabled 1: enabled
[17]	RW	hd_lcd_clksel	HD_LCD working clock select 0: The HD frequency division clock is used as the DHD channel clock. 1: The LCD frequency division clock is used as the DHD channel clock.
[16:15]	RW	reserved	Reserved

[14]	RW	vo_out_clksel	VDP output clock (chip output clock) frequency select 0: The HD clock is used as the VDP output associated clock. 1: The LCD clock is used as the VDP output associated clock.
[13:12]	RW	hd_clksel	DHD frequency bit[12]: DHD clock source select 0: The HD clock frequency is 27 MHz. 1: The HD clock frequency is 74.25 MHz. bit[13]: DHD clock frequency division 0: divide-by-2 clock of the DHD clock 1: DHD clock
[11]	RW	reserved	Reserved
[10]	RW	vou_sd_cken	VDP SD DATE clock gating 0: disabled 1: enabled
[9]	RW	vou_hd_cken	VDP HD clock gating register 0: disabled 1: enabled
[8]	RW	vou_acken	VDP AXI bus clock gating register 0: disabled 1: enabled
[7]	RW	vo_out_cken	DP output clock (output clock of the chip) clock gating register 0: disabled 1: enabled
[6]	RW	vou_pcken	VDP APB clock gating register 0: disabled 1: enabled
[5]	RW	vou_ppc_cken	VDP working clock gating 0: disabled 1: enabled
[4]	RW	vou_cfg_cken	VDP CFG clock gating (internally configured) register 0: disabled 1: enabled
[3]	RW	reserved	Reserved
[2]	RW	vo_out_pctrl	VDP output clock (output clock of the chip) phase control 0: normal phase 1 (default): inverted phase
[1]	RW	reserved	Reserved

[0]	RW	vo_srst_req	VDP soft reset request 0: deassert reset 1: reset

PERI_CRG14

PERI_CRG14 is a PWM clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0038	PERI_CRG14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												pwm_clksel		pwm_cken	pwm_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	reserved	Reserved
[3:2]	RW	pwm_clksel	PWM clock select 00: 3 MHz 01: 50 MHz 1x: 24 MHz
[1]	RW	pwm_cken	PWM clock gating register 0: disabled 1: enabled
[0]	RW	pwm_srst_req	PWM soft reset request 0: deassert reset 1: reset

PERI_CRG16

PERI_CRG16 is a VEDU clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0040	PERI_CRG16	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vedu_clksel		veduclk_loaden		veduclk_skipcfg				reserved		vedu_cken	vedu_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved
[11:10]	RW	vedu_clksel	VEDU clock select 00: 166.6 MHz 01: 198 MHz 10: reserved 11: reserved
[9]	RW	veduclk_loaden	VEDU clock skip enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	veduclk_skipcfg	VEDU clock skip N: *N*-beat clocks are disabled for every 32-beat VEDU clocks.
[3:2]	RW	reserved	Reserved
[1]	RW	vedu_cken	VEDU clock gating 0: disabled 1: enabled
[0]	RW	vedu_srst_req	VEDU soft reset request 0: deassert reset 1: reset

PERI_CRG18

PERI_CRG18 is a VPSS clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x0048	PERI_CRG18	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vps_clksel		vpsclk_loaden		vpsclk_skipcfg				reserved		vps_cken	vps_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved
[11:10]	RW	vps_clksel	VPSS clock selection 00: 148.5 MHz 01: 198 MHz 10: 250 MHz 11: reserved
[9]	RW	vpsclk_loaden	Skip configuration enable for the VPSS clock To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	vpsclk_skipcfg	Skip configuration of the VPSS clock N: *N*-beat clocks are disabled for every 32-beat VPSS clocks.
[3:2]	RW	reserved	Reserved
[1]	RW	vps_cken	VPSS clock gating register 0: disabled 1: enabled
[0]	RW	vps_srst_req	VPSS soft reset request 0: deassert reset 1: reset

PERI_CRG23

PERI_CRG23 is a VGS clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x005C	PERI_CRG23	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vgs_clksel		vgsclk_loaden		vgsclk_skipcfg				reserved		vgs_cken	vgs_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved
[11:10]	RW	vgs_clksel	VGS clock selection 00: 198 MHz 01: 250 MHz 10: 297 MHz 11: 396 MHz
[9]	RW	vgsclk_loaden	Skip configuration enable for the VGS clock To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[8:4]	RW	vgsclk_skipcfg	Skip configuration of the VGS clock N: *N*-beat clocks are disabled for every 32-beat VGS clocks.
[3:2]	RW	reserved	Reserved
[1]	RW	vgs_cken	VGS clock gating register 0: disabled 1: enabled
[0]	RW	vgs_srst_req	VGS soft reset request 0: deassert reset 1: reset

PERI_CRG24

PERI_CRG24 is a JPGE clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0060	PERI_CRG24	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														jpge_cken	jpge_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved
[1]	RW	jpge_cken	JPGE clock gating 0: disabled 1: enabled
[0]	RW	jpge_srst_req	JPGE soft reset request 0: deassert reset 1: reset

PERI_CRG26

PERI_CRG26 is an LCD clock control register.

Offset Address	Register Name	Total Reset Value
0x0068	PERI_CRG26	0x005D_1746

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								lcd_mclk_div																							
Reset	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0	0	1	0	1	1	1	0	1	0	0	0	1	1	0

Bits	Access	Name	Description
[31:27]	RW	reserved	Reserved
[26:0]	RW	lcd_mclk_div	Frequency division coefficient of the LCD clock

PERI_CRG27

PERI_CRG27 is an IVE&HASH clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x006C	PERI_CRG27	0x0000_0033

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										hash_cken	hash_srst_req	ive_clksel		ive_cken	ive_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1

Bits	Access	Name	Description
[31:6]	RW	reserved	Reserved
[5]	RW	hash_cken	Hash clock gating 0: disabled 1: enabled
[4]	RW	hash_srst_req	Hash soft reset request 0: deassert reset 1: reset
[3:2]	RW	ive_clksel	IVE clock selection 00: 198 MHz 01: 250 MHz 10: 297 MHz 11: reserved
[1]	RW	ive_cken	IVE clock gating 0: disabled 1: enabled
[0]	RW	ive_srst_req	IVE soft reset request 0: deassert reset 1: reset

PERI_CRG28

PERI_CRG28 is a VICAP/VPSS online mode clock configuration register.

Offset Address	Register Name	Total Reset Value
0x0070	PERI_CRG28	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						viclk_loaden	viclk_skipcfg
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:6]	RW	reserved	Reserved
[5]	RW	viclk_loaden	VICAP/VPSS online mode clock skip enable To change the skip configuration, perform the following steps: 1. Write a new skip configuration value. 2. Write 0 to loaden. 3. Write 1 to loaden.
[4:0]	RW	viclk_skipcfg	VICAP/VPSS online mode clock skip configuration N: *N*-beat clocks are disabled for every 32-beat VICAP/VPSS online mode clocks.

PERI_CRG31

PERI_CRG31 is an LSADC & cipher clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x007C	PERI_CRG31	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							lsadc_srst_req	cipher_clksel	cipher_cken	cipher_srst_req
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:4]	RW	reserved	Reserved

[3]	RW	sar_adc_srst_req	LSADC soft reset request 0: deassert reset 1: reset
[2]	RW	cipher_clksel	Cipher clock selection 0: 198 MHz 1: 148.5 MHz
[1]	RW	cipher_cken	Cipher clock gating 0: disabled 1: enabled
[0]	RW	cipher_srst_req	Cipher soft reset request 0: deassert reset 1: reset

PERI_CRG35

PERI_CRG35 is an AIAO clock and reset control register.

Offset Address	Register Name	Total Reset Value
0x008C	PERI_CRG35	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														aiao_cken	aiao_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved
[1]	RW	aiao_cken	AIAO clock gating 0: disabled 1: enabled
[0]	RW	aiao_srst_req	AIAO soft reset request 0: deassert reset 1: reset

PERI_CRG46

PERI_CRG46 is a USB2.0 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00B8	PERI_CRG46	0x0002_7FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														usb2_phy_test_srst_req	reserved	usb2_phy_clksel	usb2_phy_port0_treq	usb2_phy_req	usb2_otg_phy_srst_req	usb2_hst_phy_srst_req	reserved	usb2_utmi0_srst_req	usb2_bus_srst_req	usb2_phy_cken	reserved	usb2_utmi0_cken	usb2_hst_phy_cken	usb2_otg_utmi_cken	usb2_ohci12m_cken	usb2_ohci48m_cken	usb2_bus_cken
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:18]	RW	reserved	Reserved
[17]	RW	usb2_phy_test_srst_req	USB2.0 PHY TEST soft reset request 0: deassert reset 1: reset
[16]	RW	reserved	Reserved
[15]	RW	usb2_phy_clksel	Clock source of the USB2.0 controller 0: provided by the PHY 1: provided by the CRG
[14]	RW	usb2_phy_port0_treq	USB2.0 PHY port0 soft reset request 0: deassert reset 1: reset
[13]	RW	usb2_phy_req	USB2.0 PHY soft reset request 0: deassert reset 1: reset
[12]	RW	usb2_otg_phy_srst_req	USB2.0 controller OTG_PHY soft reset request 0: deassert reset 1: reset
[11]	RW	usb2_hst_phy_srst_req	USB2.0 controller HST_PHY soft reset request 0: deassert reset 1: reset
[10]	RW	reserved	Reserved

[9]	RW	usb2_utmi0_srst_req	USB2.0 controller UTMI0 soft reset request 0: deassert reset 1: reset
[8]	RW	usb2_bus_srst_req	USB2.0 controller bus soft reset request 0: deassert reset 1: reset
[7]	RW	usb2_phy_cken	Clock gating of the USB2.0 PHY reference clock 0: disabled 1: enabled
[6]	RW	reserved	Reserved
[5]	RW	usb2_utmi0_cken	USB2.0 controller UTMI0 clock gating 0: disabled 1: enabled
[4]	RW	usb2_hst_phy_cken	USB2.0 controller HST_PHY clock gating 0: disabled 1: enabled
[3]	RW	usb2_otg_utmi_cken	USB2.0 controller OTG_UTMI clock gating 0: disabled 1: enabled
[2]	RW	usb2_ohci12m_cken	USB2.0 controller OHCI12 MHz clock gating 0: disabled 1: enabled
[1]	RW	usb2_ohci48m_cken	USB2.0 controller OHCI48 MHz clock gating 0: disabled 1: enabled
[0]	RW	usb2_bus_cken	USB2.0 controller bus clock gating 0: disabled 1: enabled

PERI_CRG48

PERI_CRG48 is an FMC clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C0	PERI_CRG48	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												fmc_clksel			fmc_cken	fmc_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved
[4:2]	RW	fmc_clksel	FMC clock source. (In SDR mode, the FMC clock output by the chip is the divide-by-2 clock of this clock; in DDR mode, it is the divide-by-4 clock of the original clock.) 000: 24 MHz 001: 83.3 MHz 010: 148.5 MHz 011: 198 MHz (only for the DDR mode) 1X0: 297 MHz (only for the DDR mode) 1X1: reserved
[1]	RW	fmc_cken	FMC clock gating 0: disabled 1: enabled
[0]	RW	fmc_srst_req	FMC soft reset request 0: deassert reset 1: reset

PERI_CRG49

PERI_CRG49 is an eMMC/SDIO0/SDIO1 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C4	PERI_CRG49	0x0002_0202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								emmc_clk_mode	reserved		emmc_clksel		reserved		emmc_cken	emmc_srst_req	sdio1_clk_mode	reserved		sdio1_clksel		reserved		sdio1_cken	sdio1_srst_req	sdio0_clk_mode	reserved		sdio0_clksel		reserved		sdio0_cken	sdio0_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved
[23]	RW	emmc_clk_mode	eMMC phase 0: normal 1: reserved
[22]	RW	reserved	Reserved
[21:20]	RW	emmc_clksel	eMMC working clock 00: 99 MHz 01: reserved 10: 49.5 MHz 11: reserved
[19:18]	RW	reserved	Reserved
[17]	RW	emmc_cken	eMMC clock gating 0: disabled 1: enabled
[16]	RW	emmc_srst_req	eMMC soft reset request 0: deassert reset 1: reset
[15]	RW	sdio1_clk_mode	SDIO1 phase 0: normal 1: reserved
[14]	RW	reserved	Reserved
[13:12]	RW	sdio1_clksel	SDIO1 working clock 00: 49.5 MHz 01: reserved 10: reserved 11: reserved

[11:10]	RW	reserved	Reserved
[9]	RW	sdio1_cken	SDIO1 clock gating 0: disabled 1: enabled
[8]	RW	sdio1_srst_req	SDIO1 soft reset request 0: deassert reset 1: reset
[7]	RW	sdio0_clk_mode	SDIO0 phase 0: normal 1: reserved
[6]	RW	reserved	Reserved
[5:4]	RW	sdio0_clksel	SDIO0 working clock select 00: 49.5 MHz 01: reserved 10: reserved 11: reserved
[3:2]	RW	reserved	Reserved
[1]	RW	sdio0_cken	SDIO0 clock gating 0: disabled 1: enabled
[0]	RW	sdio0_srst_req	SDIO0 soft reset request 0: deassert reset 1: reset

PERI_CRG50

PERI_CRG50 is SDIO2 clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00C8	PERI_CRG50	0x0000_0002

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5 4	3 2	1	0
Name	reserved						sdio2_clk_mode	reserved	sdio2_clksel	reserved	sdio2_cken	sdio2_srst_req

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7]	RW	sdio2_clk_mode	SDIO2 phase 0: normal 1: reserved
[6]	RW	reserved	Reserved
[5:4]	RW	sdio2_clksel	SDIO2 working clock 00: 49.5 MHz 01: reserved 10: reserved 11: reserved
[3:2]	RW	reserved	Reserved
[1]	RW	sdio2_cken	SDIO2 clock gating 0: disabled 1: enabled
[0]	RW	sdio2_srst_req	SDIO2 soft reset request 0: deassert reset 1: reset

PERI_CRG53

PERI_CRG53 is a GZIP clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D4	PERI_CRG53	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				reserved				gzip_srst_req	reserved				gzip_pcken	gzip_acken	gzip_cken	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:11]	RW	reserved	Reserved
[10:8]	RW	reserved	Reserved

[7]	RW	gzip_srst_req	GZIP soft reset request 0: deassert reset 1: reset
[6:3]	RW	reserved	Reserved
[2]	RW	gzip_pcken	GZIP APB clock gating 0: disabled 1: enabled
[1]	RW	gzip_acken	GZIP AXI clock gating 0: disabled 1: enabled
[0]	RW	gzip_cken	GZIP clock gating 0: disabled 1: enabled

PERI_CRG54

PERI_CRG54 is a DMAC/DDR TEST clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00D8	PERI_CRG54	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dmac_cken	dmac_srst_req	ddrtest_cken	ddrtest_srst_req	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:6]	RW	reserved	Reserved
[5]	RW	dmac_cken	DMAC clock gating 0: disabled 1: enabled
[4]	RW	dmac_srst_req	DMAC soft reset request 0: deassert reset 1: reset
[3]	RW	ddrtest_cken	DDR TEST clock gating 0: disabled 1: enabled

[2]	RW	ddrtest_srst_req	DDR TEST soft reset request 0: deassert reset 1: reset
[1]	RO	reserved	Reserved
[0]	RO	reserved	Reserved

PERI_CRG55

PERI_CRG55 is an SoC SW feedback indicator register.

Offset Address	Register Name	Total Reset Value
0x00DC	PERI_CRG55	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										cpu_sc_seled		ddr_sc_seled		reserved		apb_sc_seled	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RO	cpu_sc_seled	CPU clock switch completion indicator 00: The clock is switched to the crystal oscillator clock. 01: The clock is switched to the APLL FOUTPOSTDIV clock. 10: The clock is switched to the APLL FOUTVCO divide-by-2 clock. 11: The clock is switched to the 594 MHz clock.
[3:2]	RO	ddr_sc_seled	DDR clock switch completion indicator 00: The clock is switched to the crystal oscillator clock. 01: The clock is switched to the APLL FOUTPOSTDIV frequency division clock. 10: The clock is switched to the 250 MHz clock. 11: The clock is switched to the 198 MHz clock.
[1]	RO	reserved	Reserved
[0]	RO	apb_sc_seled	SYSAPB clock switch completion indicator 0: The clock is switched to the crystal oscillator clock. 1: The clock is switched to the 50 MHz clock.

PERI_CRG_PLL 56

PERI_CRG_PLL56 is a GZIP reset status register.

Offset Address	Register Name	Total Reset Value
0x00E0	PERI_CRG_PLL56	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															gzip_rst_ok
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	gzip_rst_ok	GZIP reset status 0: deassert reset 1: reset

PERI_CRG57

PERI_CRG57 is a soft reset control register for other CRG interface modules.

Offset Address	Register Name	Total Reset Value
0x00E4	PERI_CRG57	0x0403_F001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			pmc_srst_req	reserved		i2c1_srst_req	reserved	i2c0_srst_req	reserved			uart_clksel	reserved	uart2_cken	uart1_cken	uart0_cken	ssp1_cken	ssp0_cken	ir_cken	reserved		uart2_srst_req	uart1_srst_req	uart0_srst_req	ssp1_srst_req	ssp0_srst_req	ir_srst_req	reserved	rtc_srst_req	reserved	test_clk_en
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:29]	RW	reserved	Reserved
[28]	RW	pmc_srst_req	PMC soft reset request 0: deassert reset 1: reset
[27:26]	RW	reserved	Reserved

[25]	RW	i2c1_srst_req	I^2C1 soft reset request 0: deassert reset 1: reset
[24]	RW	reserved	Reserved
[23]	RW	i2c0_srst_req	I^2C0 soft reset request 0: deassert reset 1: reset
[22:20]	RW	reserved	Reserved
[19]	RW	uart_clksel	UART clock select 0: 24 MHz clock 1: 6 MHz clock
[18]	RW	reserved	Reserved
[17]	RW	uart2_cken	UART2 clock gating 0: disabled 1: enabled
[16]	RW	uart1_cken	UART1 clock gating 0: disabled 1: enabled
[15]	RW	uart0_cken	UART0 clock gating 0: disabled 1: enabled
[14]	RW	ssp1_cken	SSP1 clock gating 0: disabled 1: enabled
[13]	RW	ssp0_cken	SSP0 clock gating 0: disabled 1: enabled
[12]	RW	ir_cken	IR clock gating 0: disabled 1: enabled
[11:10]	RW	reserved	Reserved
[9]	RW	uart2_srst_req	UART2 soft reset request 0: deassert reset 1: reset
[8]	RW	uart1_srst_req	UART1 soft reset request 0: deassert reset 1: reset

[7]	RW	uart0_srst_req	UART0 soft reset request 0: deassert reset 1: reset
[6]	RW	ssp1_srst_req	SSP1 soft reset request 0: deassert reset 1: reset
[5]	RW	ssp0_srst_req	SSP0 soft reset request 0: deassert reset 1: reset
[4]	RW	ir_srst_req	IR soft reset request 0: deassert reset 1: reset
[3]	RW	reserved	Reserved
[2]	RW	rtc_srst_req	Soft reset request of the external temperature sensor controller in the RTC 0: deassert reset 1: reset
[1]	RW	reserved	Reserved
[0]	RW	test_clk_en	Test clock enable 0: All test clocks are disabled. 1: All test clocks are enabled.

PERI_CRG58

PERI_CRG58 is a CRG status register.

Offset Address	Register Name	Total Reset Value
0x00E8	PERI_CRG58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													epll_lock	vpll_lock	apll_lock
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved

[2]	RO	epll_lock	EPLL lock status 0: unlocked 1: locked
[1]	RO	vpll_lock	VPLL lock status 0: unlocked 1: locked
[0]	RO	apll_lock	APLL lock status 0: unlocked 1: locked

PERI_CRG59

PERI_CRG59 is an ETH clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x00EC	PERI_CRG59	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ethcore_clksel	reserved	ethphy_clksel		ext_fephy_srst_req	ethrmii_clksel	eth_cken	hrst_eth_s
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:8]	RW	reserved	Reserved
[7]	RW	ethcore_clksel	ETH clock source select 0: 99 MHz 1: 54 MHz
[6]	RW	reserved	Reserved
[5:4]	RW	ethphy_clksel	ETH PHY output clock source select 00: 25 MHz 01: 24 MHz 1x: 27 MHz
[3]	RW	ext_fephy_srst_req	EPHY soft reset request 0: deassert reset 1: reset

[2]	RW	ethrmii_clksel	ETH RMII clock source select 0: internal CRG clock 1: PAD input clock
[1]	RW	eth_cken	ETH clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	hrst_eth_s	ETH soft reset request 0: deassert reset 1: reset

PERI_CRG64

PERI_CRG64 is an RSA clock and soft reset control register.

Offset Address	Register Name	Total Reset Value
0x0100	PERI_CRG64	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										rsa_cken	rsa_srst_req	trng_cken	trng_srst_req	klad_cken	klad_srst_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:6]	RW	reserved	Reserved
[5]	RW	rsa_cken	RSA clock gating 0: The clock is disabled. 1: The clock is enabled.
[4]	RW	rsa_srst_req	RSA soft reset request 0: deassert reset 1: reset
[3]	RW	trng_cken	TRNG clock gating 0: The clock is disabled. 1: The clock is enabled.
[2]	RW	trng_srst_req	TRNG soft reset request 0: deassert reset 1: reset

[1]	RW	klad_cken	KLAD clock gating 0: The clock is disabled. 1: The clock is enabled.
[0]	RW	klad_srst_req	KLAD soft reset request 0: deassert reset 1: reset

PERI_CRG66

PERI_CRG66 is an APLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x0108	PERI_CRG66	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				apll_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:13]	RW	reserved	Reserved
[12:0]	RW	apll_ssmod_cfg	ssmod divval[12:9]: SSMOD divval control 0x0: not divided 0x1: not divided 0x2: divided by 2 0x3: divided by 3 ... 0xF: divided by 15 ssmod spread[8:4]: SSMOD spread control 0x0: 0 0x1: 0.1% 0x 2: 0.2% 0x 3: 0.3% 0x 4: 0.4% 0x 5: 0.5% 0x 6: 0.6% 0x 7: 0.7% ... 0x1F: 3.1% ssmod downspread[3]: SSMOD downspread control 0: central spread spectrum 1: down spread spectrum

			ssmod_disable[2]: SSMOD disable control 0: enabled 1: disabled ssmod_rst_req[1]: SSMOD reset control 0: not reset 1: reset ssmod_cken[0]: SSMOD clock gating 0 (default): disabled 1: enabled

PERI_CRG68

PERI_CRG68 is a VPLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x0110	PERI_CRG68	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vpll_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:13]	RW	reserved	Reserved
[12:0]	RW	vpll_ssmod_ctrl	ssmod divval[12:9]: SSMOD divval control 0x0: not divided 0x1: not divided 0x2: divided by 2 0x3: divided by 3 ... 0xF: divided by 15 ssmod spread[8:4]: SSMOD spread control 0x0: 0 0x1: 0.1% 0x2: 0.2% 0x3: 0.3% 0x4: 0.4% 0x5: 0.5% 0x6: 0.6% 0x7: 0.7% ... 0x1F: 3.1%

			ssmod downspread[3]: SSMOD downspread control 0: central spread spectrum 1: down spread spectrum ssmod_disable[2]: SSMOD disable control 0: enabled 1: disabled ssmod_rst_req[1]: SSMOD reset control 0: not reset 1: reset ssmod_cken[0]: SSMOD clock gating 0 (default): disabled 1: enabled

PERI_CRG70

PERI_CRG70 is an EPLL spread spectrum configuration register.

Offset Address	Register Name	Total Reset Value
0x0118	PERI_CRG70	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				epll_ssmod_cfg											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:13]	RW	reserved	Reserved
[12:0]	RW	epll_ssmod_cfg	ssmod divval[12:9]: SSMOD divval control 0x0: not divided 0x1: not divided 0x2: divided by 2 0x3: divided by 3 ... 0xF: divided by 15 ssmod spread[8:4]: SSMOD spread control 0x0: 0 0x1: 0.1% 0x2: 0.2% 0x3: 0.3% 0x4: 0.4% 0x5: 0.5% 0x6: 0.6%

			0x7: 0.7% ... 0x1F: 3.1% ssmod downspread[3]: SSMOD downspread control 0: central spread spectrum 1: down spread spectrum ssmod_disable[2]: SSMOD disable control 0: enabled 1: disabled ssmod_rst_req[1]: SSMOD reset control 0: not reset 1: reset ssmod_cken[0]: SSMOD clock gating 0: disabled (default) 1: enabled

3.3 Processor Subsystem

Hi3516C V300 has an embedded processor ARM926EJ-S, which has the following features:

- 32-bit ARM v5TEJ and 5-stage pipeline, compatible with the 32-bit ARM and the 16-bit thumb instruction set
- Independent 32 KB I-cache, 32 KB D-cache, and 4-way set-associative cache. The cache line size is 32 bytes. The D-cache supports configurable write-back and write-through operations.
- Configurable pseudo-random or round-robin replacement algorithm for the cache
- Memory management unit (MMU)
- Little-endian mode
- Fast interrupt requests (FIQs) and interrupt requests (IRQs)
- Joint Test Action Group (JTAG) debugging interface

3.4 Interrupt System

3.4.1 Interrupt Source Allocation

Table 3-8 describes the allocation of ARM9 interrupt sources.

Table 3-8 Allocation of ARM9 interrupt sources

ARM9	Interrupt Source
0	Global soft interrupt
1	WatchDog
2	RTC
3	Timer0/Timer1
4	Timer2/Timer3
5	UART0
6	SSP0
7	SSP1
8	GZIP/DDRT
9	AIAO
10	USB_DEVICE
11	FMC/eMMC
12	ETH
13	CIPHER
14	DMAC
15	USB_EHCI
16	USB_OHCI
17	VPSS
18	SDIO0
19	IR/LSADC
20	I^2C0/I^2C1
21	IVE
22	VICAP
23	VDP
24	VEDU
25	UART2
26	JPGE
27	SDIO1/SDIO2
28	MIPI
29	VGS

ARM9	Interrupt Source
30	UART1
31	GPIO0−GPIO8

3.4.2 Register Summary

Table 3-9 describes interrupt control registers.

Table 3-9 Summary of interrupt control registers (base address: 0x1004_0000)

Offset Address	Register	Description	Page
0x000	INT_IRQSTATUS	IRQ interrupt status register	3-51
0x004	INT_FIQSTATUS	FIQ interrupt status register	3-52
0x008	INT_RAWINTR	Raw interrupt status register	3-52
0x00C	INT_INTSELECT	Interrupt source select register	3-53
0x010	INT_INTENABLE	Interrupt enable register	3-53
0x014	INT_INTENCLEAR	Interrupt enable clear register	3-54
0x018	INT_SOFTINT	Software interrupt register	3-54
0x01C	INT_SOFTINTCLEAR	Software interrupt clear register	3-55
0x020	INT_PROTECTION	Protection enable register	3-55

3.4.3 Register Description

INT_IRQSTATUS

INT_IRQSTATUS is an IRQ interrupt status register. The 32 bits correspond to 32 interrupt sources. For details, see Table 3-8.

Offset Address	Register Name	Total Reset Value
0x000	INT_IRQSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	irqstatus																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	irqstatus	Status of the IRQ interrupt source 0: No interrupt is generated. 1: An IRQ interrupt is generated and sent to the processor.

INT_FIQSTATUS

INT_FIQSTATUS is an FIQ interrupt status register. The 32 bits correspond to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x004	INT_FIQSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fiqstatus																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fiqstatus	Status of the FIQ interrupt source 0: No interrupt is generated. 1: An FIQ interrupt is generated and sent to the processor.

INT_RAWINTR

INT_RAWINTR is a raw interrupt status register. It shows the status of raw interrupt requests and the status of the software interrupts that are generated by configuring INT_SOFTINT. The 32 bits correspond to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x008	INT_RAWINTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rawinterrupt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rawinterrupt	Status of the raw interrupt source request 0: No interrupt is generated. 1: An interrupt is generated.

INT_INTSELECT

INT_INTSELECT is an interrupt source select register. It determines whether the selected interrupt source generates the IRQ interrupt or FIQ interrupt. The 32 bits correspond to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x00C	INT_INTSELECT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intselect																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	intselect	Interrupt request type of the interrupt source 0: IRQ interrupt 1: FIQ interrupt

INT_INTENABLE

INT_INTENABLE is an interrupt enable register. It is used to enable interrupt request lines. During reset, the value of INT_INTENABLE is changed to 0x0000_0000. As a result, all interrupt sources are masked. The 32 bits correspond to 32 interrupt sources.

Offset Address	Register Name	Total Reset Value
0x010	INT_INTENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intenable																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	intenable	The mask status of each interrupt source is returned when this register is read. 0: masked 1: not masked The interrupt source is enabled by bit when this register is written. 0: The current value of the corresponding bit is not affected. 1: The corresponding bit is set to 1 to enable the corresponding interrupt request.

INT_INTENCLEAR

INT_INTENCLEAR is an interrupt enable clear register. It is used to clear the corresponding bits of INT_INTENABLE. INT_INTENCLEAR is write-only and has no default reset value.

Offset Address	Register Name	Total Reset Value
0x014	INT_INTENCLEAR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intenableclear																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	intenableclear	Mask of the interrupt source corresponding to INT_INTENABLE 0: The current value of the corresponding bit of INT_INTENABLE is not affected. 1: The corresponding bit of INT_INTENABLE is cleared and the corresponding interrupt request is masked.

INT_SOFTINT

INT_SOFTINT is a software interrupt register. It controls whether the interrupt source input line generates software interrupts by using software. The software interrupts can be cleared by writing INT_SOFTINTCLEAR after the interrupt service routine (ISR) ends.

Offset Address	Register Name	Total Reset Value
0x018	INT_SOFTINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softint																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	softint	Generation of a raw software interrupt on a specified interrupt source 0: The current value of the corresponding bit is not affected. 1: The corresponding bit is set to 1 and a software interrupt request is generated.

INT_SOFTINTCLEAR

INT_SOFTINTCLEAR is a software interrupt clear register. It is used to clear the corresponding bit of INT_SOFTINT. INT_SOFTINTCLEAR is write-only and has no default reset value.

Offset Address	Register Name	Total Reset Value
0x01C	INT_SOFTINTCLEAR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softintclear																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	softintclear	Mask of the interrupt request corresponding to INT_SOFTINT 0: The corresponding bit of INT_SOFTINT is not affected. 1: The corresponding bit of INT_SOFTINT is cleared and the corresponding interrupt request is masked.

INT_PROTECTION

INT_PROTECTION is a protection enable register. It is used to enable or disable the access to protected registers.

CAUTION

- This register is cleared during reset and the INT registers can be accessed in user mode or privileged mode.

- When the CPU fails to generate the correct protection information (HPROT), the INT registers can be accessed in user mode after this register is reset.

Offset Address	Register Name	Total Reset Value
0x020	INT_PROTECTION	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															protection
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	protection	Register access protection enable 0: disabled. The CPU can access INT registers in user mode or privileged mode. 1: enabled. The CPU can access INT registers only in privileged mode.

3.5 System Controller

3.5.1 Overview

The system controller manages important system functions and configures some functions of the peripherals.

3.5.2 Features

The system controller has the following features:

- Controls the system address remap and monitors its status.
- Provides general peripheral registers
- Provides write protection for key registers.
- Provides chip identification (ID) registers.

3.5.3 Function Description

3.5.3.1 Soft Reset

The system controller can soft-reset the entire chip.

After the global soft reset register SC_SYSRES is configured, the system controller transmits a reset request to the on-chip reset module for setting the Hi3516C V300.

3.5.3.2 System Address Remap Control

For details, see section 1.4 "Address Space Mapping."

3.5.3.3 Write Protection for Key Registers

To prevent the entire system from being affected by misoperation on the system controller, the system controller provides write protection for the key configuration register: global soft reset control register SC_SYSRES. You must configure SC_LOCKEN to enable the write permission before writing to SC_SYSRES. After the write operation is complete, you need to disable the write permission by configuring SC_LOCKEN, ensuring that SC_SYSRES is not incorrectly written by software.

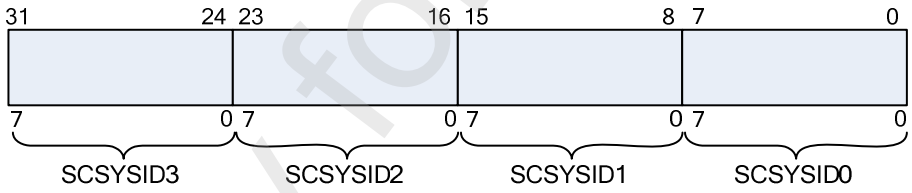
NOTE

By default, write protection is not enabled for key registers after reset. You are advised to enable write protection by configuring SC_LOCKEN when the system starts.

3.5.3.4 System ID Register of the Chip

The system controller provides a chip ID register SC_SYSID. This register is a virtual 32-bit read-only register. It consists of four 8-bit ID registers: SCSYSID3, SCSYSID2, SCSYSID1, and SCSYSID0. After the values of these four registers are read and combined, the value of SC_SYSID, namely, 0x3516_C300, is obtained. Figure 3-5 shows the bit allocation of chip ID registers.

Figure 3-5 Bit allocation of chip ID registers



3.5.4 System Controller Registers

3.5.4.1 Register Summary

Table 3-10 describes system controller registers.

Table 3-10 Summary of system controller registers (base address: 0x1202_0000)

Offset Address	Register	Description	Page
0x0000	SC_CTRL	System control register	3-58
0x0004	SC_SYSRES	System soft reset register	3-59
0x001C	SOFTINT	Software interrupt register	3-60
0x0044	SC_LOCKEN	Key register lock register	3-60

Offset Address	Register	Description	Page
0x008C	SYSSTAT	System status register	3-61
0x0EE0	SCSYSID0	Chip ID register 0	3-62
0x0EE4	SCSYSID1	Chip ID register 1	3-62
0x0EE8	SCSYSID2	Chip ID register 2	3-62
0x0EEC	SCSYSID3	Chip ID register 3	3-63

3.5.4.2 Register Description

SC_CTRL

SC_CTRL is a system control register. It is used to specify the operations to be performed by the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address: 0x0000 | Register Name: SC_CTRL | Total Reset Value: 0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									timeren3ov	reserved	timeren2ov	reserved	timeren1ov	reserved	timeren0ov	reserved						remapstat	remapclear	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:23]	RW	reserved	Reserved
[22]	RW	timeren3ov	Timer 3 count clock select 0: 3 MHz clock 1: bus (50 MHz) clock
[21]	RW	reserved	Reserved

[20]	RW	timeren2ov	Timer 2 count clock select 0: 3 MHz clock 1: bus (50 MHz) clock
[19]	RW	reserved	Reserved
[18]	RW	timeren1ov	Timer 1 count clock select 0: 3 MHz clock 1: bus (50 MHz) clock
[17]	RW	reserved	Reserved
[16]	RW	timeren0ov	Timer 0 count clock select 0: 3 MHz clock 1: bus (50 MHz) clock
[15:10]	RW	reserved	Reserved
[9]	RO	remapstat	Address remap status 0: The address is not remapped. 1: The address is remapped. The BOOTROM, NANDC CS0, or SFC CS1 is remapped to address 0.
[8]	RW	remapclear	Address remap clear 0: The remap status is retained. 1: The remap status is cleared. For details about the address mapping relationships before and after remapping is cleared, see section 1.3 "Boot Mode" and section 1.3.4 "Address Space Mapping" in chapter 1.
[7:0]	RO	reserved	Reserved, Reading this field returns 0, and writing to this field has no effect.

SC_SYSRES

SC_SYSRES is a system soft reset register. When a value is written to this register, the system controller sends a system soft reset request to the reset module. Then the reset module resets the system.

CAUTION

Write protection for this register can be enabled by configuring SC_LOCKEN. This register can be written only when write protection is disabled.

Offset Address	Register Name	Total Reset Value
0x0004	SC_SYSRES	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	softresreq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:0]	WO	softresreq	Writing any value to this register soft-resets the system.

SOFTINT

SOFTINT is a software interrupt register.

Offset Address	Register Name	Total Reset Value
0x001C	SOFTINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															software_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	software_int	Writing 1 to this bit generates the software interrupt.

SC_LOCKEN

SC_LOCKEN is a key register lock registers.

Offset Address	Register Name	Total Reset Value
0x0044	SC_LOCKEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	scper_lockl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	scper_lockl	Register for locking key system control registers. The key registers include SC_CTRL and SC_SYSRES.

			When 0x1ACC_E551 is written to SC_LOCKEN, the write permission for all registers is enabled; when any other value is written to SC_LOCKEN, the write permission is disabled. Reading this register returns the lock status but not the written value. 0x0000_0000: The write permission is enabled (unlocked). 0x0000_0001: The write permission is disabled (locked).

SYSSTAT

SYSSTAT is a system status register.

Offset Address	Register Name	Total Reset Value
0x008C	SYSSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				arm9_standbywfi	reserved																	update_mode	secure_boot_mode	sfc_addr_mode	sfc_device_mode	boot_mode	reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RO	arm9_standbywfi	WFI state of the CPU, active high
[25:10]	RO	reserved	Reserved
[9]	RO	update_mode	Update mode flag 0: non-update mode 1: update mode
[8]	RO	secure_boot_mode	Secure boot mode flag 0: non-secure boot 1: secure boot
[7]	RO	sfc_addr_mode	Boot address mode of the SPI NOR flash (when sfc_device_mode is 0) 0: 3-byte mode 1: 4-byte mode Boot mode of the SPI NAND flash (when sfc_device_mode is 1) 0: 1-wire boot mode 1: 4-wire boot mode

[6]	RO	sfc_device_mode	SPI flash component type 0: SPI NOR flash 1: SPI NAND flash
[5:4]	RO	boot_mode	Chip boot mode 00: The chip boots from the SPI flash. 01: The chip boots from the eMMC. 10: FastBoot for updating the SPI flash. 11: FastBoot for updating the eMMC.
[3:0]	RO	reserved	Reserved

SCSYSID0

SCSYSID0 is chip ID register 0.

Offset Address	Register Name	Total Reset Value
0x0EE0	SCSYSID0	0x00

Bit	7	6	5	4	3	2	1	0
Name	sysid0							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	sysid0	Reading this register returns 0x00.

SCSYSID1

SCSYSID1 is chip ID register 1.

Offset Address	Register Name	Total Reset Value
0x0EE4	SCSYSID1	0xC3

Bit	7	6	5	4	3	2	1	0
Name	sysid1							
Reset	1	1	0	0	0	0	1	1

Bits	Access	Name	Description
[7:0]	RO	sysid1	Reading this register returns 0xC3.

SCSYSID2

SCSYSID2 is chip ID register 2.

Offset Address	Register Name	Total Reset Value
0x0EE8	SCSYSID2	0x16

Bit	7	6	5	4	3	2	1	0
Name	sysid2							
Reset	0	0	0	1	0	1	1	0

Bits	Access	Name	Description
[7:0]	RO	sysid2	Reading this register returns 0x16.

SCSYSID3

SCSYSID3 is chip ID register 3.

Offset Address	Register Name	Total Reset Value
0x0EEC	SCSYSID3	0x35

Bit	7	6	5	4	3	2	1	0
Name	sysid3							
Reset	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[7:0]	RO	sysid3	Reading this register returns 0x35.

3.5.5 Peripheral Control Registers

3.5.5.1 Register Summary

Table 3-11 describes peripheral control registers.

Table 3-11 Summary of peripheral control registers (base address: 0x1203_0000)

Offset Address	Register	Description	Page
0x0000	MISC_CTRL0	MSIC function select register 0	3-65
0x000C	MISC_CTRL3	RAM Retention control register 0	3-67
0x0014	MISC_CTRL5	SYS bus control register 0	3-68
0x0018	MISC_CTRL6	SYS bus control register 1	3-69
0x001C	MISC_CTRL7	SYS bus control register 2	3-70
0x0020	MISC_CTRL8	SYS bus control register 3	3-71
0x0024	MISC_CTRL9	Media bus control register 0	3-72

Offset Address	Register	Description	Page
0x0028	MISC_CTRL10	Media bus control register 1	3-73
0x0030	MISC_CTRL12	Media bus control register 3	3-74
0x0034	MISC_CTRL13	VIVO bus control register 0	3-75
0x0038	MISC_CTRL14	VIVO bus control register 1	3-76
0x0040	MISC_CTRL16	VIVO bus control register 3	3-77
0x0044	MISC_CTRL17	DDR_QoS control register 0	3-78
0x0048	MISC_CTRL18	DDR_QoS control register 1	3-78
0x004C	MISC_CTRL19	DDR_QoS control register 2	3-79
0x0050	MISC_CTRL20	DDR_QoS control register 3	3-80
0x0054	MISC_CTRL21	DDR_QoS control register 4	3-80
0x0058	MISC_CTRL22	DDR_QoS control register 5	3-81
0x005C	MISC_CTRL23	USB2.0 control register 0	3-82
0x0060	MISC_CTRL24	USB2.0 control register 1	3-84
0x0064	MISC_CTRL25	USB2.0 control register 2	3-85
0x0078	MISC_CTRL30	SVB control register	3-86
0x007C	MISC_CTRL31	Core high performance monitor (HPM) control register 0	3-87
0x0080	MISC_CTRL32	Core HPM control register 1	3-88
0x0084	MISC_CTRL33	Core HPM status register 0	3-89
0x0088	MISC_CTRL34	Core HPM status register 1	3-90
0x008C	MISC_CTRL35	Media HPM control register 0	3-90
0x0090	MISC_CTRL36	Media HPM control register 1	3-91
0x0094	MISC_CTRL37	Media HPM status register 0	3-92
0x0098	MISC_CTRL38	Media HPM status register 1	3-93
0x009C	MISC_CTRL39	Temperature sensor (T-Sensor) control register	3-93
0x00A0	MISC_CTRL40	T-sensor status register	3-94
0x00A4	MISC_CTRL41	T-sensor temperature record register 0	3-95
0x00A8	MISC_CTRL42	T-sensor temperature record register 1	3-96
0x00AC	MISC_CTRL43	T-sensor temperature record register 2	3-96
0x00B0	MISC_CTRL44	T-sensor temperature record register 3	3-97

Offset Address	Register	Description	Page
0x00BC	MISC_CTRL47	Update mode clear register	3-97

3.5.5.2 Register Description

MISC_CTRL0

MISC_CTRL0 is MSIC function select register 0.

Offset Address	Register Name	Total Reset Value
0x0000	MISC_CTRL0	0x0020_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										vgs_bootram_mode	vo_pin_reverse	gzip_ddrt_sel	reserved			uart_txd_mask_by_lb	reserved	commtx_rx_int_en	reserved	reserved	test_clksel			vicap_vpss_online_mode	mipi_phy_mode		sspl_cs_sel	spi1_cs1_pctrl	spi1_cs0_pctrl	spi0_cs0_pctrl	reserved
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	reserved	Reserved
[21]	RW	vgs_bootram_mode	Enable of multiplexing the RAM of the VGS module as the boot RAM. This bit is set to 1 when the boot RAM is required, and it is set to 0 when the VGS function is used. 0: disabled 1: enabled
[20]	RW	vo_pin_reverse	Reverse output enable of the VO pin. When this bit is set to 1, the output of VOU656_DATA[7:0]/LCD_DATA[5:0] is reversed. 0: normal 1: reversed
[19]	RW	gzip_ddrt_sel	GZIP/DDRT function select 0: DDRT enabled and GZIP disabled 1: GZIP enabled and DDRT disabled
[18:17]	-	reserved	Reserved

[16]	RW	uart_txd_mask_by_lb	UART*_TXD pin mask when loopback is enabled 0: The UART*_TXD pin is not masked when loopback is enabled. 1: The UART*_TXDpin is masked when loopback is enabled, and it retains high-level output.
[15]	-	reserved	Reserved
[14]	RW	commtx_rx_int_en	CPU COMMTX/COMMRX interrupt enable control 0: disabled 1: enabled
[13]	RW	reserved	Reserved
[12]	RW	reserved	Reserved
[11:8]	RW	test_clksel	TEST_CLK source clock select 0000: PLL_TEST_OUT[0] 0001: PLL_TEST_OUT[1] 0010: PLL_TEST_OUT[2] 0011: PLL_TEST_OUT[3] 0100: CLK_TEST_OUT[0] 0101: CLK_TEST_OUT[1] 0110: CLK_TEST_OUT[2] 0111: CLK_TEST_OUT[3] 1000: CLK_24M 1001: CLK_RTC Other values: PLL_TEST_OUT[0]
[7]	RW	vicap_vpss_online_mode	VICAP&VPSS working mode select 0: offline mode 1: online mode
[6:5]	RW	mipi_phy_mode	MIPI PHY mode select 00: MIPI mode 01: LVDS mode 10: CMOS mode 11: reserved
[4]	RW	ssp1_cs_sel	SPI1 signal output CS select 0: CS0 1: CS1
[3]	RW	spi1_cs1_pctrl	Polarity control of SPI1 CS1 0: SPI1_CSN1 active low 1: SPI1_CSN1 active high

[2]	RW	spi1_cs0_pctrl	Polarity control of SPI1 CS0 0: SPI1_CSN0 active low 1: SPI1_CSN0 active high
[1]	RW	spi0_cs0_pctrl	Polarity control of the SPI0 CS 0: SPI0_CSN active low 1: SPI0_CSN active high
[0]	-	reserved	Reserved

MISC_CTRL3

MISC_CTRL3 is an RAM Retention control register 0.

Offset Address	Register Name	Total Reset Value
0x000C	MISC_CTRL3	0x8000_00EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	avc_ret1n_bypass	reserved																				bootrom_pgen	reserved		emmc_ret1n	sdio1_ret1n	sdio0_ret1n	reserved	usb_ret1n	ir_ret1n	cipher_ret1n	reserved
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31]	RW	avc_ret1n_bypass	Automatic RAM retention function control of the VEDU module 0: enabled 1: disabled
[30:11]	-	reserved	Reserved
[10]	RW	bootrom_pgen	Boot ROM power supply control 0: powered on 1: powered off. The boot ROM cannot work.
[9:8]	-	reserved	Reserved
[7]	RW	emmc_ret1n	RAM retention control of the eMMC 0: The eMMC RAM is in retention state. 1: The eMMC RAM is active. When the eMMC controller is disabled, this bit can be set to 0 to save power consumption.

[6]	RW	sdio1_ret1n	RAM retention control of SDIO1 0: The SDIO1 RAM is in retention state. 1: The SDIO1 RAM is active. When the SDIO1 controller is disabled, this bit can be set to 0 to save power consumption.
[5]	RW	sdio0_ret1n	RAM retention control of SDIO0 0: The SDIO0 RAM is in retention state. 1: The SDIO0 RAM is active. When the SDIO0 controller is disabled, this bit can be set to 0 to save power consumption.
[4]	-	reserved	Reserved
[3]	RW	usb_ret1n	RAM retention control of the USB 0: The USB RAM is in retention state. 1: The USB RAM is active. When the USB controller is disabled, this bit can be set to 0 to save power consumption.
[2]	RW	ir_ret1n	RAM retention control of the IR 0: The IR RAM is in retention state. 1: The IR RAM is active. When the IR controller is disabled, this bit can be set to 0 to save power consumption.
[1]	RW	cipher_ret1n	RAM retention control of the cipher 0: The Cipher RAM is in retention state. 1: The Cipher RAM is active. When the cipher controller is disabled, this bit can be set to 0 to save power consumption.
[0]	-	reserved	Reserved

MISC_CTRL5

MISC_CTRL5 is an SYS bus control register 0.

Offset Address	Register Name	Total Reset Value
0x0014	MISC_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysaxi_m2_timeout_en	sysaxi_m2_timeout_value															sysaxi_m1_timeout_en	sysaxi_m1_timeout_value														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sysaxi_m2_timeout_en	Timeout count enable of the SYS AXI bus port M2 (AHB master 0) 0: disabled 1: enabled
[30:16]	RW	sysaxi_m2_timeout_value	Timeout count of the SYS AXI bus port M2 (AHB master 0) Count value = sysaxi_timeout_value_m2 x 2
[15]	RW	sysaxi_m1_timeout_en	Timeout count enable of the SYS AXI bus port M1 (CPU) 0: disabled 1: enabled
[14:0]	RW	sysaxi_m1_timeout_value	Timeout count of the SYS AXI bus port M1 (CPU) Count value = sysaxi_timeout_value_m1 x 2

MISC_CTRL6

MISC_CTRL6 is an SYS bus control register 1.

Offset Address	Register Name	Total Reset Value
0x0018	MISC_CTRL6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sysaxi_m4_timeout_en	sysaxi_m4_timeout_value															sysaxi_m3_timeout_en	sysaxi_m3_timeout_value														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	sysaxi_m4_timeout_en	Timeout count enable of the SYS AXI bus port M4 (AHB master 2) 0: disabled 1: enabled
[30:16]	RW	sysaxi_m4_timeout_value	Timeout count of the SYS AXI bus port M4 (AHB master 2) Count value = sysaxi_timeout_value_m4 x 2
[15]	RW	sysaxi_m3_timeout_en	Timeout count enable of the SYSAXI bus port M3 (AHB master 1) 0: disabled 1: enabled
[14:0]	RW	sysaxi_m3_timeout_value	Timeout count of the SYS AXI bus port M3 (AHB master 1) Count value = sysaxi_timeout_value_m3 x 2

MISC_CTRL7

MISC_CTRL7 is an SYS bus control register 2.

Offset Address	Register Name	Total Reset Value
0x001C	MISC_CTRL7	0x0000_0012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	sysaxi_m4_pri			reserved			sysaxi_m3_pri				reserved				sysaxi_m2_pri				reserved				sysaxi_m1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:12]	RW	sysaxi_m4_pri	Priority of the SYS AXI bus port M4 (AHB master 2) The value 3 indicates the highest priority.
[11]	-	reserved	Reserved
[10:8]	RW	sysaxi_m3_pri	Priority of the SYS AXI bus port M3 (AHB master 1) The value 3 indicates the highest priority.
[7]	-	reserved	Reserved
[6:4]	RW	sysaxi_m2_pri	Priority of the SYS AXI bus port M2 (AHB master 0) The value 3 indicates the highest priority.
[3]	-	reserved	Reserved
[2:0]	RW	sysaxi_m1_pri	Priority of the SYS AXI bus port M1 (CPU) The value 3 indicates the highest priority.

MISC_CTRL8

MISC_CTRL8 is an SYS bus control register 3.

Offset Address	Register Name	Total Reset Value
0x0020	MISC_CTRL8	0x0000_0123

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	sysaxi_s4_pri			reserved			sysaxi_s3_pri			reserved			sysaxi_s2_pri			reserved			sysaxi_s1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:12]	RW	sysaxi_s4_pri	Bus access priority of the SYS AXI S4 (MDDRC) port The value 3 indicates the highest priority.
[11]	-	reserved	Reserved
[10:8]	RW	sysaxi_s3_pri	Bus access priority of the SYS AXI S3 (media APB) port The value 3 indicates the highest priority.
[7]	-	reserved	Reserved
[6:4]	RW	sysaxi_s2_pri	Bus access priority of the SYS AXI S2 (SYS APB) port The value 3 indicates the highest priority.
[3]	-	reserved	Reserved
[2:0]	RW	sysaxi_s1_pri	Bus access priority of the SYS AXI S1 (AHB_SUBSYS) port The value 3 indicates the highest priority.

MISC_CTRL9

MISC_CTRL9 is a MEDIA bus control register 0.

Offset Address	Register Name	Total Reset Value
0x0024	MISC_CTRL9	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mediaaxi_m2_timeout_en	mediaaxi_m2_timeout_value															mediaaxi_m1_timeout_en	mediaaxi_m1_timeout_value														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mediaaxi_m2_timeout_en	Timeout count enable of the media AXI bus port M2 (IVE) 0: disabled 1: enabled
[30:16]	RW	mediaaxi_m2_timeout_value	Timeout count of the media AXI bus port M2 (IVE) Count value = mediaaxi_timeout_value_m2 x 2
[15]	RW	mediaaxi_m1_timeout_en	Timeout count enable of the media AXI bus port M1 (VGS) 0: disabled 1: enabled
[14:0]	RW	mediaaxi_m1_timeout_value	Timeout count of the media AXI bus port M1 (VGS) Count value = mediaaxi_timeout_value_m1 x 2

MISC_CTRL10

MISC_CTRL10 is a MEDIA bus control register 1.

Offset Address	Register Name	Total Reset Value
0x0028	MISC_CTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mediaaxi_m4_timeout_en	mediaaxi_m4_timeout_value															mediaaxi_m3_timeout_en	mediaaxi_m3_timeout_value														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	mediaaxi_m4_timeout_en	Timeout count enable of the media AXI bus port M4 (DDRT/GZIP) 0: disabled 1: enabled
[30:16]	RW	mediaaxi_m4_timeout_value	Timeout count of the media AXI bus port M4 (DDRT/GZIP) Count value = mediaaxi_timeout_value_m4 x 2
[15]	RW	mediaaxi_m3_timeout_en	Timeout count enable of the media AXI bus port M3 (JPGE) 0: disabled 1: enabled
[14:0]	RW	mediaaxi_m3_timeout_value	Timeout count of the media AXI bus port M3 (JPGE) Count value = mediaaxi_timeout_value_m3 x 2

MISC_CTRL12

MISC_CTRL12 is a MEDIA bus control register 3.

Offset Address	Register Name	Total Reset Value
0x0030	MISC_CTRL12	0x0000_0123

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	mediaaxi_m4_pri			reserved			mediaaxi_m3_pri				reserved				mediaaxi_m2_pri				reserved				mediaaxi_m1_pri		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:12]	RW	mediaaxi_m4_pri	Priority of the media AXI bus port M4 (DDRT/GZIP) The value 3 indicates the highest priority.
[11]	-	reserved	Reserved
[10:8]	RW	mediaaxi_m3_pri	Priority of the media AXI bus port M3 (JPGE) The value 3 indicates the highest priority.
[7]	-	reserved	Reserved
[6:4]	RW	mediaaxi_m2_pri	Priority of the media AXI bus port M2 (IVE) The value 3 indicates the highest priority.
[3]	-	reserved	Reserved
[2:0]	RW	mediaaxi_m1_pri	Priority of the media AXI bus port M1 (VGS) The value 3 indicates the highest priority.

MISC_CTRL13

MISC_CTRL13 is a VIVO bus control register 0.

Offset Address	Register Name	Total Reset Value
0x0034	MISC_CTRL13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vivoaxi_m2_timeout_en	vivoaxi_m2_timeout_value															vivoaxi_m1_timeout_en	vivoaxi_m1_timeout_value														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vivoaxi_m2_timeout_en	Timeout count enable of the VIVO AXI bus port M2 (AIAO) 0: disabled 1: enabled
[30:16]	RW	vivoaxi_m2_timeout_value	Timeout count of the VIVO AXI bus port M2 (AIAO) Count value = vivoaxi_timeout_value_m2 x 2
[15]	RW	vivoaxi_m1_timeout_en	Timeout count enable of the VIVO AXI bus port M1 (VICAP) 0: disabled 1: enabled
[14:0]	RW	vivoaxi_m1_timeout_value	Timeout count of the VIVO AXI bus port M1 (VICAP) Count value = vivoaxi_timeout_value_m1 x 2

MISC_CTRL14

MISC_CTRL14 is a VIVO bus control register 1.

Offset Address	Register Name	Total Reset Value
0x0038	MISC_CTRL14	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vivoaxi_m3_timeout_en	vivoaxi_m3_timeout_value															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15]	RW	vivoaxi_m3_timeout_en	Timeout count enable of the VIVO AXI bus port M3 (VDP) 0: disabled 1: enabled
[14:0]	RW	vivoaxi_m3_timeout_value	Timeout count of the VIVO AXI bus port M3 (VDP) Count value = vivoaxi_timeout_value_m3 x 2

MISC_CTRL16

MISC_CTRL16 is a VIVO bus control register 3.

Offset Address	Register Name	Total Reset Value
0x0040	MISC_CTRL16	0x0000_0012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					vivoaxi_m3_pri			reserved		vivoaxi_m2_pri		reserved		vivoaxi_m1_pri	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:8]	RW	vivoaxi_m3_pri	Priority of the VIVO AXI bus port M3 (VDP) The value 3 indicates the highest priority.

[7]	-	reserved	Reserved
[6:4]	RW	vivoaxi_m2_pri	Priority of the VIVO AXI bus port M2 (AIAO) The value 3 indicates the highest priority.
[3]	-	reserved	Reserved
[2:0]	RW	vivoaxi_m1_pri	Priority of the VIVO AXI bus port M1 (VICAP) The value 3 indicates the highest priority.

MISC_CTRL17

MISC_CTRL17 is a DDR_QOS control register 0.

Offset Address	Register Name	Total Reset Value
0x0044	MISC_CTRL17	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		gzip_qosmap	hash_qosmap	jpge_qosmap	aio_qosmap	vicap_qosmap	vdp_qosmap
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:20]	RW	gzip_qosmap	QoS group of the IVE/GZIP
[19:16]	RW	hash_qosmap	QoS group of the HASH
[15:12]	RW	jpge_qosmap	QoS group of the JPGE
[11:8]	RW	aio_qosmap	QoS group of the AIAO
[7:4]	RW	vicap_qosmap	QoS group of the VICAP
[3:0]	RW	vdp_qosmap	QoS group of the VDP

MISC_CTRL18

MISC_CTRL18 is a DDR_QOS control register 1.

Offset Address	Register Name	Total Reset Value
0x0048	MISC_CTRL18	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	sdio2_qosmap	emmc_qosmap	fmc_qosmap	sdio1_qosmap	sdio0_qosmap	arm9_qosmap	vpss_qosmap	vgs_qosmap
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	sdio2_qosmap	QoS group of the SDIO2
[27:24]	RW	emmc_qosmap	QoS group of the eMMC
[23:20]	RW	fmc_qosmap	QoS group of the FMC
[19:16]	RW	sdio1_qosmap	QoS group of the SDIO1
[15:12]	RW	sdio0_qosmap	QoS group of the SDIO0
[11:8]	RW	arm9_qosmap	QoS group of the ARM9
[7:4]	RW	vpss_qosmap	QoS group of the VPSS
[3:0]	RW	vgs_qosmap	QoS group of the VGS

MISC_CTRL19

MISC_CTRL19 is a DDR_QOS control register 2.

Offset Address	Register Name	Total Reset Value
0x004C	MISC_CTRL19	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ive_qosmap	vedu_qosmap	usb_qosmap	cipher_qosmap	dma_m2_qosmap	dma_m1_qosmap	eth_qosmap
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:24]	RW	ive_qosmap	QoS group of the IVE
[23:20]	RW	vedu_qosmap	QoS group of the VEDU
[19:16]	RW	usb_qosmap	QoS group of the USB
[15:12]	RW	cipher_qosmap	QoS group of the cipher
[11:8]	RW	dma_m2_qosmap	M2 QoS group of the DMAC
[7:4]	RW	dma_m1_qosmap	M1 QoS group of the DMAC
[3:0]	RW	eth_qosmap	QoS group of the ETH

MISC_CTRL20

MISC_CTRL20 is a DDR_QOS control register 3.

Offset Address	Register Name	Total Reset Value
0x0050	MISC_CTRL20	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										gzip_to		reserved		hash_to		reserved		jpge_to		reserved		aio_to		reserved		vicap_to		reserved		vdp_to	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	reserved	Reserved
[21:20]	RW	gzip_to	Timeout group of the GZIP
[19:18]	-	reserved	Reserved
[17:16]	RW	hash_to	Timeout group of the HASH
[15:14]	-	reserved	Reserved
[13:12]	RW	jpge_to	Timeout group of the JPGE
[11:10]	-	reserved	Reserved
[9:8]	RW	aio_to	Timeout group of the AIAO
[7:6]	-	reserved	Reserved
[5:4]	RW	vicap_to	Timeout group of the VICAP
[3:2]	-	reserved	Reserved
[1:0]	RW	vdp_to	Timeout group of the VDP

MISC_CTRL21

MISC_CTRL21 is a DDR_QOS control register 4.

Offset Address	Register Name	Total Reset Value
0x0054	MISC_CTRL21	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		sdio2_to		reserved		emmc_to		reserved		fmc_to		reserved		sdio1_to		reserved		sdio0_to		reserved		arm9_to		reserved		vpss_to		reserved		vgs_to	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:28]	RW	sdio2_to	Timeout group of the SDIO2
[27:26]	-	reserved	Reserved
[25:24]	RW	emmc_to	Timeout group of the eMMC
[23:22]	-	reserved	Reserved
[21:20]	RW	fmc_to	Timeout group of the FMC
[19:18]	-	reserved	Reserved
[17:16]	RW	sdio1_to	Timeout group of the SDIO1
[15:14]	-	reserved	Reserved
[13:12]	RW	sdio0_to	Timeout group of the SDIO0
[11:10]	-	reserved	Reserved
[9:8]	RW	arm9_to	Timeout group of the ARM9
[7:6]	-	reserved	Reserved
[5:4]	RW	vpss_to	Timeout group of the VPSS
[3:2]	-	reserved	Reserved
[1:0]	RW	vgs_to	Timeout group of the VGS

MISC_CTRL22

MISC_CTRL22 is a DDR_QOS control register 5.

Offset Address	Register Name	Total Reset Value
0x0058	MISC_CTRL22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						ive_to		reserved		vedu_to		reserved		usb_to		reserved		cipher_to		reserved		dma_m2_to		reserved		dma_m1_to		reserved		eth_to	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:24]	RW	ive_to	Timeout group of the IVE
[23:22]	-	reserved	Reserved
[21:20]	RW	vedu_to	Timeout group of the VEDU
[19:18]	-	reserved	Reserved
[17:16]	RW	usb_to	Timeout group of the USB
[15:14]	-	reserved	Reserved
[13:12]	RW	cipher_to	Timeout group of the cipher
[11:10]	-	reserved	Reserved
[9:8]	RW	dma_m2_to	Timeout group of the DMAC master 2
[7:6]	-	reserved	Reserved
[5:4]	RW	dma_m1_to	Timeout group of the DMAC master 1
[3:2]	-	reserved	Reserved
[1:0]	RW	eth_to	Timeout group of the ETH

MISC_CTRL23

MISC_CTRL23 is a USB2.0 control register 0.

Offset Address	Register Name	Total Reset Value
0x005C	MISC_CTRL23	0x0003_13A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb_chipid	reserved												usb_host_ss_hubsetup_min	usb_host_ovrcur_pctrl	usb_host_pwren_pctrl	reserved				usb_host_port_ovrcur_en	usb_host_ohci_12ms_cntsel	usb_host_port_pwren_en	reserved			usb_host_incr16_en	usb_host_incr8_en	usb_host_incr4_en	usb_host_incr_align_en	usb_host_autopd_on_ovrcur_en	reserved			usb_host_app_start_clk	usb_host_ohci_susp_lgcy	usb_host_utmi_word_if
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	usb_chipid	Working mode of the USB port 0: host mode 1: device mode
[30:19]	-	reserved	Reserved
[18]	RW	usb_host_ss_hubsetup_min	Number of idle cycles after the USB full-speed preamble packet 0: 5 1: 4
[17]	RW	usb_host_ovrcur_pctrl	Polarity control of the USB port overcurrent protection 0: active low 1: active high
[16]	RW	usb_host_pwren_pctrl	Polarity control of the USB port power 0: active low 1: active high
[15]	-	reserved	Reserved
[14]	RW	usb_host_port_ovrcur_en	Overcurrent protection enable of the USB port 0: disabled 1: enabled
[13]	RW	usb_host_ohci_12ms_cntsel	Reserved
[12]	RW	usb_host_port_pwren_en	USB port power enable 0: disabled 1: enabled
[11:10]	-	reserved	Reserved

[9]	RW	usb_host_incr16_en	BURST16 enable of the USB controller 0: disabled 1: enabled
[8]	RW	usb_host_incr8_en	BURST8 enable of the USB controller 0: disabled 1: enabled
[7]	RW	usb_host_incr4_en	BURST4 enable of the USB controller 0: disabled 1: enabled
[6]	RW	usb_host_incr_align_en	Burst alignment enable of the USB controller 0: disabled 1: enabled
[5]	RW	usb_host_autopd_on_ovrcur_en	Enable of automatic port power cutoff during USB host overcurrent 0: disabled 1: enabled
[4:3]	-	reserved	Reserved
[2]	RW	usb_host_app_start_clk	OHCI clock control signal 0: The OHCI works normally. (default) 1: The OHCI clock is enabled in suspend mode.
[1]	RW	usb_host_ohci_susp_lgcy	Suspended strap input signal of the OHCI
[0]	RW	usb_host_utmi_word_if	Data bit width select of the UTMI interface 0: 8 bits 1: 16 bits

MISC_CTRL24

MISC_CTRL24 is a USB2.0 control register 1.

Offset Address	Register Name	Total Reset Value
0x0060	MISC_CTRL24	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															usb_phy_reg_access	reserved										usb_dev_scaledown_mode		reserved		usb_dev_dbg_addr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved
[16]	RW	usb_phy_reg_access	Access mode of USB PHY registers 0: register mode 1: bus mode
[15:6]	-	reserved	Reserved
[5:4]	RW	usb_dev_scaledown_mode	USB device scale-down mode 00: Scale-down is disabled, and the actual timing value is used. 01: Scale-down of all timings except those suspended or resumed in device mode is enabled 10: Scale-down of timings suspended or resumed in device mode is enabled 11: Scale-down of timings of bit 0 and bit 1 is enabled.
[3:2]	-	reserved	Reserved
[1:0]	RW	usb_dev_dbg_addr	Address segment of USB device registers

MISC_CTRL25

MISC_CTRL25 is a USB2.0 control register 2.

Offset Address	Register Name	Total Reset Value
0x0064	MISC_CTRL25	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	usb2_phy_test_rddata								usb2_phy_test_wrdata								reserved				usb2_phy_test_wren	usb2_phy_test_addr										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	usb2_phy_test_rddata	Read data of USB PHY registers (This field is valid only when the access mode of the USB PHY register is register mode.)
[23:16]	RW	usb2_phy_test_wrdata	Write data of USB PHY registers (This field is valid only when the access mode of the USB PHY register is register mode.)
[15:12]	-	reserved	Reserved
[11]	WO	usb2_phy_test_wren	Write control signal of USB PHY registers. Writing 1 to this bit starts the write operation on USB PHY registers. (This field is valid only when the access mode of the USB PHY register is register mode.)
[10:0]	RW	usb2_phy_test_addr	Interface address of USB PHY registers (This field is valid only when the access mode of the USB PHY register is register mode.)

MISC_CTRL30

MISC_CTRL30 is an SVB control register.

Offset Address	Register Name	Total Reset Value
0x0078	MISC_CTRL30	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								svb_pwm_duty								reserved				svb_pwm_period								reserved	svb_pwm_load	svb_pwm_inv	svb_pwm_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	svb_pwm_duty	Number of high-level cycles output by the SVB. The actual number is the configured value plus 1.
[15:14]	-	reserved	Reserved
[13:4]	RW	svb_pwm_period	Number of cycles output by the SVB. The actual number is the configured value plus 1.
[3]	-	reserved	Reserved
[2]	WO	svb_pwm_load	SVB output parameter load control. Writing 1 to this bit enables the parameters to take effect.
[1]	RW	svb_pwm_inv	SVB output phase control 0: normal 1: inversed
[0]	RW	svb_pwm_enable	SVB enable control 0: disabled 1: enabled

MISC_CTRL31

MISC_CTRL31 is core HPM control register 0.

Offset Address	Register Name	Total Reset Value
0x007C	MISC_CTRL31	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_hpm_srst_req	core_hpm_monitor_en	core_hpm_en	reserved													core_hpm_monitor_period								reserved				core_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	core_hpm_srst_req	Core HPM reset request, active high 0: deassert reset 1: reset
[30]	RW	core_hpm_monitor_en	Core HPM cyclic monitoring enable 0: single monitoring 1: cyclic monitoring
[29]	RW	core_hpm_en	Core HPM measure enable 0: disabled 1: enabled
[28:16]	-	reserved	Reserved
[15:8]	RW	core_hpm_monitor_period	Core HPM cyclic monitoring period The monitoring period is core_hpm_monitor_period x 2.048 ms.
[7:6]	-	reserved	Reserved
[5:0]	RW	core_hpm_div	Frequency division ratio of the core HPM reference clock The actual frequency divider is the configured value plus 1.

MISC_CTRL32

MISC_CTRL32 is core HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0080	MISC_CTRL32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								core_hpm_offset		core_hpm_shift		core_hpm_lowlimit								core_hpm_uplimit											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:22]	RW	core_hpm_offset	Core HPM offset
[21:20]	RW	core_hpm_shift	Core HPM shift
[19:10]	RW	core_hpm_lowlimit	Lower limit of the core HPM
[9:0]	RW	core_hpm_uplimit	Upper limit of the core HPM

MISC_CTRL33

MISC_CTRL33 is core HPM status register 0.

Offset Address	Register Name	Total Reset Value
0x0084	MISC_CTRL33	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_hpm_up_warning		core_hpm_low_warning		core_hpm_pc_valid		reserved		core_hpm_pc_record1								reserved								core_hpm_pc_record0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	core_hpm_up_warning	Core HPM overflow alarm, active high

[30]	RO	core_hpm_low_warning	Core HPM underflow alarm, active high
[29]	RO	core_hpm_pc_valid	Core HPM output validity indicator 0: invalid 1: valid
[28:26]	-	reserved	Reserved
[25:16]	RO	core_hpm_pc_record1	Source code type 1 of the core HPM
[15:10]	-	reserved	Reserved
[9:0]	RO	core_hpm_pc_record0	Source code type 0 of the core HPM

MISC_CTRL34

MISC_CTRL34 is core HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x0088	MISC_CTRL34	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	core_hpm_rcc				reserved	core_hpm_pc_record3											reserved				core_hpm_pc_record2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	core_hpm_rcc	RCC code in the core HPM output
[26]	-	reserved	Reserved
[25:16]	RO	core_hpm_pc_record3	Source code type 3 of the core HPM
[15:10]	-	reserved	Reserved
[9:0]	RO	core_hpm_pc_record2	Source code type 2 of the core HPM

MISC_CTRL35

MISC_CTRL35 is media HPM control register 0.

Offset Address	Register Name	Total Reset Value
0x008C	MISC_CTRL35	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media_hpm_srst_req	media_hpm_monitor_en	media_hpm_en	reserved													media_hpm_monitor_period								reserved				media_hpm_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	media_hpm_srst_req	Media HPM reset request, active high 0: deassert reset 1: reset
[30]	RW	media_hpm_monitor_en	Media HPM cyclic monitoring enable 0: single monitoring 1: cyclic monitoring
[29]	RW	media_hpm_en	Media HPM measure enable 0: disabled 1: enabled
[28:16]	-	reserved	Reserved
[15:8]	RW	media_hpm_monitor_period	Media HPM cyclic monitoring period The cyclic monitoring period is media_hpm_monitor_period x 2.048 ms.
[7:6]	-	reserved	Reserved
[5:0]	RW	media_hpm_div	Frequency divider of the media HPM reference clock The actual frequency divider is the configured value plus 1.

MISC_CTRL36

MISC_CTRL36 is media HPM control register 1.

Offset Address	Register Name	Total Reset Value
0x0090	MISC_CTRL36	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								media_hpm_offset		media_hpm_shift		media_hpm_lowlimit												media_hpm_uplimit							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:22]	RW	media_hpm_offset	Media HPM offset
[21:20]	RW	media_hpm_shift	Media HPM shift
[19:10]	RW	media_hpm_lowlimit	Lower limit of the media HPM
[9:0]	RW	media_hpm_uplimit	Upper limit of the media HPM

MISC_CTRL37

MISC_CTRL37 is media HPM status register 0.

Offset Address	Register Name	Total Reset Value
0x0094	MISC_CTRL37	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media_hpm_up_warning	media_hpm_low_warning	media_hpm_pc_valid	reserved					media_hpm_pc_record1								reserved								media_hpm_pc_record0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	media_hpm_up_warning	Media HPM overflow alarm, active high

[30]	RO	media_hpm_low_warning	Media HPM underflow alarm, active high
[29]	RO	media_hpm_pc_valid	Media HPM output validity indicator 0: invalid 1: valid
[28:26]	-	reserved	Reserved
[25:16]	RO	media_hpm_pc_record1	Source code type 1 of the media HPM
[15:10]	-	reserved	Reserved
[9:0]	RO	media_hpm_pc_record0	Source code type 0 of the media HPM

MISC_CTRL38

MISC_CTRL38 is media HPM status register 1.

Offset Address	Register Name	Total Reset Value
0x0098	MISC_CTRL38	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	media_hpm_rcc				reserved	media_hpm_pc_record3											reserved				media_hpm_pc_record2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	media_hpm_rcc	RCC code in the media HPM output
[26]	-	reserved	Reserved
[25:16]	RO	media_hpm_pc_record3	Source code type 3 of the media HPM
[15:10]	-	reserved	Reserved
[9:0]	RO	media_hpm_pc_record2	Source code type 2 of the media HPM

MISC_CTRL39

MISC_CTRL39 is a T-sensor control register.

Offset Address	Register Name	Total Reset Value
0x009C	MISC_CTRL39	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsensor_en	tsensor_monitor_en	tsensor_cnt16_bypass	reserved	tsensor_monitor_period								tsensor_uplimit												tsensor_lowlimit							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	tsensor_en	T-sensor enable 0: disabled 1: enabled
[30]	RW	tsensor_monitor_en	T-sensor temperature cyclic monitoring enable 0: single monitoring 1: cyclic monitoring
[29]	RW	tsensor_cnt16_bypass	Bypass of obtaining the average value of 16 measurements of the T-sensor
[27:20]	RW	tsensor_monitor_period	T-sensor temperature cyclic monitoring period. The timing baseline is 2 ms.
[19:10]	RW	tsensor_uplimit	Temperature overflow value
[9:0]	RW	tsensor_lowlimit	Temperature underflow value

MISC_CTRL40

MISC_CTRL40 is a T-sensor status register.

Offset Address	Register Name	Total Reset Value
0x00A0	MISC_CTRL40	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										tsensor_vcalib1_en	tsensor_temp_calib	tsensor_temp_ct_sel		tsensor_low_warning	tsensor_up_warning
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved
[5]	RW	tsensor_vcalib1_en	TSensor VCALIB1 enable 0: disabled 1: enabled
[4]	RW	tsensor_temp_calib	TSensor calibration algorithm select 0: enabled 1: disabled
[3:2]	RW	tsensor_temp_ct_sel	Time select for converting a temperature code value of the TSensor 00: 0.512 ms 01: 1.024 ms 10: 0.256 ms 11: 2.048 ms
[1]	RO	tsensor_low_warning	Temperature underflow alarm, active high
[0]	RO	tsensor_up_warning	Temperature overflow alarm, active high

MISC_CTRL41

MISC_CTRL41 is T-sensor temperature record register 0.

Offset Address	Register Name	Total Reset Value
0x00A4	MISC_CTRL41	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tsensor_result1		reserved		tsensor_result0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RO	tsensor_result1	Temperature record 1
[15:10]	-	reserved	Reserved
[9:0]	RO	tsensor_result0	Temperature record 0

MISC_CTRL42

MISC_CTRL42 is T-sensor temperature record register 1.

Offset Address	Register Name	Total Reset Value
0x00A8	MISC_CTRL42	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		tsensor_result3		reserved		tsensor_result2	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RO	tsensor_result3	Temperature record 3
[15:10]	-	reserved	Reserved
[9:0]	RO	tsensor_result2	Temperature record 2

MISC_CTRL43

MISC_CTRL43 is T-sensor temperature record register 2.

Offset Address	Register Name	Total Reset Value
0x00AC	MISC_CTRL43	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	tsensor_result5			reserved		tsensor_result4	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RO	tsensor_result5	Temperature record 5
[15:10]	-	reserved	Reserved
[9:0]	RO	tsensor_result4	Temperature record 4

MISC_CTRL44

MISC_CTRL44 is T-sensor temperature record register 3.

Offset Address	Register Name	Total Reset Value
0x00B0	MISC_CTRL44	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	tsensor_result7			reserved		tsensor_result6	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RO	tsensor_result7	Temperature record 7
[15:10]	-	reserved	Reserved
[9:0]	RO	tsensor_result6	Temperature record 6

MISC_CTRL47

MISC_CTRL47 is an update mode clear register.

Offset Address	Register Name	Total Reset Value
0x00BC	MISC_CTRL47	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update_mode_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	WO	update_mode_clear	Writing 1 to this bit clears the update mode. This register is configured when the update is complete.

3.6 DMA Controller

3.6.1 Overview

The direction memory access (DMA) operation is a high-speed data transfer operation. It supports data read/write between peripherals and memories without using the CPU. The direction memory access controller (DMAC) directly transfers data between a memory and a peripheral, between peripherals, or between memories. This avoids the CPU intervention and reduces the interrupt handling overhead of the CPU.

3.6.2 Features

The DMAC has the following features:

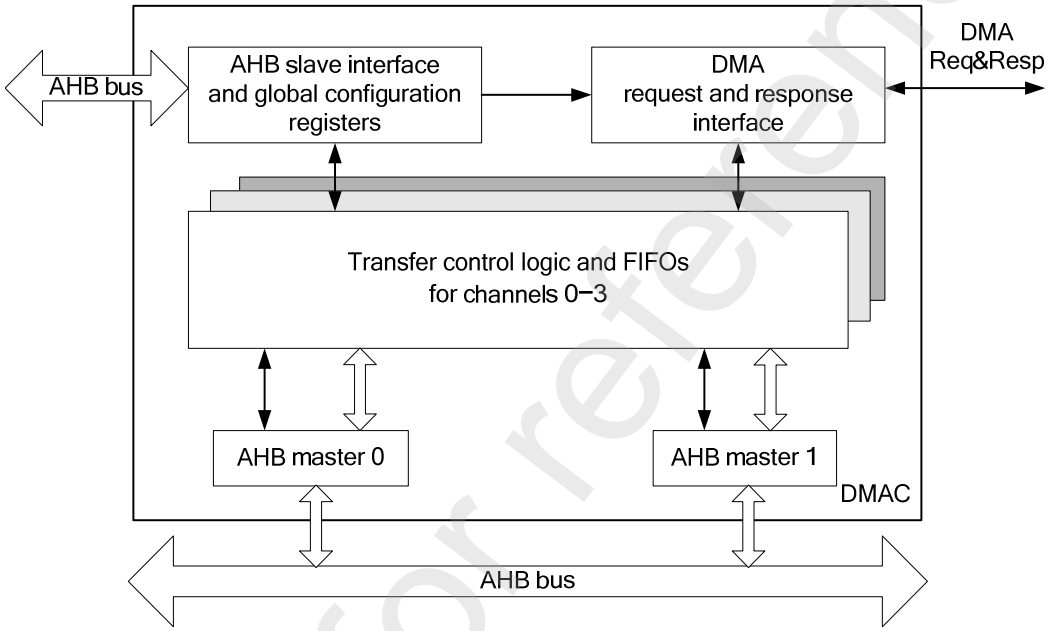
- Transfers data in 8-bit, 16-bit, or 32-bit mode.
- Provides four DMA channels. Each channel can be configured to support unidirectional transfer.
- Provides two 32-bit master bus interfaces for data transfer.
- Supports the DMA requests controlled through software.
- Programs the DMA burst size.
- Configures the source address and the destination address as automatic incremental or decremented addresses during DMA transfer.
- Supports DMA transfer with the linked list.
- Supports the DMAC flow control.

3.6.3 Function Description

Functional Block Diagram

Figure 3-6 shows the functional block diagram of the DMAC.

Figure 3-6 Functional block diagram of the DMAC



NOTE

- The priorities of DMAC channels are fixed. DMA channel 0 has the highest priority; whereas channel 3 has the lowest priority. When the DMA requests from two peripherals are valid simultaneously, the channel with the higher priority starts data transfer first.
- DMA channel 0 and DMA channel 1 have one 4 x 32-bit FIFO each, and DMA channel 2 and DMA channel 3 have one 16 x 32-bit FIFO each.

Each DMA channel has a group of transfer control logic and one FIFO. The transfer control logic automatically performs the following operations:

Step 1 Read data from the source address specified by the software.

Step 2 Buffer data in the FIFO.

Step 3 Fetch data from the FIFO.

Step 4 Write the data to the destination address specified by the software.

----End

Workflow

The workflow of the DMAC is as follows:

Step 1 The software selects one DMA channel for DMA transfer, configures the following items, and enables the channel:

- Source address
- Destination address
- Header pointer of the linked list
- Amount of the transferred data
- Source and destination peripheral request signal numbers
- Masters used at the source and destination ends of the channel.

After the channel is enabled, the DMAC starts to check the activities of the DMA request lines of the source peripheral and destination device connected to this channel.

Step 2 The source device transmits a DMA request to the DMAC. If the source device is a memory, the DMAC considers that the DMA request is always valid by default.

Step 3 The DMAC channel responds to the DMA request of the source device. Then the DAMC reads data from the source device and stores it in the internal FIFO of the channel.

Step 4 The destination device transmits a DMA request to the DMAC. If the destination device is a memory, the DMAC considers that the DMA request is always valid by default.

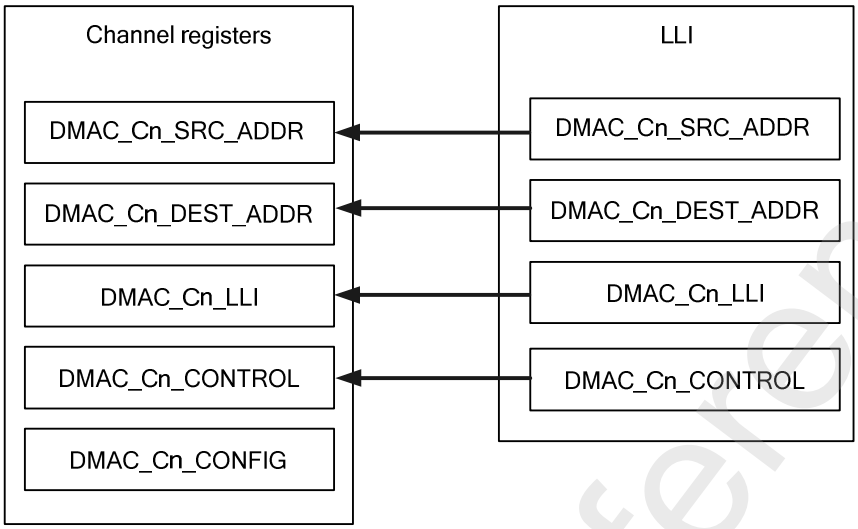
Step 5 The DMA channel responds to the DMA request of the destination device. Then the DMAC fetches data from the internal FIFO of the channel and writes it to the destination device.

Step 6 The steps 2 and step 3 as well as step 4 and 5 may be performed concurrently, because the source and destination devices may transmit DMA requests to the DMAC at the same time. When the FIFO overrun or underrun occurs on the DMA channel, the DMAC blocks the DMA requests of the source device or destination device until the FIFO is full or empty. When the DMAC interacts with the source device and destination device for several times, step 2 to step 5 are performed repeatedly until the specified data is completely transferred and a maskable transfer terminal interrupt is sent. If the value of DMAC_Cn_LLI is not 0, read linked list item (LLI) nodes by considering the register value as an address, load the read values to DMAC_Cn_SRC_ADDR, DMAC_Cn_DEST_ADDR, DMAC_Cn_LLI, and DMAC_Cn_CONTROL in sequence (see Figure 3-6), and then go to step 2. If the value of DMAC_Cn_LLI is 0, the current DMA transfer is stopped. In this case, the channel is disabled automatically and the transfer ends.

----End

Figure 3-7 illustrates how to update channel registers through the LLI.

Figure 3-7 Updating channel registers through the LLI



Connection Between the DMA and Peripherals

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC.

The DMAC provides the following two DMA request signals for each peripheral:

- DMACBREQ

  Burst transfer request signal. It triggers a burst transfer and the burst size is preconfigured.

- DMACSREQ

  Single transfer request signal. It triggers a single transfer. That is, the DMAC reads a data segment from a peripheral or writes a data segment to a peripheral.

The DMAC provides a request clear signal DMACLR. This signal is sent to each peripheral by the DMAC as a response to the DMA request signal of each peripheral.

DMAC Request Signals

Table 3-12 describes the mapping between DMAC hardware request signals and devices.

Table 3-12 DMAC hardware request signals and corresponding peripheral requests

DMAC Hardware Request Signal No.	Device Request
0	DMA request of the I^2C0 RX channel
1	DMA request of the I^2C0 TX channel
2	Reserved
3	Reserved
4	DMA request of the I^2C1 RX channel

DMAC Hardware Request Signal No.	Device Request
5	DMA request of the I^{2}C1 TX channel
6	DMA request of the UART0 RX channel
7	DMA request of the UART0 TX channel
8	DMA request of the UART1 RX channel
9	DMA request of the UART1 TX channel
10	DMA request of the UART2 RX channel
11	DMA request of the UART2 TX channel
12	DMA request of the SSP0 RX channel
13	DMA request of the SSP0 TX channel
14	DMA request of the SSP1 RX channel
15	DMA request of the SSP1 TX channel

The source and destination requests of each DMA channel are configured by software. For example, DMA request 5 is the request of the UART0 RX channel. To transmit the UART0 RX data by using channel 3, you must configure DMA request 5 as the source request of channel 3.

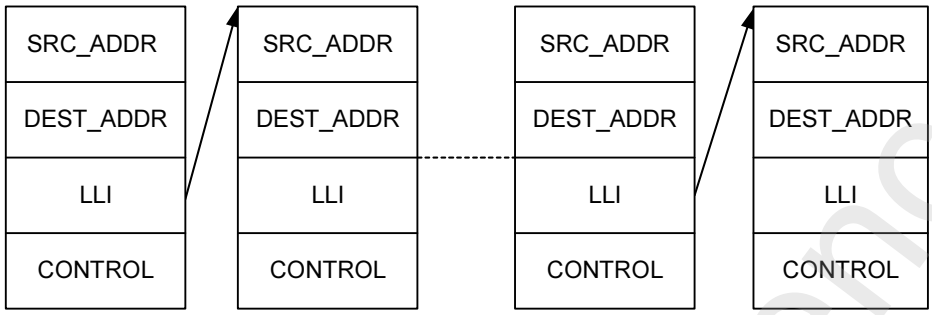
As memories do not provide DMA request signals, when a memory is used for DMA transfer, the DMAC considers that the DMA request of the memory is always valid by default. In addition, an idle cycle is inserted after each bus operation during the DMAC transfer on channel 2 or channel 3. In this way, the master with a higher priority channel can transfer data on the bus first. Therefore, to prevent other channels from waiting for the bus for a long time, you are advised to transmit data from memory to memory using channel 2 or channel 3.

DMA Linked List

The data structure of the DMAC LLI node is as follows:

- Channel register DMAC_Cn_SRC_ADDR, for setting the start address for the source device
- Channel register DMAC_Cn_DEST_ADDR, for setting the start address for the destination device
- Channel register DMAC_Cn_LLI, for setting the address for the next node
- Channel register DMAC_Cn_CONTROL, for setting the master, data width, burst size, address increment, and transfer size of the source device and destination device

Figure 3-8 Structure of DMAC LLIs



CAUTION

The LLI field value must be less than or equal to 0xFFFF_FFF0. Otherwise, the address is wrapped around to 0x0000_0000 during a 4-word burst transfer. As a result, the data structure of LLI nodes cannot be stored in a consecutive address area.

If the LLI field is set to 0, the current node is at the end of the linked list. In this case, the corresponding channel is disabled after data blocks corresponding to the current node are transferred.

3.6.4 Operating Mode

Clock Gating

In the following cases, the DMAC and DMAC clock can be disabled using the software to reduce power consumption:

- All DMA channels are idle and there is no DMA transfer request.
- DMAC_Cn_CONFIG[0] is set to 0 and all the DMA channels are disabled.

To disable the DMAC clock, perform the following steps:

Step 1 Write 0 to DMAC_Cn_CONFIG[0] to disable DMAC channels.

Step 2 Write 0 to DMAC_CONFIG [0] to disable the DMAC.

Step 3 Write 0 to PERI_CRG54 [5] to disable DMAC bus clock gating. Then the DMAC clock is disabled.

Step 4 Enable the clock and the DMAC again when the DMAC is required for data transfer.

----End

Initialization

To initialize the DMAC, perform the following steps:

Step 1 Write to DMAC_CONFIG to set the endianness of DMAC master 1 and DMAC master 2, and write 1 to DMAC_CONFIG[0] to enable the DMAC.

Step 2 Write 1 to all the bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear all interrupts.

Step 3 Write 0 to the corresponding bits of DMAC_SYNC to set the DMA request signal groups to be synchronized.

Step 4 Configure and disable channels in sequence. You can disable all the channels by writing 0 to DMAC_Cn_CONFIG[0] of each channel.

----End

Enabling a Channel

After the DMAC is initialized, the DMAC can transmit data only when a DMAC channel is configured and enabled. To enable a DMA channel, perform the following steps:

Step 1 Read DMAC_ENABLED_CHNS to search for idle channels and select one.

Step 2 Write 1 to the corresponding bits of DMAC_INT_ERR_CLR and DMAC_INT_TC_CLR to clear the interrupt status of the selected channel.

Step 3 Write to DMAC_Cn_SRC_ADDR to set the access start address for the source device.

Step 4 Write to DMAC_Cn_DEST_ADDR to set the access start address for the destination device.

Step 5 Write to DMAC_Cn_LLI to set the linked list information. If the channel is used for single-block data transfer, set DMAC_Cn_LLI to 0. If the channel is used for linked list data transfer, set DMAC_Cn_LLI to the linked list header pointer.

Step 6 Write to DMAC_Cn_CONTROL to set the master, data width, burst size, address increment, and transfer size of the source device and destination device.

Step 7 Write to DMAC_Cn_CONFIG to set the DMA request signal, flow control mode, and interrupt mask of this channel.

Step 8 Write 1 to DMAC_Cn_CONFIG[0] to enable this channel.

----End

Usage of DMAC_Cn_CONTROL÷

The DMAC_Cn_CONTROL register contains the control information about the DMA channels, such as the transfer size, burst size, and transfer bit width.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register value is updated when being loaded from an LLI node after a complete data block is transferred.

If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. As a result, the register can be read after the channel stops data transfer.

Table 3-13 lists the mapping between the value of dbsize or sbsize of DMAC_Cn_CONTROL and the burst length.

Table 3-13 Mapping between the value of dbsize or sbsize and the burst length

Value of bsize or sbSize	Burst Length
000	1
001	4
010	8
011	16
100	32
101	64
110	128
111	256

Table 3-14 describes mapping between the value of dwidth or swidth of DMAC_Cn_CONTROL and the transfer data width.

Table 3-14 Mapping between the value of dwidth or swidth and the transfer bit width

Value of swidth or dwidth	Transfer Bit Width
000	Byte (8 bits)
001	Halfword (16 bits)
010	Word (32 bits)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Note the following when configuring DMAC_Cn_CONTROL:

- When the transfer bit width of the source device is smaller than that of the destination device, the product of the transfer bit width and transfer size of the source device must be an integral multiple of the transfer bit width of the destination device. Otherwise, data retention and data loss occur in the FIFO.
- swidth and dwidth fields cannot be set to undefined bit widths.
- If the transfer size field is set to 0 and the DMAC is a flow controller, the DMAC does not transfer data. In this case, the programmer needs to disable the DMA channel and reprogram it.
- Never conduct common write/read tests on the DMAC_Cn_CONTROL register, because the transfer size field is different from the common register field whose written value and

read value may be the same. During the write operation, this field serves as a control register, because it determines the number of data segments transferred by the DMAC. During the read operation, this field serves as a status register, because it returns the number (in the unit of the bit width of the source device) of the remaining data segments to be transferred.

- When the transfer size field is set to a value greater than the depth of the FIFO (peripheral FIFO but not the DMAC FIFO) of the source device or destination device, the mode of DMAC source address or destination address must be set to non-incremental mode. Otherwise, the peripheral FIFO may overflow.

The bus access information is provided for the source device or destination device over the master interface signals during data transfer. Such information is related to the bits DMAC_Cn_CONTROL[30:28] and DMAC_Cn_CONFIG[16] that are configured by programming channel registers. Table 3-15 describes the three protection bits of the prot field of DMAC_Cn_CONTROL.

Table 3-15 Definitions of the prot_stat field of DMAC_Cn_CONTROL

Bit	Description	Purpose
[2]	Cacheable or non-cacheable	Indicates whether the access is cacheable. 0: non-cacheable 1: cacheable For example, this bit can notify an advanced microcontroller bus architecture (AMBA) bridge of the following information: When finding the first read operation of the 8-digit burst, this bridge can originate one 8-digit burst read operation on the destination bus directly instead of transmitting the read operations on the source bus to the destination bus one by one. This bit controls the output of the bus signal HPROT[3].
[1]	Bufferable or non-bufferable	Indicates whether the access is bufferable. 0: non-bufferable 1: bufferable For example, this bit is used to notify an AMBA bridge that the write operation on the source bus can be complete without waiting. That is, the operation can be performed even when the bridge does not arbitrate the operation to the destination bus and the slave device does not receive data completely. This bit controls the output of the bus signal HPROT[2].
[0]	Privileged or User	Access mode. 0: user mode 1: privileged mode This bit controls the output of the bus signal HPROT[1].

NOTE

AMBA: advanced microcontroller bus architecture

Usage of DMAC_Cn_CONFIG

Table 3-16 describes the flow controllers and transfer types corresponding to the flow_cntrl field of DMAC_Cn_CONFIG.

Table 3-16 Flow controllers and transfer types corresponding to the flow_cntrl field

Bit Value	Transfer Mode	Controller
000	Memory to memory	DMAC
001	Memory to peripheral	DMAC
010	Peripheral to memory	DMAC
011	Source device to destination device	DMAC
100	Source device to destination device	Destination device
101	Memory to peripheral	Destination device
110	Peripheral to memory	Source device
111	Source device to destination device	Source device

Interrupt Handling

When data transfer is complete or an error occurs during data transfer, interrupts are reported to the interrupt controller. An interrupt is handled as follows:

Step 1 Read DMAC_INT_STAT to find the channel that transmits an interrupt request. When multiple channels initiate interrupt requests at the same time, the interrupt request with the highest priority is handled first.

Step 2 Read DMAC_INT_TC_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is a transfer terminal interrupt. If the value is 1, the interrupt is a transfer terminal interrupt. In this case, go to step 4; otherwise, go to step 3.

Step 3 Read DMAC_INT_ERR_STAT to query the value of the selected bit to check whether the interrupt sent by the corresponding channel is an error interrupt. If the selected bit is 1, the interrupt is an error interrupt. In this case, go to step 5; otherwise, end the operation.

Step 4 Handle the transfer terminal interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_TC_CLR to clear the interrupt status of the corresponding channel.
2. Fetch or use up the data buffered in the memory. If necessary (for example, you need to create a buffer in the memory), configure and enable the channel again.
3. End interrupt handling.

Step 5 Handle the error interrupt as follows:

1. Write 1 to the selected bit of DMAC_INT_ERR_CLR to clear the interrupt status of the corresponding channel.
2. Provide the error information. If necessary, configure and enable the channel again.

3. End interrupt handling.

----End

3.6.5 Register Summary

NOTE

The *n* in the offset addresses for DMA registers indicates the DMA channel and its value range is 0−3.

Table 3-17 describes the DMAC registers.

Table 3-17 Summary of the DMAC registers (base address: 0x1003_0000)

Offset Address	Register	Description	Page
0x0000	DMAC_INT_STAT	DMAC interrupt status register	3-109
0x0004	DMAC_INT_TC_STAT	DMAC transfer terminal interrupt status register	3-110
0x0008	DMAC_INT_TC_CLR	DMAC transfer terminal interrupt clear register	3-110
0x000C	DMAC_INT_ERR_STAT	DMAC error interrupt status register	3-112
0x0010	DMAC_INT_ERR_CLR	DMAC error interrupt clear register	3-113
0x0014	DMAC_RAW_INT_TC_STAT	DMAC raw transfer terminal interrupt status register	3-114
0x0018	DMAC_RAW_INT_ERR_STAT	DMAC raw error interrupt status register	3-115
0x001C	DMAC_ENABLED_CHNS	DMAC channel enable status register	3-116
0x0020	DMAC_SOFT_BREQ	DMAC software burst transfer request register	3-116
0x0024	DMAC_SOFT_SREQ	DMAC software single transfer request register	3-117
0x0028	DMAC_SOFT_LBREQ	DMAC software last burst request register	3-118
0x002C	DMAC_SOFT_LSREQ	DMAC software last single request register	3-118
0x0030	DMAC_CONFIG	DMAC configuration register	3-119
0x0034	DMAC_SYNC	DMAC request line sync enable register	3-120
0x0100 + *n* x 0x20	DMAC_Cn_SRC_ADDR	Source address register of DMA channel *n* (*n* = 0−3)	3-120
0x0104 +	DMAC_Cn_DEST_ADDR	Destination address register of DMA	3-121

Offset Address	Register	Description	Page
n x 0x20		channel *n* (*n* = 0−3)	
0x0108 + *n* x 0x20	DMAC_Cn_LLI	LLI information register of DMA channel *n* (*n* = 0−3)	3-121
0x010C + *n* x 0x20	DMAC_Cn_CONTROL	Control register of DMA channel *n* (*n* = 0−3)	3-122
0x110 + *n* x 0x20	DMAC_Cn_CONFIG	Configuration register of DMA channel *n* (*n* = 0−3)	3-125

3.6.6 Register Description

DMAC_INT_STAT

DMAC_INT_STAT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0000	DMAC_INT_STAT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							ch3_int_stat	ch2_int_stat	ch1_int_stat	ch0_int_stat
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_stat	Masked interrupt status of channel 3 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[2]	RO	ch2_int_stat	Masked interrupt status of channel 2 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.
[1]	RO	ch1_int_stat	Masked interrupt status of channel 1 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.

[0]	RO	ch0_int_stat	Masked interrupt status of channel 0 0: No interrupt is generated. 1: A transfer error interrupt or transfer terminal interrupt is generated.

DMAC_INT_TC_STAT

DMAC_INT_TC_STAT is a DMAC transfer terminal interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	DMAC_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_stat		ch2_int_tc_stat		ch1_int_tc_stat		ch0_int_tc_stat	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_tc_stat	Status of the masked transfer terminal interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_tc_stat	Status of the masked transfer terminal interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_tc_stat	Status of the masked transfer terminal interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_int_tc_stat	Status of the masked transfer terminal interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_INT_TC_CLR

DMAC_INT_TC_CLR is a DMAC transfer terminal interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0008	DMAC_INT_TC_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_tc_clr		ch2_int_tc_clr		ch1_int_tc_clr		ch0_int_tc_clr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	ch3_int_tc_clr	Transfer terminal interrupt clear for channel 3 0: not cleared 1: cleared
[2]	WO	ch2_int_tc_clr	Transfer terminal interrupt clear for channel 2 0: not cleared 1: cleared
[1]	WO	ch1_int_tc_clr	Transfer terminal interrupt clear for channel 1 0: not cleared 1: cleared
[0]	WO	ch0_int_tc_clr	Transfer terminal interrupt clear for channel 0 0: not cleared 1: cleared

DMAC_INT_ERR_STAT

DMAC_INT_ERR_STAT is a DMAC error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x000C	DMAC_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_stat		ch2_int_err_stat		ch1_int_err_stat		ch0_int_err_stat	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_int_err_stat	Status of the masked error interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_int_err_stat	Status of the masked error interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_int_err_stat	Status of the masked error interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_int_err_stat	Status of the masked error interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_INT_ERR_CLR

DMAC_INT_ERR_CLR is a DMAC transfer error interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0010	DMAC_INT_ERR_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_int_err_clr		ch2_int_err_clr		ch1_int_err_clr		ch0_int_err_clr	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	WO	ch3_int_err_clr	Error interrupt clear for channel 3 0: not cleared 1: cleared
[2]	WO	ch2_int_err_clr	Error interrupt clear for channel 2 0: not cleared 1: cleared
[1]	WO	ch1_int_err_clr	Error interrupt clear for channel 1 0: not cleared 1: cleared
[0]	WO	ch0_int_err_clr	Error interrupt clear for channel 0 0: not cleared 1: cleared

DMAC_RAW_INT_TC_STAT

DMAC_RAW_INT_TC_STAT is a DMAC raw transfer terminal interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	DMAC_RAW_INT_TC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_tc	ch2_raw_int_tc	ch1_raw_int_tc	ch0_raw_int_tc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_raw_int_tc	Status of the raw transfer terminal interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_tc	Status of the raw transfer terminal interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_tc	Status of the raw transfer terminal interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_tc	Status of the raw transfer terminal interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_RAW_INT_ERR_STAT

DMAC_RAW_INT_ERR_STAT is a DMAC raw error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	DMAC_RAW_INT_ERR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_raw_int_err		ch2_raw_int_err		ch1_raw_int_err		ch0_raw_int_err	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_raw_int_err	Status of the raw error interrupt of channel 3 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	ch2_raw_int_err	Status of the raw error interrupt of channel 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	ch1_raw_int_err	Status of the raw error interrupt of channel 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	ch0_raw_int_err	Status of the raw error interrupt of channel 0 0: No interrupt is generated. 1: An interrupt is generated.

DMAC_ENABLED_CHNS

DMAC_ENABLED_CHNS is a DMAC channel enable status register.

Offset Address	Register Name	Total Reset Value
0x001C	DMAC_ENABLED_CHNS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												ch3_enabled		ch2_enabled		ch1_enabled		ch0_enabled	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RO	ch3_enabled	Channel 3 enable 0: disabled 1: enabled
[2]	RO	ch2_enabled	Channel 2 enable 0: disabled 1: enabled
[1]	RO	ch1_enabled	Channel 1 enable 0: disabled 1: enabled
[0]	RO	ch0_enabled	Channel 0 enable 0: disabled 1: enabled

DMAC_SOFT_BREQ

DMAC_SOFT_BREQ is a DMAC software burst transfer request register.

Software controls the generation of a DMA burst transfer request by using this register.

When this register is read, the device that is requesting the DMA burst transfer can be queried. This register and any peripheral can generate a DMA request each.

Offset Address	Register Name	Total Reset Value
0x0020	DMAC_SOFT_BREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_breq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_breq	Controls whether to generate a DMA burst transfer request When this register is written: 0: no effect 1: A DMA burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared. When this register is read: 0: The peripheral corresponding to the request signal DMACBREQ[15:0] does not send any DMA burst request. 1: The peripheral corresponding to the request signal DMACBREQ[15:0] is requesting the DMA burst transfer.

DMAC_SOFT_SREQ

DMAC_SOFT_SREQ is a DMAC software single transfer request register.

Software controls the generation of DMA single transfer requests by using this register.

When this register is read, the device that is requesting the DMA single transfer can be queried. This register and any of the 16 DMA request input signals of the DMAC can generate a DMA request each.

Offset Address	Register Name	Total Reset Value
0x0024	DMAC_SOFT_SREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_sreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_sreq	Controls whether to generate a DMA single transfer request When this register is written: 0: no effect 1: A DMA single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

			When this register is read: 0: The peripheral corresponding to the request signal DMACSREQ[15:0] does not send a DMA single request. 1: The peripheral corresponding to the request signal DMACSREQ[15:0] is requesting the DMA single transfer.

DMAC_SOFT_LBREQ

DMAC_SOFT_LBREQ is a DMAC software last burst request register.

Software controls the generation of the DMA last burst transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x0028	DMAC_SOFT_LBREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lbreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	soft_lbreq	Last burst request issued by the software 0: no effect 1: A DMA last burst transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_SOFT_LSREQ

DMAC_SOFT_LSREQ is a DMAC software last single transfer request register.

Software controls the generation of the DMA last single transfer requests by using this register.

Offset Address	Register Name	Total Reset Value
0x002C	DMAC_SOFT_LSREQ	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_lsreq															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	soft_lsreq	Last single transfer request issued by software 0: no effect 1: A DMA last single transfer request is generated. When the transfer is complete, the corresponding bit is cleared.

DMAC_CONFIG

DMAC_CONFIG is a DMAC configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	DMAC_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													m2_endianness	m1_endianness	dmac_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	m2_endianness	Byte endianness of master 2 0: little endian 1: big endian
[1]	RW	m1_endianness	Byte endianness of master 1 0: little endian 1: big endian
[0]	RW	dmac_enable	DMA enable 0: disabled 1: enabled

DMAC_SYNC

DMAC_SYNC is a DMAC request line sync enable register.

Offset Address	Register Name	Total Reset Value
0x0034	DMAC_SYNC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dmac_sync															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dmac_sync	Controls whether to synchronize the request signals 0: The sync logic provided for the DMA request signals of the corresponding peripheral is enabled. 1: The sync logic provided for the DMA request signals of the corresponding peripheral is disabled.

DMAC_Cn_SRC_ADDR

DMAC_Cn_SRC_ADDR is a source address register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x100 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- The source address is incremented.
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last source address read by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0100 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_SRC_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_addr	DMA source address

DMAC_Cn_DEST_ADDR

DMAC_Cn_DEST_ADDR is a destination address register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x104 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register contains the destination address for the data to be transferred. Before a channel is enabled, its corresponding register must be programmed by using software. After the channel is enabled, the register is updated in any of the following cases:

- Destination address increment
- A complete data block is transferred and then loaded from LLI nodes.
- If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel stops data transfer. At this time, the read value is the last destination address written by the DMAC.

Offset Address	Register Name	Total Reset Value
0x0104 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_DEST_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_addr	DMA destination address

DMAC_Cn_LLI

DMAC_Cn_LLI is an LLI information register of DMA channel *n* (*n* = 0−3).

Its offset address is 0x108 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3. For details, see section "DMA Linked List."

Offset Address	Register Name	Total Reset Value
0x0108 + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_LLI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ll_item																														reserved	ll_master
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	ll_item	The bit[31:2] in the next LLI node address and the address bit[1:0] are set to 0. A linked list address must be 4-byte aligned.
[1]	RW	reserved	Reserved. This bit value must be 0 during write operations, and this bit must be masked during read operations.
[0]	RW	ll_master	Master for loading the next LLI node 0: master 1 1: master 2

DMAC_Cn_CONTROL

DMAC_Cn_CONTROL is a control register of DMA channel *n* (*n* = 0–3).

Its offset address is 0x10C + n x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

Offset Address	Register Name	Total Reset Value
0x010C + *n* x 0x20 (*n* = 0–3)	DMAC_Cn_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_tc_enable		prot_stat		dest_incr	src_incr	dest_select	src_select	dwidth				swidth				dbsize				sbsize				trans_size							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_tc_enable	Transfer terminal interrupt enable. This bit determines whether the current LLI node triggers a transfer terminal interrupt. 0: do not trigger 1: trigger
[30:28]	RW	prot_stat	HPROT[2:0] access protection signal transmitted by the master
[27]	RW	dest_incr	Destination address increment 0: The destination address is not incremented 1: The destination address is incremented once after a data segment is transferred If the destination device is a peripheral, the destination address is not incremented. If the destination device is a memory, the destination address is incremented.
[26]	RW	src_incr	Source address increment 0: The source address is not incremented 1: The source address is incremented once after a data segment is transferred If the source device is a peripheral, the source address is not incremented. If the source device is a memory, the source address is incremented.
[25]	RW	dest_select	Master for accessing the destination device 0: master 1 1: master 2
[24]	RW	src_select	Master for accessing the source device 0: master 1 1: master 2

[23:21]	RW	dwidth	Transfer bit width of the destination device The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of dwidth and the bit width, see Table 3-14.
[20:18]	RW	swidth	Transfer bit width of the source device The transfer bit width is invalid if it is greater than the bit width of the master. The data widths of the destination and source devices can be different. The hardware automatically packs and unpacks the data. For the mapping between the value of swidth and the bit width, see Table 3-14.
[17:15]	RW	dbsize	Burst size of the destination device It indicates the number of data segments to be transferred by the destination device in a burst transfer, that is, the number of transferred data segments when DMACCxBREQ is valid. This value must be set to a burst size supported by the destination device. If the destination device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of dbsize and the transfer length, see Table 3-13.
[14:12]	RW	sbsize	Burst size of the source device It indicates the amount of data to be transferred by the source device in a burst transfer, that is, the amount of transferred data when DMACCxBREQ is valid. The value must be set to a burst size supported by the source device. If the source device is a memory, the value is set to the storage area size beyond the storage address boundary. For the mapping between the value of sbsize and the transfer length, see Table 3-13.
[11:0]	RW	trans_size	The DMA transfer size can be configured by writing to this register only when the DMAC is a flow controller. This field indicates the amount of data to be transferred by the source device. When this register is read, the amount of data transferred through the bus connected to the destination device is obtained. If a channel is active, no valid information is obtained when this register is read. This is because that after software obtains the register value, the value changes during data transfer. Therefore, the register is read after the channel is enabled and data transfer stops.

DMAC_Cn_CONFIG

DMAC_Cn_CONFIG is a configuration register of channel *n* (*n* = 0−3).

Its offset address is 0x110 + *n* x 0x20. The value of *n* ranges from 0 to 3. The values 0–3 correspond to DMA channels 0–3.

This register is not updated when a new LLI node is loaded.

Offset Address	Register Name	Total Reset Value
0x110 + *n* x 0x20 (*n* = 0−3)	DMAC_Cn_CONFIG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													ch_halt	ch_active	ch_lock	tc_int_msk	err_int_msk	flow_ctrl		reserved		dest_periph				reserved		src_periph			ch_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[18]	RW	ch_halt	Halt bit 0: The DMA request is allowed. 1: The subsequent DMA requests are ignored and the contents in the channel FIFO are completely transmitted. This bit can disable a DMA channel without data loss by working with the Active bit and the Channel Enable bit.
[17]	RW	ch_active	Active bit 0: There is no data in the channel FIFO. 1: There is data in the channel FIFO. This bit can disable a DMA channel without data loss by working with the Halt bit and Channel Enable bit.
[16]	RW	ch_lock	Lock bit 0: Lock transfer on the bus is disabled. 1: Lock transfer on the bus is enabled.
[15]	RW	tc_int_msk	Transfer terminal interrupt mask 0: The transfer terminal interrupts of the channel are masked. 1: The transfer terminal interrupts of the channel are not masked.

[14]	RW	err_int_msk	Transfer error interrupt mask 0: The error interrupts of the channel are masked. 1: The error interrupts of the channel are not masked.
[13:11]	RW	flow_ctrl	Flow control and transfer type This field specifies the flow controller and transfer type. The flow controller can be the DMAC, source device, or destination device. The transfer type can be memory to peripheral, peripheral to memory, peripheral to peripheral, or memory to memory. For details, see Table 3-16.
[10]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[9:6]	RW	dest_periph	Destination device. This field is used to select a peripheral request signal as the request signal for the DMA destination device of the channel. If the destination device for DMA transfer is a memory, this field is ignored.
[5]	RW	reserved	Reserved This bit value must be 0 during write operations, and this bit must be masked during read operations.
[4:1]	RW	src_periph	Source device. This field is used to select a peripheral request signal as the request signal for the DMA source device of the channel. If the source device for DMA transfer is a memory, this field is ignored.
[0]	RW	ch_en	Channel enable. The current status of the channel can be queried by reading this field or DMAC_ENABLED_CHNS. 0: disabled 1: enabled Clearing this bit can disable a channel. When this bit is cleared, the current bus transfer continues until the data transfer is complete. Then, the channel is disabled and the remaining data in the FIFO is lost. When the last LLI node is transferred or an error occurs during transfer, the channel is also disabled and this bit is cleared. If you want to disable a channel without data loss, the Halt bit must be set to 1 so the subsequent DMA requests are ignored by the channel. After this, the Active bit must be polled until its value becomes 0, indicating that there is no data in the channel FIFO. At this time, the Enable bit can be cleared. Before enabling a channel by setting this bit to 1, you must reinitialize the channel; otherwise, unexpected results may occur. When a channel is disabled by writing DMAC_Cn_CONFIG [0], DMAC_Cn_CONFIG [0] can be reset again only after the corresponding bit of DMAC_ENABLED_CHNS is 0. This is because disabling the channel does not take effect immediately after DMAC_Cn_CONFIG [0] is cleared. The running delay

			during a bus burst operation also needs to be considered.

3.7 Timer

3.7.1 Overview

The timer module implements the timing and counting functions. It not only serves as the system clock of the operating system, but also can be used by applications for timing and counting. The Hi3516C V300 has four timers.

3.7.2 Features

Timer has the following features:

- Provides 16-bit or 32-bit down counter that has a programmable 8-bit prescaler.
- Provides a configurable count clock, that is, the clock can serve as the 50 MHz bus clock or 3 MHz crystal oscillator clock.
- Supports three count modes: free-running mode, periodic mode, and one-shot mode.
- Loads the initial value through either of the following registers: TIMERx_LOAD and
- TIMERx_BGLOAD.
- Reads the current count value at any time.
- Generates an interrupt when the count value is decreased to 0.

3.7.3 Function Description

The timer is a 32-bit or 16-bit configurable down counter. The counter value is decremented by 1 on each rising edge of the count clock. When the count value reaches 0, the timer generates an interrupt.

The timer supports three count modes:

- Free-running mode

  The timer counts continuously. When the count value reaches 0, the timer wraps its value around to the maximum value automatically and then continues to count. When the count length is 32 bits, the maximum value is 0xFFFF_FFFF. When the count length is 16 bits, the maximum value is 0xFFFF. In free-running mode, the count value is decremented immediately from the loaded value. When the value reaches 0, the value is wrapped around to the maximum value.

- Periodic mode

  The timer counts continuously. When the count value reaches 0, the timer loads an initial value from

  TIMERx_BGLOAD again and then continues to count.

- One-shot mode

The initial value is loaded to the timer. When the count value of the timer reaches 0, the timer stops counting. The timer starts to count again only when a new value is loaded and the timer is enabled.

Each timer has a prescaler that divides the frequency of the working clock of each timer by 1, 16, or 256. In this way, flexible frequencies of the count clock are provided. An initial value is loaded to the timer as follows:

- An initial value can be loaded by writing TIMERx_LOAD. When the timer works, if a value is written to TIMERx_LOAD, the timer recounts starting from this value immediately. This method is applicable to all count modes.
- The count cycle in periodic mode can be set by writing
- TIMERx_BGLOAD. The current count value of the timer is not affected immediately when TIMERx_BGLOAD is written. Instead, the timer continues to count until the count value reaches 0. Then the timer loads the new value of
- TIMERx_BGLOAD and starts to count.

3.7.4 Operating Mode

Initialization

The timer must be initialized when the system is initialized. To initialize timer*X* (*X* ranges from 0 to 3), do as follows:

Step 1 Write to TIMERx_LOAD to load an initial value to the timer.

Step 2 When the timer is required to work in periodic mode and the count cycle is different from the initial value loaded to the timer, write to TIMERx_BGLOAD to set the count cycle of the timer.

Step 3 Configure the SC_CTRL register of the system controller to set the reference clock of the clock enable signal of the timer.

Step 4 Write to TIMERx_CONTROL to set the count mode, counter length, prescaling factor, and interrupt mask of the timer, and then enable the timer to count.

----End

Interrupt Processing

The timer is used to generate interrupts periodically. Therefore, interrupt processing is a process of activating and waiting the timing interrupt. To process an interrupt, do as follows:

Step 1 Configure TIMERx_INTCLR to clear the interrupt of the timer.

Step 2 Activate the processes of waiting for the interrupt and execute the process.

Step 3 When all the processes of waiting for the interrupt are complete or the wait interrupt is in hibernate state, resume the interrupt and continue to execute the interrupted program.

----End

Clock Selection

Each timer has two optional count clocks. The following sections describe how to select a clock by taking timer0 as an example.

To select the bus clock as the count clock, do as follows:

Step 1 Set SC_CTRL [timeren0ov] to 1.

Step 2 Initialize the timer and start to count.

----End

To select the 3 MHz crystal oscillator clock as the count clock, do as follows:

Step 1 Set SC_CTRL [timeren0sel] to 0.

Step 2 Initialize the timer and start to count.

----End

3.7.5 Register Summary

The timer module consists of four timers and each timer involves a group of registers. The four groups of registers have the same features except that their base addresses are different. The details about their base addresses are as follows:

- The base address of timer 0: 0x1200_0000.
- The base address of timer 1: 0x1200_0020.
- The base address of timer 2: 0x1200_1000.
- The base address of timer 3: 0x1200_1020.

NOTE

The value of *X* in timer*X* ranges from 0 to 3. The registers for timer 0 to timer 3 are the same. In this section, timer 0 registers are described as an example.

Table 3-18 Summary of timer registers

Offset Address	Register	Description	Page
0x000	TIMERx_LOAD	Initial count value register	3-130
0x004	TIMERx_VALUE	Current count value register	3-130
0x008	TIMERx_CONTROL	Control register	3-131
0x00C	TIMERx_INTCLR	Interrupt clear register	3-132
0x010	TIMERx_RIS	Raw interrupt status register	3-133
0x014	TIMERx_MIS	Masked interrupt status register	3-133
0x018	TIMERx_BGLOAD	Initial count value register in periodic mode	3-134

3.7.6 Register Description

TIMERx_LOAD

TIMERx_LOAD is an initial count value register. It is used to set the initial count value of each timer. Each timer (timers 0–3) has one such register.

NOTE

- The minimum valid value written to TIMER*x*_LOAD is 1.
- When the value 0 is written to TIMER*x*_LOAD, the dual-timer module generates an interrupt immediately.

If values are written to TIMERx_BGLOAD and TIMERx_LOAD before the rising edge of TIMCLK enabled by TIMCLKENx reaches, the count value of the next rising edge of TIMCLK is changed to the value written to TIMERx_LOAD. As the value of

TIMERx_BGLOAD changes when data is written to TIMERx_LOAD, the value returned after TIMERx_BGLOAD is read is the latest value that is written to TIMERx_LOAD and TIMERx_BGLOAD. When the timer works in periodic mode and the count value decreases to 0, the initial value is loaded from TIMERx_BGLOAD to continue counting.

Offset Address	Register Name	Total Reset Value
0x000	TIMER0_LOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_load																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0_load	Initial count value of timer 0

TIMERx_VALUE

TIMERx_VALUE is a current count value register. It shows the current value of the counter that is decremented. Each timer (timers 0–3) has one such register.

After a value is written to TIMERx_LOAD, TIMERx_VALUE immediately shows the newly loaded value of the counter in the PCLK domain without waiting for the clock edge of TIMCLK enabled by TIMCLKENx.

NOTE

When a timer is in 16-bit mode, the 16 upper bits of the 32-bit TIMERx_VALUE are not set to 0 automatically. If the timer is switched from 32-bit mode to 16-bit mode and no data is written to TIMERx_LOAD, the upper 16 bits of TIMERx_VALUE may be non-zero.

Offset Address	Register Name	Total Reset Value
0x004	TIMER0_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_value																															

Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	timer0_value	Current count value of timer 0 that is decremented

TIMERx_CONTROL

TIMERx_CONTROL is a control register. Each timer (timers 0–3) has one such register.

NOTE

When the periodic mode is selected, TIMER*x*_CONTROL[timermode] must be set to 1 and TIMER*x*_CONTROL[oneshot] must be set to 0.

Offset Address	Register Name	Total Reset Value
0x008	TIMER0_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								timeren	timermode	intenable	reserved	timerpre		timersize	oneshot
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	timeren	Timer enable 0: disabled 1: enabled
[6]	RW	timermode	Timer count mode 0: free-running mode 1: periodic mode
[5]	RW	intenable	TIMERx_RIS interrupt mask 0: masked 1: not masked
[4]	RO	reserved	Reserved

[3:2]	RW	timerpre	Prescaling factor configuration 00: no prescaling. That is, the clock frequency of the timer is divided by 1 01: 4-level prescaling. That is, the clock frequency of the timer is divided by 16 10: 8-level prescaling. That is, the clock frequency of the timer is divided by 256 11: undefined. If the bits are set to 11, 8-level prescaling is considered. That is, the clock frequency of the timer is divided by 256.
[1]	RW	timersize	Counter select 0: 16-bit counter 1: 32-bit counter
[0]	RW	oneshot	Count mode select 0: periodic mode or free-running mode 1: one-shot mode

TIMERx_INTCLR

TIMERx_INTCLR is the interrupt clear register. The interrupt status of a counter is cleared after any operation is performed on this register. Each timer (timers 0–3) has one such register.

CAUTION

This register is a write-only register. The timer clears interrupts when any value is written to this register. In addition, no value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x00C	TIMER0_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	timer0_intclr	Writing this register clears the output interrupt of timer 0.

TIMERx_RIS

TIMERx_RIS is a raw interrupt status register. Each timer (timers 0–3) has one such register.

Offset Address	Register Name	Total Reset Value
0x010	TIMER0_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0ris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved. Writing this register has no effect and reading this register returns 0.
[0]	RO	timer0ris	Raw interrupt status of timer 0 0: No interrupt is generated. 1: An interrupt is generated.

TIMERx_MIS

TIMERx_MIS is a masked interrupt status register. Each timer (timers 0–3) has one such register.

Offset Address	Register Name	Total Reset Value
0x014	TIMER0_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															timer0mis
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	timer0mis	Masked interrupt status of timer 0 0: The interrupt is invalid. 1: The interrupt is valid.

TIMERx_BGLOAD

TIMERx_BGLOAD is an initial count value register in periodic mode. Each timer (timers 0–3) has one such register.

The TIMERx_BGLOAD register contains the initial count value of the timer. This register is used to reload an initial count value when the count value of the timer reaches 0 in periodic mode.

In addition, this register provides another method of accessing TIMERx_LOAD. The difference is that after a value is written to TIMERx_BGLOAD, the timer does not count starting from the input value immediately.

Offset Address	Register Name	Total Reset Value
0x018	TIMER0_BGLOAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timer0bgload																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	timer0bgload	Initial count value of timer 0 Note: This register differs from TIMERx_LOAD. For details, see the descriptions of TIMERx_LOAD.

3.8 Watchdog

3.8.1 Overview

The watchdog is used to transmit a reset signal to reset the entire system within a period after an exception occurs in the system.

3.8.2 Features

The watchdog has the following features:

- Provides a 32-bit internal down counter. The count clock source is configurable.
- Supports the configurable timeout interval, namely, initial count value.
- Locks registers to avoid any modification to them.
- Supports the generation of timeout interrupts.
- Supports the generation of reset signals.
- Supports the debugging mode.

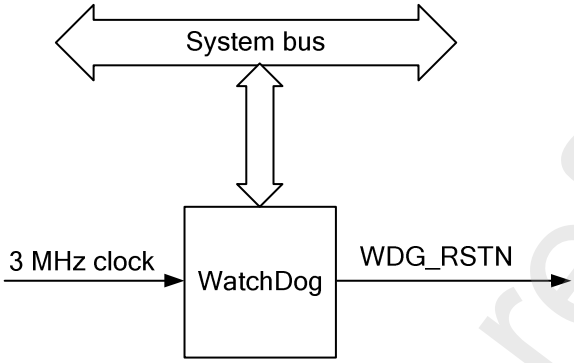
3.8.3 Function Description

Application Block Diagram

The watchdog transmits interrupt requests to the system periodically. When the system does not respond to the interrupt requests (such as the suspend case), the watchdog transmits the reset signal to reset the system. In this way, the system running status is monitored.

Figure 3-9 shows the application block diagram of the watchdog.

Figure 3-9 Application block diagram of the watchdog



Function Principle

The watchdog works based on a 32-bit down counter. The initial value is loaded by WDG_LOAD. When the watchdog clock is enabled, the count value is decremented by 1 on the rising edge of each count clock. When the count value reaches 0, the watchdog generates an interrupt. On the next rising edge of the count clock, the counter reloads the initial value from WDG_LOAD and continues to count in decremental mode.

If the count value of the counter reaches 0 for the second time but the CPU does not clear the watchdog interrupt, the watchdog transmits the reset signal and the counter stops counting.

You can enable or disable the watchdog by configuring WDG_CONTROL as required. That is, you can control the watchdog whether to generate interrupts and reset signals.

- When the interrupt generation function is disabled, the watchdog counter stops counting.
- When the interrupt generation function is enabled again, the watchdog counter counts starting from the preset value of WDG_LOAD instead of the last count value. Before an interrupt is generated, the initial value can be reloaded.

The count clock of the watchdog can be a crystal oscillator clock or a bus clock so different count time ranges are available.

By configuring WDG_LOCK, you can disable the operation of writing to the internal registers of the watchdog.

- Writing 0x1ACC_E551 to WDG_LOCK to enable the write permission for all the registers of the watchdog.
- Writing any other values to WDG_LOCK to disable the write permission for all the registers of the watchdog except WDG_LOCK.

This feature avoids modifications to the watchdog registers by software. Therefore, the watchdog operation is not terminated by mistake by software when an exception occurs.

In debugging mode, the watchdog is disabled automatically to avoid the intervention to the normal debugging.

3.8.4 Operating Mode

Configuring the Frequency of the Count Clock

The count time T_{WDG} of the watchdog is calculated as follows:

$$T_{WDG} = Value_{WDG\_LOAD} \times \left(\frac{1}{f_{clk}} \right)$$

NOTE

The definition of each parameter in the preceding formula is as follows:

- T_{WDG} indicates the count time of the watchdog.
- $Value_{WDG\_LOAD}$ indicates the initial count value of the watchdog.
- f_{clk} indicates the frequency of the watchdog count clock.

The range of the count time of the watchdog is 0s to 1400s.

Initializing the System

The watchdog counter stops counting after the system power-on reset. Before the system is initialized, the watchdog must be initialized and enabled. To initialize the watchdog, perform the following steps:

Step 1 Write to WDG_LOAD to set the initial count value.

Step 2 Write to WDG_CONTROL to enable the interrupt mask function and start the watchdog counter.

Step 3 Write to WDG_LOCK to lock the watchdog to avoid the watchdog settings being modified by the software by mistake.

----End

Processing an Interrupt

After an interrupt is received from the watchdog, the interrupt must be cleared in time and the initial count value must be reloaded to the watchdog to restart counting. A watchdog interrupt is processed as follows:

Step 1 Write 0x1ACC_E551 to WDG_LOCK to unlock the watchdog.

Step 2 Write to WDG_INTCLR to clear the watchdog interrupt and load the initial count value to the watchdog to restart counting.

Step 3 Write any other values rather than 0x1ACC_E551 to WDG_LOCK to lock the watchdog.

----End

Disabling the Watchdog

You can control the status of the watchdog by writing 0 or 1 to WDG_CONTROL[inten].

- 0: disabled
- 1: enabled

3.8.5 Register Summary

Table 3-19 describes watchdog registers.

Table 3-19 Summary of watchdog registers (base address: 0x1208_0000)

Offset Address	Register	Description	Page
0x0000	WDG_LOAD	Initial count value register	3-137
0x0004	WDG_VALUE	Current count value register	3-137
0x0008	WDG_CONTROL	Control register	3-138
0x000C	WDG_INTCLR	Interrupt clear register	3-138
0x0010	WDG_RIS	Raw interrupt register	3-139
0x0014	WDG_MIS	Masked interrupt status register	3-139
0x0C00	WDG_LOCK	Lock register	3-140

3.8.6 Register Description

WDG_LOAD

WDG_LOAD is an initial count value register. It is used to configure the initial count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0000	WDG_LOAD	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_load																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	wdg_load	Initial count value of the watchdog counter

WDG_VALUE

WDG_VALUE is a current count value register It is used to read the current count value of the internal counter of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0004	WDG_VALUE	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdogvalue																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RO	wdogvalue	Current count value of the watchdog counter

WDG_CONTROL

WDG_CONTROL is a control register. It is used to enable or disable the watchdog and control the interrupt and reset functions of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0008	WDG_CONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														resen	inten
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	resen	Output enable of the watchdog reset signal 0: disabled 1: enabled
[0]	RW	inten	Output enable of the watchdog interrupt signal 0: The counter stops counting, the current count value remains unchanged, and the watchdog is disabled. 1: The counter, interrupt and watchdog are enabled.

WDG_INTCLR

WDG_INTCLR is an interrupt clear register. It is used to clear watchdog interrupts so the watchdog can reload an initial value for counting. This register is write-only. When a value is written to this register, the watchdog interrupts are cleared. No written value is recorded in this register and no default reset value is defined.

Offset Address	Register Name	Total Reset Value
0x000C	WDG_INTCLR	-

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_intclr																															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Access	Name	Description
[31:0]	WO	wdg_intclr	Writing any value to this register clears the watchdog interrupts and enables the watchdog to reload an initial count value from WDG_LOAD to restart counting.

WDG_RIS

WDG_RIS is a raw interrupt status register. It shows the raw interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0010	WDG_RIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogris
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wdogris	Status of the raw interrupts of the watchdog. When the count value reaches 0, this bit is set to 1. 0: No interrupt is generated. 1: An interrupt is generated.

WDG_MIS

WDG_MIS is a masked interrupt status register. It shows the masked interrupt status of the watchdog.

Offset Address	Register Name	Total Reset Value
0x0014	WDG_MIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wdogmis

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wdogmis	Status of the masked interrupts of the watchdog 0: No interrupt is generated or the interrupt is masked. 1: An interrupt is generated.

WDG_LOCK

WDG_LOCK is a lock register. It is used to control the write and read permissions for the watchdog registers.

Offset Address	Register Name	Total Reset Value
0x0C00	WDG_LOCK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdg_lock																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdg_lock	Writing 0x1ACC_E551 to this register enables the write permission for all the registers. Writing other values disables the write permission for all the registers. When this register is read, the lock status rather than the written value of this register is returned. 0x0000_0000: The write permission is available (unlocked). 0x0000_0001: The write permission is unavailable (locked).

3.9 RTC

3.9.1 Overview

The RTC is used to display the time in real time and periodically generate alarms.

3.9.2 Features

The RTC has the following features:

- Provides a 40-bit counter. Of the 40 bits, 16 bits are for counting days, five bits are for counting hours, six bits are for counting minutes, six bits are for counting seconds, and the other seven bits are for counting 10 ms.

- Provides a 100 Hz count clock.
- Supports the configurable initial count value.
- Supports the configurable count comparison value.
- Generates the timeout interrupt.
- Supports soft reset.
- Supports configurable frequency division parameters.
- Stores user data in a 64-bit user register.
- Supports battery low-voltage detection.

3.9.3 Function Description

The RTC has a 40-bit up counter for counting days, hours, minutes, seconds, and 10 ms. The initial values are loaded from RTC_LR_10MS, RTC_LR_S, RTC_LR_M, RTC_LR_H, RTC_LR_D_L, and RTC_LR_D_H. This section assumes that the counter is divided into the day counter, hour counter, minute counter, second counter, and 10 ms counter. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt. Then, the counter continues to count in incremental mode on the rising edge of the next count clock.

By configuring RTC_IMSC, you can allow or forbid the RTC to generate interrupts. Note the following two cases:

- When the function of generating interrupts is disabled, the RTC counter continues to count in incremental mode and no interrupts are generated. RTC_MSC_INT shows the status of masked interrupts and RTC_RAW_INT shows the status of raw interrupts.
- When the function of generating interrupts is enabled, the RTC counter still counts in incremental mode. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC generates an interrupt.

The RTC uses a 100 Hz count clock and a 16-bit day counter. The value of the day counter can be used to reckon the specific year, month, and day.

3.9.4 Operating Mode

3.9.4.1 Count Clock Frequency

The RTC uses a 100 Hz count clock. The maximum RTC count time (T_{RTC}) is calculated as follows:

$T_{RTC} = 2^{16} = 65536$ days

NOTE

T_{RTC} is the RTC count time.

3.9.4.2 Soft Reset

The RTC can be separately soft-reset by configuring RTC_POR_N. After soft reset, the value of each RTC configuration register is restored to its default value. Therefore, these registers must be initialized again.

To soft-reset the RTC, perform the following steps:

Step 1 Write 0 to RTC_POR_N.

Step 2 Wait 30 ms.

----End

3.9.4.3 Initializing the RTC

The system needs to initialize the RTC when the RTC is powered on for the first time. The initialization process is as follows:

Step 1 Configure RTC_POR_N to reset the RTC.

Step 2 Wait 30 ms.

Step 3 Configure RTC_IMSC to set the interrupt mask bit of the RTC.

Step 4 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the RTC match value.

Step 5 Configure RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H to set the initial count value of the RTC.

Step 6 Set RTC_LORD to 1 to load the initial count value to the RTC counter.

Step 7 Wait 5 ms.

Step 8 Based on the 100 Hz count clock, the RTC counts starting from the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H. When the count value is equal to the values of RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H, the RTC determines whether to generate an interrupt based on the settings of RTC_IMSC.

----End

3.9.4.4 Handling Interrupts

If the system receives an interrupt from the RTC, the configured time is reached. Then user-defined operations can be performed. The RTC counter, however, still counts in incremental mode. To clear an RTC interrupt, set RTC_INT_CLR to 1. To continue to configure time, write a new match value to RTC_MR_10MS, RTC_MR_S, RTC_MR_M, RTC_MR_H, RTC_MR_D_L, and RTC_MR_D_H.

3.9.4.5 Accessing RTC Registers

Internal RTC registers are located in the RTC module, not on the bus. The RTC registers on the bus are used only for accessing internal RTC registers.

To write to internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This example assumes that the clock is 50 MHz and the expected SPI clock is 5 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (50/5)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to write 0x10 to RTC_MR_10MS, write 0x01060010 to SPI_RW. That is, spi_start is 1, spi_rw is 0, spi_add is 0x06, and spi_wdata is 0x10.

----End

To read internal RTC registers, perform the following steps:

Step 1 Configure SPI_CLK_DIV.

This step assumes that the clock is 50 MHz and the expected SPI clock is 5 MHz. The configured value of SPI_CLK_DIV is calculated as follows: (50/5)/2 – 1 = 4 = 0x04. If you have configured SPI_CLK_DIV and do not want to change the SPI clock frequency, skip this step.

Step 2 Read SPI_RW bit[31] until it is 0.

Step 3 Configure SPI_RW.

The internal offset address for RTC_MR_10MS is 0x06. If you want to read SPI_RW, write 0x01860000 to SPI_RW. That is, spi_start is 1, spi_rw is 0, and spi_add is 0x06.

Step 4 Read SPI_RW bit[31] until it is 0. SPI_RW [15:8] is the value that is returned after RTC_MR_10MS is read.

----End

3.9.5 Register Summary

Table 3-20 describes RTC registers.

Table 3-20 Summary of RTC registers (base address: 0x1209_0000)

Offset Address	Register	Description	Page
0x0000	SPI_CLK_DIV	SPI clock divider register	3-146
0x0004	SPI_RW	SPI read/write register	3-146
0x0080	CONVER_T	External temperature sensor DS1820 (DS18B20) measurement control register	3-147
0x0084	CRC_EN	External temperature sensor DS1820 (DS18B20) measurement CRC check enable register	3-148
0x0088	INT_MASK	External temperature sensor DS1820 (DS18B20) measurement interrupt mask register	3-148
0x008C	INT_CLEAR	External temperature sensor DS1820 (DS18B20) measurement interrupt clear register	3-149

Offset Address	Register	Description	Page
0x0090	BUSY	External temperature sensor DS1820 (DS18B20) measurement status register	3-149
0x0094	INT_RAW	External temperature sensor DS1820 (DS18B20) measurement interrupt status register	3-150
0x0098	INT_TCAP	External temperature sensor DS1820 (DS18B20) measurement interrupt status register	3-150
0x009C	T_VALUE	External temperature sensor DS1820 (DS18B20) measurement value register	3-151
0x00A0	FILTER_NUM	Filter glitch width configuration register	3-151

Table 3-21 describes the internal RTC registers.

Table 3-21 Summary of internal RTC registers (base address: 0x00)

Offset Address	Register	Description	Page
0x00	RTC_10MS_COUNT	Count value register for the RTC 10 ms counter	3-152
0x01	RTC_S_COUNT	Count value register for the RTC second counter	3-152
0x02	RTC_M_COUNT	Count value register for the RTC minute counter	3-153
0x03	RTC_H_COUNT	Count value register for the RTC hour counter	3-153
0x04	RTC_D_COUNT_L	Lower-8-bit count value register for the RTC day counter	3-154
0x05	RTC_D_COUNT_H	Upper-8-bit count value register for the RTC day counter	3-154
0x06	RTC_MR_10MS	Match value register for the RTC 10 ms counter	3-154
0x07	RTC_MR_S	Match value register for the RTC second counter	3-155
0x08	RTC_MR_M	Match value register for the RTC minute counter	3-155

Offset Address	Register	Description	Page
0x09	RTC_MR_H	Match value register for the RTC hour counter	3-156
0x0A	RTC_MR_D_L	Lower-8-bit match value register for the RTC day counter	3-156
0x0B	RTC_MR_D_H	Upper-8-bit match value register for the RTC day counter	3-156
0x0C	RTC_LR_10MS	Configured value register for the RTC 10 ms counter	3-157
0x0D	RTC_LR_S	Configured value register for the RTC second counter	3-157
0x0E	RTC_LR_M	Configured value register for the RTC minute counter	3-158
0x0F	RTC_LR_H	Configured value register for the RTC hour counter	3-158
0x10	RTC_LR_D_L	Lower-8-bit configured value register for the RTC day counter	3-159
0x11	RTC_LR_D_H	Upper-8-bit configured value register for the RTC day counter	3-159
0x12	RTC_LORD	RTC configured value loading enable register	3-160
0x13	RTC_IMSC	RTC interrupt enable register	3-160
0x14	RTC_INT_CLR	RTC interrupt clear register	3-161
0x15	RTC_MSC_INT	RTC mask interrupt status register.	3-161
0x16	RTC_RAW_INT	RTC raw interrupt status register	3-162
0x17	RTC_CLK	RTC output clock select register	3-163
0x18	RTC_POR_N	RTC reset control register	3-163
0x1A	RTC_UV_CTRL	RTC internal low-voltage detection control register	3-164
0x51	SDM_COEF_OUSIDE_H	External frequency division coefficient upper four bits register	3-164
0x52	SDM_COEF_OUSIDE_L	External frequency division coefficient lower eight bits register	3-165
0x53	USER_REGISTER1	64-bit user register 1	3-165
0x54	USER_REGISTER2	64-bit user register 2	3-166
0x55	USER_REGISTER3	64-bit user register 3	3-166
0x56	USER_REGISTER4	64-bit user register 4	3-166

Offset Address	Register	Description	Page
0x57	USER_REGISTER5	64-bit user register 5	3-167
0x58	USER_REGISTER6	64-bit user register 6	3-167
0x59	USER_REGISTER7	64-bit user register 7	3-167
0x5A	USER_REGISTER8	64-bit user register 8	3-168

3.9.6 RTC Register Description

SPI_CLK_DIV

SPI_CLK_DIV is an SPI clock divider register.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_CLK_DIV	0x0000_003B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi_clk_div							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	spi_clk_div	Clock divider of the SPI. The SPI clock frequency cannot be higher than 5 MHz. The value 5 MHz is recommended. The field value ranges from 1 to 255. The value of spi_clk_div is used to calculate the frequencies of the SPI TX and RX clocks. The formula is as follows: FSPICLK = FAPBCLK/[2 x (spi_clk_div + 1)]. FAPBCLK is the clock frequency. If the clock is 50 MHz and the expected SPI clock is 5 MHz, the configured value of spi_clk_div is calculated as follows: (50/5)/2 – 1 = 4

SPI_RW

SPI_RW is an SPI read/write register.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_RW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_busy	reserved							spi_start	spi_rw	spi_add						spi_rdata								spi_wdata							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	spi_busy	SPI read/write status indicator 0: The SPI is idle, and a new read/write operation can be initiated over the SPI. 1: A read/write operation is being performed over the SPI, and no new operation is allowed.
[30:25]	RO	reserved	Reserved
[24]	W1_PULSE	spi_start	SPI read/write start. Writing 1 automatically clears this field. Writing has no effect when spi_busy is 1. That is, no new SPI operation is started before the previous read/write operation is complete. If a start request is sent, hardware ignores this request.
[23]	RW	spi_rw	SPI operation type 0: write 1: read
[22:16]	RW	spi_add	SPI operation address The address range is 0–127.
[15:8]	RO	spi_rdata	Data read from the SPI
[7:0]	RW	spi_wdata	Data to be written to the SPI

CONVER_T

CONVER_T is an external temperature sensor DS1820 (DS18B20) measurement control register.

Offset Address	Register Name	Total Reset Value
0x0080	CONVER_T	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															conver_t
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	conver_t	External temperature sensor DS1820 (DS18B20) measurement start. This field must be set to 1. 1: start. Hardware automatically sets this field to 0 when the interrupt is cleared.

CRC_EN

CRC_EN is an external temperature sensor DS1820 (DS18B20) measurement CRC check enable register.

Offset Address	Register Name	Total Reset Value
0x0084	CRC_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															crc_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	crc_en	External temperature sensor DS1820 (DS18B20) measurement CRC check enable 0: disabled 1: enabled

INT_MASK

INT_MASK is an external temperature sensor DS1820 (DS18B20) measurement interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0088	INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	int_mask	External temperature sensor DS1820 (DS18B20) measurement interrupt mask 0: not masked 1: masked

INT_CLEAR

INT_CLEAR is an external temperature sensor DS1820 (DS18B20) measurement interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x008C	INT_CLEAR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	int_clear	External temperature sensor DS1820 (DS18B20) measurement interrupt clear Writing 1 clears the interrupt. Hardware automatically sets this field to 0 after the interrupt is cleared.

BUSY

BUSY is an external temperature sensor DS1820 (DS18B20) measurement status register.

Offset Address	Register Name	Total Reset Value
0x0090	BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	busy	External temperature sensor DS1820 (DS18B20) measurement status 0: ready 1: busy

INT_RAW

INT_RAW is an external temperature sensor DS1820 (DS18B20) raw measurement interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0094	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														int_err	get_tmprt_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	int_err	Error interrupt
[0]	RO	get_tmprt_int	External temperature sensor DS1820 (DS18B20) measurement completion interrupt

INT_TCAP

INT_TCAP is an external temperature sensor DS1820 (DS18B20) measurement interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0098	INT_TCAP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_tcap
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	int_tcap	Masked interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

T_VALUE

T_VALUE is an external temperature sensor DS1820 (DS18B20) measurement value register.

Offset Address	Register Name	Total Reset Value
0x009C	T_VALUE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				t_value											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	t_value	Temperature measured by the external temperature sensor DS1820 (DS18B20)

FILTER_NUM

FILTER_NUM is a filter glitch width configuration register.

Offset Address	Register Name	Total Reset Value
0x00A0	FILTER_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												filter_num			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	filter_num	Filter glitch width for inputs. The glitch with the width of (N + 1) APB clocks is filtered.

3.9.7 Internal Register Description

RTC_10MS_COUNT

RTC_10MS_COUNT is a count value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x00	RTC_10MS_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_10ms_count						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RO	rtc_10ms_count	RTC 10 ms counter value. It indicates the currently counted time. Its unit is 10 ms. The value range is 0–99.

RTC_S_COUNT

RTC_S_COUNT is a count value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x01	RTC_S_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_s_count					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RO	rtc_s_count	RTC second counter value. It indicates the currently counted seconds. The value range is 0–59.

RTC_M_COUNT

RTC_M_COUNT is a count value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x02	RTC_M_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_m_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RO	rtc_m_count	RTC minute counter value. It indicates the currently counted minutes. The value range is 0–59.

RTC_H_COUNT

RTC_H_COUNT is a count value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x03	RTC_H_COUNT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_h_count				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved
[4:0]	RO	rtc_h_count	RTC hour counter value. It indicates the currently counted hours. The value range is 0–23.

RTC_D_COUNT_L

RTC_D_COUNT_L is a lower-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x04	RTC_D_COUNT_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_l	Lower eight bits of the RTC day counter value. This field works with RTC_D_COUNT_H to indicate the currently counted days. The day range is 0–65535.

RTC_D_COUNT_H

RTC_D_COUNT_H is an upper-8-bit count value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x05	RTC_D_COUNT_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_d_count_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	rtc_d_count_h	Upper eight bits of the RTC day counter value. This field works with RTC_D_COUNT_L to indicate the currently counted days. The day range is 0–65535.

RTC_MR_10MS

RTC_MR_10MS is a match value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x06	RTC_MR_10MS	0x7F

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_mr_10ms						

Reset	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RW	rtc_mr_10ms	Match value of the RTC 10 ms counter The value range is 0–99.

RTC_MR_S

RTC_MR_S is a match value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x07	RTC_MR_S	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_s					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_mr_s	Match value of the RTC second counter The value range is 0–59.

RTC_MR_M

RTC_MR_M is a match value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x08	RTC_MR_M	0x3F

Bit	7	6	5	4	3	2	1	0
Name	reserved		rtc_mr_m					
Reset	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved

[5:0]	RW	rtc_mr_m	Match value of the RTC minute counter The value range is 0–59.

RTC_MR_H

RTC_MR_H is a match value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x09	RTC_MR_H	0x1F

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_mr_h				
Reset	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved
[4:0]	RW	rtc_mr_h	Match value of the RTC hour counter The value range is 0–23.

RTC_MR_D_L

RTC_MR_D_L is a lower-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0A	RTC_MR_D_L	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_l							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_l	Lower eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_H to indicate the matched day. The day range is 0–65535.

RTC_MR_D_H

RTC_MR_D_H is an upper-8-bit match value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x0B	RTC_MR_D_H	0xFF

Bit	7	6	5	4	3	2	1	0
Name	rtc_mr_d_h							
Reset	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[7:0]	RW	rtc_mr_d_h	Upper eight bits of the match value of the RTC day counter. This field works with RTC_MR_D_L to indicate the matched day. The day range is 0–65535.

RTC_LR_10MS

RTC_LR_10MS is a configured value register for the RTC 10 ms counter.

Offset Address	Register Name	Total Reset Value
0x0C	RTC_LR_10MS	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_lr_10ms						
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7]	RO	reserved	Reserved
[6:0]	RW	rtc_lr_10ms	Configured value of the RTC 10 ms counter The value range is 0–99.

RTC_LR_S

RTC_LR_S is a configured value register for the RTC second counter.

Offset Address	Register Name	Total Reset Value
0x0D	RTC_LR_S	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved	rtc_lr_s						

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_lr_s	Configured value of the RTC second counter The value range is 0–59.

RTC_LR_M

RTC_LR_M is a configured value register for the RTC minute counter.

Offset Address	Register Name	Total Reset Value
0x0E	RTC_LR_M	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_lr_m				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	rtc_lr_m	Configured value of the RTC minute counter The value range is 0–59.

RTC_LR_H

RTC_LR_H is a configured value register for the RTC hour counter.

Offset Address	Register Name	Total Reset Value
0x0F	RTC_LR_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved			rtc_lr_h				
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:5]	RO	reserved	Reserved

[4:0]	RW	rtc_lr_h	Configured value of the RTC hour counter The value range is 0–23.

RTC_LR_D_L

RTC_LR_D_L is a lower-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x10	RTC_LR_D_L	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_l							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_l	Lower eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_H to indicate the configured day. The day range is 0–65535.

RTC_LR_D_H

RTC_LR_D_H is an upper-8-bit configured value register for the RTC day counter.

Offset Address	Register Name	Total Reset Value
0x11	RTC_LR_D_H	0x00

Bit	7	6	5	4	3	2	1	0
Name	rtc_lr_d_h							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	rtc_lr_d_h	Upper eight bits of the configured value of the RTC day counter. This field works with RTC_LR_D_L to indicate the configured day. The day range is 0–65535.

RTC_LORD

RTC_LORD is an RTC configured value loading enable register.

Offset Address	Register Name	Total Reset Value
0x12	RTC_LORD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					rtc_lock_bypass	rtc_lock	rtc_load
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	reserved	Reserved
[2]	RW	rtc_lock_bypass	RTC lock enable 0: enabled. The RTC count value (0x00−0x05) is updated only after the RTC is successfully locked. 1: disabled. The RTC count value (0x00−0x05) is updated in real time.
[1]	RW	rtc_lock	RTC lock. If software writes 1, hardware is automatically cleared after the RTC is successfully locked. Note: This field is valid only when rtc_lock_bypass is 0.
[0]	RW	rtc_load	RTC configured value loading enable. When the field is enabled, the RTC configured value will be loaded to the RTC accumulator. If software writes 1 to load the configured value, hardware will automatically set this field to 0 after successful loading.

RTC_IMSC

RTC_IMSC is an RTC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x13	RTC_IMSC	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved					rtc_imsc	rtc_imsc_uv	rtc_imsc_time
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:3]	RO	reserved	Reserved

[2]	RW	rtc_imsc	RTC global interrupt output enable 0: disabled 1: enabled
[1]	RW	rtc_imsc_uv	Battery low-voltage detection interrupt output enable 0: disabled 1: enabled
[0]	RW	rtc_imsc_time	RTC timing interrupt output enable 0: disabled 1: enabled

RTC_INT_CLR

RTC_INT_CLR is an RTC interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x14	RTC_INT_CLR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_int_clr
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved
[0]	WO	rtc_int_clr	RTC interrupt clear register. Writing any value by software clears the interrupt. Reading back the value has no effect.

RTC_MSC_INT

RTC_MSC_INT is an RTC mask interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15	RTC_MSC_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						mask_int_uv	mask_int_time

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1]	RO	mask_int_uv	Status of the masked battery low-voltage detection interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	mask_int_time	Status of the masked RTC timing interrupt 0: No interrupt is generated. 1: An interrupt is generated.

RTC_RAW_INT

RTC_RAW_INT is an RTC raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16	RTC_RAW_INT	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved						raw_int_uv	raw_int_time
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1]	RO	raw_int_uv	Status of the raw battery low-voltage detection interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	raw_int_time	Status of the raw RTC timing interrupt 0: No interrupt is generated. 1: An interrupt is generated.

RTC_CLK

RTC_CLK is an RTC output clock select register.

Offset Address	Register Name	Total Reset Value
0x17	RTC_CLK	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved							clk_out_sel
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:2]	RO	reserved	Reserved
[1:0]	RW	clk_out_sel	Output test clock of the RTC 00: crystal oscillator clock 01: corrected 100 Hz clock 1x: 1 Hz clock

RTC_POR_N

RTC_POR_N is an RTC reset control register.

Offset Address	Register Name	Total Reset Value
0x18	RTC_POR_N	0x01

Bit	7	6	5	4	3	2	1	0
Name	reserved							rtc_por_n
Reset	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[7:1]	RO	reserved	Reserved
[0]	RW	rtc_por_n	RTC reset. This field is automatically set to 1 after the RTC is successfully reset. 0: reset

RTC_UV_CTRL

RTC_UV_CTRL is an RTC internal low-voltage detection control register.

Offset Address	Register Name	Total Reset Value
0x1A	RTC_UV_CTRL	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		bat_uv_ctrl_en	bat_uv_ctrl_sel	reserved		sample_time	
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5]	RW	bat_uv_ctrl_en	Low-voltage detection enable 0: disabled 1: enabled
[4]	RW	bat_uv_ctrl_sel	Low-voltage detection source select 0: no filtering 1: filtering
[3:2]	RO	reserved	Reserved
[1:0]	RW	sample_time	Low-voltage detection cycle 00: 1s 01: 1 minute 10: 10 minutes 11: 30 minutes

SDM_COEF_OUSIDE_H

SDM_COEF_OUSIDE_H is an external frequency division coefficient upper four bits register.

Offset Address	Register Name	Total Reset Value
0x51	SDM_COEF_OUSIDE_H	0x8

Bit	7	6	5	4	3	2	1	0
Name	Reserved				Sdm_coef_ouside_h			

Reset	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3:0]	RW	Sdm_coef_ousi de_h	Upper four bits of the frequency division coefficient in fixed frequency-division mode

SDM_COEF_OUSIDE_L

SDM_COEF_OUSIDE_L is an external frequency division coefficient lower eight bits register.

Offset Address	Register Name	Total Reset Value
0x52	SDM_COEF_OUSIDE_L	0x1B

Bit	7	6	5	4	3	2	1	0
Name	sdm_coef_ouside_l							
Reset	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[7:0]	RW	sdm_coef_ousid e_l	Lower eight bits of the frequency division coefficient in fixed frequency-division mode Note: When clock divider registers (addresses of 0x51 and 0x52) are read or written, you need to read or write to the upper four bits and then the lower eight bits continuously. The clock divider is calculated as follows: (f – 32700) x 30.52. f indicates the oscillation frequency of the external crystal and ranges from 32700 to 32799.

USER_REGISTER1

USER_REGISTER1 is 64-bit user register 1.

Offset Address	Register Name	Total Reset Value
0x53	USER_REGISTER1	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register1							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register1	64-bit user register 1 corresponding to bit[7:0]

USER_REGISTER2

USER_REGISTER2 is 64-bit user register 2.

Offset Address	Register Name	Total Reset Value
0x54	USER_REGISTER2	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register2	64-bit user register 2 corresponding to bit[15:8]

USER_REGISTER3

USER_REGISTER3 is 64-bit user register 3.

Offset Address	Register Name	Total Reset Value
0x55	USER_REGISTER3	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register3							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register3	64-bit user register 3 corresponding to bit[23:16]

USER_REGISTER4

USER_REGISTER4 is 64-bit user register 4.

Offset Address	Register Name	Total Reset Value
0x56	USER_REGISTER4	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register4							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register4	64-bit user register 4 corresponding to bit[31:24]

USER_REGISTER5

USER_REGISTER5 is 64-bit user register 5.

Offset Address	Register Name	Total Reset Value
0x57	USER_REGISTER5	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register5							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register5	64-bit user register 5 corresponding to bit[39:32]

USER_REGISTER6

USER_REGISTER6 is 64-bit user register 6.

Offset Address	Register Name	Total Reset Value
0x58	USER_REGISTER6	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register6							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register6	64-bit user register 6 corresponding to bit[47:40]

USER_REGISTER7

USER_REGISTER7 is 64-bit user register 7.

Offset Address	Register Name	Total Reset Value
0x59	USER_REGISTER7	0x0

Bit	7	6	5	4	3	2	1	0
Name	user_register7							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register7	64-bit user register 7 corresponding to bit[55:48]

USER_REGISTER8

USER_REGISTER8 is 64-bit user register 8.

Offset Address	Register Name	Total Reset Value
0x5A	USER_REGISTER8	0x0

Bit	7	6	5	4	3	2	1	0
Name	2							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	user_register8	64-bit user register 8 corresponding to bit[63:56]

3.10 Power Management and Low-Power Mode

3.10.1 Overview

- The power controller controls the power supply of the power-off area to turn on or off the chip.
- In low-power mode, the power consumption of the chip is reduced effectively. The Hi3516C V300 reduces its power consumption in the following low-power control modes:
  - Clock gating and clock frequency adjustment

    The clock disabling function is used to disable unnecessary clocks to reduce the power consumption of the chip. In addition, the frequency of the system working clock can be adjusted. That is, when the function requirement is met, you can adjust the clock frequency to reduce the power consumption of the chip.
  - Module low-power control

    When a module is idle, it can be disabled or switched to low-power mode to reduce the power consumption.
  - DDR low-power control

    The power consumption of the DDRC and related pins can be controlled dynamically. You can enable this function to reduce the power consumption of the chip. You can also enable the self-refresh function of the DDR to reduce the power consumption of the entire product.
  - Adaptive voltage scaling (AVS)

3.10.2 Power Management

Figure 3-10 shows the rough block diagram of the power network when the power controller module is used to control the power-on and power-off timings of the chip. The power controller module and RTC module are in the always-on area. Other chip power supplies controlled by PWR_SEQ 0–2 are in the power-off area. In power-off mode, all the chip areas

are powered off except the power control module and RTC module. In this case, the chip power consumption is the lowest, and the standby current is at the μA level. See Figure 3-10.

CAUTION

- The working clock of the power controller module is the 32768 Hz clock provided by the RTC. Therefore, the RTC must be in working mode when the power controller function is required (that is, the 32768 Hz RTC crystal must be connected, and the AVDD_BAT pin must be supplied with power).
- The reset time of the power controller cannot be less than 0.3 ms.

Figure 3-10 Block diagram of the power network when the power controller module is used

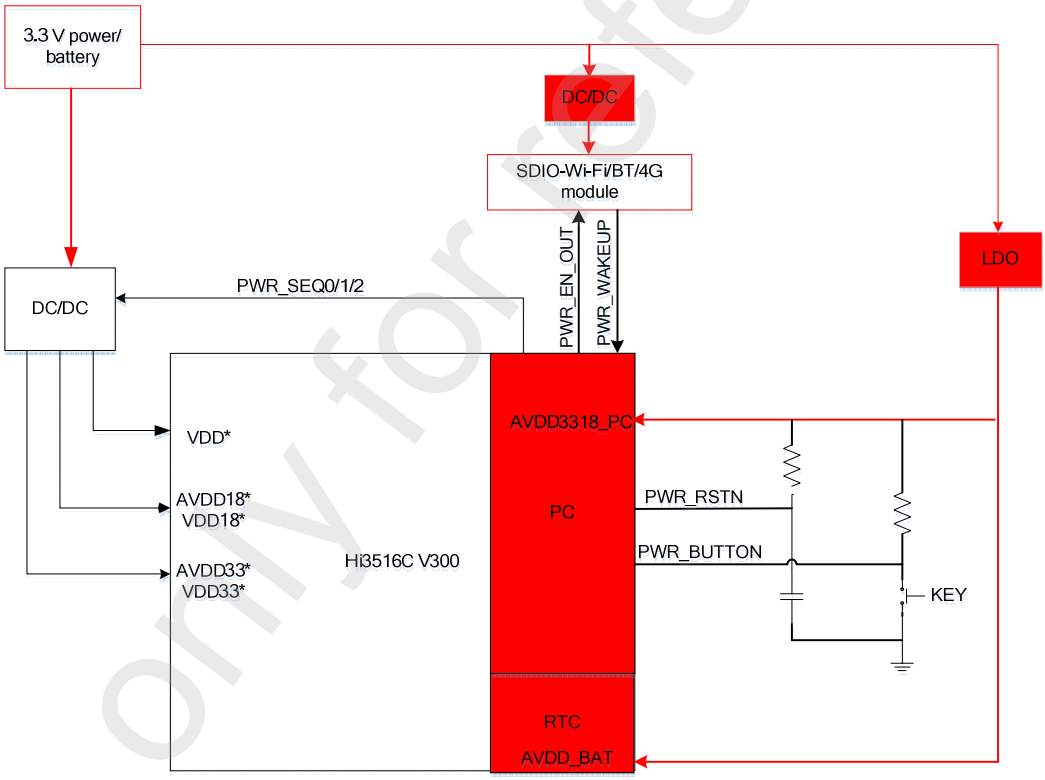
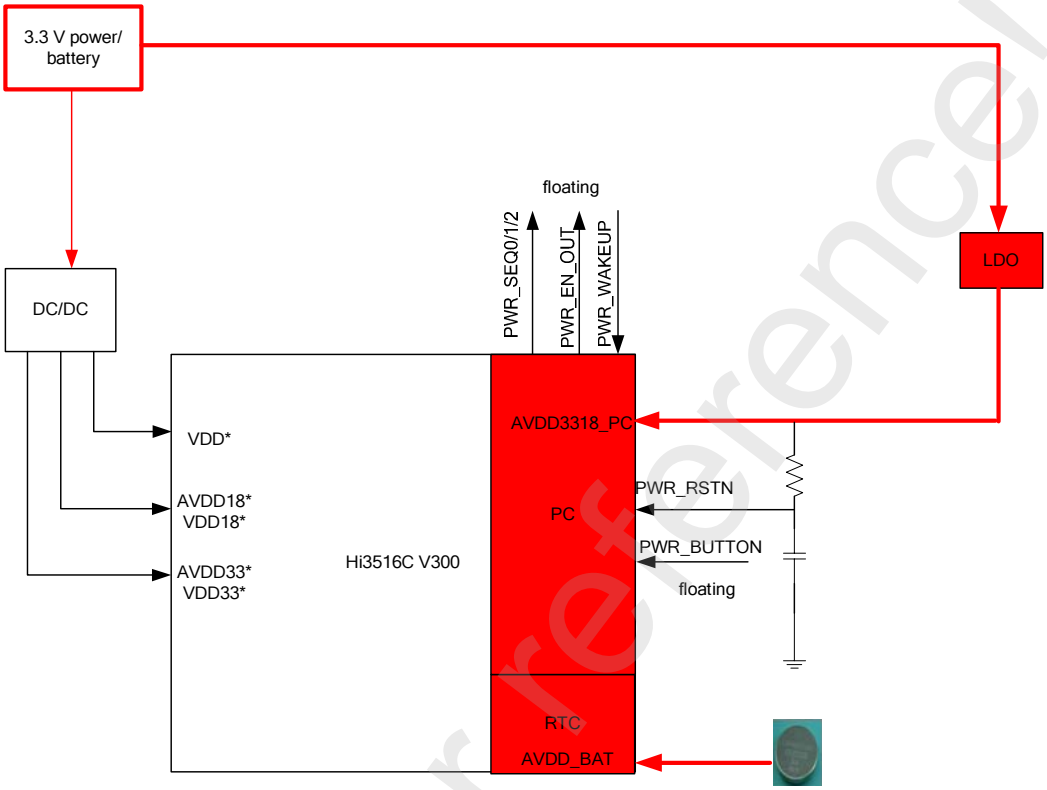


Figure 3-11 shows the processing of related pins when the power controller function is not used. PWR_RSTN must connect to the RC reset circuit for the power supply of AVDD3318_PC. The pins PWR_BUTTON, PWR_SEQ0/1/2, and PWR_EN_OUT are floated and not connected.

Figure 3-11 Processing of peripheral pins when the power controller function is not used



3.10.2.1 Features

The power controller has the following features:

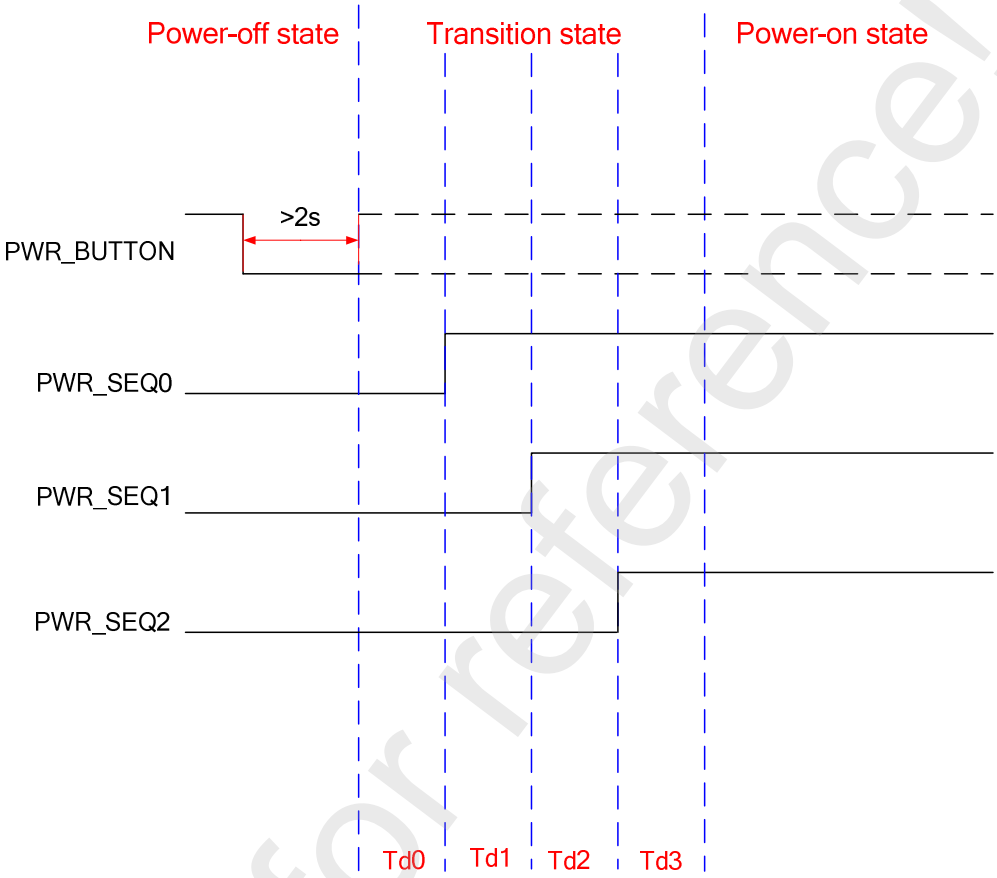
- Configurable polarity of the wakeup source
- Configurable time interval of the power-on and power-off timings
- Configurable power-off sequence
- RTC scheduled power-on
- Power-off timing triggering by pressing the PWR_BUTTON0 key for 10s when exceptions occur

3.10.2.2 Function Description

The logic functions normally only when the power controller module is in non-reset status (PWR_RSTN is high). The power control function is triggered by external wakeup pins (PWR_WAKEUP and PWR_BUTTON) or the RTC scheduled interrupt.

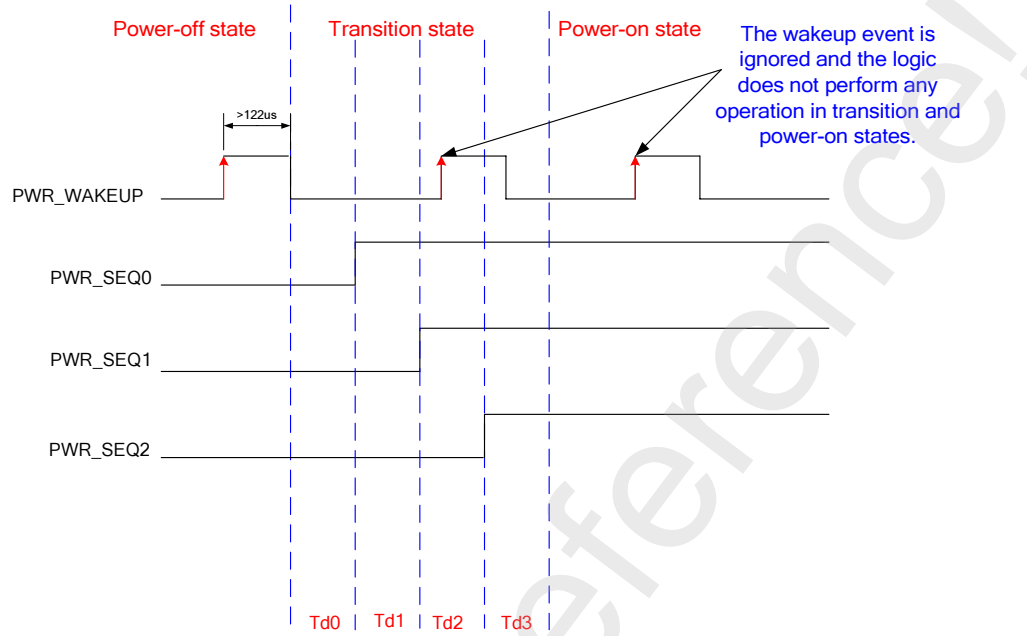
In power-off mode, the power-on timing can be triggered after PWR_BUTTON retains the low level for 2s. See Figure 3-12.

Figure 3-12 PWR_BUTTON power-on timing



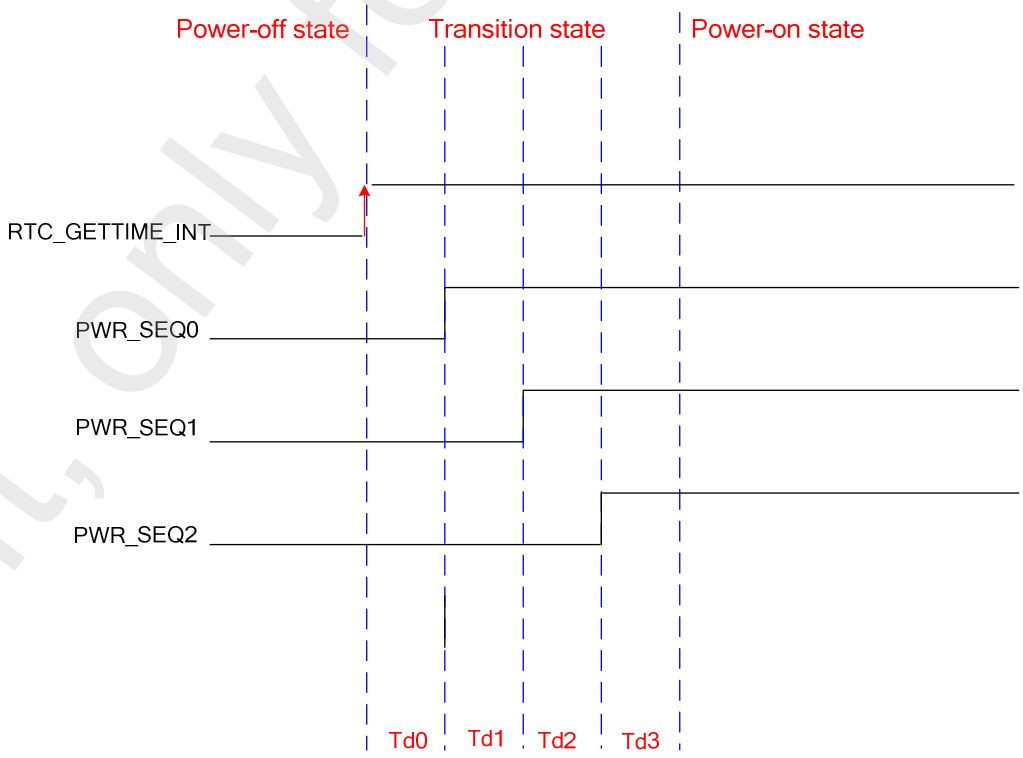
PWR_WAKEUP trigger the power-on timing on the rising edge by default. The power-on timing can be reconfigured to be triggered on the rising edge, falling edge, high level, or low level in power-on mode. See Figure 3-13. (Take rising-edge triggering as an example.)

Figure 3-13 Power-on timing of PWR_WAKEUP (rising-edge triggering)



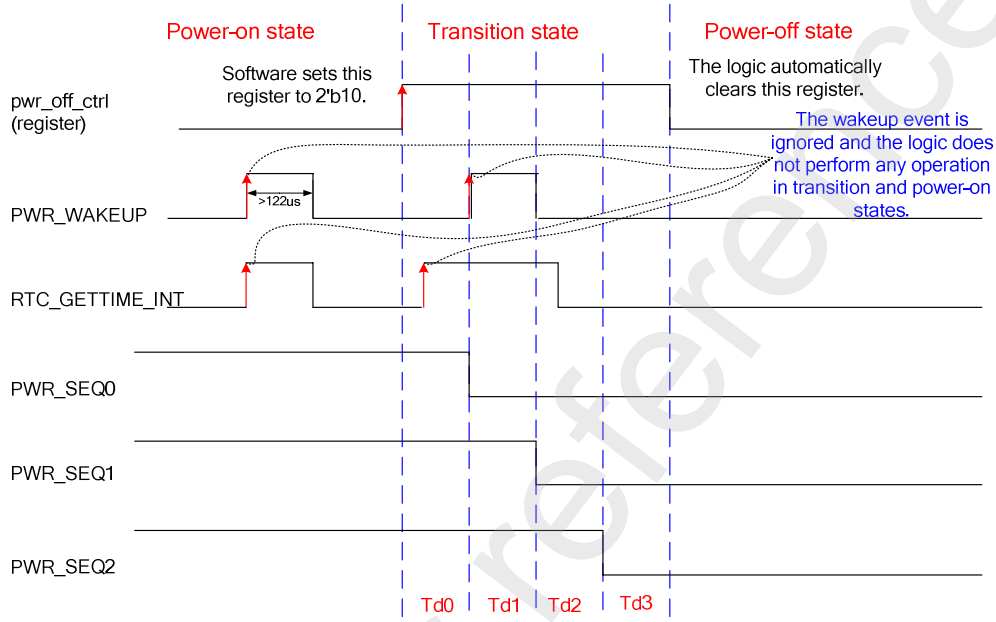
In power-off mode, the power-on timing is triggered when the RTC timing interrupt is generated and rtc_int_mask is 0. See Figure 3-14.

Figure 3-14 Power-on timing of the RTC timing interrupt



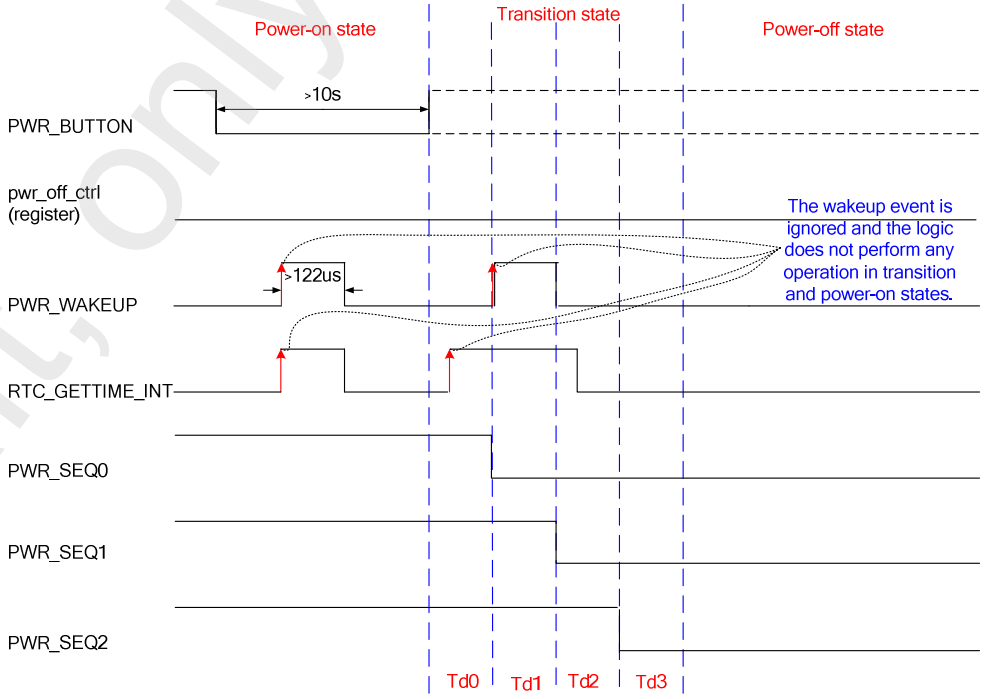
In power-on mode, the power-off timing can be triggered by setting pwr_off_ctrl to 2'b10. See Figure 3-15. (Take power-off sequence mode 0 as an example.)

Figure 3-15 Power-off timing when exceptions occur (power-off sequence mode 0)



If software exceptions occur in power-on mode, the power-off timing can be triggered after PWR_BUTTON0 retains the low level for more than 10s. See Figure 3-16. (Take power-off sequence mode 0 as an example.)

Figure 3-16 Power-off timing when exceptions occur (power-off sequence mode 0)

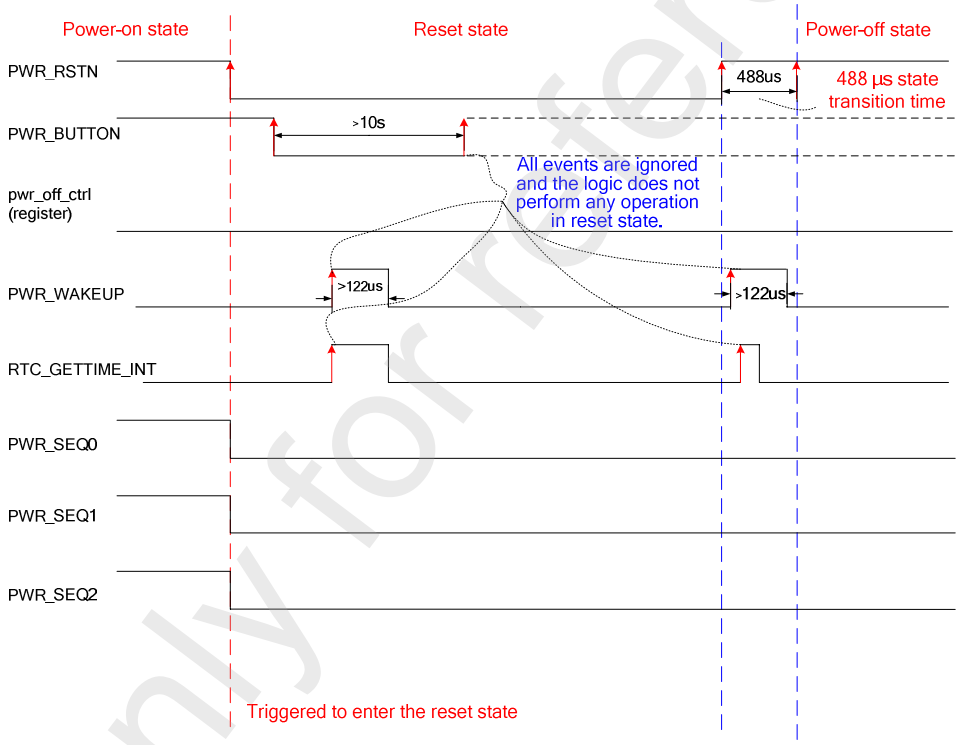


Td0 to Td3 are programmable values and correspond to registers pwr_td0 to pwr_td3 respectively. The value range is 1–255. The timing unit is ms, and the default reset value is 16.

The power controller module performs the dejitter operation on the input signals (PWR_WAKEUP and PWR_BUTTON). The levels with the width less than 122 µs will be filtered out.

The PWR_RSTN resets the entire power controller module. When the reset signal is pulled high, the logic requires 488 µs state jump time, and this time period is also the reset time. The power control module enters the reset state after reset takes effect. In reset state, all events are ignored and PWR_SEQ 0–2 output 0. See Figure 3-17.

Figure 3-17 Reset state diagram



The power supplies involved in the power-on and power-off timings are classified into groups based on the power-on/power-off sequence requirements in hardware design user guide. That is, the high-voltage power supplies are turned on before the low-voltage power supplies, and the low-voltage power supplies are turned off before the high-voltage power supplies (power-off sequence mode 0). Table 3-22 lists the power pin groups.

Table 3-22 Connection modes of the power pins

Power-on/Power-off Timing Group	Connection Mode 1	Connection Mode 2
Controlled by PWR_SEQ0	DVDD33	DVDD33
	DVDD3318_SENSOR[1]	-
	DVDD3318_VI[2]	-

Power-on/Power-off Timing Group	Connection Mode 1	Connection Mode 2
	DVDD3318_UART1[3]	-
	DVDD3318_RMII[4]	-
	DVDD3318_FLASH[5]	-
	DVDD3318_SARADC[6]	-
	AVDD_DDRPLL1	AVDD_DDRPLL1
	AVDD_DDRPLL2	AVDD_DDRPLL2
	AVDD33_AC	AVDD33_AC
	AVDD33_PLL	AVDD33_PLL
	AVDD33_USB	AVDD33_USB
	AVDD33_VDAC	AVDD33_VDAC
	AVDD3318_MIPI[7]	-
Controlled by PWR_SEQ1	-	DVDD3318_SENSO[8]
	-	DVDD3318_VI[9]
	-	DVDD3318_UART1[10]
	-	DVDD3318_RMII[11]
	-	DVDD3318_FLASH[12]
	-	DVDD3318_SARADC[13]
	-	AVDD3318_MIPI[14]
	VDDIO_CK_DDR	VDDIO_CK_DDR
	VDDIO_DDR	VDDIO_DDR
Controlled by PWR_SEQ2	VDD	VDD
	AVDD09_PLL	AVDD09_PLL

NOTE

- 1: DVDD3318_SENSO connects to the 3.3 V power.
- 2: DVDD3318_VI connects to the 3.3 V power.
- 3: DVDD3318_UART1 connects to the 3.3 V power.
- 4: DVDD3318_RMII connects to the 3.3 V power.
- 5: DVDD3318_FLASH connects to the 3.3 V power.
- 6: DVDD3318_SARADC connects to the 3.3 V power.
- 7: AVDD3318_MIPI connects to the 3.3 V power.
- 8: DVDD3318_SENSO connects to the 1.8 V power.
- 9: DVDD3318_VI connects to the 1.8 V power.

- 10: DVDD3318_UART1 connects to the 1.8 V power.
- 11: DVDD3318_RMII connects to the 1.8 V power.
- 12: DVDD3318_FLASH connects to the 1.8 V power.
- 13: DVDD3318_SARADC connects to the 1.8 V power.
- 14: AVDD3318_MIPI connects to the 1.8 V power.

3.10.2.3 Summary of Power Controller Registers

Table 3-23 lists power controller registers.

Table 3-23 Summary of power controller registers (base address: 0x1209_8000)

Offset Address	Register	Description	Page
0x000	PWR_CTRL0	PWR control register 0	3-176
0x004	PWR_CTRL1	PWR control register 1	3-178
0x008	PWR_STATUS	PWR status register	3-178
0x00C	PWR_PD_SEL	PWR power-off timing control register	3-179

3.10.2.4 Description of Power Controller Registers

PWR_CTRL0

PWR_CTRL0 is PWR control register 0.

CAUTION

When exceptions occur, this register will be reset after the PWR_BUTTON0 key is held down for 10s to trigger the power-off timing.

Offset Address	Register Name	Total Reset Value
0x000	PWR_CTRL0	0x0000_0060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								PWR_PAD_GPIO_EN	wakeup_mask	rtc_int_mask	wakeup_act_mode			pwr_pen	pwr_off_ctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7]	RW	PWR_PAD_GPIO_EN	If this bit is set to 0 when the core power supply is not turned on, the pins (PWR_BUTTON, PWR_WAKEUP, PWR_EN_OUT, PWR_SEQ0, PWR_SEQ1, and PWR_SEQ2) related to the power controller will be configured as the power control function. After the core power supply is turned on and becomes stable, if you need to configure these pins as the GPIO function, you need to set this bit to 1.
[6]	RW	wakeup_mask	Wakeup mask 0: not masked 1: masked
[5]	RW	rtc_int_mask	RTC interrupt wakeup mask 0: not masked 1: masked
[4:3]	RW	wakeup_act_mode	Wakeup valid mode select 00: active on the rising edge 01: active on the falling edge 10: active high 11: active low
[2]	RW	pwr_pen	PWR_EN_OUT output control 0: output 0 1: output 1
[1:0]	WO	pwr_off_ctrl	Power-off control 10: powered off Other values: reserved Note: When the logic completes the power-off operation, this bit is automatically cleared.

PWR_CTRL1

PWR_CTRL1 is PWR control register 1.

Offset Address	Register Name	Total Reset Value
0x004	PWR_CTRL1	0x1010_1010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pwr_td3								pwr_td2								pwr_td1								pwr_td0							
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	pwr_td3	Power timing parameter 3. The unit is ms, and the minimum value is 1.
[23:16]	RW	pwr_td2	Power timing parameter 2. The unit is ms, and the minimum value is 1.
[15:8]	RW	pwr_td1	Power timing parameter 1. The unit is ms, and the minimum value is 1.
[7:0]	RW	pwr_td0	Power timing parameter 0. The unit is ms, and the minimum value is 1.

PWR_STATUS

PWR_STATUS is a PWR status register.

Offset Address	Register Name	Total Reset Value
0x008	PWR_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								wakeup_in	button_in	wakeup_source				reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8]	RO	wakeup_in	Input of the PWR_WAKEUP pin
[7]	RO	button_in	Input of the PWR_BUTTON pin
[6:2]	RO	wakeup_source	Wakeup source bit6: RTC bit5: PWR_BUTTON

			bit4: reserved bit3: reserved bit2: PWR_WAKEUP
[1:0]	RO	reserved	Reserved

PWR_PD_SEL

PWR_PD_SEL is a PWR power-off timing control register.

Offset Address	Register Name	Total Reset Value
0x00C	PWR_PD_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														pd_seq_mode_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved
[2:0]	RW	pd_seq_mode_sel	Power-off timing select control 0: mode 1. The power-off timing is SEQ0->SEQ1->SEQ2. 1: mode 2. The power-off timing is SEQ1->SEQ0->SEQ2. 2: mode 3. The power-off timing is SEQ2->SEQ0->SEQ1. 3: mode 4. The power-off timing is SEQ2->SEQ1->SEQ0. 4: mode 5. The power-off timing is SEQ1->SEQ2->SEQ0. 5: mode 6. The power-off timing is SEQ0->SEQ2->SEQ1. Other values: mode 1. The power-off timing is SEQ0->SEQ1->SEQ2.

3.10.3 Clock Gating and Clock Frequency Adjustment

The system supports clock gating of each module. When a module is idle, its clock can be disabled to reduce chip power consumption. For details about the process, see the description in section "clock gating" of each module.

The working frequencies of some modules can also be adjusted separately. This reduces the power consumption of the system further. For details about the clock source of each module, see section 3.2.3 "Clock Distribution".

3.10.4 Module Low-Power Control

Most PHY modules including the USB 2.0 host/device and PLL modules support low-power operating modes. The clocks of a module can be disabled by configuring the corresponding CRG control registers. The unused PLLs can be disabled by configuring corresponding registers to reduce the power consumption. For details, see section 3.2 "Clock."

3.10.5 DDR Low-Power Control

For details about the low-power control mode of the DDRC, see the description of "Configuring the Low-Power Mode" in section 4.1.4 "Operating Mode."

3.10.6 Core AVS

The AVS technology further reduces power consumption by dynamically adjusting the voltage in real time based on the chip technology, temperature, and circuit timings. The system obtains the chip PVT information by using the high performance monitor (HPM) and implements automatic voltage scaling by using the PWM output signal in the PMC. For details, see section 3.10.7 "PMC."

3.10.7 PMC

3.10.7.1 Function Description

The PMC provides basic information about power consumption management of the chip and controls the power consumption.

- SVB PWM

  The PMC provides a programmable SVB PWM module. The peripheral PWM voltage scaling circuit can be used to adjust the power supply voltage of the chip through the PWM outputs of the chip.

- High performance monitor (HPM) control

  The HPM can be used to obtain the comprehensive PVT information about the chip. The reference power supply voltage scaling solution can be developed based on the PVT information.

- Internal temperature detection

  The chip has an integrated temperature sensor for obtaining the internal chip temperature and providing temperature information for temperature protection.

3.10.7.2 Operating Mode

SVB

The SVB PWM module in the PMC has a 24 MHz working clock, a 10-bit cycle counter, and a 10-bit duty cycle counter. The count cycle and duty cycle of the PWM output can be specified by configuring the PWM-related registers in the SVB.

To configure the count cycle and duty cycle of the SVB PWM output, perform the following steps:

Step 1 Calculate the number of PWM count cycles and the count value of the high level based on the required PWM output frequency and duty cycle.

The number of count cycles is calculated as follows:

svb_pwm_period = (24000000/Freq) – 1

The count value of the high level is calculated as follows:

svb_pwm_duty = (24000000/Freq) x duty – 1

Step 2 Set the number of PWM cycles by configuring MISC_CTRL30 bit[13:4] and the number of high-level cycles by configuring MISC_CTRL30 bit[25:16].

Step 3 Set MISC_CTRL30 bit[2] to 1 to load the configured parameters and enable the parameters to take effect.

Step 4 Set MISC_CTRL30 bit[0] to 1 to enable the PWM output.

----End

For example, the voltage of the core power supply is controlled by the SVB_PWM signal. Perform the following steps if the required SVB_PWM output frequency is 200 kHz and the duty cycle is 75%:

Step 1 Calculate the required number of count cycles and count value of the high level.

Pwm_period = (24000000/200000) − 1 = 119

Pwm_duty = (24000000/200000) x 0.75 – 1 = 89

Step 2 Set the number of SVB PWM cycles to 119 and the number of high-level cycles to 89.

Step 3 Set the SVB PWM load control.

Step 4 Enable the SVB PWM.

----End

HPM Control

Hi3516C V300 has two HPMs for obtaining the PVT information of the chip: core HPM and media HPM.

The reference clock source of the core HPM is the working clock of the CPU, and that of the media HPM is the working source clock of the VEDU. To make the HPM values more accurate, you are advised to set a appropriate frequency divider for the HPM reference clock so that the frequency of the HPM reference clock is about 50 MHz.

- The core HPM control registers are the peripheral control registers MISC_CTRL31–MISC_CTRL34.
- The media HPM control registers are the peripheral control registers MISC_CTRL35–MISC_CTRL38.

The following describes the HPM configuration procedure by taking the core HPM monitoring value as an example:

Step 1 Set the HPM capture mode (MISC_CTRL31[30]).

Step 2 If the cyclic capture mode is used, set the capture cycle by configuring MISC_CTRL31 bit[15:8]. If the single capture mode is used, skip this step.

The formula for calculating the cyclic capture cycle is as follows:

$$T = (N \times 2048) / 1000\ ms$$

N is the value of MISC_CTRL31 bit[15:8].

Step 3 Set the frequency divider of the HPM reference clock so that the frequency of the HPM reference clock is about 50 MHz.

The formula for calculating the frequency divider of the reference clock is as follows:

$$hpm\_div = (Freq_{clk\_source} / 50) - 1$$

For example, if the CPU frequency $Freq_{clk\_source}$ is 600 MHz, then:

core_hpm_div = (600 MHz/50 MHz) – 1 = 11

In this case, set MISC_CTRL31 bit[5:0] to 11.

Step 4 Deassert the HPM reset by configuring MISC_CTRL31 bit[31].

Step 5 Wait until the HPM output validity indicator (MISC_CTRL33 bit[29] is 1, and read the HPM monitoring value.

- In single capture mode, MISC_CTRL33 bit[9:0] record the HPM monitoring value.
- In cyclic capture mode, MISC_CTRL33 bit[9:0], MISC_CTRL33 bit[25:16], MISC_CTRL34 bit[9:0], and MISC_CTRL34 bit[25:16] record the latest four HPM monitoring values. MISC_CTRL33 bit[9:0] record the latest monitoring value.

----End

Internal Temperature Detection

The chip has an integrated T-Sensor and the detected temperature ranges from −40ºC (−40ºF) to +140ºC (284ºF). To enable the temperature sensor to collect data, perform the following steps:

The registers related to the T-sensor are peripheral control registers MISC_CTRL39–MISC_CTRL44.

Step 1 Set the T-Sensor capture mode by configuring MISC_CTRL39 bit[30].

Step 2 If the cyclic capture mode is used, set the capture cycle by configuring MISC_CTRL39 bit[27:20]. If the single capture mode is used, skip this step.

The formula for calculating the cyclic capture cycle is as follows:

$$T = (N \times 2)\ ms$$

N is the value of MISC_CTRL39 bit[27:20].

Step 3 Enable the T-Sensor by configuring MISC_CTRL39 bit[31] and start to collect the temperature.

Step 4 Read the temperature value captured by the T-sensor by reading MISC_CTRL39 bit[31].

In single capture mode, only temperature code 0 recorded in MISC_CTRL41 bit[9:0] is valid.

In cyclic capture mode, the latest eight temperature codes (codes 0−7) are recorded in MISC_CTRL41 bit[31:0] and MISC_CTRL44 bit[31:0]. The latest recorded temperature data is temperature code 0.

Step 5 Calculate the corresponding temperature value based on the recorded temperature code.

The temperature value T (in ℃) is calculated as follows: T = (((tsensor_result –125)/806) x165) – 40(℃).

Note that tsensor_result is the temperature record code obtained in step 4.

----End

Contents

Figures

Tables

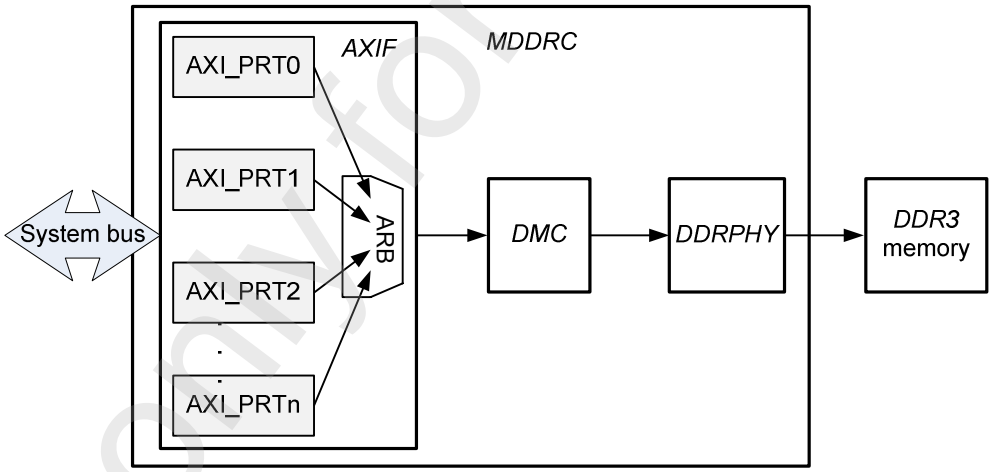
4 Memory Interfaces

4.1 DDRC

4.1.1 Overview

The DDR SDRAM controller (DDRC) controls access to the DDR3 SDRAM. Figure 4-1 shows the DDRC structure.

Figure 4-1 DDRC structure



4.1.2 Features

The DDRC has the following features:

- One DDR3 SDRAM chip select (CS)
- 16-bit DDR3 SDRAM data bus
- Maximum 4 Gbits storage space
- 533 MHz DDR3 SDRAM interface clock frequency and 1.066 Gbit/s data rate
- Various DDR3 SDRAM low-power modes, such as the power-down and self-refresh modes

- Burst8 transfer mode for the DDR3 SDRAM

4.1.3 Function Description

4.1.3.1 Application Block Diagram

By using the DDRC, the master devices of the system-on-chip (SoC) such as the CPU can access the external DDR3 SDRAM. It supports the DDR3 SDRAM complying with the JEDEC (JESD79) standard after the timing parameter registers of the DDRC are configured by using the CPU.

Table 4-1 lists the DDR3 SDRAMs supported by the DDRC from several mainstream DRAM vendors. The descriptions in Table 4-1 are based on the working frequencies of DDR3 SDRAMs. The restrictions such as the capacity are not taken into consideration.

Table 4-1 DDR3 SDRAMs supported by the DDRC

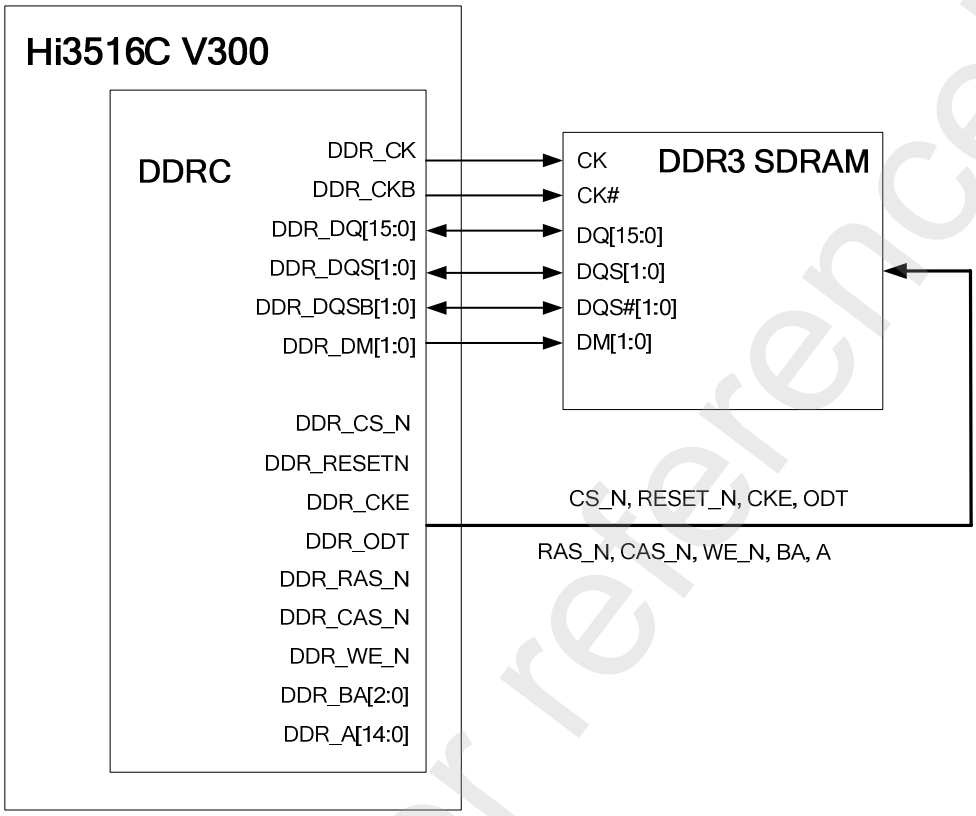
Vendor	400 MHz	533 MHz	667 MHz
JESD79 (DDR3 standard)	DDR3-800 DDR3-1066 DDR3-1333 DDR3-1600	DDR3-1066 DDR3-1333 DDR3-1600	DDR3-1333 DDR3-1600

NOTE

For details about the supported component types, see the JEDEC standard and the component data sheet.

Figure 4-2 shows the connection between the DDRC and a 16-bit DDR3 SDRAM.

Figure 4-2 Connecting the DDRC to a 16-bit DDR3 SDRAM

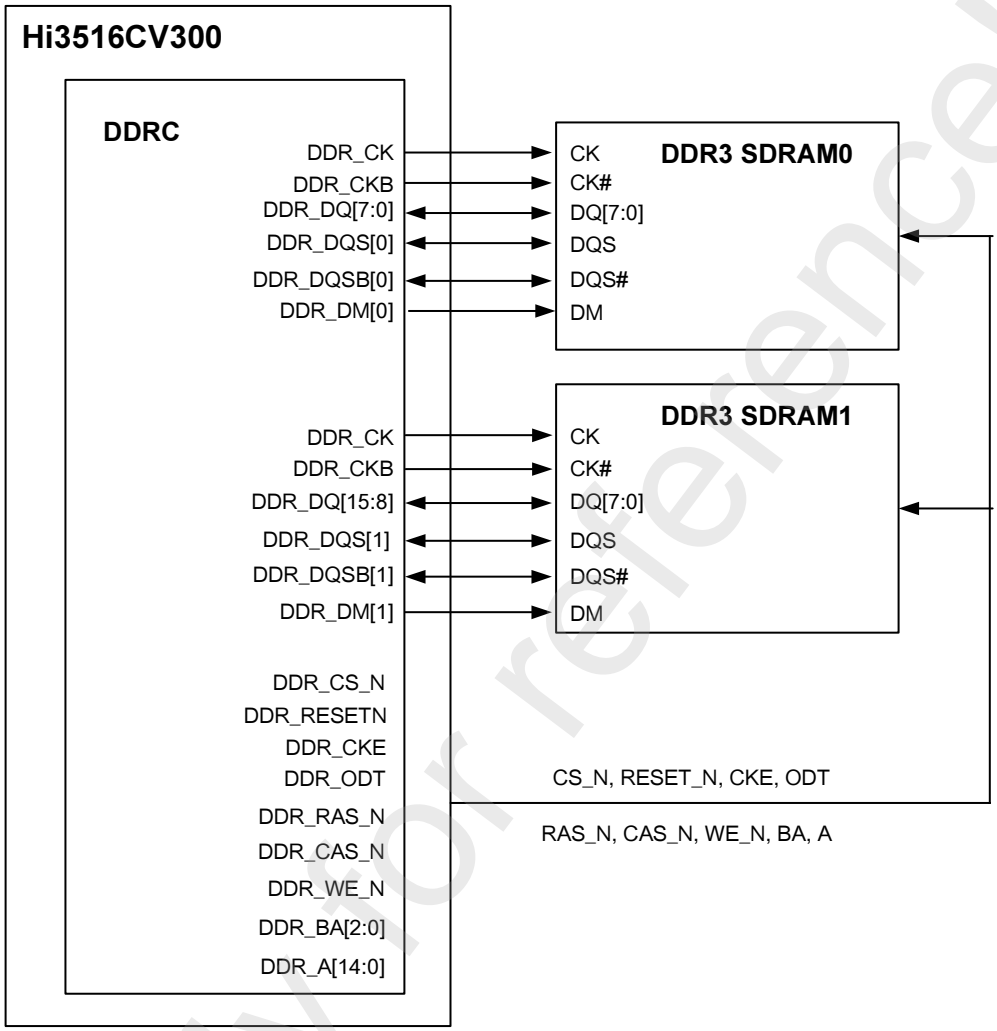


NOTE

- The DDR3 SDRAM is a 16-bit memory.
- The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_ODT, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA [2:0], and DDR_A [14:0]) connect to the command control signals of the DDR3 SDRAM respectively. The DDRC command control bus uses the one-drive-one mode.

Figure 4-3 shows the connection between the DDRC and two 8-bit DDR3 SDRAMs.

Figure 4-3 Connecting the DDRC to two 8-bit DDR3 SDRAMs



NOTE

- The DDR3 SDRAM*x* is an 8-bit memory.
- The DDRC command control signals (DDR_CS_N, DDR_CKE, DDR_ODT, DDR_RESET_N, DDR_RAS_N, DDR_CAS_N, DDR_WE_N, DDR_BA[2:0], and DDR_A[14:0]) connect to the command control signals of the DDR3 SDRAMx respectively. The DDRC command control bus uses the one-drive-two mode.

4.1.3.2 Function Implementation

As the timings of the DDRC interface comply with the JESD79 standard, the DDRC can access (read or write) data in the DDR3 SDRAM and control the status of the DDR3 SDRAM (including automatic refresh and low power control) by sending the command words of the DDR3 SDRAM.

Command Truth Value Table

The DDRC can read and write to the DDR3 SDRAM and control command words. Table 4-2 lists the command truth values of the DDRC. For details, see the JEDEC standard and component data sheet.

Table 4-2 Command truth values of the DDRC

Function	DDR3_CKE	DDR3_CSN	DDR3_RASN	DDR3_CASN	DDR3_WEN	DDR3_ADR			DDR3_BA
						15:11	AP(10)	9:0	
DESELECT	H	H	X	X	X	X	X	X	X
ACTIVE	H	L	L	H	H	V	V	V	V
READ	H	L	H	L	H	V	V	V	V
WRITE	H	L	H	L	L	V	V	V	V
PRECHARGE	H	L	L	H	L	V	L	V	BA
PRECHARGE ALL	H	L	L	H	L	V	H	V	V
AUTO REFRESH	H	L	L	L	H	V	V	V	V
SELF REFRESH ENTRY	H->L	L	L	L	H	V	V	V	V
SELF REFRESH EXIT	L->H	L	H	H	H	V	V	V	V
MODE REGISTER SET	H	L	L	L	L	V	V	V	V
ZQCL	H	L	H	H	L	X	H	X	X
ZQCS	H	L	H	H	L	X	L	X	X

NOTE

- H indicates high level; L indicates low level; V indicates valid; X indicates ignored.
- **ZQ Calibration Long** (ZQCL): It is used to start ZQ calibration on the DDR3 SDRAM when the DDR3 SDRAM is initialized during power-on.
- **ZQ Calibration Short** (ZQCS): It is used to start ZQ calibration on the DDR3 SDRAM when the ambient environment is changed.

Auto Refresh

When DDRC_CFG_TIMING2[taref] is set to a non-zero value, the DDRC refreshes the DDR3 SDRAM by automatically generating a periodical auto refresh command. At ambient temperature, the DDR3 SDRAM is required to implement 8,192 auto-refresh operations within 64 ms. That is, the auto-refresh cycle is 7.8 µs. The relationship between the value of DDRC_CFG_TIMING2[taref] (taref) and the auto-refresh cycle T (T = 7.8 µs) is as follows:

$T \geq taref \times (16 \times DDR\ clock\ cycle)$

When DDRC_CFG_TIMING2[taref] is configured, the internal counter of the DDRC automatically loads the taref value and then counts in decremented mode. When the count value reaches 0, the DDRC initiates an auto-refresh operation and the counter reloads the taref value to count.

Low-Power Management

The DDRC supports two modes of low-power management: common low-power mode and auto-refresh low-power mode.

When DDRC_CFG_PD[pd_en] is set to 1 to enable the SDRAM low-power mode, and the system is idle (the DDR is not read or written through the DDRC bus interface for a period), the DDR3 SDRAM enters the common low-power mode automatically.

To switch the system mode to standby mode, you can force the DDR3 SDRAM to enter the auto-refresh mode by setting DDRC_CTRL_SREF[sref_req] to 1. In this mode, the power consumption of the DDR3 SDRAM is minimized, data in the DDR3 SDRAM is retained, but the system cannot access the DDR3 SDRAM.

Arbitration Mechanism

The DDRC uses the priority scheduling algorithm and flow control algorithm.

The priority mapping mode can be selected by configuring AXI_QOSCFG0n[pri_map_mode]. If AXI_QOSCFG0n[pri_map_mode] is set to 1, the system bus signal is used as the QoS priority. If AXI_QOSCFG0n[pri_map_mode] is set to 0, AXI_QOSCFG0n[id_map] needs to be configured to select some bits of the ID for QoS configuration. The DDRC adds priority attributes to the read/write commands sent to the bus by configuring AXI_WRPRI and AXI_RDPRI, and then schedules the commands based on the priority attributes to implement highly effective access to the DDR3 SDRAM.

The DDRC adds response timeout attributes to commands sent to the bus by setting AXI_WRTOUT and AXI_RDTOUT to non-zero values. The mapping mode of the timeout value can be selected by configuring AXI_QOSCFG0n[tout_map_mode]. If AXI_QOSCFG0n[tout_map_mode] is set to 1, the 2 bit select signals of the system bus are used the address to search for one of the four preset timeout values. If AXI_QOSCFG0n[tout_map_mode] is set to 0, AXI_QOSCFG0n[tout_id_map] needs to be configured to select 2 bit signals of the ID as the address to search for one of the four preset timeout values. Then the bus command response timeout is ensured based on the response timeout priority scheduling algorithm.

The DDRC adds the flow control attributes to bus interfaces by configuring DDRC_CFG_PERF[flux_en] and AXI_FLUX0n[flux_cfg0]. The DDRC allocates traffic to each bus interface to ensure sufficient bandwidth of each interface when the traffic is heavy. The commands with the response timeout attributes are not controlled after the timeout period elapse.

Traffic Statistics and Command Latency Statistics

The DDRC supports traffic statistics. The interface read and write traffic statistics can be collected to determine whether dynamic frequency scaling (DFS) is required, that is, whether to increase or reduce the DDRC frequency. The DDRC can collect the read and write traffic statistics of a specific ID, or the overall read and write traffic statistics. The DDRC can also collect DDR interface usage statistics. The statistic counter supports the continuous counts and one-time count. When counting continuously, the counter is a non-saturating counter, and it is wrapped when the maximum count is reached to facilitate the continuous count.

Therefore, the system needs to read the count value before the counter is wrapped. When counting for only one time, the counter stops counting when the statistic time elapses. The system can obtain the instantaneous traffic and latency by using this function.

The DDRC can collect command latency statistics, including the maximum latency of the read and write access to a specific ID and the accumulative latency statistics.

The process for collecting statistics is as follows:

Step 1 Set the statistic mode to continuous triggering or one-time triggering by configuring DDRC_CFG_PERF.perf_mode. If the one-time triggering is selected, set the perf_prd field to configure the statistic cycle.

Step 2 Set the ID for which statistics are to be collected by configuring DDRC_CFG_STAID.

Step 3 Set the mask value of the ID by configuring DDRC_CFG_STAIDMSK. The DDRC determines whether to collect statistics of the current access based on sta_idmask and the accessed ID. Statistics of multiple IDs can be collected by using this method.

Step 4 Enable the statistic function by configuring DDRC_CTRL_PERF[perf_en]. For the one-time count, counting is complete when DDRC_CTRL_PERF[perf_en] restores to 0. For the continuous count, the software needs to write 0 to DDRC_CTRL_PERF[perf_en] to stop counting.

Step 5 Observe the collected statistics by using DDRC_HIS_FLUX_WR, DDRC_HIS_FLUX_RD, DDRC_HIS_FLUX_WCMD, DDRC_HIS_FLUX_RCMD, DDRC_HIS_FLUXID_WR, DDRC_HIS_FLUXID_RD, DDRC_HIS_FLUXID_WCMD, DDRC_HIS_FLUXID_RCMD, DDRC_HIS_WLATCNT0, DDRC_HIS_WLATCNT1, DDRC_HIS_RLATCNT0, DDRC_HIS_RLATCNT1, and DDRC_HIS_INHERE_RLAT_CNT.

----End

Address Mapping

The DDRC can convert the access address for the system bus into that for the DDR3 SDRAM. You can set the address mapping mode to row-bank-column (RBC) by configuring DDRC_CFG_RNKVOL[mem_map]. Currently only the RBC mode is supported. Then you can set the SDRAM row and column address bit width by configuring DDRC_CFG_RNKVOL[mem_row] and DDRC_CFG_RNKVOL[mem_col]. The DDRC then converts the system bus address into the DDR3 SDRAM address based on the address mapping algorithm.

The following describes the mapping algorithms for the system bus address and the address for the DDR3 SDRAM by using the RBC mode as an example. Assume that the system bus address is BUSADR[31:0], the valid address is BUSADR[m – 1:0], and the address for the DDR3 SDRAM is DDRADR[13:0]. When DDRADR[13:0] serves as the row address, its valid address is DDRROW[x – 1:0]; when DDRADR[13:0] serves as the column address, its valid address is DDRCOL[y – 1:0]. In addition, the bank address for the DDR is DDRBA[z – 1:0] and the width of the storage data bus of the DDRC is DW. In this case, the address mappings are as follows:

- When DDRC_CFG_RNKVOL[mem_map] is set to 2'b00, the RBC mapping mode is as follows:

  BUSADR[m − 1:0] = {DDRROW[x − 1:0], DDRBA[z − 1:0], DDRCOL[y − 1:0], DW{b0}}

In the preceding expressions, the following condition is met: m = x + y + z + DW. When the data bit width of the DDR SDRAM connected to the DDRC is 16 bits, DW is 1.

- When DDRC_CFG_RNKVOL[mem_map] is set to 2'b00 and A10 acts as the AP function bit of the DDR, the mapping between the system bus addresses and the DDR3 SDRAM addresses is shown in Table 4-3.

Table 4-3 describes the address mapping in RBC mode.

Table 4-3 DDRC address mapping in 16-bit mode

Memory Type	Row Address Width	Column Address Width	DDR BA			Row/Column Address	DDR ADR								
Mbit x bw			2	1	0		15	14	13	12	11	10/ AP	9	8	7:0
1 Gbit 8bank															
64 x 16	13	10	13	12	11	Row address	-	-	-	26	25	24	23	22	21:14
						Column address	-	-	-	-	-	AP	10	9	8:1
2 Gbit 8bank															
128 x 16	14	10	13	12	11	Row address	-	-	27	26	25	24	23	22	21:14
						Column address	-	-	-	-	-	AP	10	9	8:1
4 Gbit 8bank															
256 x 16	15	10	13	12	11	Row address	-	28	27	26	25	24	23	22	21:14
						Column address	-	-	-	-	-	AP	10	9	8:1

4.1.4 Operating Mode

4.1.4.1 Soft Reset

The DDRC does not support separate soft reset. It can be reset only by a global soft reset. After reset, the DDR3 DRAM must be reinitialized according to the following initialization processes.

4.1.4.2 Initializing the DDR3 SDRAM

After power-on, the system can access the DDR3 SDRAM only when the DDR3 SDRAM is initialized. Before initializing the DDR3 SDRAM, note the following:

- Power on the DDR3 SDRAM by complying with the JEDEC standard. That is, provide VDD, VDDQ, and then VREF and VTT in sequence.
- Initialize the DDR3 SDRAM only after the system enters normal mode.

The following describes the procedure for initializing the DDRC when the ratio of the working frequency of the DDRC to that of the DDR3 SDRAM is 1:2.

Step 1 Set DDRC_CFG_SREF to 0x8100 to back-press the DDRC commands when the DDR enters the auto-refresh mode.

Step 2 Set DDRC_CFG_AREF to 0x0 to disable auto-refresh during initialization.

Step 3 Set DDRC_CFG_PD to disable the power-down function during initialization.

Step 4 Set DDRC_CFG_WORKMODE to 0x11002011.

Step 5 Set DDRC_CFG_DDRMODE to 0x16 to set the DDR bit width to 16 bits, DDR type to DDR3, and DDRC burst length to BL4.

Step 6 Set DDRC_CFG_RNKVOL to 0x142.

NOTE

The row and column bit widths vary according to DDR SDRAMs. Change the value of DDRC_CFG_RNKVOL based on the used DDR SDRAM.

Step 7 Configure the DDRC working timing parameter registers, including DDRC_CFG_TIMING0−DDRC_CFG_TIMING5.

Step 8 Set DDRC_CFG_ODT to 0x1 to enable ODT on write or disable ODT on read.

Step 9 Set the working mode, time parameters, IO drive, and ODT resistance of the DDR PHY that is connected to DMC0 as well as the delay parameters of read/write command channels. The involved registers include PHYTIMER0, PHYTIMER1, PLLTIMER, DLYMEASCTRL, DRAMCFG, ACPHYCTL4, DRAMTIMER0, DRAMTIMER1, DRAMTIMER2, DRAMTIMER3, DRAM TIMER4, DRAMTIMER5, IOCTL(Static_reg), MISC, MODEREG01, MODEREG23, MODEREG45, MODEREG67, PHYCTRL0, and ACPHYBOUND.

Step 10 Configure the registers RNK2RNK, DMSEL, and DQSSEL(Static_reg) of DDR PHY0, and select the ADDR/CMD signal swapping mode and DQ/DQS signal swapping mode.

Step 11 Configure the register PHYINITCTRL of the DDR PHY that is connected to DMC0, and start DDR PHY0 for initialization.

Step 12 Software queries PHYINITCTRL[init_en] until its value is 0, indicating that the initialization is complete.

Step 13 Set DDRC_CFG_TIMING2 to enable auto-refresh.

Step 14 Set DDRC_CTRL_SREF to 0x2 to enable the DDRC to exit the self-refresh mode.

Step 15 Software queries DDRC_CURR_FUNC[in_sref] until its value is 0, indicating that the DDRC exits self-refresh.

Step 16 Set DDRC_CTRL_SREF[sref_done] to 1.

----End

After the preceding steps are complete, the DDR3 SDRAM works properly.

4.1.4.3 Low-Power Configuration

The DDRC supports two types of low-power modes for the DDR3 SDRAM: DDR3 SDRAM power-down mode and DDR3 SDRAM self-refresh mode.

When DDRC_CFG_PD[pd_en] and DDRC_CFG_PD[pd_prd] are set to valid values, the DDRC automatically forces the DDR3 SDRAM to enter the low-power mode if the system is idle. When DDRC_CFG_PD[pd_en] is set to 1 and the DDRC does not access

the DDR3 SDRAM within DDRC_CFG_PD[pd_prd] bus clock cycles, the DDRC forces the DDR3 SDRAM to enter the low-power mode.

When DDRC_CTRL_SREF[sr_req] is set to 1, the DDRC forces the DDR3 SDRAM to enter the self-refresh mode without responding to the bus requests after completing the current access operation.

4.1.5 AXI Registers of the DDRC

4.1.5.1 Register Summary

Table 4-4 describes AXI registers.

NOTE

The variable **ports** in the offset addresses indicates the number of AXI ports and ranges from 0 to 6.

Table 4-4 Summary of EMI registers (base address: 0x1206_0000)

Offset Address	Register	Description	Page
0x000	AXI_CONFIG	DDRC function configuration register	4-11
0x004	AXI_CKGCFG	DDRC clock gating configuration register	4-13
0x01C	AXI_STATUS	DDRC interface status register	4-14
0x020	AXI_CHCFG0	MDDRC channel configuration register 0	4-15
0x024	AXI_CHCFG1	MDDRC channel configuration register 1	4-16
0x028	AXI_CHCFG2	MDDRC channel configuration register 2	4-18
0x02C	AXI_CHCFG3	MDDRC channel configuration register 3	4-20
0x030	AXI_CHCFG4	MDDRC channel configuration register 4	4-22
0x034	AXI_CHCFG5	MDDRC channel configuration register 5	4-23
0x038	AXI_LPCFG	MDDRC low-power zone configuration register	4-24
0x040 + 0x4 x *ports*	AXI_QOSCFG0	DDRC QoS configuration register 0	4-25
0x080 + 0x4 x *ports*	AXI_QOSCFG1	DDRC QoS configuration register 1	4-26
0x0C0 + 0x4 x *ports*	AXI_WRPRI	DDRC write command priority configuration register	4-27
0x100 + 0x4 x *ports*	AXI_RDPRI	DDRC read command priority configuration register	4-28
0x140 + 0x4 x *ports*	AXI_WRTOUT	DDRC write command timeout configuration register	4-30
0x180 + 0x4 x *ports*	AXI_RDTOUT	DDRC read command timeout configuration register	4-30

Offset Address	Register	Description	Page
0x200 + 0x4 x *ports*	AXI_OSTDCFG0	DDRC port command outstanding configuration register 0	4-31
0x240	AXI_OSTDCFG1	DDRC port command outstanding configuration register 1	4-32
0x244	AXI_OSTDCFG2	DDRC port command outstanding configuration register 2	4-32
0x248	AXI_OSTDSTATUS	DDRC channel command outstanding status register	4-35
0x280 + 0x4 x *ports*	AXI_FLUX0	DDRC port bandwidth traffic control configuration register for channel 0	4-35

4.1.5.2 Register Description

AXI_CONFIG

AXI_CONFIG is a DDRC function configuration register.

Offset Address	Register Name	Total Reset Value
0x000	AXI_CONFIG	0x0006_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													wr_rcv_mode	exclusive_en	rd_wrap_split_en	reserved												bank_width			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	wr_rcv_mode	Mode of receiving the write command over the DDRC AXI port 0: The write command is received directly. 1: The write command is received only after the expected written data arrives.
[17]	RW	exclusive_en	Exclusive command enable 0: disabled 1: enabled
[16]	RW	rd_wrap_split_en	WRAP read command split enable 0: not split 1: split
[15:4]	RO	reserved	Reserved
[3:0]	RW	bank_width	Bank bit width 1000: 256 bits 1001: 512 bits 1010: 1 KB 1011: 2 KB 1100: 4 KB 1101: 8 KB 1110: 16 KB 1111: 32 KB Other values: reserved For example, if the column is 10 for a 32-bit DDR, the bank width is calculated as follows: bank_width = (32/8) x (2^10) = 4 KB

AXI_CKGCFG

AXI_CKGCFG is a DDRC clock gating configuration register.

Offset Address	Register Name	Total Reset Value
0x004	AXI_CKGCFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			sta_ckg_pub0	reserved			sta_ckg_dmc0	reserved			sta_ckg_apb	reserved			dyn_ckg_rdr	reserved							dyn_ckg_axi6	dyn_ckg_axi5	dyn_ckg_axi4	dyn_ckg_axi3	dyn_ckg_axi2	dyn_ckg_axi1	dyn_ckg_axi0
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RW	reserved	Reserved
[28]	RW	sta_ckg_pub0	Static clock gating for PUB0 0: disabled 1: enabled
[27:25]	RW	reserved	Reserved
[24]	RW	sta_ckg_dmc0	Dynamic clock gating for DMC0 0: disabled 1: enabled
[23:21]	RO	reserved	Reserved
[20]	RW	sta_ckg_apb	Static clock gating for the register configuration module 0: disabled 1: enabled
[19:17]	RO	reserved	Reserved
[16]	RW	dyn_ckg_rdr	Dynamic clock gating for the REORDER module 0: The clock is always enabled. 1: Clock gating is automatic when the module is idle.
[15:7]	RW	reserved	Reserved
[6]	RW	dyn_ckg_axi6	Dynamic clock gating for AXI port 6 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[5]	RW	dyn_ckg_axi5	Dynamic clock gating for AXI port 5 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.

[4]	RW	dyn_ckg_axi4	Dynamic clock gating for AXI port 4 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[3]	RW	dyn_ckg_axi3	Dynamic clock gating for AXI port 3 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[2]	RW	dyn_ckg_axi2	Dynamic clock gating for AXI port 2 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[1]	RW	dyn_ckg_axi1	Dynamic clock gating for AXI port 1 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.
[0]	RW	dyn_ckg_axi0	Dynamic clock gating for AXI port 0 0: The clock is always enabled. 1: Clock gating is automatic when the AXI module is idle.

AXI_STATUS

AXI_STATUS is a DDRC interface status register.

Offset Address	Register Name	Total Reset Value
0x01C	AXI_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									axist6	axist5	axist4	axist3	axist2	axist1	axist0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	axist6	Status of controller bus interface 6 0: The interface is idle. 1: A command is being executed.
[5]	RO	axist5	Status of controller bus interface 5 0: The interface is idle. 1: A command is being executed.
[4]	RO	axist4	Status of controller bus interface 4 0: The interface is idle. 1: A command is being executed.

[3]	RO	axist3	Status of controller bus interface 3 0: The interface is idle. 1: A command is being executed.
[2]	RO	axist2	Status of controller bus interface 2 0: The interface is idle. 1: A command is being executed.
[1]	RO	axist1	Status of controller bus interface 1 0: The interface is idle. 1: A command is being executed.
[0]	RO	axist0	Status of controller bus interface 0 0: The interface is idle. 1: A command is being executed.

AXI_CHCFG0

AXI_CHCCFG0 is MDDRC channel configuration register 0.

Offset Address	Register Name	Total Reset Value
0x020	AXI_CHCFG0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							ch_addr_msk_idx
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	RW	reserved	Reserved

[2:0]	RW	ch_addr_msk_idx	Sequence number of mask for the address space index Four consecutive bits in the address are obtained for searching the channel configuration table. 000: addr[ADDR_WIDTH − 1: ADDR_WIDTH − 4] 001: addr[ADDR_WIDTH − 2: ADDR_WIDTH − 5] 010: addr[ADDR_WIDTH − 3: ADDR_WIDTH − 6] 011: addr[ADDR_WIDTH − 4: ADDR_WIDTH − 7] 100: addr[ADDR_WIDTH − 5: ADDR_WIDTH − 8] 101: addr[ADDR_WIDTH − 6: ADDR_WIDTH − 9] 110: addr[ADDR_WIDTH − 7: ADDR_WIDTH − 10] 111: addr[ADDR_WIDTH − 8: ADDR_WIDTH − 11] ADDR_WIDTH: bit width of the system address (32 bits to 40 bits) Prevent upper-bit addresses from being wrapped. For example, when the address bit width is 32 bits, if it is set to 3, addr[31:29] must be fixed.

AXI_CHCFG1

AXI_CHCCFG1 is MDDRC channel configuration register 1.

Offset Address	Register Name	Total Reset Value
0x024	AXI_CHCFG1	0x0000_0000

Bit	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Name	ch_start15	ch_start14	ch_start13	ch_start12	ch_start11	ch_start10	ch_start9	ch_start8	ch_start7	ch_start6	ch_start5	ch_start4	ch_start3	ch_start2	ch_start1	ch_start0
Reset	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0

Bits	Access	Name	Description
[31:30]	RW	ch_start15	Channel configuration table, start channel of address space 15 0−3 correspond to channels 0−3.
[29:28]	RW	ch_start14	Channel configuration table, start channel of address space 14 0−3 correspond to channels 0−3.
[27:26]	RW	ch_start13	Channel configuration table, start channel of address space 13 0−3 correspond to channels 0−3.
[25:24]	RW	ch_start12	Channel configuration table, start channel of address space 12 0−3 correspond to channels 0−3.
[23:22]	RW	ch_start11	Channel configuration table, start channel of address space 11 0−3 correspond to channels 0−3.

[21:20]	RW	ch_start10	Channel configuration table, start channel of address space 10 0−3 correspond to channels 0−3.
[19:18]	RW	ch_start9	Channel configuration table, start channel of address space 9 0−3 correspond to channels 0−3.
[17:16]	RW	ch_start8	Channel configuration table, start channel of address space 8 0−3 correspond to channels 0−3.
[15:14]	RW	ch_start7	Channel configuration table, start channel of address space 7 0−3 correspond to channels 0−3.
[13:12]	RW	ch_start6	Channel configuration table, start channel of address space 6 0−3 correspond to channels 0−3.
[11:10]	RW	ch_start5	Channel configuration table, start channel of address space 5 0−3 correspond to channels 0−3.
[9:8]	RW	ch_start4	Channel configuration table, start channel of address space 4 0−3 correspond to channels 0−3.
[7:6]	RW	ch_start3	Channel configuration table, start channel of address space 3 0−3 correspond to channels 0−3.
[5:4]	RW	ch_start2	Channel configuration table, start channel of address space 2 0−3 correspond to channels 0−3.
[3:2]	RW	ch_start1	Channel configuration table, start channel of address space 1 0−3 correspond to channels 0−3.
[1:0]	RW	ch_start0	Channel configuration table, start channel of address space 0 0−3 correspond to channels 0−3.

AXI_CHCFG2

AXI_CHCCFG2 is MDDRC channel configuration register 2.

Offset Address	Register Name	Total Reset Value
0x028	AXI_CHCFG2	0x0000_0000

Bit	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Name	ch_mode15	ch_mode14	ch_mode13	ch_mode12	ch_mode11	ch_mode10	ch_mode9	ch_mode8	ch_mode7	ch_mode6	ch_mode5	ch_mode4	ch_mode3	ch_mode2	ch_mode1	ch_mode0
Reset	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0

Bits	Access	Name	Description
[31:30]	RW	ch_mode15	Channel configuration table, channel mode of address space 15 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[29:28]	RW	ch_mode14	Channel configuration table, channel mode of address space 14 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[27:26]	RW	ch_mode13	Channel configuration table, channel mode of address space 13 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[25:24]	RW	ch_mode12	Channel configuration table, channel mode of address space 12 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[23:22]	RW	ch_mode11	Channel configuration table, channel mode of address space 11 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved

[21:20]	RW	ch_mode10	Channel configuration table, channel mode of address space 10 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[19:18]	RW	ch_mode9	Channel configuration table, channel mode of address space 9 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[17:16]	RW	ch_mode8	Channel configuration table, channel mode of address space 8 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[15:14]	RW	ch_mode7	Channel configuration table, channel mode of address space 7 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[13:12]	RW	ch_mode6	Channel configuration table, channel mode of address space 6 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[11:10]	RW	ch_mode5	Channel configuration table, channel mode of address space 5 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[9:8]	RW	ch_mode4	Channel configuration table, channel mode of address space 4 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved

[7:6]	RW	ch_mode3	Channel configuration table, channel mode of address space 3 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[5:4]	RW	ch_mode2	Channel configuration table, channel mode of address space 2 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[3:2]	RW	ch_mode1	Channel configuration table, channel mode of address space 1 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved
[1:0]	RW	ch_mode0	Channel configuration table, channel mode of address space 0 00: address-independent 01: reserved 10: dual-channel-interleaved 11: quad-channel-interleaved

AXI_CHCFG3

AXI_CHCCFG3 is MDDRC channel configuration register 3.

Offset Address	Register Name	Total Reset Value
0x02C	AXI_CHCFG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch_invld15	ch_invld14	ch_invld13	ch_invld12	ch_invld11	ch_invld10	ch_invld9	ch_invld8	ch_invld7	ch_invld6	ch_invld5	ch_invld4	ch_invld3	ch_invld2	ch_invld1	ch_invld0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15]	RW	ch_invld15	Channel configuration table, address space 15 mask enable 0: The current address space is valid. 1: The current address space is invalid.

[14]	RW	ch_invld14	Channel configuration table, address space 14 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[13]	RW	ch_invld13	Channel configuration table, address space 13 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[12]	RW	ch_invld12	Channel configuration table, address space 12 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[11]	RW	ch_invld11	Channel configuration table, address space 11 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[10]	RW	ch_invld10	Channel configuration table, address space 10 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[9]	RW	ch_invld9	Channel configuration table, address space 9 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[8]	RW	ch_invld8	Channel configuration table, address space 8 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[7]	RW	ch_invld7	Channel configuration table, address space 7 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[6]	RW	ch_invld6	Channel configuration table, address space 6 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[5]	RW	ch_invld5	Channel configuration table, address space 5 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[4]	RW	ch_invld4	Channel configuration table, address space 4 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[3]	RW	ch_invld3	Channel configuration table, address space 3 mask enable 0: The current address space is valid. 1: The current address space is invalid.

[2]	RW	ch_invld2	Channel configuration table, address space 2 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[1]	RW	ch_invld1	Channel configuration table, address space 1 mask enable 0: The current address space is valid. 1: The current address space is invalid.
[0]	RW	ch_invld0	Channel configuration table, address space 0 mask enable 0: The current address space is valid. 1: The current address space is invalid.

AXI_CHCFG4

AXI_CHCCFG4 is MDDRC channel configuration register 4.

Offset Address	Register Name	Total Reset Value
0x030	AXI_CHCFG4	0x7654_3210

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ch_sect7	ch_sect6	ch_sect5	ch_sect4	ch_sect3	ch_sect2	ch_sect1	ch_sect0
Reset	0 1 1 1	0 1 1 0	0 1 0 1	0 1 0 0	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	ch_sect7	Channel configuration table, position of the channel section to which address space 7 is mapped
[27:24]	RW	ch_sect6	Channel configuration table, position of the channel section to which address space 6 is mapped
[23:20]	RW	ch_sect5	Channel configuration table, position of the channel section to which address space 5 is mapped
[19:16]	RW	ch_sect4	Channel configuration table, position of the channel section to which address space 4 is mapped
[15:12]	RW	ch_sect3	Channel configuration table, position of the channel section to which address space 3 is mapped
[11:8]	RW	ch_sect2	Channel configuration table, position of the channel section to which address space 2 is mapped
[7:4]	RW	ch_sect1	Channel configuration table, position of the channel section to which address space 1 is mapped
[3:0]	RW	ch_sect0	Channel configuration table, position of the channel section to which address space 0 is mapped

AXI_CHCFG5

AXI_CHCCFG5 is MDDRC channel configuration register 5.

Offset Address	Register Name	Total Reset Value
0x034	AXI_CHCFG5	0xFEDC_BA98

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ch_sect15	ch_sect14	ch_sect13	ch_sect12	ch_sect11	ch_sect10	ch_sect9	ch_sect8
Reset	1 1 1 1	1 1 1 0	1 1 0 1	1 1 0 0	1 0 1 1	1 0 1 0	1 0 0 1	1 0 0 0

Bits	Access	Name	Description
[31:28]	RW	ch_sect15	Channel configuration table, position of the channel section to which address space 15 is mapped
[27:24]	RW	ch_sect14	Channel configuration table, position of the channel section to which address space 14 is mapped
[23:20]	RW	ch_sect13	Channel configuration table, position of the channel section to which address space 13 is mapped
[19:16]	RW	ch_sect12	Channel configuration table, position of the channel section to which address space 12 is mapped
[15:12]	RW	ch_sect11	Channel configuration table, position of the channel section to which address space 11 is mapped
[11:8]	RW	ch_sect10	Channel configuration table, position of the channel section to which address space 10 is mapped
[7:4]	RW	ch_sect9	Channel configuration table, position of the channel section to which address space 9 is mapped
[3:0]	RW	ch_sect8	Channel configuration table, position of the channel section to which address space 8 is mapped

AXI_LPCFG

AXI_LPCFG is a low-power zone configuration register of the MDDRC.

Offset Address	Register Name	Total Reset Value
0x038	AXI_LPCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lp_zone_size																reserved															lp_zone_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lp_zone_size	Size of the low-power zone The zone size (in MB) equals lp_zone_size plus 1 and increases by the multiple of 2. 0x0000: 1 MB 0x0001: 2 MB 0x0003: 4 MB 0x0007: 8 MB ... If the address space where the low-power zone is located is dual-/quad-channel interleaved, the size of the low-power zone cannot exceed half or a quarter of the address space.
[15:1]	RW	reserved	Reserved
[0]	RW	lp_zone_en	Low-power zone enable 0: disabled 1: enabled

AXI_QOSCFG0

AXI_QOSCFG0 is DDRC QoS configuration register 0.

Offset Address	Register Name	Total Reset Value
0x040 + 0x4 x *ports* (*ports* = 0–6)	AXI_QOSCFG0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pri_deliver_en	push_deliver_en	reserved					tout_map_mode	tout_id_map								reserved			pri_map_mode	pri_id_map											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	pri_deliver_en	Port priority deliver enable 0: disabled 1: enabled
[30]	RW	push_deliver_en	Push priority deliver enable 0: disabled 1: enabled
[29:25]	RO	reserved	Reserved
[24]	RW	tout_map_mode	Timeout mapping mode of the read/write command 0: mapping mode specified by tout_id_map 1: mapping mode specified by the command associated signal wr(rd)_tout_sel
[23:16]	RW	tout_id_map	Two bits of the read/write command ID for timeout configuration id_map[7:4]: bit[1] for ID mapping id_map[3:0]: bit[0] for ID mapping For example, if ID_MAP is set to 0x32, {ID[3], ID[2]} of the read/write command ID is used for ID mapping and priority configuration. Note that the lower four bits of the read/write command ID indicate the AXI port ID. That is, read/write command ID = {Bus ID, 4-bit AXI port ID}.

[15:13]	RO	reserved	Reserved
[12]	RW	pri_map_mode	Priority mapping mode of the read/write command 0: mapping mode specified by pri_id_map 1: QoS mapping mode specified by using the AxQOS[2:0] signal of the AXI4 read/write command
[11:0]	RW	pri_id_map	Three bits of the read/write command ID for QoS configuration pri_id_map[11:8]: bit[2] for ID mapping pri_id_map[7:4]: bit[1] for IP mapping pri_id_map[3:0]: bit[0] for ID mapping For example, if ID_MAP is set to 0x320, {ID[3], ID[2], ID[0]} of the read/write command ID is used for ID mapping and priority configuration. Note that the lower four bits of the read/write command ID indicate the AXI port ID. That is, read/write command ID = {Bus ID, 4-bit AXI port ID}.

AXI_QOSCFG1

AXI_QOSCFG1 is DDRC QoS configuration register 1.

Offset Address	Register Name	Total Reset Value
0x080 + 0x4 x *ports* (*ports* = 0–6)	AXI_QOSCFG1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		wr_pri_apt	wr_age_prd	reserved		rd_pri_apt	rd_age_prd
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	wr_pri_apt	Write command priority adaptation cycle 0x0: disabled 0x1−0xF: (*n* x 16) clock cycles
[19:16]	RW	wr_age_prd	Write command aging cycle 0x0: disabled 0x1−0xF: (*n* x 16) clock cycles
[15:8]	RO	reserved	Reserved
[7:4]	RW	rd_pri_apt	Read command priority adaptation cycle 0x0: disabled 0x1−0xF: (*n* x 16) clock cycles

[3:0]	RW	rd_age_prd	Read command aging cycle 0x0: disabled 0x1−0xF: (*n* x 16) clock cycles

AXI_WRPRI

AXI_WRPRI is a DDRC write command priority configuration register.

Offset Address: 0x0C0 + 0x4 x *ports* (*ports* = 0–6)

Register Name: AXI_WRPRI

Total Reset Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	wr_pri7			reserved	wr_pri6			reserved	wr_pri5			reserved	wr_pri4			reserved	wr_pri3			reserved	wr_pri2			reserved	wr_pri1			reserved	wr_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	wr_pri7	Priority when the write command ID mapping is 7 000: highest priority ... 111: lowest priority
[27]	RO	reserved	Reserved
[26:24]	RW	wr_pri6	Priority when the write command ID mapping is 6 000: highest priority ... 111: lowest priority
[23]	RO	reserved	Reserved
[22:20]	RW	wr_pri5	Priority when the write command ID mapping is 5 000: highest priority ... 111: lowest priority
[19]	RO	reserved	Reserved
[18:16]	RW	wr_pri4	Priority when the write command ID mapping is 4 000: highest priority ... 111: lowest priority

[15]	RO	reserved	Reserved
[14:12]	RW	wr_pri3	Priority when the write command ID mapping is 3 000: highest priority ... 111: lowest priority
[11]	RO	reserved	Reserved
[10:8]	RW	wr_pri2	Priority when the write command ID mapping is 2 000: highest priority ... 111: lowest priority
[7]	RO	reserved	Reserved
[6:4]	RW	wr_pri1	Priority when the write command ID mapping is 1 000: highest priority ... 111: lowest priority
[3]	RO	reserved	Reserved
[2:0]	RW	wr_pri0	Priority when the write command ID mapping is 0 000: highest priority ... 111: lowest priority

AXI_RDPRI

AXI_RDPRI is a DDRC read command priority configuration register.

Offset Address	Register Name	Total Reset Value
0x100 + 0x4 x *ports* (*ports* = 0–6)	AXI_RDPRI	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	rd_pri7			reserved	rd_pri6			reserved	rd_pri5			reserved	rd_pri4			reserved	rd_pri3			reserved	rd_pri2			reserved	rd_pri1			reserved	rd_pri0		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved

[30:28]	RW	rd_pri7	Priority when the read command ID mapping is 7 000: highest priority ... 111: lowest priority
[27]	RO	reserved	Reserved
[26:24]	RW	rd_pri6	Priority when the read command ID mapping is 6 000: highest priority ... 111: lowest priority
[23]	RO	reserved	Reserved
[22:20]	RW	rd_pri5	Priority when the read command ID mapping is 5 000: highest priority ... 111: lowest priority
[19]	RO	reserved	Reserved
[18:16]	RW	rd_pri4	Priority when the read command ID mapping is 4 000: highest priority ... 111: lowest priority
[15]	RO	reserved	Reserved
[14:12]	RW	rd_pri3	Priority when the read command ID mapping is 3 000: highest priority ... 111: lowest priority
[11]	RO	reserved	Reserved
[10:8]	RW	rd_pri2	Priority when the read command ID mapping is 2 000: highest priority ... 111: lowest priority
[7]	RO	reserved	Reserved
[6:4]	RW	rd_pri1	Priority when the read command ID mapping is 1 000: highest priority ... 111: lowest priority
[3]	RO	reserved	Reserved

[2:0]	RW	rd_pri0	Priority when the read command ID mapping is 0 000: highest priority ... 111: lowest priority

AXI_WRTOUT

AXI_WRTOUT is a DDRC write command timeout configuration register.

Offset Address	Register Name	Total Reset Value
0x140 + 0x4 x *ports* (*ports* = 0–6)	AXI_WRTOUT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	wr_tout3		wr_tout2		wr_tout1		wr_tout0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	wr_tout3	Write command timeout period (level 3) The configuration mode is the same as that of wr_tout0.
[23:16]	RW	wr_tout2	Write command timeout period (level 2) The configuration mode is the same as that of wr_tout0.
[15:8]	RW	wr_tout1	Write command timeout period (level 1) The configuration mode is the same as that of wr_tout0.
[7:0]	RW	wr_tout0	Write command timeout period (level 0) 0x0: disabled 0x01–0xFF: (*n* x 4) clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bit. That is, the lower two bits are fixed at 0.

AXI_RDTOUT

AXI_RDTOUT is a DDRC read command timeout configuration register.

Offset Address	Register Name	Total Reset Value
0x180 + 0x4 x *ports* (*ports* = 0–6)	AXI_RDTOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_tout3								rd_tout2								rd_tout1								rd_tout0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rd_tout3	Read command timeout period (level 3) The configuration mode is the same as that of rd_tout0.
[23:16]	RW	rd_tout2	Read command timeout period (level 2) The configuration mode is the same as that of rd_tout0.
[15:8]	RW	rd_tout1	Read command timeout period (level 1) The configuration mode is the same as that of rd_tout0.
[7:0]	RW	rd_tout0	Read command timeout period (level 0) 0x0: disabled 0x01–0xFF: (*n* x 4) clock cycles **NOTE** When the timeout period is set to 8 bits, the actual count value is 10 bit. That is, the lower two bits are fixed at 0.

AXI_OSTDCFG0

AXI_OSTDCFG0 is DDRC port command outstanding configuration register 0.

Offset Address	Register Name	Total Reset Value
0x200 + 0x4 x *ports* (*ports* = 0–6)	AXI_OSTDCFG0	0x1F1F_1F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												port_ostd_lvl0			
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	port_ostd_lvl0	OSTD threshold of the command transmitted from the port to channel 0 (used with the AXI_OSTDCFG2 register)

AXI_OSTDCFG1

AXI_OSTDCFG1 is DDRC port command outstanding configuration register 1.

Offset Address	Register Name	Total Reset Value
0x240	AXI_OSTDCFG1	0x1F1F_1F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											dmc_ostd_lvl0					
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	dmc_ostd_lvl0	Accumulated OSTD threshold of commands transmitted from all ports to channel 0 (used with the AXI_OSTDCFG2 register)

AXI_OSTDCFG2

AXI_OSTDCFG2 is DDRC port command outstanding configuration register 2.

Offset Address	Register Name	Total Reset Value
0x244	AXI_OSTDCFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		ostd_mode6		ostd_mode5		ostd_mode4		ostd_mode3		ostd_mode2		ostd_mode1		ostd_mode0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved

[13:12]	RW	ostd_mode6	OSTD mode of port 6 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[11:10]	RW	ostd_mode5	OSTD mode of port 5 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[9:8]	RW	ostd_mode4	OSTD mode of port 4 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.

[7:6]	RW	ostd_mode3	OSTD mode of port 3 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[5:4]	RW	ostd_mode2	OSTD mode of port 2 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.
[3:2]	RW	ostd_mode1	OSTD mode of port 1 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.

[1:0]	RW	ostd_mode0	OSTD mode of port 0 00: The OSTD statistics of the current port are disabled. 01: green port. The mode is controlled by channel. When the OSTD of the current port reaches port_ostd_lvl, the port is blocked. 10: non-green port mode 0. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl, the current port is blocked. 11: non-green port mode 1. The mode is controlled by channel. If the accumulated OSTD of all ports reaches dmc_ostd_lvl or the OSTD of the current port reaches port_ostd_lvl, the current port is blocked.

AXI_OSTDSTATUS

AXI_OSTDSTATUS is a DDRC channel command outstanding status register.

Offset Address	Register Name	Total Reset Value
0x248	AXI_OSTDSTATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											ostd_st0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RO	ostd_st0	Command OSTD status of channel 0. The statistics are valid when at least a port is in non-green port mode.

AXI_FLUX0

AXI_FLUX0 is a DDRC port bandwidth traffic control configuration register for channel 0.

Offset Address	Register Name	Total Reset Value
0x280 + 0x4 x *ports* (*ports* = 0–6)	AXI_FLUX0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										flux_port_en0	flux_ovfl_en0	reserved				flux_ovfl_lvl0				reserved				flux_cfg0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	flux_port_en0	AXI interface DDRC traffic statistics enable 0: disabled 1: enabled
[20]	RW	flux_ovfl_en0	AXI interface traffic overflow allow enable 0: disabled 1: enabled When this field is set to 1, the bandwidth of the AXI interface can exceed the configured traffic if the AXI interface traffic exceeds the bandwidth limit, there is no AXI interface with traffic overflow, and a command request is initiated.
[19:17]	RO	reserved	Reserved
[16:12]	RW	flux_ovfl_lvl0	AXI interface traffic overflow threshold 0x0–0x10: DMC threshold for allowing traffic overflow Other values: reserved When the AXI interface traffic exceeds the configured bandwidth of flux, flux_ovfl is 1, and the number of commands to be processed in the DMC is less than the configured threshold, transmission is allowed. Otherwise, no arbitration is performed.
[11:10]	RO	reserved	Reserved
[9:0]	RW	flux_cfg0	Allowed bandwidth of the AXI interface 0x0–0x3FF: ratio of the maximum DDR bandwidth to the total bandwidth accessed by the AXI interface. The total bandwidth is 1024. The configured value is a ratio of the allowed bandwidth to the total bandwidth. Other values: reserved

4.1.6 DMC Registers of the DDRC

4.1.6.1 Register Summary

Table 4-5 describes DMC registers.

Table 4-5 DMC registers (base address: 0x1206_1000)

Offset Address	Register	Description	Page
0x000	DDRC_CTRL_SREF	DDRC self-refresh control register	4-40
0x004	DDRC_CTRL_INIT	DDRC initialization control register	4-41
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0x0C0	DDRC_CFG_ODT	DDR ODT feature configuration register	4-66
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0x200	DDRC_CFG_DDRPHY	DDR I/O configuration register	4-67
0x210	DDRC_CFG_SFC	DDRC software DDR command attribute register	4-68
0x214	DDRC_CFG_SFC_ADDR0	Read/Write memory address register 0 for the software configuration module	4-69

Offset Address	Register	Description	Page
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0x21C	DDRC_CFG_SFC_WDATA0	Write data register 0 for the software configuration module	4-70
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0x278	DDRC_CFG_STAIDMSK	DDR performance statistics command ID mask register	4-73
0x280	DDRC_INTMSK	DDRC interrupt mask register	4-73
0x284	DDRC_RINT	DDRC raw interrupt register	4-74
0x288	DDRC_INTSTS	DDRC interrupt status register	4-75
0x290	DDRC_CURR_STATUS	DDRC status register	4-75
0x294	DDRC_CURR_FUNC	DDRC FUNC module status register	4-76
0x2A0	DDRC_CURR_EXECST	DDRC command state machine status register	4-77
0x2A4	DDRC_CURR_WGFIFOST	DDRC write data FIFO status register	4-78
0x380	DDRC_HIS_FLUX_WR	DDRC all write command traffic statistics register	4-78
0x384	DDRC_HIS_FLUX_RD	DDRC all read command traffic statistics register	4-79
0x388	DDRC_HIS_FLUX_WCMD	DDRC all write command count register	4-79
0x38C	DDRC_HIS_FLUX_RCMD	DDRC all read command	4-80

Offset Address	Register	Description	Page
		count register	
0x390	DDRC_HIS_FLUXID_WR	DDRC specified ID write traffic statistics registers	4-80
0x394	DDRC_HIS_FLUXID_RD	DDRC specified ID read traffic statistics registers	4-81
0x398	DDRC_HIS_FLUXID_WCMD	DDRC all ID write command count register	4-81
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0x3A0	DDRC_HIS_WLATCNT0	DDRC specified ID write command latency statistics register 0	4-82
0x3A4	DDRC_HIS_WLATCNT1	DDRC specified ID write command latency statistics register 1	4-82
0x3A8	DDRC_HIS_RLATCNT0	DDRC specified ID read command latency statistics register 0	4-83
0x3AC	DDRC_HIS_RLATCNT1	DDRC specified ID read command latency statistics register 1	4-83
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	Read channel inherent latency register	4-84
0x3BC	DDRC_HIS_CMD_SUM	DMC accumulated command count register	4-84
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0x4AC	DDRC_HIS_SFC_RDATA1	SFC read data register	4-85
0x4B0	DDRC_HIS_SFC_RDATA2	SFC read data register	4-85
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0x4BC	DDRC_TEST_GENPOSE0	Push timeout control register	4-86

4.1.6.2 Register Description

DDRC_CTRL_SREF

DDRC_CTRL_SREF is a DDRC self-refresh control register.

Offset Address	Register Name	Total Reset Value
0x000	DDRC_CTRL_SREF	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sref_done	sref_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	sref_done	DDR PHY self-refresh done 1: The transition from 0 to 1 indicates that the DDR PHY completes all required operations after exiting the self-refresh status and the DMC can accept new requests.
[0]	RW	sref_req	SDRAM self-refresh request 0: exit the self-refresh status 1: enter the self-refresh status

DDRC_CTRL_INIT

DDRC_CTRL_INIT is a DDRC initialization control register.

Offset Address	Register Name	Total Reset Value
0x004	DDRC_CTRL_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dfi_init_start	init_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	dfi_init_start	DFI initialization start 0: normal state 1: DFI interface initialization is started, and the PHY implements related control processes. This bit is automatically cleared by hardware after initialization is complete.

[0]	RW	init_req	Initialization enable 0: Initialization is complete or initialization is performed properly. 1: The SDRAM starts to be initialized.

DDRC_CTRL_SFC

DDRC_CTRL_SFC is a DDRC software configuration command start register.

Offset Address	Register Name	Total Reset Value
0x00C	DDRC_CTRL_SFC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															cmd_req
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	cmd_req	Request of executing the configuration command of the DDRC 0: The command is not executed or the parameter is automatically cleared after the command is executed. 1: The command is requested to be executed.

DDRC_CTRL_PERF

DDRC_CTRL_PERF is a DDRC performance statistics enable register.

Offset Address	Register Name	Total Reset Value
0x010	DDRC_CTRL_PERF	0x0014_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															perf_en
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RW	perf_en	Performance statistics mode 0: disabled 1: enabled **NOTE** When perf_mode is 0 and this bit is enabled, the performance statistics register starts cyclic counting. When perf_mode is 1, this bit is automatically cleared after counting is complete.

DDRC_CFG_SREF

DDRC_CFG_SREF is a DDRC self-refresh configuration register.

Offset Address	Register Name	Total Reset Value
0x020	DDRC_CFG_SREF	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				sref_arefnum	reserved	clk_switch reserved sref_odis	reserved sref_cc
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	sref_arefnum	Number of self-refresh operations initiated after DDRn SDRAM exits the self-refresh status during the DFS process 0x0: No self-refresh operation is initiated. 0x1–0xF: *n*
[11:9]	RO	reserved	Reserved
[8]	RW	clk_switch	DDRC low-power clock switch. Whether to back press AXI interface command when the DDRC enters the low-power status (DDR self-refresh). 0: The interface commands are not back pressed, and an error is returned directly. 1: The interface commands are back pressed, and the original command is executed after the clock is switched.
[7:5]	RO	reserved	Reserved

[4]	RW	sref_odis	Output disable for the DDR command and data I/O in self-refresh mode. 0: enabled 1: disabled **NOTE** The configuration is a static configuration. It is recommended that this bit be set to 1 to disable the output of the DDR command and data I/O after the DDR enters the self-refresh status. It is recommended that this bit be set to 0 to enable the output of the DDR command and data I/O before the DDR exits the self-refresh status.
[3:1]	RO	reserved	Reserved
[0]	RW	sref_cc	SDRAM clock control in self-refresh mode 0: The SDRAM clock is enabled. 1: The SDRAM clock is disabled.

DDRC_CFG_PD

DDRC_CFG_PD is a DDR power-down status register.

Offset Address	Register Name	Total Reset Value
0x028	DDRC_CFG_PD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								t_clk_cke				reserved			pd_ac	reserved			pd_cc	pd_prd								reserved			pd_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	t_clk_cke	Relationship between CKL and CKE 0x0–0x7: The delay relative to CKE when the PHY disables the clock is related to the DDR PHY. For example, it is set to 5 for SNPS G2 MULTIPHY or 0 for SNPS 32PHY.
[19:17]	RW	reserved	Reserved
[16]	RW	pd_ac	SDRAM address command dynamic disable in power-down mode 0: enabled 1: disabled **NOTE** This field is valid when pd_en is enabled. The control pins exclude CKE, ODT, CSN, and RESET_N.

[15:13]	RO	reserved	Reserved
[12]	RW	pd_cc	SDRAM clock control in power-down mode 0: The SDRAM clock is enabled. 1: The SDRAM clock is disabled. Note: This field is valid only when the LPDDR SDRAM or LPDDR2 SDRAM is used.
[11:4]	RW	pd_prd	SDRAM power-down cycle. When the DDRC does not receive any command in consecutive pd_prd cycles, it forces the SDRAM to enter the power-down status. When a command is received, the DDRC forces the SDRAM to exit the power-down status. 0x00: not to enter the power-down status 0x01−0xFF: *n* clock cycles **NOTE** This field is valid only when pd_en is 1.
[3:1]	RO	reserved	Reserved
[0]	RW	pd_en	Automatic power-down enable for the SDRAM 0: disabled 1: enabled

DDRC_CFG_AREF

DDRC_CFG_AREF is a DDRC auto-refresh mode register.

Offset Address	Register Name	Total Reset Value
0x02C	DDRC_CFG_AREF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aref_alarm_num								reserved			aref_alarm_en	reserved			aref_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:8]	RW	aref_alarm_num	The auto-refresh command is forced to be transmitted if a specific number of auto-refresh commands cannot be transmitted. 0x0–0xFF: lack of (*n* + 1) auto-refresh commands Note that only one auto-refresh command is considered when *n* is 255 because the upper bits are lost after the bits of the 8-bit counter are carried.
[7:5]	RO	reserved	Reserved
[4]	RW	aref_alarm_en	Auto-refresh loss alarm enable (AREF function) 0: disabled 1: enabled
[3:2]	RO	reserved	Reserved
[1:0]	RW	aref_mode	Auto-refresh mode 00: An auto-refresh operation is performed every one tREFI cycle. 01: Two auto-refresh operations are performed every three tREFI cycles. 10: Four auto-refresh operations are performed every five tREFI cycles. 11: Eight auto-refresh operations are performed every nine tREFI cycles.

DDRC_CFG_WORKMODE

DDRC_CFG_WORKMODE is a DDRC operating mode register.

Offset Address	Register Name	Total Reset Value
0x040	DDRC_CFG_WORKMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		hdr_mode	read_mode	reserved			wrap_en	reserved			apre_en	func_clkon	data_clkon	cmd_clkon	clk_ratio
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13]	RW	hdr_mode	DFI interface mode select 0: SDR mode 1: HDR mode Hi3516C V300 supports only the HDR mode.

[12]	RW	read_mode	DDRC read mode 0: associated read mode 1: delay read mode The associated read mode is a mode in which the DDRC samples data based on the data valid signal from the PHY. The delay read mode is a mode in which the DDRC samples the data from the PHY after the internal delay of the DDRC. NOTE This field must be set to 0 when DDRC_DTRCTRL[train_mode] is set to 0.
[11:9]	RO	reserved	Reserved
[8]	RW	wrap_en	Wrap command optimization enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	apre_en	Auto-precharge enable 0: disabled 1: enabled
[3]	RW	func_clkon	Functional module clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[2]	RW	data_clkon	Data channel clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[1]	RW	cmd_clkon	Command channel clock enable 0: The clock is internally controlled. 1: The clock is forcibly enabled.
[0]	RW	clk_ratio	Operating mode of the DDRC 0: The ratio of the DDRC frequency to the PHY frequency is 1:1. 1: The ratio of the DDRC frequency to the PHY frequency is 1:2.

DDRC_CFG_DDRMODE

DDRC_CFG_DDRMODE is a DDR operating mode register.

Offset Address	Register Name	Total Reset Value
0x050	DDRC_CFG_DDRMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rank		reserved		odt_on	zqc_en	reserved			bc_en	reserved			brstlen	reserved			mem_width	reserved			dram_type
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:20]	RW	rank	DDRC rank 00: 1 rank 01: 2 ranks 10: 3 ranks 11: 4 ranks
[19:18]	RO	reserved	Reserved
[17]	RW	odt_on	Whether the ODT signal output to the SDRAM is fixed 0: The signal is controlled by the DDRC. 1: The output is fixed at the wodt configuration of rank 0.
[16]	RW	zqc_en	DDR3 SDRAM ZQ enable 0: disabled 1: enabled **NOTE** This field is valid only for the DDR3 SDRAM or LPDDR2 SDRAM and its default value is 0.
[15:13]	RO	reserved	Reserved
[12]	RW	bc_en	DDR3 burst chop mode 0: disabled 1: enabled **NOTE** This field is valid only for the DDR3 SDRAM.
[11:9]	RO	reserved	Reserved

[8]	RW	brstlen	Burst length of the DDRC 0: BL4 1: BL8 The burst mode of the DDR2 SDRAM can be set to burst4 or burst8 mode. The burst mode of the DDR3 SDRAM must be burst8 mode. **NOTE** When DDRC_CFG_WORKMODE[clk_ratio] is 1, this bit must be set to 0 (BL4) for the DDR3 SDRAM, which indicates the burst8 mode.
[7:6]	RO	reserved	Reserved
[5:4]	RW	mem_width	Bit width of the storage data bus 00: 8 bits 01: 16 bits 10: 32 bits 11: 64 bits
[3]	RO	reserved	Reserved
[2:0]	RW	dram_type	External memory type 000: reserved 001: LPDDR 010: LPDDR2 011: LPDDR3 100: DDR 101: DDR2 110: DDR3 111: DDR4

DDRC_CFG_RNKVOL

DDRC_CFG_RNKVOL is a DDRC-controlled DDR capacity configuration register.

Offset Address	Register Name	Total Reset Value
0x060	DDRC_CFG_RNKVOL	0x0000_0022

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				mem_map	reserved	mem_bank	reserved	mem_row	reserved	mem_col

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:12]	RW	mem_map	Address translation mode of the SDRAM 00: {Rank, Row, Ba, Col, DW} = AXI_Address 01: {Rank, Ba, Row, Col, DW}= AXI_Address 10: {Rank, Row, Ba, Col, cs, Col, DW}= AXI_Address 11: {Rank, Ba, Row, Col, cs, Col, DW}= AXI_Address This parameter can be set to 10 or 11 only when DDRC_CFG_AREF [dual_ch] is valid. When there are multiple ranks, the configuration must be the same for each rank.
[11:9]	RO	reserved	Reserved
[8]	RW	mem_bank	Number of banks of a single SDRAM 0: 4 banks 1: 8 banks
[7]	RO	reserved	Reserved
[6:4]	RW	mem_row	Bit width of the row address of a single SDRAM 000: 11 bits 001: 12 bits 010: 13 bits 011: 14 bits 100: 15 bits 101: 16 bits Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	mem_col	Bit width of the column address of a single SDRAM 000: 8 bits 001: 9 bits 010: 10 bits 011: 11 bits 100: 12 bits Other values: reserved **NOTE** The DDRC does not support the DDR whose col address is less than 8. That is, the 32-bit LPDDR2 with the capacity of 64 Mbits is not supported.

DDRC_CFG_EMRS01

DDRC_CFG_EMRS01 is a configuration register for DDR mode register 0 and mode register 1.

Offset Address	Register Name	Total Reset Value
0x070	DDRC_CFG_EMRS01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs1																mrs															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs1	DDR*n* SDRAM extended mode register 1
[15:0]	RW	mrs	DDR*n* SDRAM mode register

DDRC_CFG_EMRS23

DDRC_CFG_EMRS23 is a configuration register for DDR mode register 2 and mode register 3.

Offset Address	Register Name	Total Reset Value
0x074	DDRC_CFG_EMRS23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	emrs3																emrs2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	emrs3	DDR*n* SDRAM extended mode register 3
[15:0]	RW	emrs2	DDR*n* SDRAM extended mode register 2

DDRC_CFG_TIMING0

DDRC_CFG_TIMING0 is DDRC timing parameter register 0.

Timing parameters in the register are obtained from DDR user manuals.

- If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value.
- If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x080	DDRC_CFG_TIMING0	0xFFFF_FF3F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4 3 2 1 0
Name	tmrd	trrd	trp	trcd	trc		reserved	tras
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Number of wait cycles for the load mode register (LMR) command. The value is the larger value between tMOD and tMRD for the DDR2 or LPDDR2 and is tMRD for the DDR3. 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[27:24]	RW	trrd	Number of wait cycles from ACT bank A to ACT bank B 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[23:19]	RW	trp	Number of wait cycles for the disable command (PRE period) 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles
[18:14]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write command 0x0–0x3: 3 clock cycles 0x4–0xF: *n* clock cycles
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command 0x00–0x01: 1 clock cycle 0x02–0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved
[5:0]	RW	tras	Number of wait cycles from the ACT bank command to the disable command (PRE) 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles

DDRC_CFG_TIMING1

DDRC_CFG_TIMING1 is DDRC timing parameter register 1.

Timing parameters in the register are obtained from DDR user manuals.

- If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value.

- If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x084	DDRC_CFG_TIMING1	0xFF24_51FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tsre								trtw				twl				tcl				reserved				trfc							
Reset	1	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command 0x0: reserved 0x01–0xFF: (*n* x 4) clock cycles This field is set to the larger value between tXSDLL and tXS for the DDR3 SDRAM.
[23:20]	RW	trtw	Delay from the last read data command to the first write data command 0x0–0x1: 1 clock cycle 0x2–0xF: (*n* + 1) clock cycles **NOTE** In DDR2/DDR3 mode, the field value depends on the latency of the board, package, and I/O; in LPDDR/LPDDR2/LPDDR3 mode, the field value depends on the latency of the board, package, and I/O and tdqsckmax.
[19:16]	RW	twl	Number of wait cycles from the write command to the write data command 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, 0x3 indicates three clock cycles. The clock cycles are obtained from DDR user manuals. You can directly configure this field based on the clock cycles.
[15:12]	RW	tcl	Column address strobe latency (CL) from the read command to the read data operation 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles The clock cycles are obtained from DDR user manuals. You can directly configure this field based on the clock cycles.
[11:9]	RO	reserved	Reserved

[8:0]	RW	trfc	Number of wait cycles for the AREF period or AREF to the ACT command. The field value is set to the maximum value of max{trfc, tzqcs}. 0x00: reserved 0x01–0x1FF: *n* clock cycles

DDRC_CFG_TIMING2

DDRC_CFG_TIMING2 is DDRC timing parameter register 2.

Timing parameters in the register are obtained from DDR user manuals.

- If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value.
- If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x88	DDRC_CFG_TIMING2	0xF303_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				reserved								tfaw				reserved	taref										
Reset	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of retaining the self-refresh mode 0x0: reserved 0x1–0xF: *n* clock cycles The field value must be the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE.
[27:24]	RW	twtr	Number of wait cycles for the last write data to the write-to-read command 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles For example, the value 0x3 indicates three clock cycles.
[23:18]	RO	reserved	Reserved
[17:12]	RW	tfaw	Number of clock cycles for four consecutive activation commands 0x00–0x3F: *n* clock cycles For example, the value 0x14 indicates 20 clock cycles.
[11]	RO	reserved	Reserved

[10:0]	RW	taref	Number of auto-refresh cycles 0x000: forbidden 0x001–0x7FF: The auto-refresh cycle of the SDRAM is (16 x *n*) clock cycles. For example, the value 0x008 indicates 128 (16 x 8) clock cycles. The interval tREFI is 7800/16/tclk. Tclk is the running cycle of the DDRC. When DDRC_CFG_AREF [aref_mode] is 1, the interval must be set to 8 x tREFI.

DDRC_CFG_TIMING3

DDRC_CFG_TIMING3 is DDRC timing parameter register 3.

Timing parameters in the register are obtained from DDR user manuals.

- If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value.
- If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x8C	DDRC_CFG_TIMING3	0xFFDF_F0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd												tzqinit								taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles 0x000: The ZQCS command is forbidden. 0x001–0x3FF: (*n* x 128) AREF cycles The number of ZQCS command cycles is equal to (*n* x 128) taref clock cycles.
[21:12]	RW	tzqinit	Number of ZQ initialization delay cycles 0x0–0x1FF: (*n* + 1) clock cycles The field value must be the larger value between tZQINIT and tDLLK.
[11:8]	RW	taond	Number of ODT enable/disable cycles In DDR2 mode (taond/taofd): 0x0: 2/2.5 0x1: 3/3.5 0x2: 4/4.5

			0x3: 5/5.5 Other values: reserved In DDR3 mode, this value is set to tWL − 1. In 1:2 mode, this value needs to be set to tWL − 2. However, if the PHY has been separately processed, the value tWL − 1 is used. In LPDDR3 mode, the value is set to tODTon(max)/tCK.
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode 0x0–0xF: *n* clock cycles (in decimal) For example, 0x7 indicates seven clock cycles. The field value is the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3 mode, the field value is the larger value between tXP and tCKE.
[3:0]	RW	trtp	Wait delay from the read command to the disable command 000–010: 2 clock cycles 011–111: *n* clock cycles Trtp is calculated as follows: Trtp = AL + BL/2 + Max (trtp, 2) – 2 **NOTE** For DDR2, Trtp is greater than or equal to 2; for DDR3, Trtp is greater than or equal to 4.

DDRC_CFG_TIMING4

DDRC_CFG_TIMING4 is DDRC timing parameter register 4.

Timing parameters in the register are obtained from DDR user manuals.

- If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value.
- If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x090	DDRC_CFG_TIMING4	0x01FF_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tmod				twlo				reserved				twldqsen				reserved				twlmrd			
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0		0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved

[24:20]	RW	tmod	Delay from the MRS command to ODT and ZQCL validity 0x0–0x1: 1 clock cycle 0x2–0x1F: *n* clock cycles
[19:16]	RW	twlo	DDR3 write level status delay 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles The parameter is equal to (twlo + twloe).
[15:14]	RO	reserved	Reserved
[13:8]	RW	twldqsen	DDR3 write level start delay 0x0 and 0x1: one clock cycle 0x2−0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved
[5:0]	RW	twlmrd	Delay of the initial valid DDR3 write level DQS 0x0 and 0x1: one clock cycle 0x2−0x3F: n clock cycles

DDRC_CFG_TIMING5

DDRC_CFG_TIMING5 is DDRC timing parameter register 5.

Timing parameters in the register are obtained from DDR user manuals.

- If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value.
- If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x094	DDRC_CFG_TIMING5	0x1113_FF1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												trnk2rnk				tzqcs								reserved				twr			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved

[19:16]	RW	trnk2rnk	Rank-to-rank delay 0000–1111: *n* clock cycles Note: In DDR2/DDR3 mode, the field value depends on the latency of the board, package, and I/O; in LPDDR/LPDDR2/LPDDR3 mode, the field value depends on the latency of the board, package, and I/O, and tdqsckmax.
[15:8]	RW	tzqcs	ZQCS calibration delay period 0x0–0xFF: (*n* + 1) clock cycles The field value must be greater than or equal to 10 due to the DMC design.
[7:5]	RO	reserved	Reserved
[4:0]	RW	twr	Number of wait cycles of write recovery 0x0–0x1: 1 clock cycle 0x2–0x1F: *n* clock cycles **NOTE** When DFS is required, tWR must be set based on the maximum chip frequency that may be used. tWR cannot be changed when the DDR frequency changes.

DDRC_CFG_TIMING6

DDRC_CFG_TIMING6 is DDRC timing parameter register 6.

Timing parameters in the register are obtained from DDR user manuals.

- If DDRC_CFG_WORKMODE[clk_ration] is 1, convert the time specified in the DDR user manuals into the DDR clock cycle and then divide it by 2. If the value has a remainder, add 1 to the value.
- If DDRC_CFG_WORKMODE[clk_ration] is 0, convert the time specified in the DDR user manuals into the DDR clock cycle and then use it directly.

Offset Address	Register Name	Total Reset Value
0x098	DDRC_CFG_TIMING6	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tcksrx				tcksre			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	tcksrx	tCKSRX for the DDR3 or DDR4, that is, number of advanced valid beats before the DDR exits the self-refresh status 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles

[3:0]	RW	tcksre	tCKSRE for the DDR3 or DDR4, that is, number of beats to be retained after the DDR enters the self-refresh status 0x0–0x1: 1 clock cycle 0x2–0xF: *n* clock cycles

DDRC_CFG_NXT_TIMING0

DDRC_CFG_NXT_TIMING0 is DDRC timing parameter register 0 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0A0	DDRC_CFG_NXT_TIMING0	0xFFFF_FF3F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2 1 0
Name	tmrd	trrd	trp	trcd	trc		reserved		tras
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0	1 1	1 1 1 1

Bits	Access	Name	Description
[31:28]	RW	tmrd	Number of wait cycles for the loading command of the loading mode register (LMR) 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[27:24]	RW	trrd	Number of wait cycles from ACT bank A to ACT bank B 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[23:19]	RW	trp	Number of wait cycles for the disable command (PRE period) 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[18:14]	RW	trcd	Number of wait cycles from the ACT bank command to the read or write command 0x0−0x3: three clock cycles 0x4−0xF: *n* clock cycles
[13:8]	RW	trc	Number of wait cycles from an ACT bank command to the next ACT bank command 0x00–0x01: one clock cycle 0x02−0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved

[5:0]	RW	tras	Number of wait cycles from the ACT bank command to the disable command (PRE) 0x00–0x01: one clock cycle 0x02−0x3F: *n* clock cycles

DDRC_CFG_NXT_TIMING1

DDRC_CFG_NXT_TIMING1 is DDRC timing parameter register 1 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0A4	DDRC_CFG_NXT_TIMING1	0xFF24_51FF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tsre		trtw	twl	tcl	reserved	trfc	
Reset	1 1 1 1	1 1 1 1	0 0 1 0	0 1 0 0	0 1 0 1	0 0 0 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	tsre	Number of wait cycles from the self-refresh exit command to the read command 0x0: one clock cycle 0x01–0xFF: *n* x 4 clock cycles When the DDR3 SDRAM is used, the value is set to tXSDLL.
[23:20]	RW	trtw	Delay from the last read data command to the first write data command 0x0 and 0x1: one clock cycle 0x2−0xF: *n* + 1 clock cycles
[19:16]	RW	twl	Number of wait cycles from the write command to the data write operation 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles For example, the value 0x3 indicates three clock cycles. Note: In DDR2 mode, twl is set to tcl − 1 and the condition (twl − taond ≥ 1) must be met.
[15:12]	RW	tcl	Column address strobe latency (CL) from the read command to the data read operation 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles
[11:9]	RO	reserved	Reserved

[8:0]	RW	trfc	Number of wait cycles for the AREF period or AREF to the ACT command. The field value is set to the maximum value of max{trfc, tzqcs}. 0x00–0x01: one clock cycle 0x02−0xFF: *n* clock cycles

DDRC_CFG_NXT_TIMING2

DDRC_CFG_NXT_TIMING2 is DDRC timing parameter register 2 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0A8	DDRC_CFG_NXT_TIMING2	0xF303_F000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tcke				twtr				reserved				tfaw								reserved	taref										
Reset	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	tcke	Minimum cycle of retaining the low-power mode 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles The field value must be the maximum value among tCKESR, tCKSRE, tCKSRX, and tCKE.
[27:24]	RW	twtr	Number of wait cycles for the last data write operation to the write-to-read command 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles For example, the value 0x3 indicates three clock cycles.
[23:18]	RO	reserved	Reserved
[17:12]	RW	tfaw	Number of clock cycles for four consecutive activation commands 0x00−0x3F: *n* clock cycles For example, the value 0x14 indicates 20 clock cycles.
[11]	RO	reserved	Reserved

[10:0]	RW	taref	Number of auto-refresh cycles 0x000: auto-refresh disabled 0x001–0x7FF: The auto-refresh cycle of the SDRAM is (16 x n) clock cycles. For example, the value 0x008 indicates 128 (16 x 8) clock cycles. The interval tREF is 7800/16/tclk. Tclk is the running cycle of the SDRAM.

DDRC_CFG_NXT_TIMING3

DDRC_CFG_NXT_TIMING3 is DDRC timing parameter register 3 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0AC	DDRC_CFG_NXT_TIMING3	0xFFDF_F0F2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tzq_prd												tzqinit								taond				txard				trtp			
Reset	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:22]	RW	tzq_prd	Number of ZQCS command cycles 0x000: The ZQCS command is disabled. 0x001–0x3FF: (*n* x 128) AREF cycles The number of ZQCS command cycles is equal to (*n* x 128) taref clock cycles.
[21:12]	RW	tzqinit	Number of ZQ initialization delay cycles 0x0–0x3ff: (*n* + 1) clock cycles The value needs to be set to the larger one between tZQINIT and tDLLK.
[11:8]	RW	taond	Number of ODT enable/disable cycles In DDR2 mode (taond/taofd): 0x0: 2/2.5 0x1: 3/3.5 0x2: 4/4.5 0x3: 5/5.5 Other values: reserved In DDR3 mode, the value is set to tWL − 1. In 1:2 mode, the value needs to be set to tWL – 2. However, if the PHY has been separately processed, the value tWL − 1 is used. In LPDDR3 mode, the value is set to tODTon(max)/tCK.
[7:4]	RW	txard	Number of wait cycles of exiting the DDR low-power mode

			0x0–0xF: *n* clock cycles. *n* indicates a decimal value. For example, 0x7 indicates seven clock cycles. The field value is the maximum value among tXP, tXARD, tXARDS, and tXS. In DDR3 mode, when the register is set to tXS, txard only needs to be set to an equivalent clock cycle of 10 ns.
[3:0]	RW	trtp	Wait delay from the read command to the disable command 0000−0010: two clock cycles 0011–1111: *n* clock cycles Trtp = AL + BL/2 + Max (trtp, 2) – 2

DDRC_CFG_NXT_TIMING4

DDRC_CFG_NXT_TIMING4 is DDRC timing parameter register 4 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0B0	DDRC_CFG_NXT_TIMING4	0x01FF_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tmod				twlo				reserved				twldqsen				reserved				twlmrd			
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RW	reserved	Reserved
[24:20]	RW	tmod	Delay from the MRS command to ODT valid 0x0 and 0x1: one clock cycle 0x02−0x1F: *n* clock cycles
[19:16]	RW	twlo	DDR3 write level status delay parameter 0x0 and 0x1: one clock cycle 0x2−0xF: *n* clock cycles The parameter is equal to (twlo + twloe).
[15:14]	RO	reserved	Reserved
[13:8]	RW	twldqsen	DDR3 write level start delay 0x0 and 0x1: one clock cycle 0x2−0x3F: *n* clock cycles
[7:6]	RO	reserved	Reserved

[5:0]	RW	twlmrd	Delay of the initial valid DDR3 write level DQS 0x0 and 0x1: one clock cycle 0x2−0x3F: *n* clock cycles

DDRC_CFG_NXT_TIMING5

DDRC_CFG_NXT_TIMING5 is DDRC timing parameter register 5 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0B4	DDRC_CFG_NXT_TIMING5	0x1113_FF1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												trnk2rnk				tzqcs								reserved				twr			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:20]	RW	reserved	Reserved
[19:16]	RW	trnk2rnk	Rank-to-rank delay 0000–1111: *n* clock cycles
[15:8]	RW	tzqcs	ZQCS calibration delay period 0x0−0xFF: (*n* + 1) clock cycles
[7:5]	RW	reserved	Reserved
[4:0]	RW	twr	Number of wait cycles of write recovery 0x0 and 0x1: one clock cycle 0x2−0x1F: *n* clock cycles **NOTE** When DFS is required, tWR must be set based on the maximum chip frequency that may be used. tWR cannot be changed when the DDR frequency changes.

DDRC_CFG_NXT_TIMING6

DDRC_CFG_NXT_TIMING6 is DDRC timing parameter register 6 for switching the frequency.

Offset Address	Register Name	Total Reset Value
0x0B8	DDRC_CFG_NXT_TIMING6	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				todt_sft				tcksrx				tcksre			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:12]	RW	reserved	Reserved
[11:8]	RW	todt_sft	ODT delay control in LPDDR3 mode, for compensating the delay of the DDR PHY for ODT IO of POP LPDDR3 0x0–0xF: *n* clock cycles ODT delay = tWL − taond + todt_sft. Note that the maximum ODT delay cannot exceed 0xF.
[7:4]	RW	tcksrx	tCKSRX for the DDR3 or DDR4, that is, number of advanced valid beats before the DDR exits the self-refresh status 0x0 and 0x1: one clock cycle 0x2–0xF: *n* clock cycles
[3:0]	RW	tcksre	tCKSRE for the DDR3 or DDR4, that is, number of beats to be retained after the DDR enters the self-refresh status 0x0 and 0x1: one clock cycle 0x2–0xF: *n* clock cycles

DDRC_CFG_BLDATA

DDRC_CFG_BLDATA is a DDRC pre-received write data configuration register.

Offset Address	Register Name	Total Reset Value
0x0BC	DDRC_CFG_BLDATA	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												bl_data			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	bl_data	Number of DMC data segments corresponding to each DDR command in the current mode 0x0–0xF: *n* data segments

DDRC_CFG_ODT

DDRC_CFG_ODT is a DDR ODT feature configuration register.

Offset Address	Register Name	Total Reset Value
0x0C0	DDRC_CFG_ODT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rodt3	rodt2	rodt1	rodt0	wodt3	wodt2	wodt1	wodt0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RW	rodt3	Read ODT enable for rank 3 0: disabled 1: enabled
[27:24]	RW	rodt2	Read ODT enable for rank 2 0: disabled 1: enabled
[23:20]	RW	rodt1	Read ODT enable for rank 1 0: disabled 1: enabled
[19:16]	RW	rodt0	Read ODT enable for rank 0 0: disabled 1: enabled
[15:12]	RW	wodt3	Write ODT enable for rank 3 0: disabled 1: enabled
[11:8]	RW	wodt2	Write ODT enable for rank 2 0: disabled 1: enabled
[7:4]	RW	wodt1	Write ODT enable for rank 1 0: disabled 1: enabled
[3:0]	RW	wodt0	Write ODT enable for rank 0 0: disabled 1: enabled

DDRC_CFG_DMCLVL

DDRC_CFG_DMCLVL is a DDRC command queue depth threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x0C4	DDRC_CFG_DMCLVL	0x0000_010C

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							que_level
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	1 1 0 0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	que_level	Depth of the command register FIFO in the DMC 0x1−0x10: depth of *n* commands Other values: reserved

DDRC_CFG_DDRPHY

DDRC_CFG_DDRPHY is a DDR IO configuration register.

Offset Address	Register Name	Total Reset Value
0x200	DDRC_CFG_DDRPHY	0x0000_1000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				phy_upden	trdlat	reserved	phy_zqen	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	phy_upden	dfi_phyupd_en enable in response to the DDR PHY 0: disabled 1: enabled
[11:8]	RW	trdlat	Inherent delay of the DDR PHY 0x0–0xF: (*n* + 1) clock cycles The value needs to be set to 8 when synopsys3/2phy is used.
[7:5]	RW	reserved	Reserved

[4]	RW	phy_zqen	DDRPHY dfi_ctrlupd_req enable 0: disabled 1: enabled
[3:0]	RO	reserved	Reserved

DDRC_CFG_SFC

DDRC_CFG_SFC is a DDRC software DDR command attribute register.

Offset Address	Register Name	Total Reset Value
0x210	DDRC_CFG_SFC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2 1 0
Name	cmd_mrs				cmd_ma		cmd_rank	reserved	cmd_type
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0 0 0

Bits	Access	Name	Description
[31:16]	RW	cmd_mrs	Value of the DDR mode register when the LMR command is configured. This field is valid for the lower eight bits of the LPDDR2.
[15:8]	RW	cmd_ma	Address for the mode register to be configured when the LMR command is configured in LPDDR mode
[7:4]	RW	cmd_rank	DDR rank for executing commands 0: The configuration command is not executed. 1: The configuration command is executed. **NOTE** Each bit controls a rank. For example, cmd_rank[0] control DDR rank 0.
[3]	RO	reserved	Reserved
[2:0]	RW	cmd_type	DDR command configuration 000: enter the deep power-down status 001: exit the deep power-down status 010: LMR command 011: ZQCL 100: WRITE command 101: read command 110: precharge all command 111: read MRS command

DDRC_CFG_SFC_ADDR0

DDRC_CFG_SFC_ADDR0 is read/write memory address register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x214	DDRC_CFG_SFC_ADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sfc_row																sfc_col															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	sfc_row	Row address for the memory that is read or written by the software configuration module
[15:0]	RW	sfc_col	Column address for the memory that is read or written by the software configuration module **NOTE** The DDRC access address must be aligned based on the current DMC bit width. For example, if the current DMC bit width is 128 bits: When the 64-/72-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:1], 1'b0}. When the 32-/36-bit external DDR is connected, the DMC addresses are accessed based on {sfc_col[15:2]0.2'b0}.

DDRC_CFG_SFC_ADDR1

DDRC_CFG_SFC_ADDR1 is read/write memory address register 1 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x218	DDRC_CFG_SFC_ADDR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sfc_bank	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	sfc_bank	Bank address for the memory that is read or written by the software configuration module

DDRC_CFG_SFC_WDATA0

DDRC_CFG_SFC_WDATA0 is write data configuration register 0 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x21C	DDRC_CFG_SFC_WDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata0	Bits 127−96 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA1

DDRC_CFG_SFC_WDATA1 is write data configuration register 1 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x220	DDRC_CFG_SFC_WDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata1	Bits 95−64 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA2

DDRC_CFG_SFC_WDATA2 is write data configuration register 2 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x224	DDRC_CFG_SFC_WDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata2	Bits 63−32 of the written data of the software configuration module

DDRC_CFG_SFC_WDATA3

DDRC_CFG_SFC_WDATA3 is write data configuration register 3 for the software configuration module.

Offset Address	Register Name	Total Reset Value
0x228	DDRC_CFG_SFC_WDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdata3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdata3	Bits 31−0 of the written data of the software configuration module

DDRC_CFG_PERF

DDRC_CFG_PERF is a DDRC performance statistics mode register.

Offset Address	Register Name	Total Reset Value
0x270	DDRC_CFG_PERF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		flux_en	perf_mode	perf_prd																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved

[29]	RW	flux_en	DMC traffic monitoring enable 0: disabled 1: enabled When traffic monitoring is enabled, the statistics module provides the number of cycles occupied by the DDR interface by ID to each request port. The traffic can be controlled by using this field and the port traffic setting function.
[28]	RW	perf_mode	Performance statistics mode 0: continuous trigger mode. The performance counter continues to count. This ensures no overflow within 1s in continuous count mode. 1: single trigger mode. When the performance statistics time reaches perf_prd, the count value is retained and counting stops. **NOTE** After the count value overflows, the value is retained.
[27:0]	RW	perf_prd	Performance statistics cycle 0x0–0x1: invalid 0x2–0xFFFFFFF: statistics cycles The actual statistics cycle is perf_prd x 16 x tclk (tclk is the bus clock cycle of the DDRC) **NOTE** This field is valid only when perf_mode is 1. When perf_mode is 0, the performance counter keeps on counting.

DDRC_CFG_STAID

DDRC_CFG_STAID is a DDRC performance statistics command ID register.

Offset Address	Register Name	Total Reset Value
0x274	DDRC_CFG_STAID	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												sta_id																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:0]	RW	sta_id	Performance statistics by a specified ID. This field works with sta_idmask.

DDRC_CFG_STAIDMSK

DDRC_CFG_STAIDMSK is a DDR performance statistics command ID mask register.

Offset Address	Register Name	Total Reset Value
0x278	DDRC_CFG_STAIDMSK	0x0000_1FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				sta_idmask											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved NOTE This field must be set to 0.
[12:0]	RW	sta_idmask	Specified ID mask The DDRC performance statistics register collects statistics only for specified ID commands. Cmd_id&sta_idmask = sta_id

DDRC_INTMSK

DDRC_INTMSK is a DDRC interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x280	DDRC_INTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																aref_alarm_int_mask	reserved			rdtimeout_int_mask	reserved							sref_err_int_mask	reserved				flux_int_mask	serr_int_mask
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	aref_alarm_int_mask	DDR AREF command error interrupt mask enable 0: enabled 1: disabled
[15:13]	RO	reserved	Reserved

[12]	RW	rdtimeout_int_mask	DDR PHY read data timeout interrupt mask enable 0: enabled 1: disabled
[11:6]	RO	reserved	Reserved
[5]	RW	sref_err_int_mask	Interface command error interrupt enable in DDR self-refresh mode 0: enabled 1: disabled
[4:2]	RO	reserved	Reserved
[1]	RW	flux_int_mask	DDR FLUX statistics period reach interrupt mask enable 0: enabled 1: disabled
[0]	RW	serr_int_mask	DDR ECC single-bit error interrupt mask enable 0: enabled 1: disabled

DDRC_RINT

DDRC_RINT is a DDRC raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x284	DDRC_RINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															aref_alarm_rint	reserved			rdtimeout_rint	reserved							sref_err_rint	reserved				flux_rint	serr_rint
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	INT_WC	aref_alarm_rint	DDR AREF command error raw interrupt. Writing 1 clears the interrupt.
[15:13]	RO	reserved	Reserved
[12]	INT_WC	rdtimeout_rint	DDR PHY read data timeout raw interrupt. Writing 1 clears the interrupt.
[11:6]	RO	reserved	Reserved

[5]	INT_WC	sref_err_rint	Self-refresh interface command access interrupt. Writing 1 clears the interrupt.
[4:2]	RO	reserved	Reserved
[1]	RW	flux_rint	DDR FLUX statistics period reach interrupt. Writing 1 clears the interrupt.
[0]	INT_WC	serr_rint	DDR ECC single-bit error raw interrupt. Writing 1 clears the interrupt.

DDRC_INTSTS

DDRC_INTSTS is a DDRC interrupt status register.

Offset Address	Register Name	Total Reset Value
0x288	DDRC_INTSTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			aref_alarm_intsts	reserved	rdtimeout_intsts	reserved	sref_err_intsts	reserved	flux_intsts	serr_intsts
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	INT	aref_alarm_intsts	DDR AREF command error interrupt
[15:13]	RO	reserved	Reserved
[12]	INT	rdtimeout_intsts	DDR PHY read data timeout interrupt
[11:6]	RO	reserved	Reserved
[5]	INT	sref_err_intsts	Self-refresh interface command access interrupt
[4:2]	RO	reserved	Reserved
[1]	RW	flux_intsts	DDR FLUX statistics period reach interrupt
[0]	INT	serr_intsts	DDR ECC single-bit error interrupt

DDRC_CURR_STATUS

DDRC_CURR_STATUS is a DDRC status register.

Offset Address	Register Name	Total Reset Value
0x290	DDRC_CURR_STATUS	0x0000_0101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							busy_func	reserved			busy_dmc	reserved			busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	busy_func	Status of the DDRC FUNC module. This field is in the SREF status during reset. 0: idle 1: A command is being processed.
[7:5]	RO	reserved	Reserved
[4]	RO	busy_dmc	Status of the DDRC DMC 0: idle 1: A command is being processed.
[3:1]	RO	reserved	Reserved
[0]	RO	busy	Overall status of the DDRC 0: idle 1: A command is being processed.

DDRC_CURR_FUNC

DDRC_CURR_FUNC is a DDRC FUNC module status register.

Offset Address	Register Name	Total Reset Value
0x294	DDRC_CURR_FUNC	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			in_phyupd	reserved															in_sfc	in_pd				reserved		dfi_init_complete	in_init	reserved			in_sref

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28]	RO	in_phyupd	DDRC PHY update status 0: idle 1: The PHY is being updated.
[27:13]	RO	reserved	Reserved
[12]	RO	in_sfc	DDRC SFC status 0: idle 1: An SFC command is being processed.
[11:8]	RO	in_pd	DDRC power-down status 0: normal 0: power-down status Each bit represents a rank.
[7:6]	RO	reserved	Reserved
[5]	RO	dfi_init_complete	DFI initialization status 0: initializing 1: normal operating mode
[4]	RO	in_init	DDRC initialization status 0: normal 1: initializing
[3:1]	RO	reserved	Reserved
[0]	RO	in_sref	DDR self-refresh status 0: normal 1: self-refresh

DDRC_CURR_EXECST

DDRC_CURR_EXECST is a DDRC command state machine status register.

Offset Address	Register Name	Total Reset Value
0x2A0	DDRC_CURR_EXECST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_ct																dmc_cv															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dmc_ct	Controller command type 0: read command 1: write command
[15:0]	RO	dmc_cv	Controller command validity flag 0: invalid 1: valid

DDRC_CURR_WGFIFOST

DDRC_CURR_WGFIFOST is a DDRC write data FIFO status register.

Offset Address	Register Name	Total Reset Value
0x2A4	DDRC_CURR_WGFIFOST	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															wgntfifo_e
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	wgntfifo_e	WGNT_FIFO empty or full status. The empty status indicates that all written data is received, and the non-empty status indicates that the written data is not completely received. 0: not empty 1: empty

DDRC_HIS_FLUX_WR

DDRC_HIS_FLUX_WR is a DDRC all write command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x380	DDRC_HIS_FLUX_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr	Write traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RD

DDRC_HIS_FLUX_RD is a DDRC all read command traffic statistics register.

Offset Address	Register Name	Total Reset Value
0x384	DDRC_HIS_FLUX_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd	Read traffic statistics of all masters with the IDs of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_WCMD

DDRC_HIS_FLUX_WCMD is a DDRC all write command count register.

Offset Address	Register Name	Total Reset Value
0x388	DDRC_HIS_FLUX_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_wr_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_wr_cmd	Write command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle.

			When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUX_RCMD

DDRC_HIS_FLUX_RCMD is a DDRC all read command count register.

Offset Address	Register Name	Total Reset Value
0x38C	DDRC_HIS_FLUX_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_rd_cmd	Read command count of the masters with all IDs of the DDRC. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_WR

DDRC_HIS_FLUXID_WR is a DDRC specified ID write traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x390	DDRC_HIS_FLUXID_WR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr	Write traffic statistics of the master with the specified ID of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_RD

DDRC_HIS_FLUXID_RD is a DDRC specified ID read traffic statistics registers.

Offset Address	Register Name	Total Reset Value
0x394	DDRC_HIS_FLUXID_RD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd	Read traffic statistics of the master with the specified ID of the DDRC. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_WCMD

DDRC_HIS_FLUXID_WCMD is a DDRC all ID write command count register.

Offset Address	Register Name	Total Reset Value
0x0398	DDRC_HIS_FLUXID_WCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_wr_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_wr_cmd	Read traffic statistics of the master based on specified IDs. The counting is performed in the valid statistics cycle. The unit is the DMC bit width. When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_FLUXID_RCMD

DDRC_HIS_FLUXID_RCMD is a DDRC all ID read command count register.

Offset Address	Register Name	Total Reset Value
0x039C	DDRC_HIS_FLUXID_RCMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fluxid_rd_cmd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fluxid_rd_cmd	Read command count of the master based on specified IDs. The counting is performed in the valid statistics cycle. When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_WLATCNT0

DDRC_HIS_WLATCNT0 is DDRC specified ID write command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A0	DDRC_HIS_WLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_max																wlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	wlatcnt_max	Maximum latency of the write command with the specified ID of the DDRC This field is cleared when the next statistics start.
[15:0]	RO	wlatcnt_min	Minimum latency of the write command with the specified ID of the DDRC. The maximum value is retained if overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_WLATCNT1

DDRC_HIS_WLATCNT1 is DDRC specified ID write command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3A4	DDRC_HIS_WLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wlatcnt_all																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	wlatcnt_all	Accumulated latency of the write command with the specified ID in the statistics cycle (the results of the lower four bits are ignored) When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the write command with the specified ID by dividing wlatcnt_all by fluxid_wr_cmd.

DDRC_HIS_RLATCNT0

DDRC_HIS_RLATCNT0 is a DDRC specified ID read command latency statistics register 0.

Offset Address	Register Name	Total Reset Value
0x3A8	DDRC_HIS_RLATCNT0	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_max																rlatcnt_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	rlatcnt_max	Maximum latency of the read command with the specified ID of the DDRC The actual maximum read latency is rlatcnt_max plus inhere_rlatcnt. The maximum value is retained if overflow occurs. This field is cleared when the next statistics start.
[15:0]	RO	rlatcnt_min	Minimum latency of the read command with the specified ID of the DDRC Note that the actual minimum read latency is rlatcnt_min plus inhere_rlatcnt. The maximum value is retained if overflow occurs. This field is cleared when the next statistics start.

DDRC_HIS_RLATCNT1

DDRC_HIS_RLATCNT1 is DDRC specified ID read command latency statistics register 1.

Offset Address	Register Name	Total Reset Value
0x3AC	DDRC_HIS_RLATCNT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rlatcnt_all																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rlatcnt_all	Accumulated latency of the read command with the specified ID in the statistics cycle (the results of the lower four bits are ignored) When perf_mode is 0, the value is wrapped when overflow occurs. When perf_mode is 1, the value is retained when overflow occurs. This field is cleared when the next statistics start. **NOTE** Software can obtain the average latency of the read command with the specified ID by using rlatcnt_all/fluxid_rd_cmd+inhere_rlatcnt.

DDRC_HIS_INHERE_RLAT_CNT

DDRC_HIS_INHERE_RLAT_CNT is a read channel inherent latency register.

Offset Address	Register Name	Total Reset Value
0x3B0	DDRC_HIS_INHERE_RLAT_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																inhere_rlatcnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	inhere_rlatcnt	Inherent latency of the read data channel for the DDRC and PHY. The actual latency can be obtained only by using this register and rlatcnt_min, rlatcnt_max, rlatcnt_all, and fluxid_rd_cmd.

DDRC_HIS_CMD_SUM

DDRC_HIS_CMD_SUM is a DDRC accumulated command count register.

Offset Address	Register Name	Total Reset Value
0x3BC	DDRC_HIS_CMD_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmc_cmd_sum																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dmc_cmd_sum	Accumulated value of the commands that are temporarily stored in the DMC in the cycle. The value is wrapped if overflow occurs.

DDRC_HIS_SFC_RDATA0

DDRC_HIS_SFC_RDATA0 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4A8	DDRC_HIS_SFC_RDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata4	Bits 96−127 of the data read by the SFC

DDRC_HIS_SFC_RDATA1

DDRC_HIS_SFC_RDATA1 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4AC	DDRC_HIS_SFC_RDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata5	Bits 95−64 of the data read by the SFC

DDRC_HIS_SFC_RDATA2

DDRC_HIS_SFC_RDATA2 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4B0	DDRC_HIS_SFC_RDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata6	Bits 63−32 of the data read by the SFC

DDRC_HIS_SFC_RDATA3

DDRC_HIS_SFC_RDATA3 is an SFC read data register.

Offset Address	Register Name	Total Reset Value
0x4B4	DDRC_HIS_SFC_RDATA3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdata7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rdata7	Bits 0−31 of the data read by the SFC In RD_MRS mode, the values of bits 0–7 are read-back values of the LP DDR2 MRS register.

DDRC_TEST_GENPOSE0

DDRC_TEST_GENPOSE0 is a push timeout control register.

Offset Address	Register Name	Total Reset Value
0x4BC	DDRC_TEST_GENPOSE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							push_timeout_en	push_timeout							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RW	reserved	Reserved

[8]	RW	push_timeout_en	push_timeout enable 0: disabled 1: enabled
[7:0]	RW	push_timeout	Timeout value that is pushed to the preceding command when the push timeout conditions are met

4.2 Flash Memory Controller

4.2.1 Overview

The flash memory controller (FMC) provides memory controller interfaces for connecting to external SPI NAND flash, SPI NOR flash to access data.

4.2.2 Features

The FMC has the following features:

- Provides one 4 KB+256 bytes on-chip buffer.
- Supports the SPI NOR flash and SPI NAND flash.
- Supports one external CS (SPI NAND flash or SPI NOR flash).
- Supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI.
- Supports the SPI NAND flash with the following specifications:
  - 2 KB or 4 KB page size
  - 64-page or 128-page block
- Allows the system to boot of the SPI NOR flash, SPI NAND flash.
  - Provides 1 MB boot space.
  - Automatically sends the reset command of the flash and then performs data read operations in boot mode. The reset command is sent only in SPI NAND flash mode.
  - Automatically skips bad blocks (for the SPI NAND flash). A maximum of four consecutive bad blocks can be skipped.
  - Supports the adaptive boot function (for the SPI NAND flash). The FMC automatically obtains the correct page size, error checking and correction (ECC) type, and block size.
  - Supports the 1-wire and 4-wire boot modes for the SPI NAND flash and 1-wire boot mode for the SPI NOR flash.
  - Supports boot from the SPI NOR flash in 3-byte or 4-byte address mode.
- Supports the direct memory access (DMA) read and write functions of the SPI NOR flash and SPI NAND flash.

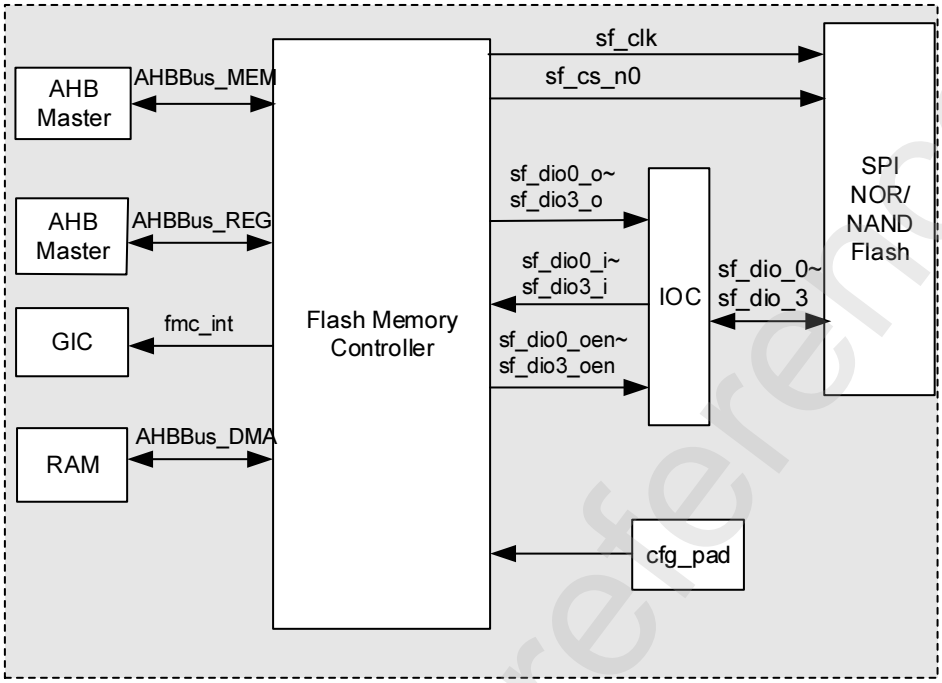
  - Supports the read and write operations in internal DMA mode for the SPI NAND flash. You can write only the entire page and read the entire page or only the control information (read only the OOB).
  - Supports the DMA read and write operations for the SPI NOR flash. The length of the data read or written can be configured.
- Supports manual configurations of commands only in ECC0 mode.
- Supports the ECC function for the SPI NAND flash.
  - 8-bit/1 KB, 16-bit/1 KB, 24-bit/1 KB, and 28-bit/1 KB Bose-Chaudhuri-Hocquenghem (BCH) code ECC (1 KB means the 1 KB level but not exactly 1024 bytes.)
  - Enable and disable of the ECC function and ECC code generation
  - Data read and write operations in ECC0 mode (transparent transmission)
  - No incorrect reporting of uncorrectable ECC errors when empty pages (data is 0xFF) are read
- Supports seven types of interrupts: operation completion interrupt, programming failure interrupt, correctable ECC error interrupt, ECC alarm interrupt, uncorrectable ECC error interrupt, advanced high-performance bus (AHB) operation error interrupt, and DMA transfer error interrupt.
- Supports the low-power mode. The unused modules can be disabled.

4.2.3 Function Description

4.2.3.1 Interface Block Diagram

The FMC is used for interaction between the AHB and external flash memories. Figure 4-4 shows the block diagram of FMC interfaces.

Figure 4-4 Block diagram of FMC interfaces



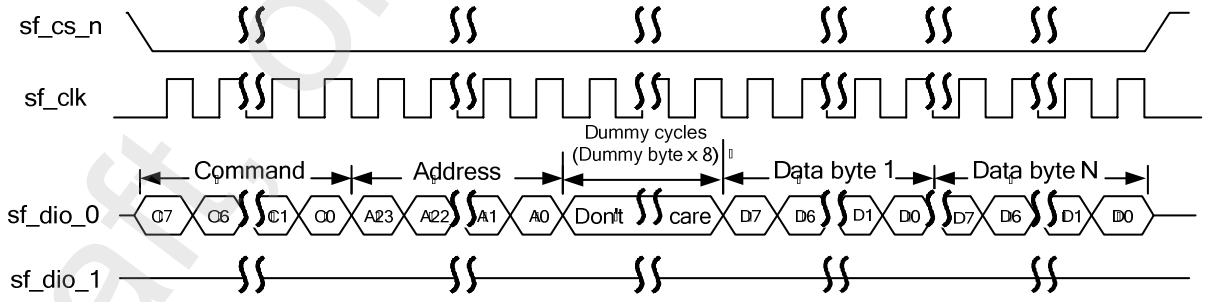
4.2.3.2 Interfaces

The FMC supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI. The standard SPI, dual I/O SPI, and quad I/O SPI support the SDR, DTR, and DDR modes.

Standard SPI

The standard SPI is connected to a 1-bit data input line and a 1-bit data output line. Figure 4-5 shows the write timing of the standard SPI.

Figure 4-5 Write timing of the standard SPI

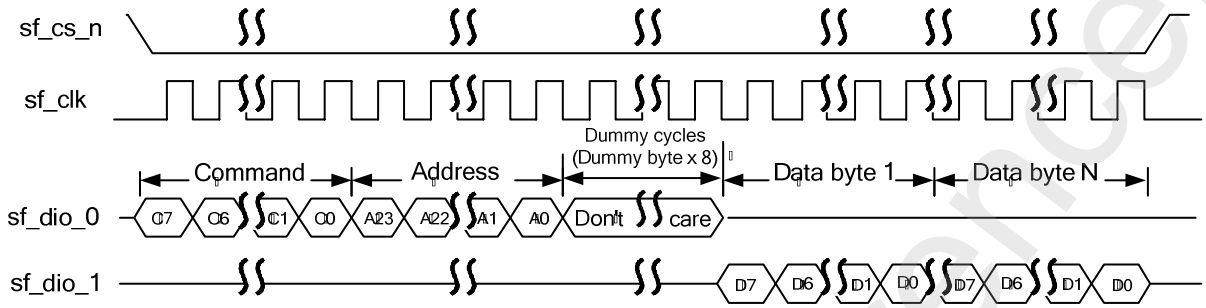


Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- Data is output in single-bit serial mode through the sf_dio_0 line.

Figure 4-6 shows the read timing of the standard SPI.

Figure 4-6 Read timing of the standard SPI



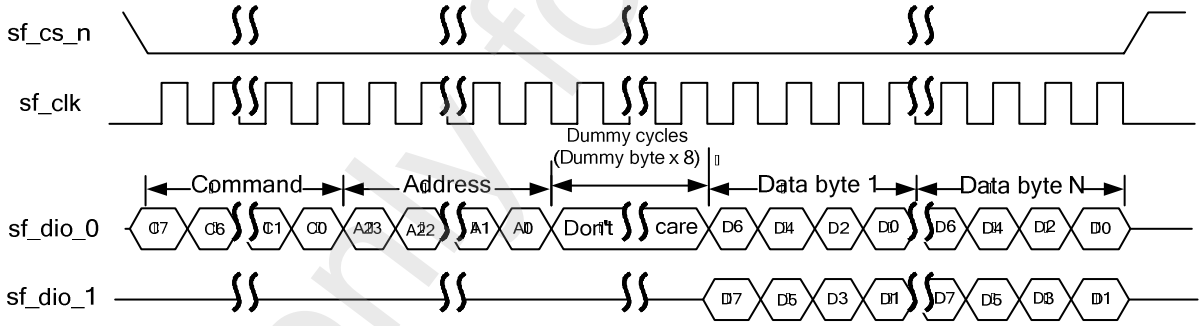
Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- Data is input in single-bit serial mode through the sf_dio_1 line.

Dual-Output/Dual-Input SPI

Figure 4-7 shows the timing of the dual-output/dual-input SPI.

Figure 4-7 Timing of the dual-output/dual-input SPI



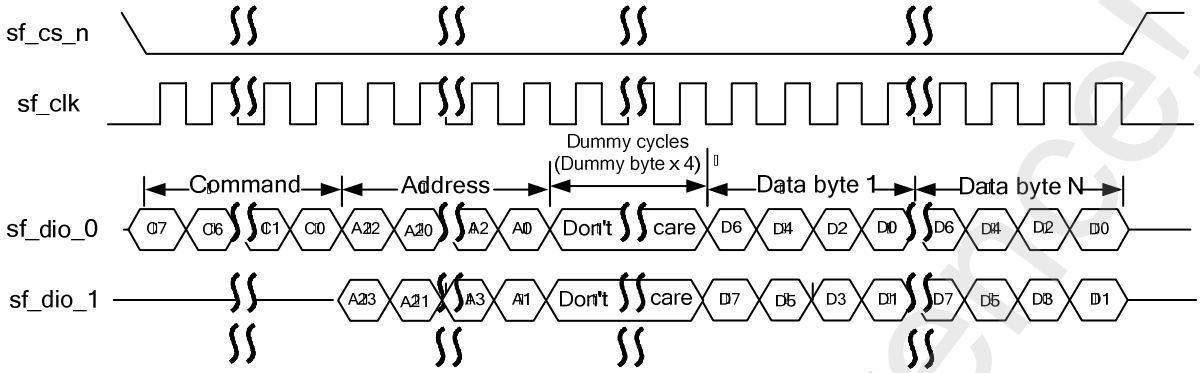
Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- The data bytes are output (written) or input (read) in 2-bit mode through the sf_dio_0 or sf_dio_1 line.

Dual I/O SPI

Figure 4-8 and Figure 4-9 show the timings of the dual I/O SPI.

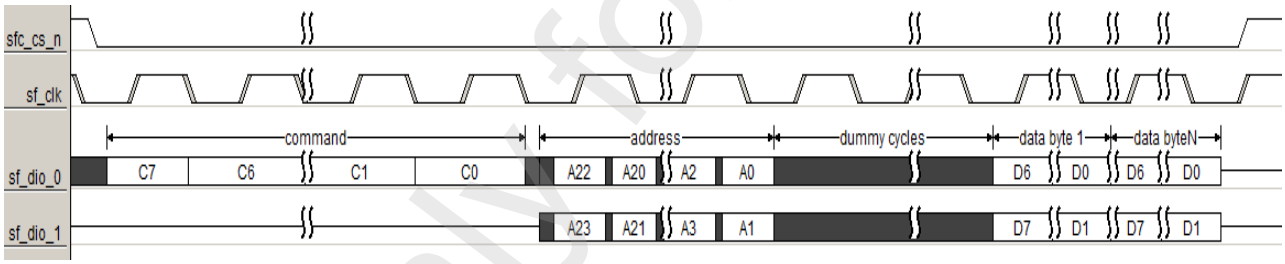
Figure 4-8 SDR timing of the dual I/O SPI



Note the following:

- The command cycles are output in single-bit serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 2-bit mode through the sf_dio_0 or sf_dio_1 line.
- The data bytes are output (written) or input (read) in 2-bit mode through the sf_dio_0 or sf_dio_1 line.

Figure 4-9 DDR/DTR timing of the dual I/O SPI



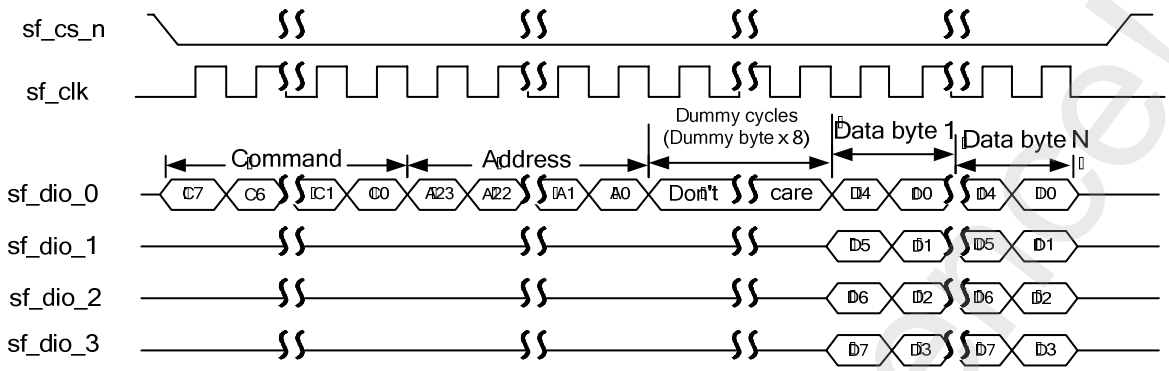
Note the following:

- The command cycles are output in single-bit serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 2-bit dual-edge active mode through the sf_dio_0 or sf_dio_1 line.
- Data is input (read) in 2-bit dual-edge active mode through the sf_dio_0 or sf_dio_1 line.
- Only the read operation is supported in DDR/DTR mode.

Quad-Output/Quad-Input SPI

Figure 4-10 shows the timing of the quad-output/quad-input SPI.

Figure 4-10 Timing of the quad-output/quad-input SPI



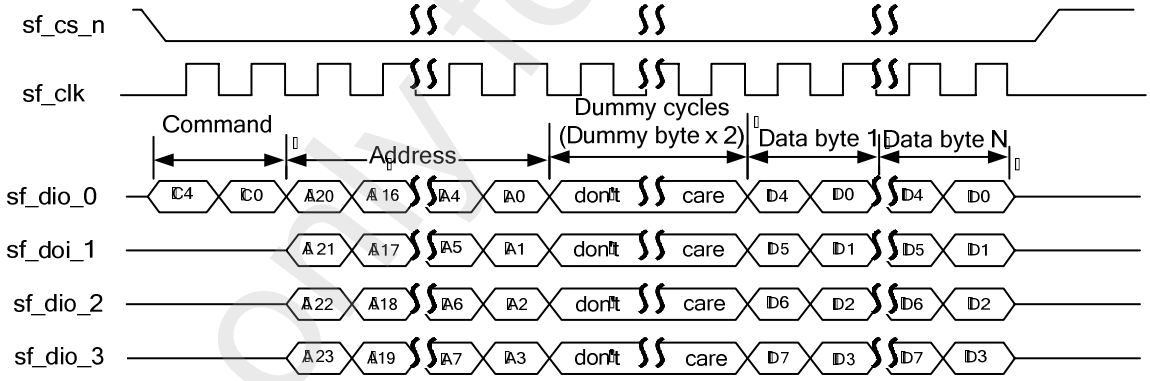
Note the following:

- The command cycles, address cycles, and dummy cycles are output in single-bit serial mode through the sf_dio_0 line.
- Data is output (written) or input (read) in 4-bit mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

Quad I/O SPI

Figure 4-11 and Figure 4-12 show the timings of the quad I/O SPI.

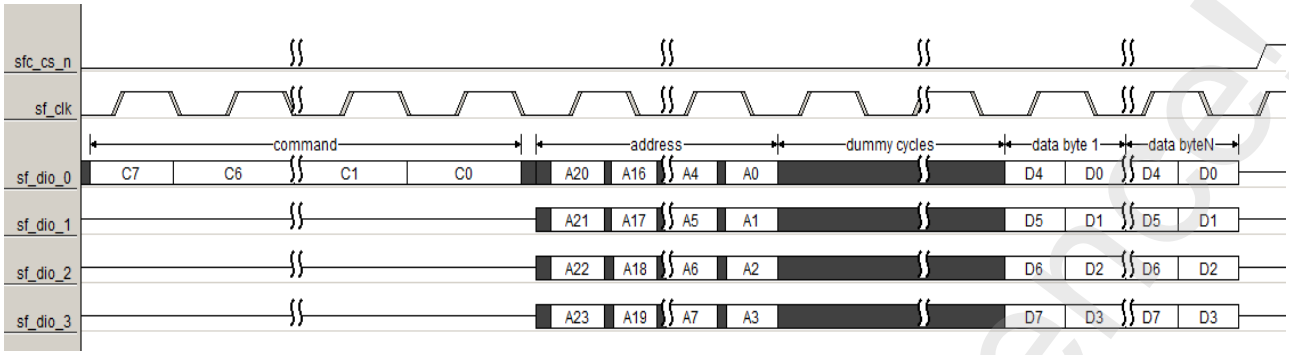
Figure 4-11 SDR timing of the quad I/O SPI



Note the following:

- The command cycles are output in single-bit serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 4-bit mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.
- The data bytes are output (written) or input (read) in 4-bit mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

Figure 4-12 DDR/DTR timing of the quad I/O SPI



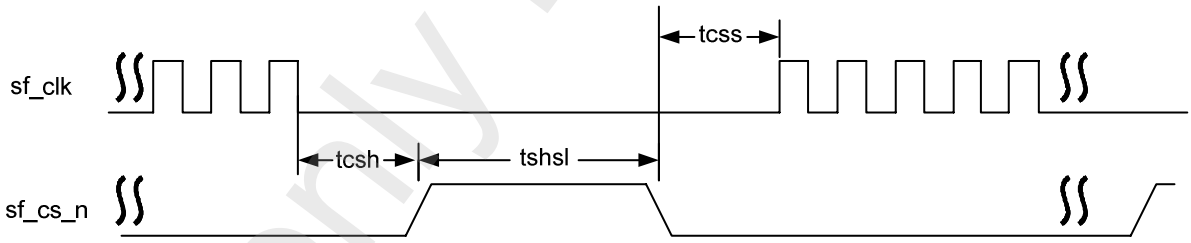
Note the following:

- The command cycles are output in single-bit single-edge data serial mode through the sf_dio_0 line.
- The address cycles and dummy cycles are output in 4-bit dual-edge mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.
- Data is input in 4-bit dual-edge sampling mode through the sf_dio_0, sf_dio_1, sf_dio_2, or sf_dio_3 line.

4.2.3.3 SPI Timings

Figure 4-13 shows the SPI timings and related parameters.

Figure 4-13 SPI output timing



NOTE

- The timings are configured in the TIMING_SPI_CFG register.
- tcsh indicates the CS# hold time.
- tcss indicates the CS# setup time.
- tshsl indicates the CS# deselect time.

4.2.3.4 SPI NAND Flash Address

Table 4-6 describes the address allocation of the SPI NAND flash. The first and second bytes indicate the column address, whereas the third, fourth, and fifth bytes indicate the row address.

Table 4-6 Address allocation of the SPI NAND flash

Byte	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1st byte	A0	A1	A2	A3	A4	A5	A6	A7
2nd byte	A8	A9	A10	A11	A12*	A13*	0	0
3rd byte	A12	A13	A14	A15	A16	A17	A18	A19
4th byte	A20	A21	A22	A23	A24	A25	A26	A27
5th byte*	A28*	A29*	0	0	0	0	0	0

NOTE

- Bits A0−A11 are configured as the valid column address when the page size is 2 KB. Bits A0−A12 are configured as the valid column address when the page size is 4 KB.
- Bit A12 (2 KB page size) and bit A13 (4 KB page size) indicate the plane address only for Micron flash memories. Other vendors do not have the concept of plane address.
- Whether bits A28 and A29 are required depends on the flash memory. If the two bits are not used, the outputs are 0.

When the read and write commands of the SPI NAND flash are issued, the column and row addresses are configured based on the following operations:

- For the write operation, the column address is configured during the loading process and the row address is configured during the programming process.
- For the read operation, the row address is configured when the page is read to cache and the column address is configured during the read operation.

In internal DMA mode, the address command is issued by the FMC. FMC_ADDRL and FMC_ADDRH are configured by software based on the operation address. The configuration values of FMC_ADDRL and FMC_ADDRH are 1st byte−4th byte and 5th byte respectively.

NOTE

- If the page size is 2 KB, bit A12 indicates the plane address. Other meanings of bit A12 are not supported; otherwise, the results of the read and write operations will be affected.
- If the page size is 4 KB, bit A13 indicates the plane address. Other meanings of bit A13 are not supported; otherwise, the results of the read and write operations will be affected.

4.2.3.5 Boot Function

The FMC is in boot mode by default. The chip can boot by reading data directly from the flash memory. The CPU can directly read the data stored in the address ranging from 0x00_0000 to 0x0F_FFFF. The size of the entire address space is 1 MB.

SPI NOR Flash

The address space of the SPI NOR flash is consecutive. The 1 MB boot data is directly mapped to address space 0x00_0000 to 0x0F_FFFF of the SPI NOR flash.

SPI NAND Flash

For the SPI NAND flash, the address space is inconsecutive and bad blocks may exist. As a result, the 1 MB boot data cannot be directly mapped to the flash. To implement the boot operation, page_size, and block_size are also required for address decoding.

The FMC supports the adaptive boot function, that is, it can automatically adapt to ecc_type, page_size, and block_size of the flash based on the block 0 data. The FMC requires that physical block 0 be a good block, and it can automatically skip other bad blocks.

During booting, the FMC automatically skips bad blocks and searches for good blocks to read boot information. A maximum of four consecutive bad blocks can be skipped at a time. If five consecutive physical bad blocks are encountered, the boot fails. During the boot process, several bad-block skip processes are allowed. A bad-block-skip process ends when a good block is encountered, and a new bad-block-skip process starts when a bad block is encountered.

The FMC logic determines whether a block is a bad block based on the following conditions:

- The bad block flag bits of the first page and last page of the current physical block are 0xff.
- The empty block flag bits of the first page and last page of the current physical block are 0x00.
- The ECC units where the OOB data is located in the first page and last page of the current physical block have no uncorrectable errors.

Table 4-7 describes the specifications supported by the SPI NAND flash in boot mode.

Table 4-7 Specifications supported in adaptive boot mode

ECC (Bit)	Page_size (KB)	Block_size (Pages/Block)	SPI NAND
8	2	64/128 (SPI NAND)	Supported
	4		Supported
16	2	64/128 (SPI NAND)	Supported
	4		Supported
24	2	64/128 (SPI NAND)	Supported
	4		Supported
28	2	64/128 (SPI NAND)	Supported
	4		Supported

4.2.3.6 Operations in Register Mode

The registers related to the operation command and address are configured by using software. Then the corresponding command is issued by configuring the FMC_OP register. The FMC issues a command to the flash memory according to the value configured by software. If data needs to be transferred to the flash memory, the internal buffer is used.

Operations such as reading ID, setting feature, and erasing are performed in this mode.

In register mode, all the operations related to the flash memory can be combined, and commands related to the address and data transfer can be issued separately.

4.2.3.7 Operations in Internal DMA Mode

The FMC can perform read and write operations in internal DMA mode for improving the access speed. In internal DMA mode, the FMC can directly access the DDR through the bus.

- DMA write operation: For the SPI NOR flash, data with any length can be transferred from any address of the DDR and written to any address of the flash memory. For the SPI NAND flash, the write operation is performed only by page.
- DMA read operation: For the SPI NOR flash, data with any length can be transferred from any address of the flash memory and written to any address of the DDR. For the SPI NAND flash, the entire page is read or only the OOB is read.
- Only-OOB read operation: When the software requires only software management information such as the bad block flag and empty block flag, only the control information needs to be read. In this case, only the OOB is read in DMA mode.

4.2.3.8 ECC

For the SPI NAND flash, the FMC supports ECC. Four ECC modes are supported, including 8-bit/1 KB ECC mode, 16-bit/1 KB ECC mode, 24-bit/1 KB ECC mode, and 28-bit/1 KB ECC mode. In 8-bit/1 KB ECC mode, errors occur in at most eight bits of the checked one ECC unit (1 KB+redundancy data) can be corrected.

The OOB information is added to the data with ECC protection, and then the ECC is added. The error correction algorithm runs by the error correction unit (1 KB). For example, the ECC is calculated for (DATA+OOB). If the page size is 2 KB, data in each error correction unit is (DATA+OOB)/2; if the page size is 4 KB, data in each error correction unit is (DATA+OOB)/4.

- The OOB is part of the software management information. For details, see the (BB+CTRL) part in the data structure.
- DATA indicates the real data. DATA indicates 2048-byte data when the page size is 2 KB and 4096-byte data when the page size is 4 KB.

The SPI NAND flash supports only the 8-bit and 24-bit ECCByte, and 16-bit and 28-bit ECC modes. If the spare area of the flash is sufficient for storing the check code, the 16-bit/1 KB ECC mode can be used for the flash that requires 4-bit/512 bytes ECC mode to improve the reliability.

When the maximum error correction capability is exceeded, the uncorrectable error interrupt is reported. The FMC supports the alarm interrupt. When the number of error bits during one error correction operation is greater than or equal to the configured error threshold (FMC_ERR_THD), an error alarm interrupt is reported. If error bits occur in one or more error correction units and the number of error bits in each error correction unit is less than the error threshold and uncorrectable error value, the correctable error interrupt flag FMC_INT[err_val_int] is changed to 1.

When the data on a page is read, if uncorrectable errors occur in one error correction unit, the uncorrectable error interrupt is reported. If an error alarm interrupt is reported for an error correction unit, the error correction alarm status is reported. If the number of error correction bits is less than the error threshold, the correctable error interrupt status is reported.

4.2.3.9 Timeout/Fail

The FMC provides the timeout mechanism for DMA write operations. The fail state is returned if the component has no feedback.

- For the NAND flash, the controller queries whether the DMA write operation is complete by constantly sending the GET FEATURE operation. If the FMC wait time exceeds the configured value of FMC_TIMEOUT_WR[timeout_wr], the DMA write operation is ended and the FMC_INT[op_fail] interrupt is reported.
- For the SPI NOR flash, the controller queries whether the DMA write operation is complete by sending the RDSR operation. If the FMC wait time exceeds the configured value of FMC_TIMEOUT_WR[timeout_wr], the DMA write operation is ended and the FMC_INT[op_fail] interrupt is reported.

4.2.4 Working Process

4.2.4.1 Initialization Process

The initialization process is as follows:

Step 1 (Optional; when the timing parameters need to be adjusted) Configure TIMING_SPI_CFG (for the SPI NAND flash or SPI NOR flash) based on the flash memory.

Step 2 Configure the interface type, ecc_type and page size of the flash memory in the FMC configuration register (FMC_CFG) according to the manual of the connected flash.

Step 3 Switch the address mode of the SPI NOR flash to the 4-byte address mode if the default address mode is 3-byte address mode. For details, see section 4.2.4.4 "Process of Changing the Address Mode of the SPI NOR Flash."

Step 4 Issue operations based on the operation configuration registers.

----End

4.2.4.2 FMC_OP Operation Process (Register Operation Mode)

To read the IDs of the component registers or configure component registers by configuring FMC_OP, perform the following steps:

Step 1 Set ecc_type of the FMC_CFG register to 0.

Step 2 Write the expected operation data from the buffer access start address for a register write operation (for example, configure the flash memory configuration register).

Step 3 Configure the operation command, operation address, and number of data segments to be read or written as required in FMC_CMD, FMC_ADDRL, and FMC_DATA_NUM respectively.

Step 4 Configure FMC_OP_CFG based on the component commands that are issued by configuring FMC_OP.

Step 5 Configure FMC_OP to issue commands. For details about the configuration value, see the description of FMC_OP.

Step 6 Check whether the operation is complete by querying FMC_OP[reg_op_start] in query mode and FMC_INT[op_done] in interrupt mode. If FMC_OP[reg_op_start] is 1 or FMC_INT[op_done] is detected, the operation is complete.

Step 7 Read the value of the component register from the buffer that stores the read results in step 6.

----End

4.2.4.3 Process of Reading the Component Status

To read the component status, perform the following steps:

Step 1 Set FMC_OP[read_status_en] and FMC_OP[reg_op_start] to 1 to issue the component status read command.

Step 2 Store the read result in FMC_FLASH_INFO.

----End

4.2.4.4 Process of Changing the Address Mode of the SPI NOR Flash

The SPI NOR flash supports the 3-byte and 4-byte address modes. You can specify the default address mode by pulling up or pulling down the corresponding pin, and dynamically change the address mode by configuring registers after the chip boots.

If the default address mode is the 3-byte address mode and the address mode of the flash memory is 4-byte address mode, perform the following steps to change the address mode after the chip boots:

Step 1 Ensure that the operations on the SPI NOR flash are complete.

Step 2 Configure the related registers to issue the command for changing the address mode of the flash memory to 4-byte address mode in register mode according to the flash memory requirements.

Step 3 Set FMC_CFG [spi_nor_addr_mode] to 1 to change the address mode of the SPI NOR flash from the 3-byte address mode to 4-byte address mode.

----End

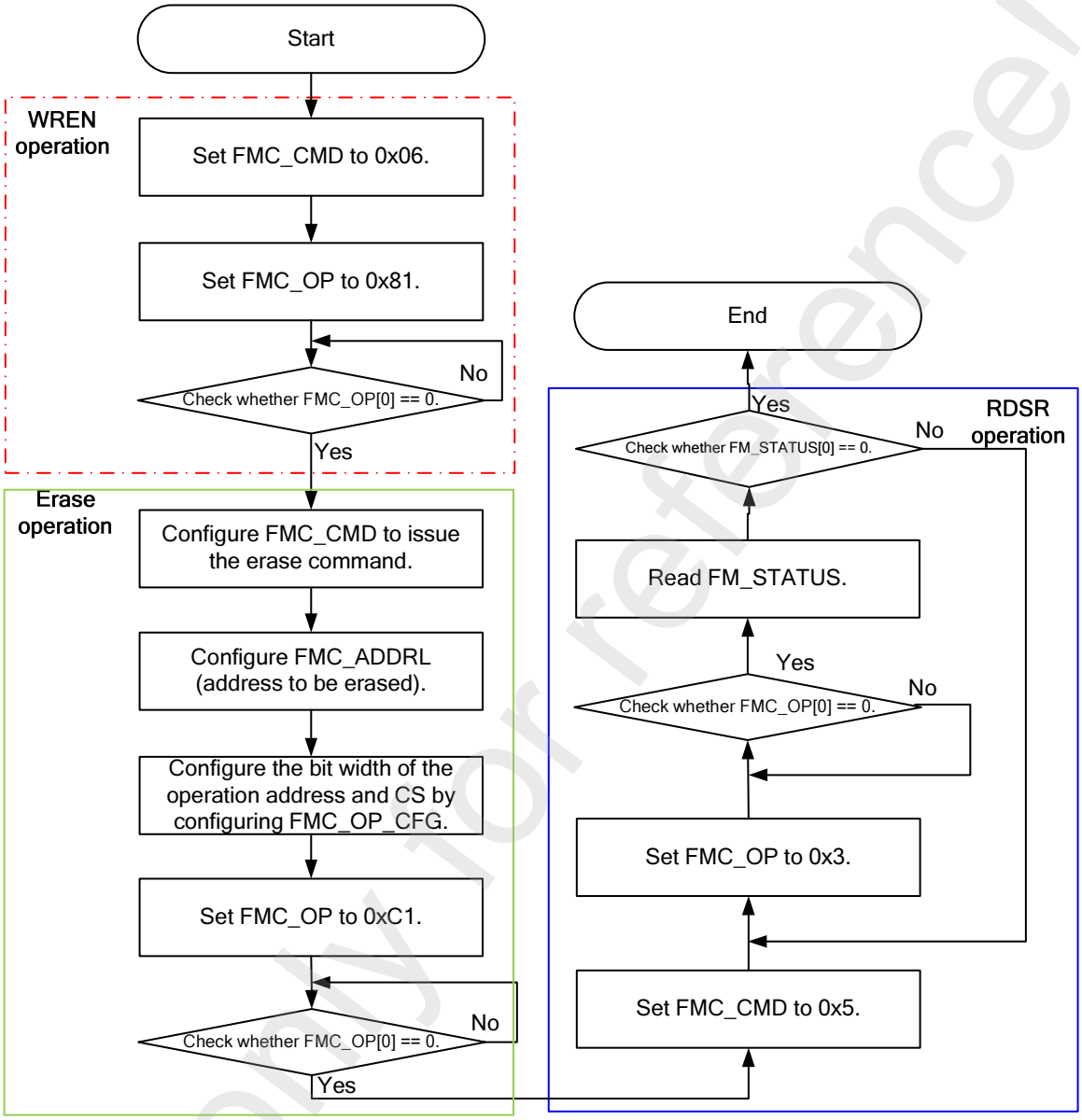
NOTE

For details about the command for changing the address mode of the SPI NOR flash, see the related flash manual.

4.2.4.5 Erase Operation Process (SPI NAND flash and SPI NOR flash)

The data in the flash memory must be erased before the program operation is performed. Note that the write enable (WREN) operation must be performed before the erase operation. Figure 4-14 shows an example of erase operation process in query mode.

Figure 4-14 Example of erase operation process



NOTE

- Figure 4-14 shows the erase operation process in query mode. If the interrupt mode is used, the operation of querying FMC_OP bit[0] is changed to interrupt handling. If FMC_INT[op_done] is detected, the operation is complete.
- During the erase operation, configure the erase instruction and operation address according to the manual of the corresponding flash.

4.2.4.6 Process of Reading Data in Internal DMA Mode (FMC_OP_CTRL Read Operation)

To read data in internal DMA mode, perform the following steps:

Step 1 Set FMC_CFG[op_mode] to 1 to ensure that the FMC is in normal mode.

Step 2 Configure the operation address of the flash memory by configuring FMC_ADDRL and FMC_ADDRH. For the SPI NOR flash, only FMC_ADDRL needs to be configured.

CAUTION

For the SPI NOR flash, the number of address cycles during the DMA operation is determined by FMC_CFG[spi_nor_addr_mode]. The 3-byte and 4-byte address modes are supported. For the SPI NAND flash, the FMC uses the 5-byte address mode by default and the address mode cannot be configured.

Step 3 Configure the start address for storing data in the DDR by configuring FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_OOB.

- For the SPI NOR flash, FMC_DMA_SADDR_OOB does not need to be configured.
- For the SPI NAND flash, if only the OOB is read, only FMC_DMA_SADDR_OOB needs to be configured.

CAUTION

- For the SPI NAND flash, the DDR address must be 4-byte-aligned.
- For the SPI NAND flash in ECC0 mode, the length configured in FMC_DMA_LEN must be 4-byte-aligned.

Step 4 Configure FMC_DMA_LEN. For the SPI NOR flash, FMC_DMA_LEN needs to be set to the length of the read data; for the SPI NAND flash in ECC0 mode, FMC_DMA_LEN needs to be set to the length of data in the spare area. This register does not need to be configured for other operations.

Step 5 Configure FMC_OP_CFG based on the requirements of the issued read command.

- For the SPI NAND flash and SPI NOR flash, FMC_OP_CFG[dummy_num] and FMC_OP_CFG[mem_if_type] need to be configured based on the number of dummy cycles in the read timings of the SPI flash and the SPI type.
- Configure FMC_OP_CFG[fm_cs] to select the CS to be operated.

Step 6 Set FMC_OP_CTRL[dma_op_ready] to 1 to issue the flash read command.

- Set FMC_OP_CTRL[rw_op] to 0 to select the DMA read operation.
- For the SPI NAND flash, if only the OOB is read, FMC_OP_CTRL[rd_op_sel] needs to be configured.
- Configure FMC_OP_CTRL[rd_opcode] based on the instruction of the flash read operation.

Step 7 Check whether the read operation is complete by querying FMC_OP_CTRL bit[0] in query mode and FMC_INT[op_done_int] in interrupt mode. If FMC_OP_CTRL bit[0] or FMC_INT[op_done_int] is 1, the read operation is complete, and data is written to the DDR.

----End

4.2.4.7 Process of Writing Data in Internal DMA Mode (FMC_OP_CTRL Write Operation)

To write data in internal DMA mode, perform the following steps:

Step 1 Set FMC_CFG[op_mode] to 1 to ensure that the FMC is in normal mode.

Step 2 Configure the operation address of the flash memory by configuring FMC_ADDRL and FMC_ADDRH. For the SPI NOR flash, only FMC_ADDRL needs to be configured.

CAUTION

For the SPI NOR flash, the number of address cycles during the DMA operation is determined by FMC_CFG[spi_nor_addr_mode]. The 3-byte and 4-byte address modes are supported. For the SPI NAND flash, the FMC uses the 5-byte address mode by default and the address mode cannot be configured.

Step 3 Configure the start address for transferring data from the DDR by configuring FMC_DMA_SADDR_D0 and FMC_DMA_SADDR_OOB. For the SPI NOR flash, FMC_DMA_SADDR_OOB does not need to be configured.

CAUTION

- For the SPI NAND flash, the DDR address must be 4-byte-aligned.
- For the SPI NAND flash in ECC0 mode, the length configured in FMC_DMA_LEN must be 4-byte-aligned.

Step 4 Configure FMC_DMA_LEN. For the SPI NOR flash, FMC_DMA_LEN needs to be set to the length of the read data; for the SPI NAND flash in ECC0 mode, FMC_DMA_LEN needs to be set to the length of data in the spare area. This register does not need to be configured for other operations.

Step 5 Configure FMC_OP_CFG based on the requirements of the issued write command.

- For the SPI NAND flash and NAND flash, configure FMC_OP_CFG[mem_if_type] based on the SPI required for the write and read operations.
- Configure FMC_OP_CFG[fm_cs] to select the CS to be operated.

Step 6 Configure FMC_OP_CTRL to issue corresponding commands.

- Set FMC_OP_CTRL[rw_op] to 1 to select the DMA write operation.
- For the SPI NAND flash and SPI NOR flash, configure FMC_OP_CTRL[wr_opcode] based on the instruction of the flash program operation.

Step 7 Check whether the write operation is complete by querying FMC_OP_CTRL bit[0] in query mode and FMC_INT[op_done_int] in interrupt mode. If FMC_OP_CTRL bit[0] is 0 or FMC_INT[op_done_int] is 1, the write operation is complete, and data is written to the flash memory.

----End

4.2.4.8 Notes

Note the following:

- You must reset the SPI NAND flash before use or after exceptions occur.
- You are advised not to configure registers when FMC_OP_CTRL [dma_op_ready] or FMC_OP [reg_op_start] is 1, indicating that the controller is performing an operation. Otherwise, the operation may become abnormal.
- Ensure that software configurations follow correct and appropriate rules; otherwise, the FMC may be suspended.

4.2.5 Data Structures (SPI NAND Flash)

When writing data to the flash memory in ECC mode, the FMC performs ECC encoding and data structure conversion on the data based on the ECC type. In ECC0 mode, the FMC does not change any written or read user data.

In ECC0 mode, the FMC transparently transmits data. During the write operation, the FMC directly writes the data in the buffer to the flash; during the read operation, the FMC directly writes the data read from the flash to the buffer.

In ECC mode, when the FMC performs the write operation, user data processing by the FMC involves ECC code generation and data reconstitution. The FMC implements ECC encoding in the internal buffer, generates the ECC code, and reconstitutes buffer data, and writes data to the flash. When the flash is read, the data processing by the FMC involves flash data reconstitution and ECC. The FMC reconstitutes data read from the flash, writes data to the internal buffer, and implements ECC in the buffer.

In non-ECC0 mode, data in the buffer and data in the flash have different structures. Table 4-8 describes the length of each data segment in various non-ECC0 modes.

Table 4-8 Data structure length in various non-ECC0 modes

ECC[a] (Bit)	ecc_len[b] (Byte)	Page_size (Byte)	oob_len[c] (Byte)	sec_len[d] (Byte)
4-bit/512 bytes (8/1 KB)	14	2048	30 + 2	1040
		4096		1032
8-bit/512 bytes (16/1 KB)	28	2048	6 + 2	1028
		4096	14 + 2	
24-bit/1 KB	42	2048	30 + 2	1040
		4096		1032
28-bit/1 KB	50	2048	30 + 2	1040
		4096		1032

a: The 4-bit/512 bytes mode is equivalent to the 8-bit/1 KB mode, and the 8-bit/512 bytes mode is equivalent to the 16-bit/1 KB mode.

b: **ecc_len** indicates the length of ECC code generated by each error correction unit.

c: **oob_len** indicates the length of the redundant area visible to the upper-layer software, which consists of the CTRL and BB.

d: **sec_len** indicates the length of the data area in each error correction unit. **sec_len** is calculated as follows: sec_len = 1024 + (oob_len x 1024)/Page_size

The following describes each data segment by taking the write operation as an example:

When the FMC writes data to the flash, data is consecutively stored in the format of data+ECC. However, special processing is required for the OOB data.

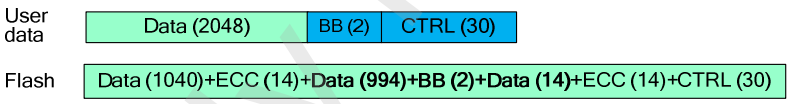
- The BB identity needs to be stored in the position of **page_size** on the flash page. That is, when the page size is 2 KB or 4 KB, the BB data is stored in the first two bytes of the 2048 or 4096 bytes. In this way, the storage of the original data or ECC data is affected.
- The CTRL data needs to be stored at the end of the valid data. Therefore, the storage format of the last data segment in the flash is data (excluding BB data and CTRL data)+ECC+CTRL.
- EB is the flag for marking the empty block and is usually stored in the last 2 bytes of the CTRL data.

4.2.5.2 8-Bit ECC Mode (8-Bit/1 KB)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 32 bytes. Figure 4-15 shows the structure of data in the buffer and flash.

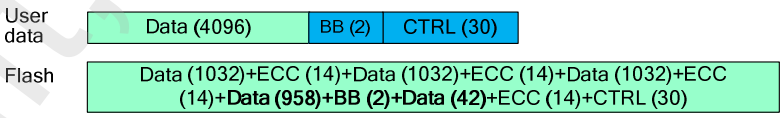
Figure 4-15 Data structure when the page size is 2 KB in 8-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 32 bytes. Figure 4-16 shows the structure of data in the buffer and flash.

Figure 4-16 Data structure when the page size is 4 KB in 8-bit ECC mode

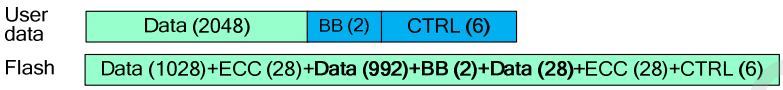


4.2.5.3 16-Bit ECC Mode (16-Bit/1 KB)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 8 bytes. Figure 4-17 shows the structure of data in the buffer and flash.

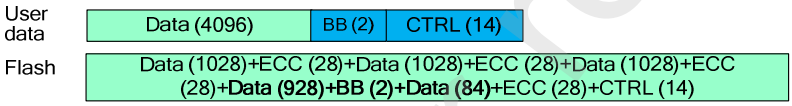
Figure 4-17 Data structure when the page size is 2 KB in 16-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 16 bytes. Figure 4-18 shows the structure of data in the buffer and flash.

Figure 4-18 Data structure when the page size is 4 KB in 16-bit ECC mode

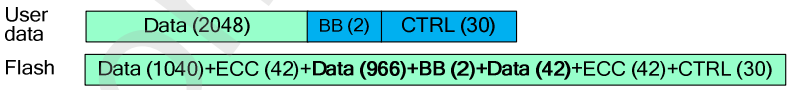


4.2.5.4 24-Bit ECC Mode (24-Bit/1 KB)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 32 bytes. Figure 4-19 shows the structure of data in the buffer and flash.

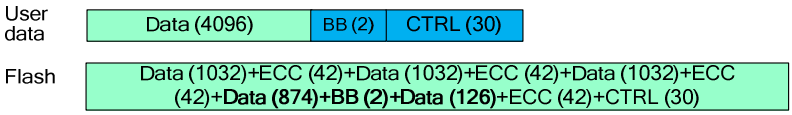
Figure 4-19 Data structure when the page size is 2 KB in 24-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 32 bytes. Figure 4-20 shows the structure of data in the buffer and flash.

Figure 4-20 Data structure when the page size is 4 KB in 24-bit ECC mode

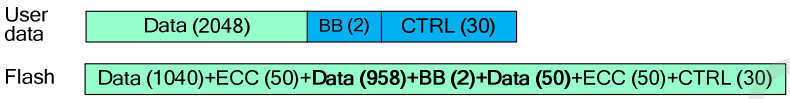


4.2.5.5 28-Bit ECC Mode (28-Bit/1 KB)

2 KB Page Size

When the page size is 2 KB, the size of the redundant area available to software is 32 bytes. Figure 4-21 shows the structure of data in the buffer and flash.

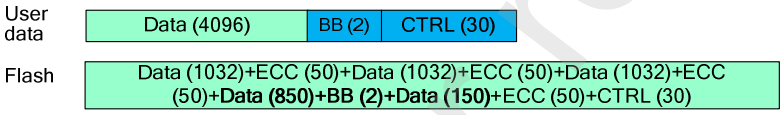
Figure 4-21 Data structure when the page size is 2 KB in 28-bit ECC mode



4 KB Page Size

When the page size is 4 KB, the size of the redundant area available to software is 32 bytes. Figure 4-22 shows the structure of data in the buffer and flash.

Figure 4-22 Data structure when the page size is 4 KB in 28-bit ECC mode



4.2.6 ECC Mode Selection

The recommended ECC performance of 1 bit/512 bytes, 4 bits/512 bytes, or 8 bits/512 bytes is provided in the component data sheet. The ECC performance of 8 bits/1 KB is equivalent to that of 4 bits/512 bytes. When you select the ECC mode for the controller, note the following:

- The priority of the ECC performance of the controller is higher than or equal to that of the recommended ECC performance.

  For example, if the recommended ECC performance is 1 bit/512 bytes or 4 bits/512 bytes, the controller can select the ECC mode with the performance of 8 bits/1 KB.

- The component page size must be greater than or equal to the required storage size of the ECC mode for the controller.

  For example, if the component page size is (2 KB + 64 bytes), the controller cannot select the ECC mode with the performance of 24 bits/1 KB because the required storage size of this ECC mode is (2 KB + 116 bytes). For details about the required storage size for the ECC mode, see section 4.2.5 "Data Structures (SPI NAND Flash)."

4.2.7 FMC Registers

Table 4-9 describes FMC registers.

Table 4-9 Summary of FMC registers (base address of 0x1000_0000)

Offset Address	Register	Description	Page
0x0000	FMC_CFG	Component configuration register	4-107
0x0004	GLOBAL_CFG	Global configuration register	4-108
0x0008	TIMING_SPI_CFG	SPI timing configuration register	4-110
0x0018	FMC_INT	Interrupt status register	4-111
0x001C	FMC_INT_EN	Interrupt enable register	4-112
0x0020	FMC_INT_CLR	Interrupt clear register	4-114
0x0024	FMC_CMD	Command word configuration register	4-114
0x0028	FMC_ADDRH	Upper-byte component address configuration register	4-115
0x002C	FMC_ADDRL	Lower-four-byte component address configuration register	4-115
0x0030	FMC_OP_CFG	Operation configuration register	4-116
0x0034	SPI_OP_ADDR	Operation address configuration register	4-116
0x0038	FMC_DATA_NUM	Data length register	4-117
0x003C	FMC_OP	Operation register	4-117
0x0040	FMC_DMA_LEN	DMA operation length register	4-119
0x0048	FMC_DMA_AHB_CTRL	DMA AHB bus control register	4-119
0x004C	FMC_DMA_SADDR_D0	DDR start address register 0 for DMA operations	4-120
0x005C	FMC_DMA_SADDR_OOB	DDR OOB information storage start address register for DMA operations	4-120
0x0068	FMC_OP_CTRL	DMA operation control register	4-121
0x006C	FMC_TIMEOUT_WR	Write operation timeout register	4-121
0x0070	FMC_OP_PARA	OP operation parameter selection register	4-122
0x0074	FMC_BOOT_SET	Boot setting register	4-122
0x0078	FMC_LP_CTRL	Low-power control register	4-123
0x00A8	FMC_ERR_THD	ECC alarm threshold register	4-124
0x00AC	FMC_FLASH_INFO	Component status register	4-125

Offset Address	Register	Description	Page
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0x00C0	FMC_ERR_NUM0_BUF0	SPI NAND flash error correction information 0 statistics register for the first buffer operation	4-125
0x00D0	FMC_ERR_ALARM_ADDRH	Upper-byte ECC alarm flash address register	4-126
0x00D4	FMC_ERR_ALARM_ADDRL	Lower-byte ECC alarm flash address register	4-126
0x00D8	FMC_ECC_INVALID_ADDRH	Upper-byte ECC uncorrectable address register	4-127
0x00DC	FMC_ECC_INVALID_ADDRL	Lower-four-byte ECC uncorrectable address register	4-127

4.2.8 Register Description

FMC_CFG

FMC_CFG is a component configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	FMC_CFG	0x0000_1820

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				spi_nand_sel		spi_nor_addr_mode		block_size			ecc_type			page_size			flash_sel			op_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:11]	RW	spi_nand_sel	Enable for the address bit of the SPI NAND flash plane 11: enabled Other values: disabled
[10]	RW	spi_nor_addr_mode	SPI address mode (valid only for the SPI NOR flash) 0 (default): 3-byte address mode 1: 4-byte address mode The reset value depends on the pin.

[9:8]	RW	block_size	Block size of the SPI NAND flash 00: 64 pages 01: 128 pages Other values: reserved
[7:5]	RW	ecc_type	ECC type of the controller 000: no ECC 001: 8-bit ECC 010: 16-bit ECC 011: 24-bit ECC 100: 28-bit ECC Other values: reserved
[4:3]	RW	page_size	Page size of the SPI NAND/NAND flash 00: 2 KB page_size 01: 4 KB page_size 10: reserved 11: reserved
[2:1]	RW	flash_sel	Flash type select 00: SPI NOR flash 01: SPI NAND flash 10: reserved 11: reserved The reset value depends on the pin.
[0]	RW	op_mode	FMC operation mode 0: BOOT mode 1: NORMAL mode

GLOBAL_CFG

GLOBAL_CFG is a global configuration register.

Offset Address	Register Name	Total Reset Value
0x0004	GLOBAL_CFG	0x0000_00C4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sample_point				ddr_mode	reserved							wp_en	rd_delay			reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	sample_point	Sampling point select based on the delay parameter of the component in DDR mode. The frequency of the sampling clock is four times that of the interface read/write clock. The delay is the lowest when the field value is 0x0, and highest when the field value is 0xB. 0x0: The sampling point is 2 sampling clock cycles after the valid edge. 0x1: The sampling point is 2.5 sampling clock cycles after the valid edge. 0x2: The sampling point is 3 sampling clock cycles after the valid edge. 0x3: The sampling point is 3.5 sampling clock cycles after the valid edge. 0x4: The sampling point is 4 sampling clock cycles after the valid edge. 0x5: The sampling point is 4.5 sampling clock cycles after the valid edge. 0x6: The sampling point is 5 sampling clock cycles after the valid edge. 0x7: The sampling point is 5.5 sampling clock cycles after the valid edge. 0x8: The sampling point is 6 sampling clock cycles after the valid edge. 0x9: The sampling point is 6.5 sampling clock cycles after the valid edge. 0xA: The sampling point is 7 sampling clock cycles after the valid edge. 0xB: The sampling point is 7.5 sampling clock cycles after the valid edge.

[11]	RW	ddr_mode	DDR mode enable 0: normal SDR mode 1: DDR mode
[10:7]	RO	reserved	Reserved
[6]	RW	wp_en	Write protection enable for the WP pin. When this bit is enabled, the chip outputs 0 to the WP pin. 0: disabled 1: enabled
[5:3]	RW	rd_delay	Number of delayed cycles (of the component working clock) for reading data from the SPI flash (in SDR mode) 000 (default): no delay 001: 0.5 cycle 010: 1 cycle 011: 1.5 cycles 100: 2 cycles 101: 2.5 cycles 110: 3 cycles 111: 3.5 cycles
[2:0]	RO	reserved	Reserved

TIMING_SPI_CFG

TIMING_SPI_CFG is an SPI timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	TIMING_SPI_CFG	0x0000_006F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				tcsh				tcss				tshsl			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	tcss	CS setup time 0x0~0x7: (n + 1) interface clock cycles (n = 0, 1, 2, …, 7)
[3:0]	RW	tshsl	CS deselect time. It is equal to the interval between two flash operations. 0x0~0xF: (n + 1) interface clock cycles (n = 0, 1, 2, …, 15)

FMC_INT

FMC_INT is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0018	FMC_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							reserved	ahb_op_int	wr_lock_int	dma_err_int	err_alarm_int	err_inval_int	err_val_int	op_fail_int	op_done_int
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	reserved	Reserved
[7]	RO	ahb_op_int	CPU read/write internal buffer interrupt enable when the FMC is reading/writing data from/to the flash memory 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	wr_lock_int	Lock address write operation interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	dma_err_int	DMA transfer bus error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	err_alarm_int	ECC alarm interrupt. An interrupt is generated when the number of error bits reaches the preset threshold. 0: No interrupt is generated. 1: An interrupt is generated.

[3]	RO	err_inval_int	Uncorrectable ECC error interrupt In 8-bit ECC mode, if errors occur in eight or more bits of the checked 1024-byte data, an interrupt is generated. In 16-bit ECC mode, if errors occur in 16 or more bits of the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if errors occur in 24 or more bits of the checked 1024-byte data, an interrupt is generated. In 28-bit ECC mode, if errors occur in 28 or more bits of the checked 1024-byte data, an interrupt is generated. In 40-bit ECC mode, if errors occur in 40 or more bits of the checked 1024-byte data, an interrupt is generated. In 64-bit ECC mode, if errors occur in 64 or more bits of the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	err_val_int	Correctable ECC error interrupt In 8-bit ECC mode, if errors occur in one to eight bits of the checked 1024-byte data, an interrupt is generated. In 16-bit ECC mode, if errors occur in one to 16 bits of the checked 1024-byte data, an interrupt is generated. In 24-bit ECC mode, if errors occur in one to 24 bits of the checked 1024-byte data, an interrupt is generated. In 28-bit ECC mode, if errors occur in one to 28 bits of the checked 1024-byte data, an interrupt is generated. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	op_fail_int	Programming (timeout) failure interrupt in DMA mode 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	op_done_int	Current controller operation completion interrupt. This bit is automatically cleared when the operation register is written. 0: No interrupt is generated. 1: An interrupt is generated.

FMC_INT_EN

FMC_INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x001C	FMC_INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							reserved	ahb_op_int_en	wr_lock_int_en	dma_err_int_en	err_alarm_int_en	err_inval_int_en	err_val_int_en	op_fail_int_en	op_done_int_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	reserved	Reserved
[7]	RW	ahb_op_int_en	CPU read/write internal buffer error interrupt enable when the FMC is reading/writing data from/to the flash memory 0: disabled 1: enabled
[6]	RW	wr_lock_int_en	Lock address write error interrupt enable 0: disabled 1: enabled
[5]	RW	dma_err_int_en	DMA transfer bus error interrupt enable 0: disabled 1: enabled
[4]	RW	err_alarm_int_en	ECC alarm interrupt enable. An interrupt is generated when the number of error bits reaches the threshold. 0: disabled 1: enabled
[3]	RW	err_inval_int_en	ECC uncorrectable error interrupt enable 0: disabled 1: enabled
[2]	RW	err_val_int_en	ECC correctable error interrupt enable 0: disabled 1: enabled
[1]	RW	op_fail_int_en	Programming operation failure interrupt enable 0: disabled 1: enabled

[0]	RW	op_done_int_en	Current operation completion interrupt enable of the FMC 0: disabled 1: enabled

FMC_INT_CLR

FMC_INT_CLR is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0020	FMC_INT_CLR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6	5	4	3	2	1	0
Name	reserved						ahb_op_int_clr	wr_lock_int_clr	dma_err_int_clr	err_alarm_int_clr	err_inval_int_clr	err_val_int_clr	op_fail_int_clr	op_done_int_clr
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	WC	ahb_op_int_clr	ahb_op_err interrupt clear. Writing 1 clears the interrupt.
[6]	WO	wr_lock_int_clr	wr_lock_err interrupt clear. Writing 1 clears the interrupt.
[5]	WC	dma_err_int_clr	DMA transfer bus error interrupt clear. Writing 1 clears the interrupt.
[4]	WC	err_alarm_int_clr	err_alarm interrupt clear. Writing 1 clears the interrupt.
[3]	WC	err_inval_int_clr	err_invalid interrupt clear. Writing 1 clears the interrupt.
[2]	WC	err_val_int_clr	err_valid interrupt clear. Writing 1 clears the interrupt.
[1]	WC	op_fail_int_clr	op_fail interrupt clear. Writing 1 clears the interrupt.
[0]	WC	op_done_int_clr	op_done interrupt clear. Writing 1 clears the interrupt.

FMC_CMD

FMC_CMD is a command word configuration register.

Offset Address	Register Name	Total Reset Value
0x0024	FMC_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								cmd1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	cmd1	First command sent to the NAND/SPI NOR/SPI NAND flash by the FMC

FMC_ADDRH

FMC_ADDRH is an upper-byte component address configuration register.

Offset Address	Register Name	Total Reset Value
0x0028	FMC_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	addrh	Upper bytes of the operation address for the SPI NAND flash

FMC_ADDRL

FMC_ADDRL is a lower-four-byte component address configuration register.

Offset Address	Register Name	Total Reset Value
0x002C	FMC_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	addrl	Lower four bytes of the operation address for the flash (component address for the SPI NOR flash)

FMC_OP_CFG

FMC_OP_CFG is an operation configuration register.

Offset Address	Register Name	Total Reset Value
0x0030	FMC_OP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				fm_cs	force_cs_en	mem_if_type			addr_num			dummy_num			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11]	RW	fm_cs	CS corresponding to the flash to be operated 0: CS0 1: reserved
[10]	RW	force_cs_en	CS forced enable. 0: disabled 1: enabled
[9:7]	RW	mem_if_type	SPI flash interface type select (read operation) 000: standard SPI 001: dual-Input/Dual-output/SPI 010: dual I/O SPI 011: quad-Input/Dual-output/ SPI 100: quad I/O SPI 101−111: reserved
[6:4]	RW	addr_num	Number of bytes of the address sent to the flash
[3:0]	RW	dummy_num	Number of bytes to be operated for dummy_en (one byte is equivalent to two clock cycles in 4-wire mode, four clock cycles in 2-wire mode, or eight clock cycles in 1-wire mode)

SPI_OP_ADDR

SPI_OP_ADDR is an operation address configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	SPI_OP_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_op_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	spi_op_addr	Operation address of the SPI NOR/NAND flash. The operation address of the SPI flash is issued for each operation. This address is different from that described in FMC_ADDRL and FMC_ADDRH.

FMC_DATA_NUM

FMC_DATA_NUM is a data length register.

Offset Address	Register Name	Total Reset Value
0x0038	FMC_DATA_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				op_data_num											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	op_data_num	Length of data to be processed during one operation. This register needs to be configured when there is data transmission and does not need to be configured for the DMA operations and AHB direct access. This register is valid only in ECC0 mode.

FMC_OP

FMC_OP is an operation register.

Offset Address	Register Name	Total Reset Value
0x003C	FMC_OP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							dummy_en	cmd1_en	addr_en	write_data_en	reserved			read_data_en	read_status_en	reg_op_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	dummy_en	Dummy byte transfer enable after the address operation is enabled 0: disabled 1: enabled
[7]	RW	cmd1_en	Enable for transmitting command 1 to the flash 0: disabled 1: enabled
[6]	RW	addr_en	Enable for writing the operation address to the flash 0: disabled 1: enabled
[5]	RW	write_data_en	Enable for writing data to the flash 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.
[4:3]	RO	reserved	Reserved
[2]	RW	read_data_en	Enable for reading data from the flash 0: disabled 1: enabled Note: read_data_en and write_data_en cannot be 1 at the same time.
[1]	RW	read_status_en	This bit is separately set to 1, indicating that the get feature command sequence starts to be sent to the SPI NAND flash and data is read to FMC_FLASH_INFO.flash_status. 0: disabled 1: enabled

[0]	RWSC	reg_op_start	Operation issue work enable 0: The controller is ready. The software can set it only to 1 to enable the logic. 1: The controller is busy. The logic can set it only to 0, indicating that the logic is complete.

FMC_DMA_LEN

FMC_DMA_LEN is a DMA operation length register.

Offset Address	Register Name	Total Reset Value
0x0040	FMC_DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				dma_len																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:0]	RW	dma_len	Data transfer length during DMA operations (in byte) This field is used to configure the length of data in the spare data in ECC0 mode for the SPI NAND flash. This field is used to configure the length of data required for the DMA read/write operation of the SPI NOR flash.

FMC_DMA_AHB_CTRL

FMC_DMA_AHB_CTRL is a DMA AHB control register.

Offset Address	Register Name	Total Reset Value
0x0048	FMC_DMA_AHB_CTRL	0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													burst16_en	burst8_en	burst4_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved

[2]	RW	burst16_en	Burst16 enable 0: disabled 1: enabled
[1]	RW	burst8_en	Burst8 enable 0: disabled 1: enabled
[0]	RW	burst4_en	Burst4 enable 0: disabled 1: enabled

FMC_DMA_SADDR_D0

FMC_DMA_SADDR_D0 is DDR start address register 0 for DMA operations.

Offset Address	Register Name	Total Reset Value
0x004C	FMC_DMA_SADDR_D0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_d0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_d0	For the SPI NOR flash, this register indicates the DDR start address for DMA operations. For the SPI NAND flash, this register indicates the base address of DDR operation data for DMA operations.

FMC_DMA_SADDR_OOB

FMC_DMA_SADDR_OOB is a DDR OOB information storage start address register for DMA operations.

Offset Address	Register Name	Total Reset Value
0x005C	FMC_DMA_SADDR_OOB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_mem_saddr_oob																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_mem_saddr_oob	DDR base address for the OOB area that stores the data to be read or written

FMC_OP_CTRL

FMC_OP_CTRL is a DMA operation control register.

Offset Address	Register Name	Total Reset Value
0x0068	FMC_OP_CTRL	0x0003_0200

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6	5 4	3 2	1	0
Name	reserved		rd_opcode		wr_opcode		reserved	rd_op_sel	reserved	rw_op	dma_op_ready
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1	0 0 0 0	0 0 1 0	0 0	0 0	0 0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	rd_opcode	SPI NAND/SPI NOR flash, DMA read command, non-bus mode (FAST_READ/READ/DUAL_READ)
[15:8]	RW	wr_opcode	SPI NAND/SPI NOR flash, DMA write command
[7:6]	RO	reserved	Reserved
[5:4]	RW	rd_op_sel	Area of data to be read 00: Data on the entire page is read. 01: Only the OOB data is read. Other values: reserved
[3:2]	RO	reserved	Reserved
[1]	RW	rw_op	Operation type 0: DMA read 1: DMA write
[0]	RWSC	dma_op_ready	Logic operation issue enable 0: The controller is ready. (The controller automatically sets it to 0.) 1: The controller is busy. (It is set to 1 by software.) This bit is set to 1 when the software issues the operation, and it is automatically set to 0 after the controller completes the operation. The software can set it to 1 but not 0.

FMC_TIMEOUT_WR

FMC_TIMEOUT_WR is a write operation timeout register.

Offset Address	Register Name	Total Reset Value
0x006C	FMC_TIMEOUT_WR	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								timeout_wr																							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	timeout_wr	Program operation busy wait time, timeout period. The timeout period is in the unit of one interface clock cycle for the SPI NAND/SPI NOR flash.

FMC_OP_PARA

FMC_OP_PARA is an OP operation parameter selection register.

Offset Address	Register Name	Total Reset Value
0x0070	FMC_OP_PARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														rd_oob_only	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	rd_oob_only	Only the sector that stores the OOB information is read when the flash read command is issued. 0: Read the page. 1: Read only the OOB data.
[0]	RO	reserved	Reserved

FMC_BOOT_SET

FMC_BOOT_SET is a boot setting register.

Offset Address	Register Name	Total Reset Value
0x0074	FMC_BOOT_SET	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											boot_otp_cfg	device_ecc_sel	reserved	boot_quad_mode	boot_page0_cfg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	boot_otp_cfg	Component configuration information, that is, the mode in which the fmc_cfg register is configured 0: adaptive boot mode 1: OTP mode
[3]	RW	device_ecc_sel	Whether to use the internal ECC for the SPI NAND flash 0: no 1: yes
[2]	RO	reserved	Reserved
[1]	RW	boot_quad_mode	Whether to use the 4-wire boot mode for the SPI NAND flash. The reset value depends on the SFC_EMMC_BOOT_MODE pin. 0: no. The 1-wire boot mode is used. 1: yes
[0]	RW	boot_page0_cfg	Boot mode 0: default boot mode 1: boot mode that does not require the pin

FMC_LP_CTRL

FMC_LP_CTRL is a low-power control register.

Offset Address	Register Name	Total Reset Value
0x0078	FMC_LP_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															clk_gate_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	clk_gate_en	Clock gating select. If the clock gating is enabled, the low-power design is used and the module working clocks are disabled by logic. 0: All clocks are enabled. 1: Clocks are disabled according to the low-power design.

FMC_ERR_THD

FMC_ERR_THD is an ECC alarm threshold register.

Offset Address	Register Name	Total Reset Value
0x00A8	FMC_ERR_THD	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_err_thd							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	fmc_err_thd	ECC alarm threshold. When the number of error bits reaches the threshold, an ECC alarm interrupt is triggered. NOTE • If an uncorrectable ECC error occurs, an uncorrectable interrupt is reported regardless of the register value. • When the register value is set to 0 or 1, an alarm interrupt is reported as long as an error occurs. • When the configured value exceeds the number of correctable error bits, no alarm interrupt is reported regardless of the number of error bits. Only the correctable error interrupt and uncorrectable error interrupt are generated.

FMC_FLASH_INFO

FMC_FLASH_INFO is a component status register.

Offset Address	Register Name	Total Reset Value
0x00AC	FMC_FLASH_INFO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	exp_bb_flag								bb_flag								exp_flash_status								flash_status							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	exp_bb_flag	Uncorrected data corresponding to the bad block flag of the current page when the extended operation of reading only the OOB data or reading the page is issued
[23:16]	RO	bb_flag	Uncorrected data corresponding to the bad block flag of the current page when the only the OOB data or the page is read
[15:8]	RO	exp_flash_status	Status register value read by the FMC from the flash during extended operations
[7:0]	RO	flash_status	Read status register. For details about the meanings of bits 7−0, see the flash component manual.

FMC_VERSION

FMC_VERSION is a version register.

Offset Address	Register Name	Total Reset Value
0x00BC	FMC_VERSION	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	FMC V100

FMC_ERR_NUM0_BUF0

FMC_ERR_NUM0_BUF0 is an SPI NAND flash error correction information 0 statistics register for the first buffer operation.

Offset Address	Register Name	Total Reset Value
0x00C0	FMC_ERR_NUM0_BUF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	err_num0_buf0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	err_num0_buf0	Error bit count for the first 4 KB data during the first buffer operation of the NAND flash with the page size of 2 KB, 4 KB, 8 KB, or 16 KB bit[31:24]: number of error bits in the fourth 1 KB data segment bit[23:16]: number of error bits in the third 1 KB data segment bit[15:8]: number of error bits in the second 1 KB data segment bit[7:0]: number of error bits in the first 1 KB data segment

FMC_ERR_ALARM_ADDRH

FMC_ERR_ALARM_ADDRH is an upper-byte ECC alarm flash address register.

Offset Address	Register Name	Total Reset Value
0x00D0	FMC_ERR_ALARM_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_err_alarm_addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	fmc_err_alarm_addrh	Upper bytes of the operation address of the flash that triggers the last interrupt when an ECC alarm interrupt is generated

FMC_ERR_ALARM_ADDRL

FMC_ERR_ALARM_ADDRL is a lower-byte ECC alarm flash address register.

Offset Address	Register Name	Total Reset Value
0x00D4	FMC_ERR_ALARM_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fmc_err_alarm_addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fmc_err_alarm_addrl	Lower-four-byte of the operation address of the flash that triggers the last interrupt when an ECC alarm interrupt is generated

FMC_ECC_INVALID_ADDRH

FMC_ECC_INVALID_ADDRH is an upper-byte ECC uncorrectable address register.

Offset Address	Register Name	Total Reset Value
0x00D8	FMC_ECC_INVALID_ADDRH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fmc_ecc_invalid_addrh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	fmc_ecc_invalid_addrh	Upper bytes of the operation address of the flash that triggers the last interrupt when an uncorrectable ECC error occurs

FMC_ECC_INVALID_ADDRL

FMC_ECC_INVALID_ADDRL is a lower-four-byte ECC uncorrectable address register.

Offset Address	Register Name	Total Reset Value
0x00DC	FMC_ECC_INVALID_ADDRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fmc_ecc_invalid_addrl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fmc_ecc_invalid_addrl	Lower-four-byte of the operation address of the flash that triggers the last interrupt when an uncorrectable ECC error occurs

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5 ETH

5.1 Overview

The Ethernet (ETH) module provides an ETH module interface that is used to receive data or transmit data through the network interface at a speed of 10 Mbit/s or 100 Mbit/s. This module also supports half-duplex or full-duplex operating mode and provides the reduced media-independent interface (RMII). With the eight configurable DMAC address filter tables, the ETH module filters input frames received through the network interface, limiting the traffic of the CPU port to protect the CPU against heavy traffic.

5.2 Function Description

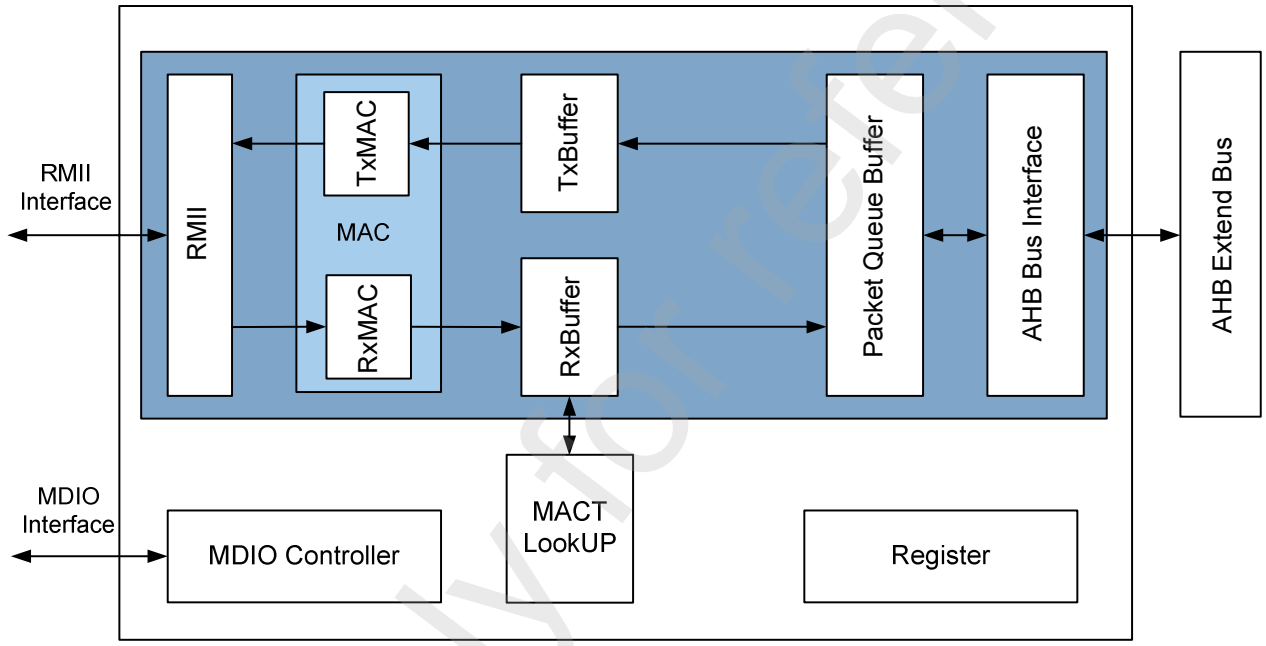
The ETH module has the following features:

- Supports one ETH module interface.
- Supports the rate of 10 Mbit/s or 100 Mbit/s.
- Supports full-duplex or half-duplex operating mode.
- Supports the RMII.
- Supports collision back-off and retransmission and late collision in half-duplex mode.
- Supports the transmission of flow control frames in full-duplex mode.
- Supports detection of frame length validity and the discarding of extra-long and extra-short frames.
- Implements cyclic redundancy check (CRC) on the input frames. The frames with CRC errors are discarded.
- Implements CRC check on the output frames
- Supports short-frame stuffing.
- Supports the loopback to external in full-duplex mode.
- Supports adaptation.
- Provides the management data input/output (MDIO) interfaces with configurable frequency.
- Provides 64 frame management queues for both data receive (RX) and data transmit (TX).
- Provides traffic limit to prevent the CPU against traffic attack.
- Supports the count of received frames and transmitted frames.

- Supports eight configurable DMAC address filter tables.
- Controls whether to forward or discard broadcast frames, multicast frames, and unicast frames.
- Supports the scatter gather (SG) function.
- Supports the checksum offload engine (COE) check and offload engine functions in the RX and TX directions.
- Supports Transmission Control Protocol (TCP) segmentation offload (TSO).
- Supports User Datagram Protocol (UDP) fragmentation offload (UFO).

Figure 5-1 shows the logic block diagram of the ETH module.

Figure 5-1 Logic block diagram of the ETH module



5.3 Signal Description

Table 5-1 and Table 5-2 list signals of the ETH interface.

Table 5-1 MDIO interface signals

Signal	Direction	Description	Pin
MDCK	O	Clock output of MDIO interface	MDCK
MDIO	I/O	Input/output signal of the MDIO interface	MDIO

Table 5-2 MII interface signals

Signal	Direction	Description	Pin
RMII_REF_CLK	I/O	Uplink RMII reference clock	RMII_CLK
RMII_TXD[1:0]	O	RMII TX data	RMII_TXD1−RMII_TXD0
RMII_TXEN	O	RMII TX data valid	RMII_TX_EN
RMII_RXD[1:0]	I	RMII RX data	RMII_RXD1−RMII_RXD0
RMII_CRS_DV	I	RMII RX data valid	RMII_RX_DV

5.4 Operating Mode

5.4.1 Process of Receiving Frames

During initialization, software needs to perform the following operations:

- Software needs to request a certain number of buffers. The number is equal to the RX queue depths and the size of each buffer is 2 KB. Then, software writes the header addresses of the buffers to the frame RX queue one by one. The times of the write operation is equal to the configured RX queue depth.
- The configured buffers should not be released during frame receiving. If the configured header address is not a word aligned address, the byte address corresponding to the header address must be a writable address.

The CPU performs the following steps when it is informed that a frame needs to be received:

Step 1 Read the frame descriptor (including the start address and frame length of the RX frame) in the register UD_GLB_IQFRM_DES.

Step 2 Process the data and write 1 to clear GLB_IRQ_RAW[iraw_rx_up] (indicating that the CPU completes the frame receiving).

----End

After receiving a frame of data, software needs to re-apply for a buffer of 2 KB and re-write the header address to the frame descriptor of the current RX queue. Otherwise, the available depth of RX queues equals to the number of buffers assigned to the CPU rather than the value configured by the CPU.

Table 5-3 describes the data structure of the frame descriptor received by the CPU.

Table 5-3 Data structure of the frame descriptor received by the CPU

Bits	Name	Description
[63:32]	rxfrm_saddr	Start address for receiving frames.

Bits	Name	Description
[31:18]	reserved	Reserved.
[17:12]	fd_in_addr	Relative address of the frame to be received in the input queue (IQ). It serves as the index (0 to iq_len - 1) of the absolute addresses for storing frames.
[11:0]	fd_in_len	Length of the frame to be received in the IQ.

NOTE

The length of the RX queue can be obtained by querying UD_GLB_ADDRQ_STAT.

The CPU can receive a frame in interrupt or query mode.

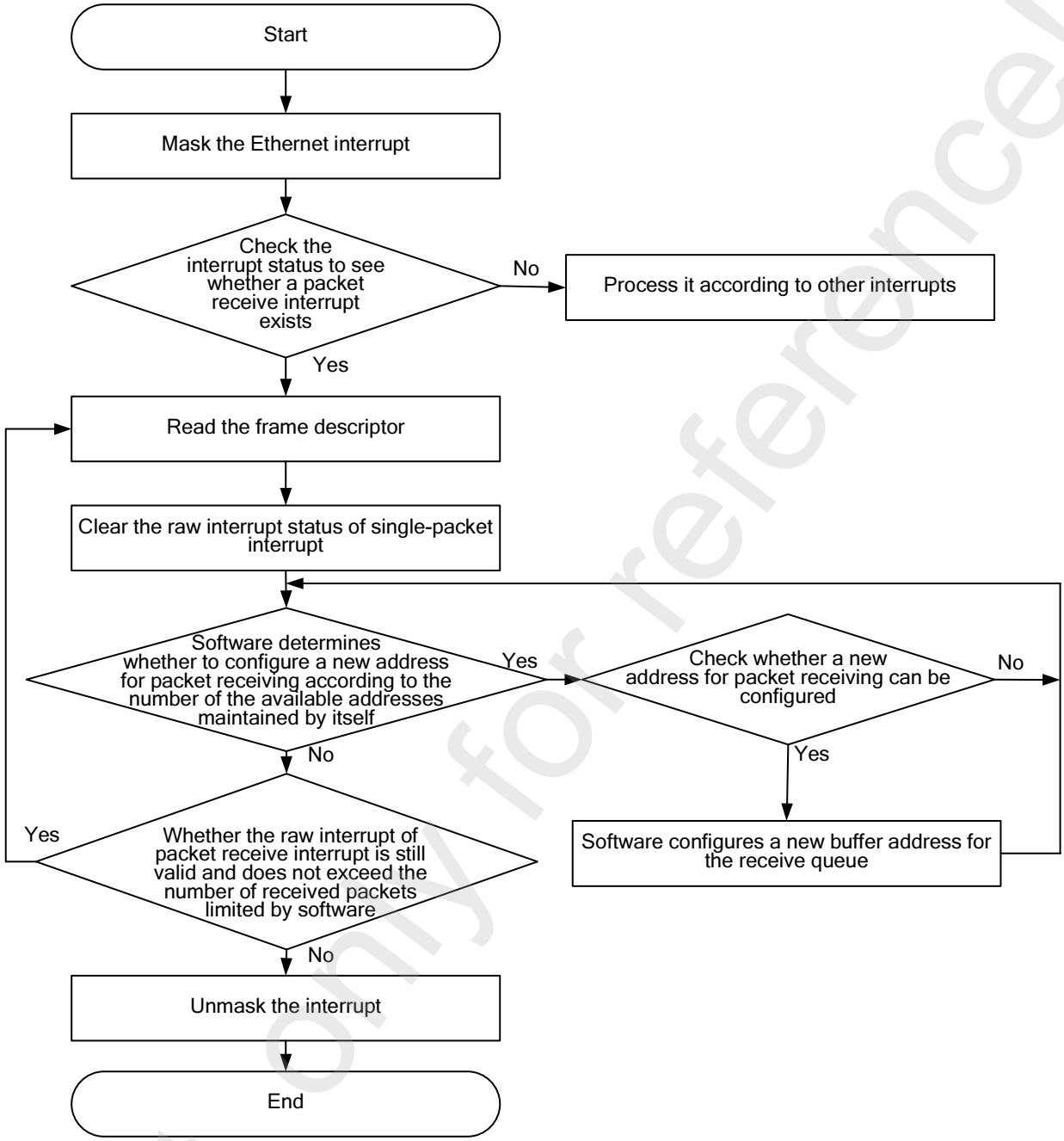
1. Receiving a frame in interrupt mode

   When the CPU enables the frame RX interrupt, depending on the frames to be received, hardware generates frame RX interrupts (single-packet interrupt and multi-packet interrupt) int_rx_up and int_rxd_up.

   int_rx_up indicates that an interrupt is reported each time a packet is received.

   int_rxd_up indicates that an interrupt is reported each time a number of specified packets are received. Figure 5-2 shows the process of receiving a frame in interrupt mode.

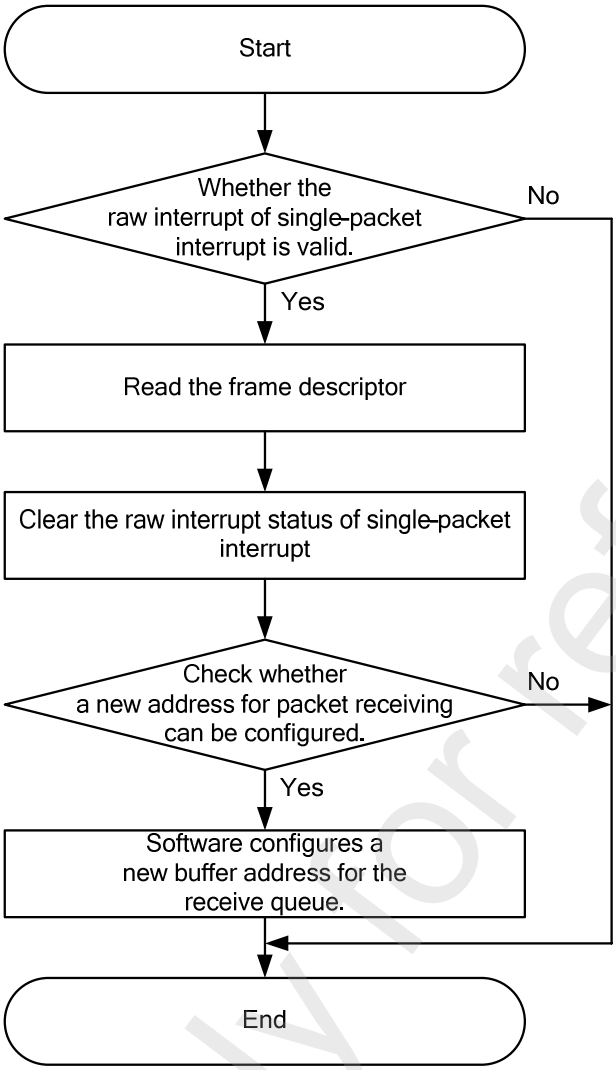
Figure 5-2 Process of receiving a frame in interrupt mode



2. Receiving a frame in query mode

   In this mode, the CPU does not enable the frame RX interrupt bit, namely, GLB_IRQ_ENA[ien_rx_up], but automatically queries GLB_IRQ_RAW[iraw_rx_up]. If GLB_IRQ_RAW[iraw_rx_up] is 1, it indicates that there is a frame to be received by the CPU. Figure 5-3 shows the process of receiving a frame in query mode.

Figure 5-3 Process of receiving a frame in query mode



5.4.2 Process of Transmitting a Frame

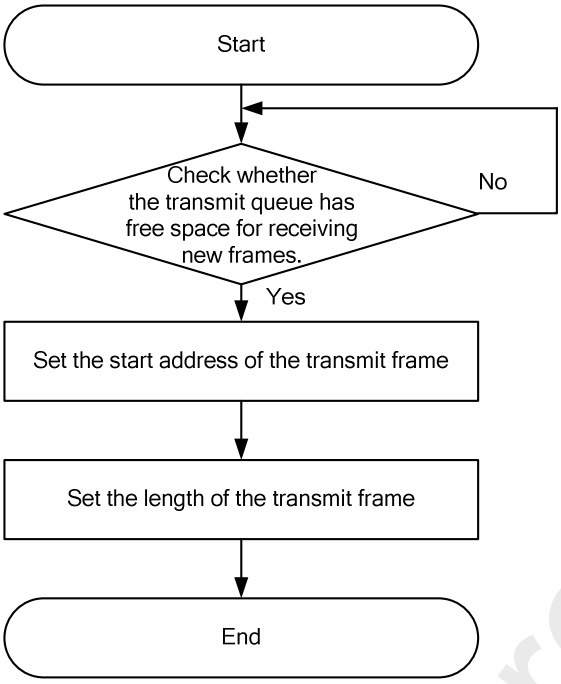
When a frame is transmitted, the CPU checks whether the current queue has any available space. If the space is sufficient, the CPU writes the header address of the buffer and then the length of the TX frame to the frame descriptor of the TX queue. The frame length trigger hardware for writing the TX frame writes the header address and frame length of the TX frame to the TX queue. Each time after a write is performed on the register, a data packet is transmitted. Therefore, software must control the write to the frame length register so that the frame length register is not written arbitrarily.

The frame format is as follows:

Destination MAC	Source MAC	Type	Data	FCS

Figure 5-4 shows the process of transmitting a frame by the CPU.

Figure 5-4 Process of transmitting a frame by the CPU



When the frame transmitted by the CPU is buffered in the SDRAM, the frame descriptor is not included. The frame descriptor is written to UD_GLB_EQ_ADDR and UD_GLB_EQFRM_LEN to notify the ETH module of adding the frame (descriptor) to the queue. Table 5-4 describes the data structure of the frame descriptor transmitted by the CPU.

Table 5-4 Data structure of the frame descriptor transmitted by the CPU

Bits	Name	Description
[63:32]	start_addr_eq	Header address of a frame to be transmitted
[31]	tso_flag	Whether to implement TSO 0: no 1: yes
[30]	vlan_flag	Whether the current packet has the virtual local area network (VLAN) flag 0: no 1: yes
[29]	ip_version	IP protocol version of the current packet 0: IPv4 1: IPv6
[28]	protocol_type	Transport layer protocol type of the current packet 0: TCP 1: UDP

Bits	Name	Description
[27]	tx_coe_flag	Whether to implement COE in the TX direction 0: no 1: yes
[26]	sg_flag	Whether to implement SG 0: no 1: yes
[25:24]	reserved	Reserved
[23:20]	ip_hdr_len	IP header length of the current packet, in the unit of word (four bytes) The IP header length is 5−15 words for an IPv4 packet and 10 words for an IPv6 packet.
[19:16]	protocol_hdr_len	TCP header length for a TCP packet, in the unit of word (four bytes), ranging from 5 words to 15 words; UDP header length for a UDP packet, in the unit of word (four bytes), 2 words
[15:11]	nfrags_num	Number of nfrags in the SKB of the current descriptor indicator. The maximum number is 16.
[10:0]	length	Maximum segment size (MSS) of the packet slice for the TSO packet, or total frame length for the SG or bypass packet

Note: The frames whose **length** is less than 20 bytes or greater than 1,900 bytes are discarded. In other words, the allowed range is from 20 bytes to 1900 bytes.

NOTE
The usage of the TX queues for the current CPU can be obtained by querying UD_GLB_ADDRQ_STAT.

The CPU can transmit a frame in interrupt or query mode.

1. Transmitting a frame in interrupt mode

   The CPU enables the nonempty-to-empty interrupt (int_freeeq_up) of the TX queue of the ETH module and allows the interrupt to be notified to the CPU. If the TX queue of the ETH module changes from nonempty to empty, it indicates the ETH module can transmit a frame. Then, hardware generates an interrupt to notify the CPU of transmitting the frame.

   If software needs to transmit a frame but the current TX queue is full, software enables the interrupt. After the TX queue is empty, an interrupt is generated to instruct software to transmit the waiting frame. Software uses the interrupt to send a group of frames at a time and then releases the buffers for storing the previously transmitted group of frames when the interrupt is valid.

2. Transmitting a frame in query mode

   Software queries the count of the TX frames. If the count is less than the configured depth of TX queue, it notifies the ETH module of the to-be transmitted frame directly. At the same time, it creates a corresponding TX frame index table whose content is the

header address of the frame that is written to the TX queue of the Ethernet MAC. After transmitting a frame, the ETH module notifies the CPU of releasing the corresponding TX buffer through the address of the TX queue. After that, the CPU queries the corresponding TX buffer through the address of the TX queue and releases the buffer.

5.4.3 Interrupt Management

Interrupt Status Register

This register indicates the generated interrupt type. For details, see GLB_IRQ_STAT in section 5.6.3 "Description of the Global Control Registers."

Interrupt Enable Register

This register controls whether to generate the related interrupts. For details, see GLB_IRQ_ENA in section 5.6.3 "Description of the Global Control Registers." If an interrupt is enabled, the interrupt status is written to the related interrupt status register.

Raw Interrupt Status Register

This register can read the raw interrupt of a type and transmit it to the CPU. For details, see GLB_IRQ_RAW in section 5.6.3 "Description of the Global Control Registers." To clear the interrupt status, the raw interrupt of the interrupt must be cleared. After the raw interrupt is cleared, the interrupt status is cleared automatically.

5.4.4 Traffic Control

When the number of frames received at a certain interval exceeds the upper limit configured by software, the subsequently received frames are selectively discarded. Through the configuration of UD_GLB_FC_DROPCTRL, the broadcast frames, multicast frames, or unicast frames are discarded if the traffic limit is exceeded. The traffic limit is configured through UD_GLB_FC_RXLIMIT.

Software configures the time interval of traffic restriction through UD_GLB_FC_TIMECTRL. For a 10-bit time interval register, the time slot can be set to up to 1,023. A 17-bit counter is used for counting the time slots of the main clock. The default count is 100,000. For a 100-MHz main clock, the time slot is 1 ms. Software can configure the upper traffic limit of a 20-bit register. If the traffic limit is set to 0, it indicates that traffic is not limited.

5.4.5 Typical Application

Clock Gating

NOTE
When the ETH module is not used, its clocks can be disabled to reduce the power consumption.

To disable the ETH clocks, perform the following steps:

Step 1 Disable the link status of the ETH interface so that the ETH module cannot transmit or RX packets.

Step 2 Clear the RX queues of ETH interface so that the ETH module cannot report the packet RX interrupt.

Step 3 Software delivers a logic command to reset the ETH module and holds the reset status.

Step 4 Set PERI_CRG59 [eth_cken] to 0 to disable the ETH clocks.

----End

To enable the ETH clocks, perform the following steps:

Step 1 Hold the reset status. Set PERI_CRG59 [eth_cken] to 1 to enable the ETH clocks.

Step 2 Set PERI_CRG59 [hrst_eth_s] to 0 to clear the reset status.

Step 3 Enable the link status of the ETH interface to ensure that the ETH module works properly.

----End

Soft Reset

To perform global soft reset on the ETH module, perform the following steps:

Step 1 Disable the link status of the ETH interface and the packet RX interrupt so that software cannot receive or transmit packets.

Step 2 After processing the current received and transmitted packets on the ETH interface, software clears the RX and TX queues and keeps the queue length the same as the value before soft reset. That is, the count values of the related pointers and queues return to 0.

Step 3 Set PERI_CRG59 [hrst_eth_s] to 1 to deliver the soft reset command for the ETH module.

Step 4 Set PERI_CRG59 [hrst_eth_s] to 0 to clear the soft reset on the ETH module.

Step 5 If packets need to be transmitted and received again, software also needs to initialize the RX and TX queues of the ETH interface.

Step 6 Enable the link status of the ETH interface to ensure that the ETH module works properly.

----End

Initialization

To initialize the ETH interface, perform the following steps:

Step 1 Configure the mode for obtaining the interface status.

The status of the ETH interface can be that of the PHY chip by means of auto-adaption or can be configured by the software. During initialization, select the mode for obtaining the interface status by configuring UD_MAC_PORTSEL[stat_ctrl]:

- If UD_MAC_PORTSEL[stat_ctrl] is set to 1, it indicates that the status of the ETH interface is configured by the software. In this case, go to Step 2.
- If UD_MAC_PORTSEL[stat_ctrl] is set to 0, it indicates that the status of the ETH interface is that of the PHY chip by means of auto-adaption. In this case, go to Step 3.

During reset, software configures the working status of the ETH interface.

Step 2 Configure the working status of the PHY chip.

- If UD_MAC_PORTSEL is set to 1, software needs to configure the rate, connection status, and duplex status in UD_MAC_PORTSET according to the actual application environment, and configures the information to the related registers of the PHY chip.

- The ETH module provides an MDIO interface to implement the read/write control for the PHY chip. During software operation, the MDIO interface writes the address of the PHY chip, the address of the register, and related control information to the MDIO_RWCTRL register. When MDIO_RWCTRL[finish] is 1, it indicates the read/write operation on the PHY chip has been finished by hardware. For details about configuration information, see the data sheet related to the PHY chip.

After the configuration is complete, go to Step 4.

Step 3 Configure the working status in auto-adaption mode.

If UD_MAC_PORTSEL[stat_ctrl] is set to 0, you must specify the rate of the PHY chip, duplex mode, address of the connection register, and offset addresses of the registers of such status bits. The information is configured through

UD_MDIO_ANEG_CTRL.

Step 4 Set the depth of RX and TX queues.

Set the RX queue depth and TX queue depth in the register UD_GLB_QLEN_SET:

- The RX queue depth indicates the maximum number of buffered frames when data is received.
- The TX queue depth indicates the maximum number of buffered frames when data is transmitted.

The RX and TX queues share 64 management spaces, so the sum of the RX queue depth and the TX queue depth cannot exceed 64. Additionally, either the RX queue depth or the TX queue depth must be more than or equal to 1. If the sum exceeds 64, the depth of the RX queue remains unchanged and the depth of the TX queue is changed to 64 minus the depth of the RX queue.

Software can set the multi-packet interrupt configuration register. By configuring the register UD_GLB_IRQN_SET[int_frm_cnt], software controls how many packets need to be received before a multi-packet interrupt is reported. In addition, software can set the aging time register UD_GLB_IRQN_SET[int_timer].

Step 5 Initialize the buffer of the RX frame queue.

After the reset, software needs to apply for a certain number of buffers, and the number is equal to the configured depth of RX queues. The size of each buffer is 2 KB. Then, software writes the header addresses of the buffers to the RX queue. The number of times of the write operation must be equal to the configured depth of RX queues.

Step 6 Execute the soft reset on the ETH module.

Through the soft reset, the logic circuits and frame management queues inside the ETH module are reset, so that the ETH module returns to the initial status. However, the registers inside the ETH module keep the original values. After clearing the reset, software re-applies for a packet RX buffer and initializes the RX queue. Otherwise, the ETH module cannot receive network packets.

NOTE

After the soft reset of the ETH module, the registers configured by software remain unchanged. For details about these registers, see the register description.

----End

Process of Receiving a Frame in Interrupt Mode

To receive a frame in interrupt mode, perform the following steps:

Step 1 Mask the Ethernet interrupt after entering the interrupt handling program.

Step 2 View the interrupt status bit GLB_IRQ_STAT[int_rx_up] to check whether a frame RX interrupt occurs. If a frame RX interrupt occurs, go to Step 3. Otherwise, continue to process other Ethernet interrupts.

Step 3 Read the frame descriptor UD_GLB_IQFRM_DES. Read the frame data of the related length (fd_in_len) according to the header address of the frame that corresponds to fd_in_addr.

Step 4 Return the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt to 0 and notify hardware of the completion of packet receiving.

Step 5 According to the number of the remaining available addresses maintained by itself, software determines whether to configure a new address for packet receiving. If a new address for packet receiving does not need to be configured, go to Step 8. Receiving a packet is complete.

Step 6 Read UD_GLB_QSTAT[cpu_addr_in_rdy] to check whether a new address for packet receiving can be configured. If a new address for packet receiving cannot be configured, return to Step 5.

Step 7 Software allocates a new buffer address to the RX queue through the register UD_GLB_IQ_ADDR. Return to Step 5.

Step 8 Read and check the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt. If the bit is valid and software can continue to receive packets (the upper limit of received packets is not exceeded), return to Step 3.

Step 9 Unmask the Ethernet interrupt.

----End

Process of Receiving a Frame in Query Mode

If the frame RX interrupt GLB_IRQ_ENA[ien_cpu_rx] is disabled, the CPU automatically queries the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt. If the bit is set to 1, it indicates that a frame needs to be received.

Receive a frame in query mode as follows:

Step 1 Read the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt. If this bit is invalid, the process ends.

Step 2 Read the frame descriptor UD_GLB_IQFRM_DES. Read the frame data of the related length (fd_in_len) according to the header address of the frame that corresponds to fd_in_addr.

Step 3 Write 1 to clear the raw interrupt signal bit GLB_IRQ_RAW[iraw_rx_up] of the single-packet interrupt and notify hardware of the completion of packet receiving.

Step 4 Read UD_GLB_QSTAT[cpu_addr_in_rdy] to check whether a new address for packet receiving can be configured. If a new address for packet receiving cannot be configured, the process ends.

Step 5 Software allocates a new buffer address to the RX queue through the register UD_GLB_IQ_ADDR.

----End

Process of Transmitting a Frame

Transmit a frame as follows:

Step 1 Read UD_GLB_ADDRQ_STAT[eq_in_rdy] and check whether the TX queue of the ETH module has free space for receiving new TX frames. If the TX queue of the ETH module has no free space, continue to wait and query for a free space.

Step 2 Configure the header address UD_GLB_EQ_ADDR of the frame to be transmitted.

Step 3 Configure the length UD_GLB_EQFRM_LEN of the frame to be transmitted. The configuration for transmitting a frame is complete.

----End

5.5 Register Summary

MDIO Control Registers

Table 5-5 describes the MDIO control registers.

Table 5-5 Summary of the MDIO control registers (base address: 0x1005_0000)

Offset Address	Name	Description	Page
0x1100	MDIO_RWCTRL	MDIO command word register	5-18
0x1104	MDIO_RO_DATA	MDIO read data register	5-19

MAC Control Registers

Table 5-6 describes the MAC control registers.

Table 5-6 Summary of the MAC controller registers (base address: 0x1005_0000)

Offset Address	Name	Description	Page
0x0200	UD_MAC_PORTSEL	Port working status control register	5-23
0x0204	UD_MAC_RO_STAT	Port status register	5-23
0x0208	UD_MAC_PORTSET	Port working status configuration register	5-24
0x020C	UD_MAC_STAT_CHANGE	Port status change indicator register for the MAC	5-25
0x0210	UD_MAC_SET	MAC function configuration register	5-26

Global Control Registers

Table 5-7 describes the Ethernet global control registers.

Table 5-7 Summary of the global control registers (base address: 0x1005_0000)

Offset Address	Name	Description	Page
0x1300	GLB_HOSTMAC_L32	Lower 32-bit register for the local MAC address	5-31
0x1304	GLB_HOSTMAC_H16	Upper 16-bit register for the local MAC address	5-32
0x1308	GLB_SOFT_RESET	Internal soft reset register	5-32
0x1310	GLB_FWCTRL	Forward control register	5-33
0x1314	GLB_MACTCTRL	MAC filter table control register	5-33
0x1318	GLB_ENDIAN_MOD	Endian control register	5-34
0x1330	GLB_IRQ_STAT	Interrupt status register	5-35
0x1334	GLB_IRQ_ENA	Interrupt enable register	5-37
0x1338	GLB_IRQ_RAW	Raw interrupt register	5-39
0x1400	GLB_MAC0_L32	MAC filter 0	5-40
0x1404	GLB_MAC0_H16	MAC filter 0	5-40
0x1408	GLB_MAC1_L32	MAC filter 1	5-41
0x140C	GLB_MAC1_H16	MAC filter 1	5-41
0x1410	GLB_MAC2_L32	MAC filter 2	5-42
0x1414	GLB_MAC2_H16	MAC filter 2	5-42
0x1418	GLB_MAC3_L32	MAC filter 3	5-43
0x141C	GLB_MAC3_H16	MAC filter 3	5-43
0x1420	GLB_MAC4_L32	MAC filter 4	5-44
0x1424	GLB_MAC4_H16	MAC filter 4	5-45
0x1428	GLB_MAC5_L32	MAC filter 5	5-45
0x142C	GLB_MAC5_H16	MAC filter 5	5-46
0x1430	GLB_MAC6_L32	MAC filter 6	5-46
0x1434	GLB_MAC6_H16	MAC filter 6	5-47
0x1438	GLB_MAC7_L32	MAC filter 7	5-47
0x143C	GLB_MAC7_H16	MAC filter 7	5-48

Offset Address	Name	Description	Page
0x0340	UD_GLB_IRQN_SET	Multi-packet interrupt configuration register	5-48
0x0344	UD_GLB_QLEN_SET	Queue length configuration register	5-49
0x0348	UD_GLB_FC_LEVEL	Traffic control register	5-50
0x034C	UD_GLB_CAUSE	Cause register for the CPU to which the packet is transmitted	5-50
0x0350	UD_GLB_RXFRM_SADDR	RX frame start address register	5-51
0x0354	UD_GLB_IQFRM_DES	RX frame descriptor register	5-51
0x0358	UD_GLB_IQ_ADDR	RX frame header address register	5-52
0x035C	UD_GLB_BFC_STAT	Counter for traffic control status of forward buffer and aging time of multi-packet interrupt	5-52
0x0360	UD_GLB_EQ_ADDR	TX queue header address register	5-53
0x0364	UD_GLB_EQFRM_LEN	TX queue frame length configuration register	5-54
0x0368	UD_GLB_QSTAT	Queue status register	5-54
0x036C	UD_GLB_ADDRQ_STAT	Address queue status register	5-55
0x0370	UD_GLB_FC_TIMECTRL	Traffic control time configuration register	5-56
0x0374	UD_GLB_FC_RXLIMIT	Traffic control limit configuration register	5-57
0x0378	UD_GLB_FC_DROPCTRL	Packet drop control register for traffic control	5-57
0x0380	UD_GLB_RX_COE_EN	RX COE enable register	5-58

Statistics Counter Control Registers

Table 5-8 describes the statistics counter control registers.

Table 5-8 Summary of the statistics counter control registers (base address: 0x1005_0000)

Offset Address	Name	Description	Page
0x0584	UD_STS_PORTCNT	Port status counter	5-58
0x05A0	UD_PORT2CPU_PKTS	Register for the total number of packets received by the CPU from the uplink or downlink port	5-59
0x05A4	UD_CPU2IQ_ADDRCNT	Register for the count of configuring packet receiving address queue by the CPU	5-60
0x05A8	UD_RX_IRQCNT	Register for the count of reporting single-packet interrupt by the uplink or downlink port	5-60
0x05AC	UD_CPU2EQ_PKTS	Register for the total number of packets transmitted by the CPU to the uplink or downlink port	5-60

Statistics Result Registers

Table 5-9 describes the statistics result registers.

Table 5-9 Summary of the statistics result registers (base address: 0x1005_0000)

Offset Address	Name	Description	Page
0x0600	UD_RX_DVCNT	RXDV rising edge count register	5-61
0x0604	UD_RX_OCTS	Register for the total number of received bytes	5-61
0x0608	UD_RX_RIGHTOCTS	Register for the total number of bytes of received correct packets	5-62
0x060C	UD_HOSTMAC_PKTS	Register for the number of packets matching the local MAC address	5-62
0x0610	UD_RX_RIGHTPKTS	Register for the total number of packets received by the port	5-63
0x0614	UD_RX_BROADPKTS	Register for the number of correct broadcast packets	5-63
0x0618	UD_RX_MULTPKTS	Register for the number of correct multicast packets	5-63

Offset Address	Name	Description	Page
0x061C	UD_RX_UNIPKTS	Register for the number of correct unicast packets	5-64
0x0620	UD_RX_ERRPKTS	Register for the total number of incorrect packets	5-64
0x0624	UD_RX_CRCERR_PKTS	Register for the count of CRC errors	5-64
0x0628	UD_RX_LENERR_PKTS	Register for the number of packets with invalid length	5-65
0x062C	UD_RX_OCRCERR_PKTS	Register for the number of packets with odd nibbles and CRC errors	5-65
0x0630	UD_RX_PAUSE_PKTS	Register for the number of received pause packets	5-66
0x0634	UD_RF_OVERCNT	Register for the count of RXFIFO overflow events	5-66
0x0638	UD_FLUX_TOL_IPKTS	Register for the total number of received packets allowed by the traffic limit	5-66
0x063C	UD_FLUX_TOL_DPKTS	Register for the total number of packets discarded due to traffic limit	5-67
0x064C	UD_MN2CPU_PKTS	Register for the number of packets not forwarded to the CPU port due to MAC limit	5-67
0x0780	UD_TX_PKTS	Register for the total number of packets transmitted successfully	5-67
0x0784	UD_TX_BROADPKTS	Register for the number of broadcast packets transmitted successfully	5-68
0x0788	UD_TX_MULTPKTS	Register for the number of multicast packets transmitted successfully	5-68
0x078C	UD_TX_UNIPKTS	Register for the number of unicast packets transmitted successfully	5-69
0x0790	UD_TX_OCTS	Register for the total number of transmitted bytes	5-69
0x0794	UD_TX_PAUSE_PKTS	Register for the number of transmitted pause frames	5-69

Offset Address	Name	Description	Page
0x0798	UD_TX_RETRYCNT	Register for the total count of retransmission	5-70
0x079C	UD_TX_COLCNT	Register for the total count of collisions	5-70
0x07A0	UD_TX_LC_PKTS	Register for the number of packets with late collision	5-70
0x07A4	UD_TX_COLOK_PKTS	Register for the number of packets transmitted successfully with collisions	5-71
0x07A8	UD_TX_RETRY15_PKTS	Register for the number of packets discarded due to more than 15 times of retransmission	5-71
0x07AC	UD_TX_RETRYN_PKTS	Register for the number of packets with the count of collisions being equal to the threshold	5-71

5.6 Register Description

5.6.1 Description of the MDIO Control Registers

MDIO_RWCTRL

MDIO_RWCTRL is an MDIO command word register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1100	MDIO_RWCTRL	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																finish	reserved	rw	phy_exaddr				frq_dv				phy_inaddr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cpu_data_in	Data used by the MDIO module to perform write operation on the PHY chip During write operation, the CPU first writes the 16-bit data to be written to the MDIO to this register.

[15]	RW	finish	PHY read/write operation complete 0: not complete 1: complete When the read/write operation is required for the second time, the CPU must clear this bit first.
[14]	RO	reserved	Reserved
[13]	RW	rw	PHY read or write access control 0: read operation 1: write operation
[12:8]	RW	phy_exaddr	Physical address of the external PHY chip One MDIO can perform read/write operation on multiple external PHY chips. Each PHY chip has one corresponding address. When the MDIO connects to only one external PHY chip, this bit is equivalent to UD_MDIO_PHYADDR[phy0_addr] or UD_MDIO_PHYADDR[phy1_addr].
[7:5]	RW	frq_dv	Frequency division factor for the MDC (the MDIO interface clock) when the MDIO performs the read/write operation on external PHY chips Take the frequency 100 MHz of the main clock as an example to describe the matching relations between frq_dv and MDC frequency. 000: The frequency of the working main clock is divided by 50 and the obtained frequency is 2 MHz. 001: The frequency of the working main clock is divided by 100 and the obtained frequency is 1 MHz. 010: The frequency of the working main clock is divided by 200 and the obtained frequency is 500 kHz. 011: The frequency of the working main clock is divided by 400 and the obtained frequency is 250 kHz. 100: The frequency of the working main clock is divided by 800 and the obtained frequency is 125 kHz. 101: The frequency of the working main clock is divided by 1600 and the obtained frequency is 62.5 kHz. 110: The frequency of the working main clock is divided by 3200 and the obtained frequency is 31.25 kHz. 111: The frequency of the working main clock is divided by 6400 and the obtained frequency is 15.625 kHz.
[4:0]	RW	phy_inaddr	Internal register address of the external PHY chip. This address is presented by a 5-bit binary number.

MDIO_RO_DATA

MDIO_RO_DATAMDIO is a read data register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1104	MDIO_RO_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cpu_data_out															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	cpu_data_out	Data register used by the MDIO module to perform read operation on the PHY chip. The MDIO module first writes the 16-bit data read from the PHY chip to this register.

UD_MDIO_PHYADDR

UD_MDIO_PHYADDR is a PHY physical address register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0108	UD_MDIO_PHYADDR	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												phy_addr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	phy_addr	Physical address of the external PHY chip

UD_MDIO_RO_STAT

UD_MDIO_RO_STAT is a PHY status register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x010C	UD_MDIO_RO_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													speed_mdio2mac	link_mdio2mac	duplex_mdio2mac

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RO	speed_mdio2mac	Port speed working status obtained from the MDIO interface, which is in either 10 Mbit/s or 100 Mbit/s working mode 0: 10 Mbit/s mode 1: 100 Mbit/s mode
[1]	RO	link_mdio2mac	Port link status obtained from the MDIO interface 0: No link exists. 1: A link exists.
[0]	RO	duplex_mdio2mac	Port duplex working status obtained from the MDIO interface 0: half-duplex 1: full-duplex

UD_MDIO_ANEG_CTRL

UD_MDIO_ANEG_CTRLPHY is an offset address configuration register for the PHY status. The register does not support soft reset.

NOTE

The PHY speed status is indicated by bit[14] of the register with the address of 17, internal_addr_speed is set to 0x11 and speed_index is set to 0xE. In this case, the ETH module reads the bit value as the current working speed mode of the PHY through the MDIO interface.

Offset Address	Register Name	Total Reset Value
0x0110	UD_MDIO_ANEG_CTRL	0x0463_1EA9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								internal_addr_speed							internal_addr_link					internal_addr_duplex				speed_index				link_index				duplex_index			
Reset	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	0	1	0	1	0	1	0	0	1

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:22]	RW	internal_addr_speed	Address of the register in the PHY chip to store the status information (speed). The default value is set according to Intel 9785.

[21:17]	RW	internal_addr_link	Address of the register in the PHY chip to store the status information (link). The default value is set according to Intel 9785.
[16:12]	RW	internal_addr_duplex	Address of the register in the PHY chip to store the status information (duplex). The default value is set according to Intel 9785.
[11:8]	RW	speed_index	Offset address in the PHY status register that is used to store the speed information. The default value is set according to Intel 9785.
[7:4]	RW	link_index	Offset address in the PHY status register that is used to store the link information. The default value is set according to Intel 9785.
[3:0]	RW	duplex_index	Offset address in the PHY status register that is used to store the duplex information. The default value is set according to Intel 9785.

UD_MDIO_IRQENA

UD_MDIO_IRQENA is a scan mask register for MDIO status changes. The register does not support soft reset.

NOTE

- If the status information about the PHY chip connecting to the port cannot be scanned and obtained by configuring
- UD_MDIO_ANEG_CTRL, you can scan the PHY status register by using MDIO_RWCTRL to check whether the port status changes and generate an interrupt to notify software of processing the interrupt.
- link_partner status change refers to the change of any bit of link, speed, and duplex for the PHY status.

Offset Address	Register Name	Total Reset Value
0x0114	UD_MDIO_IRQENA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							link_partner_ch_mask	speed_ch_mask	link_ch_mask	duplex_ch_mask
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	link_partner_ch_mask	Port link partner status scan change interrupt mask 0: mask 1: unmask

[2]	RW	speed_ch_mask	Port speed mode scan change interrupt mask 0: mask 1: unmask
[1]	RW	link_ch_mask	Port link mode scan change interrupt mask 0: mask 1: unmask
[0]	RW	duplex_ch_mask	Port duplex mode scan change interrupt mask 0: mask 1: unmask

5.6.2 Description of the MAC Control Registers

MAC control registers are registers for port control. When the port status is valid, after configuring MAC control registers, you need to perform one soft reset on them.

UD_MAC_PORTSEL

UD_MAC_PORTSEL is a port working status control register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0200	UD_MAC_PORTSEL	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								stat_ctrl
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	stat_ctrl	Port working status information select control register 0: Use the status information obtained from the MDIO interface. 1: Use the status information set by the CPU.

UD_MAC_RO_STAT

UD_MAC_RO_STAT is a port status register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0204	UD_MAC_RO_STAT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								peed_stat	link_stat	duplex_stat
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RO	speed_stat	Port current speed mode 0: 10 Mbit/s mode 1: 100 Mbit/s mode
[1]	RO	link_stat	Port current link status 0: No link exists. 1: A link exists.
[0]	RO	duplex_stat	Port current duplex status 0: half-duplex 1: full-duplex

UD_MAC_PORTSET

UD_MAC_PORTSET is a port working status configuration register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0208	UD_MAC_PORTSET	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								speed_stat_dio	link_stat_dio	duplex_stat_dio
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	speed_stat_dio	Port speed mode set by the CPU 0: 10 Mbit/s mode 1: 100 Mbit/s mode

[1]	RW	link_stat_dio	Port link status set by the CPU 0: No link exists. 1: A link exists.
[0]	RW	duplex_stat_dio	Port duplex mode set by the CPU 0: half-duplex 1: full-duplex

UD_MAC_STAT_CHANGE

UD_MAC_STAT_CHANGE is a port status change indicator register. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x020C	UD_MAC_STAT_CHANGE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													speed_stat_ch	link_stat_ch	duplex_stat_ch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	WC	speed_stat_ch	Port speed mode change indicator 0: No change occurs. 1: A change occurs. Writing 1 clears this register.
[1]	WC	link_stat_ch	Port link status change indicator 0: No change occurs. 1: A change occurs. Writing 1 clears this register.
[0]	WC	duplex_stat_ch	Port duplex mode change indicator 0: No change occurs. 1: A change occurs. Writing 1 clears this register.

UD_MAC_SET

UD_MAC_SET is a MAC function configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0210	UD_MAC_SET	0x2027_55EE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		add_pad_en	crcgen_dis	cntr_rdclr_en	cntr_clr_all	cntr_roll_dis	colthreshold				in_loop_en	ex_loop_en	pause_en	rx_shframe_en	rx_min_thr					len_max											
Reset	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	0	1	0	1	0	1	1	1	1	0	1	1	1	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	add_pad_en	Port auto add PAD enable during transmission 0: disabled 1: enabled
[28]	RW	crcgen_dis	Port CRC generation disable control 0: CRC is recalculated for the output frame. 1: CRC is not recalculated for the output frame.
[27]	RW	cntr_rdclr_en	Port statistics counter read clear enable 0: disabled 1: enabled
[26]	RW	cntr_clr_all	Port statistics counter clear control 0: not clear 1: clear **NOTE** If cntr_clr_all is set to 1, the next clear all operation can be performed only after this bit is set to 0 and then to 1.
[25]	RW	cntr_roll_dis	Port statistics acyclic counter enable 0: disabled 1: enabled
[24:21]	RW	colthreshold	Port collision count statistics threshold The default value is 0x1, which indicates the count of frames with one collision.

[20]	RW	in_loop_en	Port loopback to internal enable 0: disabled 1: enabled NOTE Loopback to internal enable and loopback to external enable cannot be configured at the same time. When the network interface is in normal state, you need to perform soft reset on the module after loopback to internal enable is configured instead of loopback to external enable and vice versa.
[19]	RW	ex_loop_en	Port loopback to external enable 0: disabled 1: enabled Note: Loopback to internal enable and loopback to external enable cannot be configured at the same time. When the network interface is in normal state, you need to perform soft reset on the module after loopback to internal enable is configured instead of loopback to external enable and vice versa.
[18]	RW	pause_en	Port pause frame TX enable 0: disabled 1: enabled
[17]	RW	rx_shframe_en	Port short frame RX enable 0: disabled 1: enabled NOTE If rx_shframe_en is set to 1, the minimum RX frame length allowed by the port is that set by rx_min_thr. If rx_shframe_en is set to 0, the minimum RX frame length allowed by the port is 64 bytes (including CRC) by default.
[16:11]	RW	rx_min_thr	Minimum RX frame length allowed by the port The value range is from 42 bytes to 63 bytes. The default value is 42 bytes. NOTE If rx_min_thr is set to a value smaller than 42, 42 is used instead of the value.
[10:0]	RW	len_max	Maximum RX frame length allowed by the port. The default value is 1518 bytes. The value is in a range of 1518 bytes to 1535 bytes. NOTE If len_max is set to a value greater than 2000, 2000 is used instead of the value. If len_max is set to a value smaller than 256, 256 is used instead of the value.

UD_MAC_EEE_INT

UD_MAC_EEE_INT is an EEE raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0480	UD_MAC_EEE_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											tx_entry_start	rx_leave_lpi	rx_entry_lpi	tx_leave_lpi	tx_entry_lpi
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RO	tx_entry_start	Raw interrupt that allows the PHY to enter the low-power idle (LPI) state in the ETH TX direction
[3]	RO	rx_leave_lpi	Raw interrupt that allows the PHY to exit the LPI state in the RX direction
[2]	RO	rx_entry_lpi	Raw interrupt that allows the PHY to enter the LPI state in the RX direction
[1]	RO	tx_leave_lpi	Raw interrupt that allows the PHY to exit the LPI state in the TX direction
[0]	RO	tx_entry_lpi	Raw interrupt that allows the PHY to enter the LPI state in the TX direction

UD_MAC_EEE_INTEN

UD_MAC_EEE_INTEN is an EEE interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0484	UD_MAC_EEE_INTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						tx_entry_start_msk	rx_leave_lpi_msk	rx_entry_lpi_msk	tx_leave_lpi_msk	tx_entry_lpi_msk	tx_entry_start_en	rx_leave_lpi_en	rx_entry_lpi_en	tx_leave_lpi_en	tx_entry_lpi_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	tx_entry_start_msk	Mask of the raw interrupt that allows the PHY to enter the LPI state in the ETH TX direction
[8]	RW	rx_leave_lpi_msk	Mask of the raw interrupt that allows the PHY to exit the LPI state in the RX direction
[7]	RW	rx_entry_lpi_msk	Mask of the raw interrupt that allows the PHY to enter the LPI state in the RX direction
[6]	RW	tx_leave_lpi_msk	Mask of the raw interrupt that allows the PHY to exit the LPI state in the TX direction
[5]	RW	tx_entry_lpi_msk	Mask of the raw interrupt that allows the PHY to enter the LPI state in the TX direction
[4]	RO	tx_entry_start_en	Enable for the raw interrupt that allows the PHY to enter the LPI state in the ETH TX direction
[3]	RO	rx_leave_lpi_en	Enable for the raw interrupt that allows the PHY to exit the LPI state in the RX direction
[2]	RO	rx_entry_lpi_en	Enable for the raw interrupt that allows the PHY to enter the LPI state in the RX direction
[1]	RO	tx_leave_lpi_en	Enable for the raw interrupt that allows the PHY to exit the LPI state in the TX direction
[0]	RO	tx_entry_lpi_en	Enable for the raw interrupt that allows the PHY to enter the LPI state in the TX direction

UD_MAC_EEE_ENA

UD_MAC_EEE_ENA is an EEE enable register.

Offset Address	Register Name	Total Reset Value
0x0488	UD_MAC_EEE_ENA	0x00F4_2400

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	eee_ls_timer							reserved / eee_assert / eee_enable
Reset	0 0 0 0	0 0 0 0	1 1 1 1	0 1 0 0	0 0 1 0	0 1 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:4]	RW	eee_ls_timer	LS timer
[3:2]	RW	reserved	Reserved
[1]	RW	eee_assert	EEE LPI state enable
[0]	RW	eee_enable	EEE enable

UD_MAC_EEE_TIMER

UD_MAC_EEE_TIMER is a timer register required for the EEE function.

Offset Address	Register Name	Total Reset Value
0x048C	UD_MAC_EEE_TIMER	0x001E_2710

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	tx_wk_timer				lpi_cond_timer			
Reset	0 0 0 0	0 0 0 0	0 0 0 1	1 1 1 0	0 0 1 0	0 1 1 1	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	tx_wk_timer	TX_WK_TIMER
[15:0]	RW	lpi_cond_timer	LPI_COND_TIMER

UD_MAC_EEE_LINK_STATUS

UD_MAC_EEE_LINK_STATUS an ETH port link status register dedicated for the EEE function.

Offset Address	Register Name	Total Reset Value
0x0490	UD_MAC_EEE_LINK_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															phy_link_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	phy_link_status	PHY link status

UD_MAC_EEE_CLK_CNT

UD_MAC_EEE_CLK_CNT is an EEE clock unit counter register.

Offset Address	Register Name	Total Reset Value
0x0494	UD_MAC_EEE_CLK_CNT	0x0000_0063

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eee_clk_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1

Bits	Access	Name	Description
[31:0]	RW	eee_clk_cnt	EEE clock unit counter

5.6.3 Description of the Global Control Registers

GLB_HOSTMAC_L32

GLB_HOSTMAC_L32 is a lower 32-bit register for the local MAC address.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1300	GLB_HOSTMAC_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	local_mac																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	local_mac	Lower 32 bits of the local MAC address

GLB_HOSTMAC_H16

GLB_HOSTMAC_H16 is an upper 16-bit register for the local MAC address.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1304	GLB_HOSTMAC_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																local_mac[47:32]															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	local_mac[47:32]	Upper 16 bits of the local MAC address

GLB_SOFT_RESET

GLB_SOFT_RESET is an internal soft reset register.

The register does not support soft reset.

NOTE

The time for each soft reset must remain for more than 2 ms.

Offset Address	Register Name	Total Reset Value
0x1308	GLB_SOFT_RESET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															soft_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RW	soft_reset	Internal soft reset 0: not reset 1: reset In soft reset state, this bit must be set to 0 to clear soft reset.

GLB_FWCTRL

GLB_FWCTRL is a forward control register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1310	GLB_FWCTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fwall2cpu_up	reserved	fw2cpu_ena_up	reserved				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	fwall2cpu_up	Whether to forcibly forward all valid input frames to the CPU port 0: no 1: yes
[6]	RO	reserved	Reserved
[5]	RW	fw2cpu_ena_up	Function enable of forwarding the input frames to the CPU port 0: disabled 1: enabled
[4:0]	RO	reserved	Reserved

GLB_MACTCTRL

GLB_MACTCTRL is a MAC filter table control register.

The register does not support soft reset.

NOTE

- If the highest byte of the destination MAC address is even, the frame is a unicast frame.
- If the highest byte of the destination MAC address is odd, the frame is a multicast frame.
- If all bytes of the destination MAC address are 0xFF, the frame is a broadcast frame.

Offset Address	Register Name	Total Reset Value
0x1314	GLB_MACTCTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mact_ena_up	reserved	broad2cpu_up	reserved	multi2cpu_up	reserved	uni2cpu_up	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	mact_ena_up	Enable bit of all MAC filters of the port 0: disabled (no MAC filter is used) 1: enabled (MAC filters are used)
[6]	RO	reserved	Reserved
[5]	RW	broad2cpu_up	Whether to forward the input broadcast frames to the CPU port 0: no 1: yes
[4]	RO	reserved	Reserved
[3]	RW	multi2cpu_up	Whether to forward the input multicast frames that are not listed in the filter table to the CPU port 0: no 1: yes
[2]	RO	reserved	Reserved
[1]	RW	uni2cpu_up	Whether to forward the input unicast frames that are not listed in the filter table to the CPU port 0: no 1: yes
[0]	RO	reserved	Reserved

GLB_ENDIAN_MOD

GLB_ENDIAN_MOD is an endian control register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1318	GLB_ENDIAN_MOD	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														in_edian	out_edian
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	in_edian	RX packet write SDRAM endian configuration 0: big-endian mode 1: little-endian mode Data consists of bytes
[0]	RW	out_edian	TX packet read SDRAM endian configuration 0: big-endian mode 1: little-endian mode

GLB_IRQ_STAT

GLB_IRQ_STAT is an interrupt status register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1330	GLB_IRQ_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			int_mdio_finish	reserved				int_rxd_up	int_freeq_up	int_stat_up	int_duplex_up	int_speed_up	int_link_up	int_tx_up	int_rx_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	int_mdio_finish	Raw interrupt status indicating whether the MDIO interface completes the operation required by the CPU 0: not completed 1: Completed and an interrupt is generated.

			After this interrupt is generated, software determines whether the MDIO completes the operation by querying MDIO_RWCTRL[finish].
[11:8]	RO	reserved	Reserved
[7]	RO	int_rxd_up	Interrupt status (multi-packet interrupt) for frames on the port to be received by the CPU 0: The interrupt is invalid. 1: The interrupt is valid. There are frames to be received by the CPU in the RX queue. After this interrupt is generated, software determines whether there are frames to be received by querying GLB_IRQ_RAW[iraw_rxd_up].
[6]	RO	int_freeeq_up	Interrupt status indicates that the status of the port output queue is changed from nonempty to empty, that is, the status of the TX queue buffer is changed from nonempty to empty, that is, the status of the TX queue buffer is changed from nonempty to empty. In this case, the CPU can write a group of new frames to be transmitted. 0: No interrupt is generated. 1: An interrupt is generated. After this interrupt is generated, software determines whether the current TX queue is empty by querying UD_GLB_ADDRQ_STAT[eq_cnt]. If the current TX queue is not empty, it indicates that the interrupt is invalid.
[5]	RO	int_stat_up	Interrupt status for port status changes, indicating that an interrupt is generated when the MDIO obtains the speed change, duplex mode change, and link status change of the PHY chip in auto-adaption mode. 0: The interrupt is invalid. 1: The interrupt is valid. The port status changes. After this interrupt is generated, software determines which status changes according to the configuration of UD_MDIO_IRQENA.
[4]	RO	int_duplex_up	Interrupt status for port duplex mode changes 0: The interrupt is invalid. 1: The interrupt is valid. The duplex mode changes. After this interrupt is generated, software determines whether the duplex mode changes by querying UD_MAC_STAT_CHANGE[duplex_stat_ch].
[3]	RO	int_speed_up	Interrupt status for port speed mode changes 0: The interrupt is invalid. 1: The interrupt is valid. The speed mode changes. After this interrupt is generated, software determines whether the speed mode changes by querying UD_MAC_STAT_CHANGE[speed_stat_ch].
[2]	RO	int_link_up	Interrupt status for port link status changes 0: The interrupt is invalid.

			1: The interrupt is valid. The link status changes. After this interrupt is generated, software determines whether the link status changes by querying UD_MAC_STAT_CHANGE[link_stat_ch].
[1]	RO	int_tx_up	Interrupt status for the completion of transmitting a frame from the CPU by the port 0: not completed 1: Completed and an interrupt is generated. After this interrupt is generated, software determines whether to release the buffer of the TX frames by querying the current TX queue address eq_out_index in UD_GLB_QSTAT.
[0]	RO	int_rx_up	Interrupt status for frames on the port to be received by the CPU 0: The interrupt is invalid. 1: The interrupt is valid. There are frames to be received by the CPU in the RX queue. After this interrupt program is started, software determines whether frames are received by querying the GLB_IRQ_RAW[iraw_rxd_up] signal.

GLB_IRQ_ENA

GLB_IRQ_ENA is an interrupt enable register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x1334	GLB_IRQ_ENA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18	17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			ien_all	ien_up	reserved	ien_mdio_finish	reserved	ien_rxd_up, ien_freeeq_up, ien_stat_up, ien_duplex_up	ien_speed_up, ien_link_up, ien_tx_up, ien_rx_up
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RW	ien_all	All interrupts enable 0: disabled (none of the interrupt can be reported) 1: enabled (all interrupts are reported according to the configuration)

[18]	RW	ien_up	All uplink port interrupts enable 0: disabled (none of the uplink port interrupt can be reported) 1: enabled (all uplink port interrupts are reported according to the configuration)
[17:13]	RO	reserved	Reserved
[12]	RW	ien_mdio_finish	Indicator enable for the MDIO to complete the operation required by the CPU 0: disabled 1: enabled
[11:8]	RO	reserved	Reserved
[7]	RW	ien_rxd_up	Interrupt enable (multi-packet interrupt) for a frame (frames) on the uplink port to be received by the CPU 0: disabled 1: enabled
[6]	RW	ien_freeeq_up	Interrupt signal enable for the TX queue of the uplink port to change from nonempty to empty 0: disabled 1: enabled
[5]	RW	ien_stat_up	Interrupt signal enable for uplink port status changes 0: disabled 1: enabled
[4]	RW	ien_duplex_up	Interrupt enable for uplink port duplex mode changes 0: disabled 1: enabled
[3]	RW	ien_speed_up	Interrupt enable for uplink port speed mode changes 0: disabled 1: enabled
[2]	RW	ien_link_up	Interrupt enable for uplink port link status changes 0: disabled 1: enabled
[1]	RW	ien_tx_up	Indicator enable for the completion of transmitting a frame from the CPU by the uplink port 0: disabled 1: enabled
[0]	RW	ien_rx_up	Interrupt enable for frames on the uplink port to be received by the CPU 0: disabled 1: enabled

GLB_IRQ_RAW

GLB_IRQ_RAW is a raw interrupt register. The register does not support soft reset. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0x1338	GLB_IRQ_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			iraw_mdio_finish	reserved				iraw_rxd_up	iraw_freeeq_up	iraw_stat_up	iraw_duplex_up	iraw_speed_up	iraw_link_up	iraw_tx_up	iraw_rx_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	iraw_mdio_finish	Raw interrupt status for the MDIO to complete the operation required by the CPU 0: No interrupt is generated. 1: An interrupt is generated.
[11:8]	RO	reserved	Reserved
[7]	WC	iraw_rxd_up	Raw interrupt status (multi-packet interrupt) for a frame (frames) on the uplink port to be received by the CPU 0: No interrupt is generated. 1: An interrupt is generated.
[6]	WC	iraw_freeeq_up	Raw interrupt status for the TX queue of the uplink port to change from nonempty to empty, indicating that the TX queue buffer changes from nonempty to empty and the CPU can write a group of new frames to be transmitted. 0: No interrupt is generated. 1: An interrupt is generated.
[5]	WC	iraw_stat_up	Raw interrupt status for uplink port status changes, indicating that an interrupt is generated when the MDIO obtains the speed change, duplex mode change, and link status change of the PHY chip in auto-adaption mode. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	iraw_duplex_up	Raw interrupt status for uplink port duplex mode changes 0: No interrupt is generated. 1: An interrupt is generated.

[3]	WC	iraw_speed_up	Raw interrupt status for uplink port speed mode changes 0: The interrupt is invalid. 1: The interrupt is valid. The speed mode changes. Writing 1 clears this register.
[2]	WC	iraw_link_up	Raw interrupt status for uplink port link status changes 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	iraw_tx_up	Raw interrupt status for the completion of transmitting a frame from the CPU by the uplink port 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	iraw_rx_up	Raw interrupt status for frames on the uplink port to be received by the CPU 0: No interrupt is generated. 1: An interrupt is generated.

GLB_MAC0_L32

GLB_MAC0_L32 is a lower 32-bit register for the filter table MAC0.

Offset Address	Register Name	Total Reset Value
0x1400	GLB_MAC0_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac0	Lower 32 bits of the filter table MAC0

GLB_MAC0_H16

GLB_MAC0_H16 is an upper 16-bit register for the filter table MAC0.

Offset Address	Register Name	Total Reset Value
0x1404	GLB_MAC0_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac0_up	reserved	flt_mac0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac0_up	Control for setting this filter to be used by the uplink port 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac0	Upper 16 bits of the filter table MAC0

GLB_MAC1_L32

GLB_MAC1_L32 is a lower 32-bit register for the filter table MAC1.

Offset Address	Register Name	Total Reset Value
0x1408	GLB_MAC1_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac1	Lower 32 bits of the filter table MAC1

GLB_MAC1_H16

GLB_MAC1_H16 is an upper 16-bit register for the filter table MAC1.

Offset Address	Register Name	Total Reset Value
0x140C	GLB_MAC1_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac1_up	reserved	flt_mac1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac1_up	Control for setting this filter to be used by the uplink port 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac1	Upper 16 bits of the filter table MAC1

GLB_MAC2_L32

GLB_MAC2_L32 is a lower 32-bit register for the filter table MAC2.

Offset Address	Register Name	Total Reset Value
0x1410	GLB_MAC2_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac2	Lower 32 bits of the filter table MAC2

GLB_MAC2_H16

GLB_MAC2_H16 is an upper 16-bit register for the filter table MAC2.

Offset Address	Register Name	Total Reset Value
0x1414	GLB_MAC2_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac2_up	reserved	flt_mac2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac2_up	Control for setting this filter to be used by the uplink port 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac2	Upper 16 bits of the filter table MAC2

GLB_MAC3_L32

GLB_MAC3_L32 is a lower 32-bit register for the filter table MAC3.

Offset Address	Register Name	Total Reset Value
0x1418	GLB_MAC3_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac3	Lower 32 bits of the filter table MAC3

GLB_MAC3_H16

GLB_MAC3_H16 is an upper 16-bit register for the filter table MAC3.

Offset Address	Register Name	Total Reset Value
0x141C	GLB_MAC3_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac3_up	reserved	flt_mac3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac3_up	Whether to forward the frames received by the downlink port that match this filter to the CPU port when the downlink port enables this filter 0: Do not forward the frames. 1: Forward the frames.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac3	Upper 16 bits of the filter table MAC3

GLB_MAC4_L32

GLB_MAC4_L32 is a lower 32-bit register for the filter table MAC4.

Offset Address	Register Name	Total Reset Value
0x1420	GLB_MAC4_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac4	Lower 32 bits of the filter table MAC4

GLB_MAC4_H16

GLB_MAC4_H16 is an upper 16-bit register for the filter table MAC4.

Offset Address	Register Name	Total Reset Value
0x1424	GLB_MAC4_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac4_up	reserved	flt_mac4															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac4_up	Control for setting this filter to be used by the uplink port 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac4	Upper 16 bits of the filter table MAC4

GLB_MAC5_L32

GLB_MAC5_L32 is a lower 32-bit register for the filter table MAC5.

Offset Address	Register Name	Total Reset Value
0x1428	GLB_MAC5_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac5	Lower 32 bits of the filter table MAC5

GLB_MAC5_H16

GLB_MAC5_H16 is an upper 16-bit register for the filter table MAC5.

Offset Address	Register Name	Total Reset Value
0x142C	GLB_MAC5_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac5_up	reserved	flt_mac5															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac5_up	Control for setting this filter to be used by the uplink port 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac5	Upper 16 bits of the filter table MAC5

GLB_MAC6_L32

GLB_MAC6_L32 is a lower 32-bit register for the filter table MAC6.

Offset Address	Register Name	Total Reset Value
0x1430	GLB_MAC6_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac6	Lower 32 bits of the filter table MAC6

GLB_MAC6_H16

GLB_MAC6_H16 is an upper 16-bit register for the filter table MAC6.

Offset Address	Register Name	Total Reset Value
0x1434	GLB_MAC6_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac6_up	reserved	flt_mac6															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac6_up	Control for setting this filter to be used by the uplink port 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac6	Upper 16 bits of the filter table MAC6

GLB_MAC7_L32

GLB_MAC7_L32 is a lower 32-bit register for the filter table MAC7.

Offset Address	Register Name	Total Reset Value
0x1438	GLB_MAC7_L32	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flt_mac7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	flt_mac7	Lower 32 bits of the filter table MAC7

GLB_MAC7_H16

GLB_MAC7_H16 is an upper 16-bit register for the filter table MAC7.

Offset Address	Register Name	Total Reset Value
0x143C	GLB_MAC7_H16	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										fw2cpu_up	reserved			mac7_up	reserved	flt_mac7															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	fw2cpu_up	Whether to forward the frames received by the uplink port that match this filter to the CPU port when the uplink port enables this filter 0: no 1: yes
[20:18]	RO	reserved	Reserved
[17]	RW	mac7_up	Control for setting this filter to be used by the uplink port 0: The uplink port does not use this filter. 1: The uplink port uses this filter.
[16]	RO	reserved	Reserved
[15:0]	RW	flt_mac7	Upper 16 bits of the filter table MAC7

UD_GLB_IRQN_SET

UD_GLB_IRQN_SET is a multi-packet interrupt configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0340	UD_GLB_IRQN_SET	0x0800_003A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				int_frm_cnt				reserved								age_timer															
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved

[28:24]	RW	int_frm_cnt	These bits are used to set the multi-packet interrupt function. That is, how many packets must be received before a multi-packet interrupt can be reported. NOTE The minimum value of int_frm_cnt can be set to 1. In this case, multi-packet interrupt is equivalent to single-packet interrupt.
[23:16]	RO	reserved	Reserved
[15:0]	RW	age_timer	After the multi-packet interrupt function is enabled, if the number of received packets cannot reach the specified number of packets required for reporting the multi-packet interrupt after a period, this period is defined as the aging time for generating the multi-packet interrupt. NOTE age_timer is counted in the unit of the main clock cycle divided by 256.

UD_GLB_QLEN_SET

UD_GLB_QLEN_SET is a queue length configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0344	UD_GLB_QLEN_SET	0x0000_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				iq_len				reserved				eq_len			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

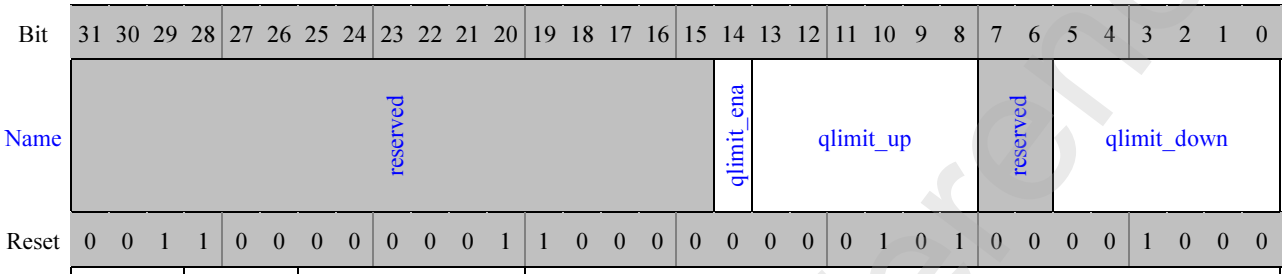
Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	iq_len	RX (packet RX) queue length configuration NOTE iq_len cannot be set to 0. Otherwise, it is forcibly set to 1. The sum of the set values of iq_len and eq_len cannot be greater than 64. Otherwise, the value (non-zero) of iq_len is firstly assigned and the value of eq_len is calculated by the formula: 64 – iq_len.
[7:6]	RO	reserved	Reserved
[5:0]	RW	eq_len	TX (packet TX) queue length configuration NOTE eq_len cannot be set to 0. Otherwise, it is forcibly set to 1.

UD_GLB_FC_LEVEL

UD_GLB_FC_LEVEL is a traffic control register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0348	UD_GLB_FC_LEVEL	0x3018_0508



Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	qlimit_ena	Traffic control enable for RX queue 0: Disabled (do not transmit the traffic control message according to the status of RX queue). 1: Enabled (transmit the traffic control message according to the status of RX queue).
[13:8]	RW	qlimit_up	Upper limit of traffic control for RX queue. When the free space of the RX queue is less than the upper limit, if traffic control for RX queue is enabled, the traffic control message is transmitted to the peer end. **NOTE** • If the upper limit qlimit_up is set to 0, the RX queue fails to enter the traffic control status. • The upper limit qlimit_up must be greater than the lower limit qlimit_down.
[7:6]	RO	reserved	Reserved
[5:0]	RW	qlimit_down	Lower limit of traffic control for RX queue. When the free space of the RX queue is equal to or greater than the upper limit, if the RX queue is in traffic control state, the current traffic control is stopped.

UD_GLB_CAUSE

UD_GLB_CAUSE is a cause register for the CPU to which the packet is transmitted.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x034C	UD_GLB_CAUSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							mact_cause
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RO	mact_cause	Packet matching result types by querying the MAC table 000: forced forwarding 001: Packet whose destination MAC address is the local MAC address. 010: broadcast packet 011: packet matching the MAC table 100: multicast packet not matching the MAC table 101: unicast packet not matching the MAC table Others: reserved

UD_GLB_RXFRM_SADDR

UD_GLB_RXFRM_SADDR is an RX frame start address register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0350	UD_GLB_RXFRM_SADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rxfrm_saddr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	rxfrm_saddr	Start address of the RX frame

UD_GLB_IQFRM_DES

UD_GLB_IQFRM_DES is an RX frame descriptor register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0354	UD_GLB_IQFRM_DES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fd_in_addr				fd_in_len												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17:12]	RO	fd_in_addr	Relative address of the first frame to be received in the input queue (IQ). It serves as the index (0 to iq_len-1) of the absolute address for storing the frames.
[11:0]	RO	fd_in_len	Length of the frame to be received in the RX queue

UD_GLB_IQ_ADDR

UD_GLB_IQ_ADDR is an RX frame header address register.

The register does not support soft reset.

NOTE

If the address assigned by software is not word aligned, the logic writes data according to the word aligned address. In this case, the previously written data is invalid. For example, if the configured header address of a frame is 0xF000_8002 (non-word-aligned address), the logic writes 0x00 or other data to both the 0xF000_8000 and 0xF000_8001 addresses. Then, the logic writes the first byte (valid data) of the RX frame to the 0xF000_8002 address, writes the second byte (valid data) of the RX frame to the 0xF000_8003 address. Subsequent data is written to the buffer in sequence. If the configured header address of the RX frame is other non-word-aligned address, the logic writes data in a similar way.

Offset Address	Register Name	Total Reset Value
0x0358	UD_GLB_IQ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	startaddr_iq																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	startaddr_iq	Header address (configured by the CPU) of the storage space corresponding to the RX frame. The RX frame requests the bus according to this address.

UD_GLB_BFC_STAT

UD_GLB_BFC_STAT is a counter for traffic control status of forward buffer and aging time of multi-packet interrupt.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x035C	UD_GLB_BFC_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	timerover_cnt																flowctrl_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	timerover_cnt	Register for the count of multi-packet interrupt aging time counter overflow events (the count reaches the configured value) **NOTE** If the value of timerover_cnt is too large in a unit of time, it indicates that UD_GLB_IRQN_SET[int_frm_cnt] is set improperly. Multi-packet interrupt is triggered by the aging time. Therefore, the configured value must be reduced.
[15:0]	RO	flowctrl_cnt	Register for the count of the forward buffer of the uplink or downlink port entering the traffic control status **NOTE** If the value of flowctrl_cnt is too large in a unit of time, it indicates that UD_GLB_FC_LEVEL[blimit_up] or UD_GLB_FC_LEVEL[blimit_down] is set to a too small value, or the external network condition is worsened. In this case, the configured value may be reduced.

UD_GLB_EQ_ADDR

UD_GLB_EQ_ADDR is a TX queue header address register.

The register does not support soft reset.

NOTE

If the header address of the TX frame is not word aligned, the logic reads data according to the word aligned address. In this case, the previously read data is invalid and discarded. For example, if the configured header address of the TX frame is 0xF000_8102 (non-word-aligned address), the logic directly discards the byte data read from the 0xF000_8100 and 0xF000_8101 addresses. Then, the logic considers the data read from the 0xF000_8102 address as the first byte (valid data) of the TX frame and considers the data read from the 0xF000_8103 address as the second byte (valid data) of the TX frame. All subsequent data is valid (until the data of the specified frame length is read). If the configured header address of the TX frame is other non-word-aligned address, the logic reads data in a similar way.

Offset Address	Register Name	Total Reset Value
0x0360	UD_GLB_EQ_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	add_fd_addr_out																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description

[31:0]	RW	add_fd_addr_out	Header address of the TX frame added by the CPU to the TX queue

UD_GLB_EQFRM_LEN

UD_GLB_EQFRM_LEN is a TX queue frame length configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0364	UD_GLB_EQFRM_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								add_fd_len_out							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:0]	RW	add_fd_len_out	Length of the TX frame added by the CPU to the TX queue Configure this register to trigger hardware so that software can write the header address and length of the TX frame to the TX queue for transmission. When transmitting a frame, software must write the header address of the frame before the length of the frame. Note: The frames whose add_fd_len_out is less than 20 bytes or greater than 1600 bytes are discarded. In other words, the allowed range is from 20 bytes to 1600 bytes.

UD_GLB_QSTAT

UD_GLB_QSTAT is a queue status register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0368	UD_GLB_QSTAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				iq_in_index				reserved				cpuw_index				reserved				eq_in_index				reserved				eq_out_index			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved

[29:24]	RO	iq_in_index	RX index of the RX (packet RX) queue
[23:22]	RO	reserved	Reserved
[21:16]	RO	cpuw_index	RX index of frame header address of the RX (packet RX) queue
[15:14]	RO	reserved	Reserved
[13:8]	RO	eq_in_index	RX index of frame descriptor of the TX (packet TX) queue
[7:6]	RO	reserved	Reserved
[5:0]	RO	eq_out_index	TX index of frame descriptor of the TX (packet TX) queue

UD_GLB_ADDRQ_STAT

UD_GLB_ADDRQ_STAT is an address queue status register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x036C	UD_GLB_ADDRQ_STAT	0x0300_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						cpuaddr_in_rdy	eq_in_rdy	reserved				cpu_cnt				reserved				iq_cnt				reserved				eq_cnt			
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RO	cpuaddr_in_rdy	Whether the CPU can configure the frame header address of the RX queue 0: The CPU cannot configure the frame header address of the RX queue. 1: The CPU can configure the frame header address of the RX queue. **NOTE** The values of cpuaddr_in_rdy and eq_in_rdy are set to 0 during reset. The values, however, are set to 1 by the circuit immediately after reset. In other words, after reset, the iq address queue and eq descriptor queue are configurable.

[24]	RO	eq_in_rdy	Whether the CPU can configure the frame descriptor (header address and length) of the TX queue 0: The CPU cannot configure the frame descriptor (header address and length) of the TX queue. 1: The CPU can configure the frame descriptor (header address and length) of the TX queue.
[23:22]	RO	reserved	Reserved
[21:16]	RO	cpu_cnt	Header address count for available frames assigned by the CPU to the RX queue
[15:14]	RO	reserved	Reserved
[13:8]	RO	iq_cnt	Used length of the RX queue (0 to iq_len)
[7:6]	RO	reserved	Reserved
[5:0]	RO	eq_cnt	Used length of the TX queue (0 to eq_len)

UD_GLB_FC_TIMECTRL

UD_GLB_FC_TIMECTRL is a traffic control time configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0370	UD_GLB_FC_TIMECTRL	0x07FF_86A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				flux_timer_cfg												flux_timer_inter															
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:17]	RW	flux_timer_cfg	Traffic limit time interval counter, which is used to count the frequency division clock generated by flux_timer_inter. If this counter is set to 0, traffic limit is not performed.
[16:0]	RW	flux_timer_inter	Traffic limit time granularity counter, which is used to count the ETH working clock (for details, see the PERI_CRG59 register). The default field value is 100000. For example, if the default ETH working clock is 54 MHz and the time granularity is 1 ms, this field is set to 54000, which is calculated as follows: 1 ms/(1/54 MHz) = [1 x 10^(-3)]/[(1/54) x 10^(-6)]=54 x 10^3=54000

UD_GLB_FC_RXLIMIT

UD_GLB_FC_RXLIMIT is a traffic control limit configuration register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0374	UD_GLB_FC_RXLIMIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												flux_cfg																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	flux_cfg	Traffic limit upper threshold register. This group of bits is used to limit the number of frames received by software in the traffic limit time interval. The frames received after the configured upper threshold is exceeded are selectively discarded or received according to the configuration. When this group of bits is all set to 0, it indicates that traffic limit is not performed.

UD_GLB_FC_DROPCTRL

UD_GLB_FC_DROPCTRL is a packet drop control register for traffic limit.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0378	UD_GLB_FC_DROPCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													flux_	flux_	broa
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	flux_uni	Whether unicast packets are discarded when the upper threshold of traffic limit is exceeded 0: Do not discard unicast packets. 1: Discard unicast packets.
[1]	RW	flux_multi	Whether multicast packets are discarded when the upper threshold of traffic limit is exceeded 0: Do not discard multicast packets. 1: Discard multicast packets.

[0]	RW	flux_broad	Whether broadcast packets are discarded when the upper threshold of traffic limit is exceeded 0: Do not discard broadcast packets. 1: Discard broadcast packets.

UD_GLB_RX_COE_EN

UD_GLB_RX_COE_EN is an RX COE enable register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0380	UD_GLB_RX_COE_EN	0x8000_E000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_coe_en	reserved															iphrd_drop	pro_drop	I6udp_drop	reserved												
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	rx_coe_en	COE enable in the RX direction
[30:16]	RO	reserved	Reserved
[15]	RW	iphdr_drop	Packet discarding enable when a checksum error occurs in the IPv4 IP header 0: The packet is transparently transmitted. 1: The packet is discarded.
[14]	RW	pro_drop	TCP/UDP packet discarding enable when a checksum error occurs 0: The packet is transparently transmitted. 1: The packet is discarded.
[13]	RW	i6udp_drop	Discarding enable for the invalid IPv6 UDP packet when the checksum domain is 0 0: The packet is transparently transmitted. 1: The packet is discarded.
[12:0]	RO	reserved	Reserved

5.6.4 Description of the Statistics Counter Control Registers

UD_STS_PORTCNT

UD_STS_PORTCNT is a port status counter.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0584	UD_STS_PORTCNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	rxsof_cnt	rxeof_cnt	rxcrcok_cnt	rxcrcbad_cnt	txsof_cnt	txeof_cnt	txcrcok_cnt	txcrcbad_cnt
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	rxsof_cnt	Count of the frame headers received by the port
[27:24]	RO	rxeof_cnt	Count of the frame trailers received by the port
[23:20]	RO	rxcrcok_cnt	Count of the frames without CRC errors received by the port
[19:16]	RO	rxcrcbad_cnt	Count of the frames with CRC errors received by the port
[15:12]	RO	txsof_cnt	Count of the frame headers transmitted by the port
[11:8]	RO	txeof_cnt	Count of the frame trailers transmitted by the port
[7:4]	RO	txcrcok_cnt	Count of the frames without CRC errors transmitted by the port
[3:0]	RO	txcrcbad_cnt	Count of the frames with CRC errors transmitted by the port

UD_PORT2CPU_PKTS

UD_PORT2CPU_PKTS is a register for the total number of packets received by the CPU from the uplink or downlink port.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A0	UD_PORT2CPU_PKTS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				pkts_cpu			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	WC	pkts_cpu	Total number of the packets received by the CPU port from the uplink or downlink port. Writing 0 clears this register. Writing 1 has no effect.

UD_CPU2IQ_ADDRCNT

UD_CPU2IQ_ADDRCNT is a register for the count of configuring packet receiving address queue by the CPU.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A4	UD_CPU2IQ_ADDRCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																addr_cpu															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	WC	addr_cpu	Count of configuring packet receiving address queue by the CPU successfully. Writing 0 clears this register. Writing 1 has no effect.

UD_RX_IRQCNT

UD_RX_IRQCNT is a register for the count of reporting single-packet interrupt by the uplink or downlink port.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05A8	UD_RX_IRQCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pkts_port															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	WC	pkts_port	Count of the frame RX interrupts reported by the uplink or downlink port. Writing 0 clears this register. Writing 1 has no effect.

UD_CPU2EQ_PKTS

UD_CPU2EQ_PKTS is a register for the total number of packets transmitted by the CPU to the uplink or downlink port.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x05AC	UD_CPU2EQ_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																pkts_cpu2tx															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	WC	pkts_cpu2tx	Total number of packets transmitted by the CPU to the uplink or downlink port. Writing 0 clears this register. Writing 1 has no effect.

5.6.5 Description of the Statistics Result Registers

Statistics result registers can be configured in two modes: read only and read clear. If UD_MAC_SET[cntr_rdclr_en] is set to 1, it indicates the read clear mode. If UD_MAC_SET[cntr_rdclr_en] is set to 0, it indicates the read only mode. The following registers are described only in read only mode.

UD_RX_DVCNT

UD_RX_DVCNT is an RXDV rising edge count register.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0600	UD_rx_DVCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rxdvrise																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rxdvrise	Count of all RXDV rising edges

UD_RX_OCTS

UD_RX_OCTS is a register for the total number of bytes received.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0604	UD_RX_OCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ifinoctets																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifinoctets	Count of all received bytes, including the bytes in correct frames, error frames, and preambles. The frames without valid start of frame delimiters (SFDs) are not counted.

UD_RX_RIGHTOCTS

UD_RX_RIGHTOCTS is a register for the total number of bytes of received correct packets.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0608	UD_RX_RIGHTOCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_rx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	octets_rx	Count of the received bytes, including the bytes in correct frames and error frames but excluding the bytes in preambles. The frames without valid SFDs are not counted.

UD_HOSTMAC_PKTS

UD_HOSTMAC_PKTS is a register for the number of packets matching the local MAC address.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x060C	UD_HOSTMAC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	local_mac_match																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	local_mac_match	Count of correct RX frames whose destination MAC address is the same as the local MAC address, excluding short frames, long frames, frames with CRC errors, pause frames, and error TX frames.

UD_RX_RIGHTPKTS

UD_RX_RIGHTPKTS is a register for the total number of packets received by the port.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0610	UD_RX_RIGHTPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	pkts	Count of all frames

UD_RX_BROADPKTS

UD_RX_BROADPKTS is a register for the number of correct broadcast packets.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0614	UD_RX_broadpkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	broadcastpkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	broadcastpkts	Count of broadcast frames with valid length and without CRC errors, excluding pause frames and error TX frames

UD_RX_MULTPKTS

UD_RX_MULTPKTS is a register for the number of correct multicast packets.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0618	UD_RX_multpkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	multicastpkts																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	multicastpkts	Count of multicast frames with valid length and without CRC errors, excluding pause frames and error TX frames

UD_RX_UNIPKTS

UD_RX_UNIPKTS is a register for the number of correct unicast packets.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x061C	UD_RX_UNIpkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifinucastpkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifinucastpkts	Count of unicast frames with valid length and without CRC errors, excluding pause frames and error TX frames

UD_RX_ERRPKTS

UD_RX_ERRPKTS is a register for the total number of incorrect packets.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0620	UD_RX_ERRPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifinerrors																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifinerrors	Count of all error frames, including frames with CRC errors, short frames, long frames, and error TX frames

UD_RX_CRCERR_PKTS

UD_RX_CRCERR_PKTS is a register for the count of CRC errors.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0624	UD_RX_crcerr_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	crcerr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	crcerr	Count of RX frames with valid length (non short and long frames) but with CRC or alignment errors

UD_RX_LENERR_PKTS

UD_RX_LENERR_PKTS is a register for the number of packets with invalid length.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0628	UD_RX_LENERR_pkts	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	abnormalsizepkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	abnormalsizepkts	Count of frames (short frames and long frames) with invalid length (less than the set minimum valid length or greater than the set maximum valid length)

UD_RX_OCRCERR_PKTS

UD_RX_OCRCERR_PKTS is a register for the number of packets with odd nibbles and CRC errors.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x062C	UD_RX_OCRCERR_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3alignmenterr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3alignmenterr	Received frames with odd nibbles and CRC errors

UD_RX_PAUSE_PKTS

UD_RX_PAUSE_PKTS is a register for the number of received pause packets.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0630	UD_RX_PAUSE_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3pause																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3pause	Count of received pause frames

UD_RF_OVERCNT

UD_RF_OVERCNT is a register for the count of RXFIFO overflow events.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0634	UD_RF_OVERCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dropevents																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dropevents	Accumulative count of RXFIFO overflow events during the reception of frames

UD_FLUX_TOL_IPKTS

UD_FLUX_TOL_IPKTS is a register for the total number of received packets allowed by the traffic limit.

The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0638	UD_flux_TOL_IPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_frame_cnt																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_frame_cnt	Total count of correct RX frames allowed by the traffic limit, excluding short frames, long frames, frames with CRC errors, pause frames, and error TX frames

UD_FLUX_TOL_DPKTS

UD_FLUX_TOL_DPKTS is a register for the total number of packets discarded due to traffic limit. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x063C	UD_flux_TOL_DPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	flux_drop_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	flux_drop_cnt	Count of correct frames discarded due to traffic limit, excluding short frames, long frames, frames with CRC errors, pause frames, and error TX frames

UD_MN2CPU_PKTS

UD_MN2CPU_PKTS is a register for the number of packets not forwarded to the CPU port due to MAC limit. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x064C	UD_MN2CPU_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mac_not2cpu_pkts																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	mac_not2cpu_pkts	Number of packets not forwarded to the CPU port due to MAC limit

UD_TX_PKTS

UD_TX_PKTS is a register for the total number of packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0780	UD_TX_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	pkts_tx	Count of all configured TX frames, excluding the frames discarded due to timeout and the TX frames whose length of UD_GLB_EQFRM_LEN is not within valid range

UD_TX_BROADPKTS

UD_TX_BROADPKTS is a register for the number of broadcast packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0784	UD_TX_BROADPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	broadcastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	broadcastpkts_tx	Count of broadcast frames transmitted successfully (excluding retransmission)

UD_TX_MULTPKTS

UD_TX_MULTPKTS is a register for the number of multicast packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0788	UD_TX_MULTPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	multicastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	multicastpkts_tx	Count of multicast frames transmitted successfully (excluding retransmission)

UD_TX_UNIPKTS

UD_TX_UNIPKTS is a register for the number of unicast packets transmitted successfully. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x078C	UD_TX_UNIPKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ifoutucastpkts_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ifoutucastpkts_tx	Count of unicast frames transmitted successfully (excluding retransmission)

UD_TX_OCTS

UD_TX_OCTS is a register for the total number of transmitted bytes. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0790	UD_TX_OCTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	octets_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	octets_tx	Total count of transmitted bytes, including the bytes of retransmit frames, correct frames, and error frames, but excluding the preamble bytes

UD_TX_PAUSE_PKTS

UD_TX_PAUSE_PKTS is a register for the number of transmitted pause frames. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0794	UD_TX_PAUSE_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3outpause																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3outpause	Count of transmitted pause frames

UD_TX_RETRYCNT

UD_TX_RETRYCNT is a register for the total count of retransmission. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x0798	UD_TX_RETRYCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	retry_times_tx																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	retry_times_tx	Total count of retransmissions of TX frames

UD_TX_COLCNT

UD_TX_COLCNT is a register for the total count of collisions. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x079C	UD_TX_COLCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	collisions																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	collisions	Count of collisions

UD_TX_LC_PKTS

UD_TX_LC_PKTS is a register for the number of packets with late collision. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A0	UD_TX_LC_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3latecol																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3latecol	Count of packets with late collision

UD_TX_COLOK_PKTS

UD_TX_COLOK_PKTS is a register for the number of packets transmitted successfully with collisions. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A4	UD_TX_COLOK_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3col_ok																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3col_ok	Count of packets transmitted successfully with collisions

UD_TX_RETRY15_PKTS

UD_TX_RETRY15_PKTS is a register for the number of packets discarded due to more than 15 times of retransmission. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07A8	UD_TX_RETRY15_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3excessivecol																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3excessivecol	Count of the packets discarded due to more than 15 times of retransmission

UD_TX_RETRYN_PKTS

UD_TX_RETRYN_PKTS is a register for the number of packets with the count of collisions being equal to the threshold. The register does not support soft reset.

Offset Address	Register Name	Total Reset Value
0x07AC	UD_TX_RETRYN_PKTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dot3colcnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	dot3colcnt	Count of packets with the count of collisions being equal to the threshold. This register is set by UD_MAC_SET[colthreshold]

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6 Video Encoder

6.1 Overview

The video encoder supports various protocols, including H.265, H.264, JPEG, and MJPEG. It consists of the VEDU and JPGE. The VEDU implements H.265/H.264 encoding, whereas the JPGE implements JPEG/MJPEG encoding.

6.2 VEDU

6.2.1 Overview

The VEDU is an encoder that supports H.265 and H.264 protocol and performs encoding by using hardware. It features low CPU usage, low bus bandwidth, short delay, and low power consumption.

6.2.2 Features

The VEDU has the following features:

- Supports ITU-T H.265 main profile @level 5.1 main-tier encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Encoding of multiple reference frames and the long-term reference frame
  - Four prediction unit (PU) types of 64x64, 32x32, 16x16, and 8x8 for inter-prediction
  - Four PU types of 32x32, 16x16, 8x8, and 4x4 for intra-prediction
  - Skip mode and merge mode with a maximum of two candidate points to be merged
  - Four transform unit (TU) types of 32x32, 16x16, 8x8, and 4x4
  - CABAC entropy encoding
  - De-blocking filtering
  - Sample adaptive offset (SAO)
  - IPCM encoding
- Supports ITU-T H.264 high profile /main profile/baseline profile @level 5.0 encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Encoding of multiple reference frames and the long-term reference frame

  - Two prediction unit (PU) types of 16x16, and 8x8 for inter-prediction
  - Four PU types of 16x16, 8x8, and 4x4 for intra-prediction
  - Trans4x4 and trans8x8
  - CABAC and CAVLC entropy encoding
  - De-blocking filtering
  - IPCM encoding
- Supports H.264 scalable video coding (SVC) time-domain layering (SVC-T).
- Supports the input picture format of semi-planar YCbCr4:2:0.
- Supports H.265/H.264 multi-stream encoding. The performance is as follows:
  - 1920 x 1080@45 fps
  - 1920 x 1080@30 fps+720 x 480@30 fps+360 x 240@30 fps
- Supports configurable picture resolutions.
  - Minimum picture resolution: 128 x 128 (H.265) or 256 x 128 (H.264)
  - Maximum picture resolution: 1920 x 1296
  - Step of the picture width or height: 2
- Supports region of interest (ROI) encoding.
  - A maximum of eight ROIs
  - Independent enable/disable control for the encoding function of each ROI
- Supports on-screen display (OSD) encoding protection that can be enabled or disabled.
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of eight regions
  - OSD overlapping with the maximum size of the source picture and within the picture position range
  - 129-level alpha blending
  - OSD overlaying control
- Supports color-to-gray encoding.
- Supports three bit rate control modes: constant bit rate (CBR), variable bit rate (VBR) and FIXQP.
- Supports the output bit rate ranging from 2 kbit/s to 30 Mbit/s.

CAUTION

The VEDU encoding protection function applies only to the OSD overlaid on the VEDU.

6.2.3 Function Description

Figure 6-1 shows the functional block diagram of the VEDU.

Based on related protocols and algorithms, the VEDU supports motion estimation, inter-prediction, intra-prediction, motion vector prediction, transform/quantization, inverse transform/inverse quantization, CABAC encoding, stream generation, de-blocking filtering, and SAO (H.265). The ARM software controls the bit rate and handles interrupts.

Before the VEDU is enabled for video encoding, software allocates three types of buffers for the VEDU in the external DDR SDRAM:

- Input picture buffer

  The VEDU reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the VICAP module.

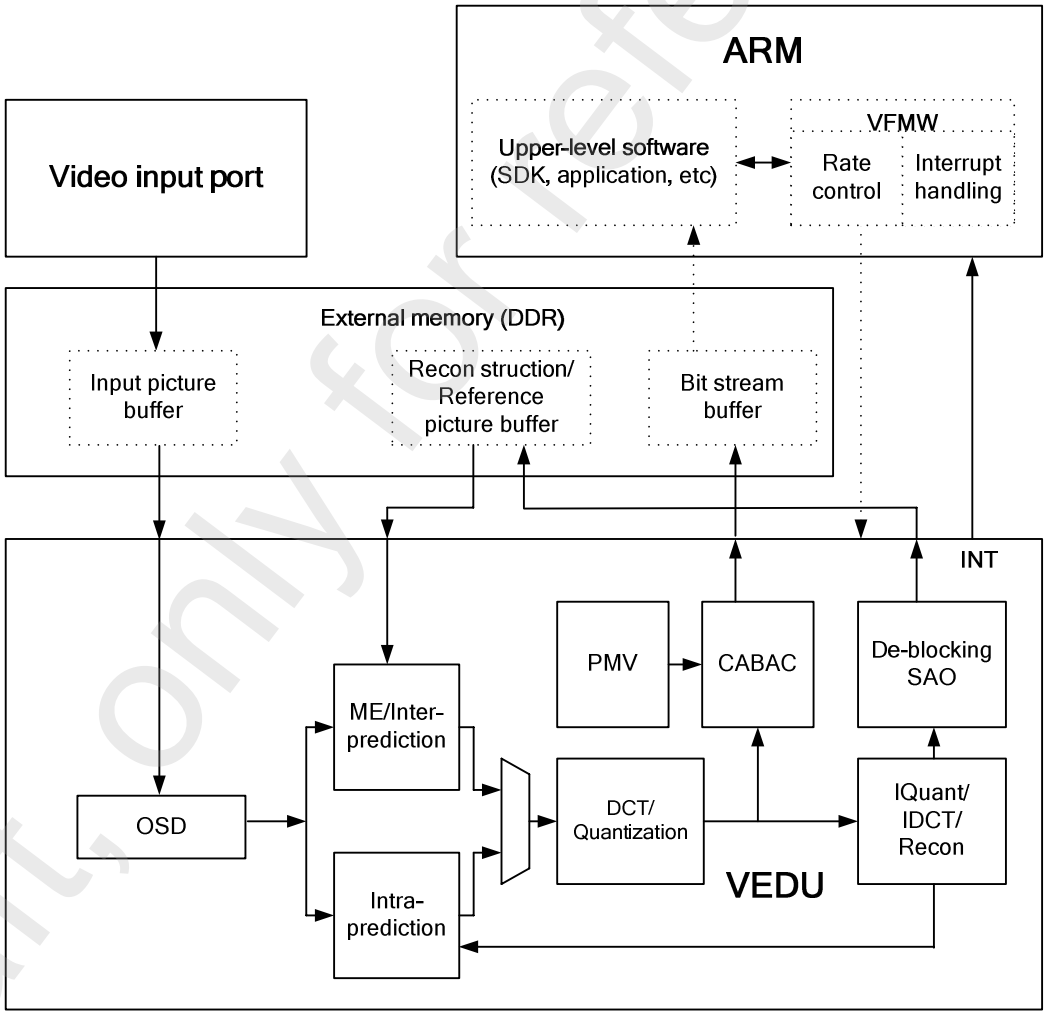
- Reconstruction/Reference picture buffer

  The VEDU writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.

- Stream buffer

  This buffer stores encoded streams. The VEDU writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-1 Encoding functional block diagram of the VEDU



6.3 JPGE

6.3.1 Overview

The JPGE provides high-performance encoding performance by using hardware. It supports 67.1-megapixel snapshot or HD MJPEG encoding.

6.3.2 Features

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding.
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
- Supports JPEG encoding of 1080p@15 fps.
- Supports configurable picture resolutions.
  - Minimum picture resolution: 32 x 32
  - Maximum picture resolution: 8192 x 8192
- Supports the picture width or height step of 4.
- Supports configurable quantization tables.
- An independent quantization table for the Y component, Cb component, and Cr component respectively
- Supports the color-to-gray function.
- Supports the MJPEG output bit rate ranging from 2 kbit/s to 30 Mbit/s.

6.3.3 Function Description

Figure 6-2 shows the functional block diagram of the JPGE.

Based on the protocols that require a large number of operands, the JPGE supports level shift, discrete cosine transform (DCT), quantization, scanning, VLC encoding, and stream generation. The VFMW configures quantization tables and handles interrupts.

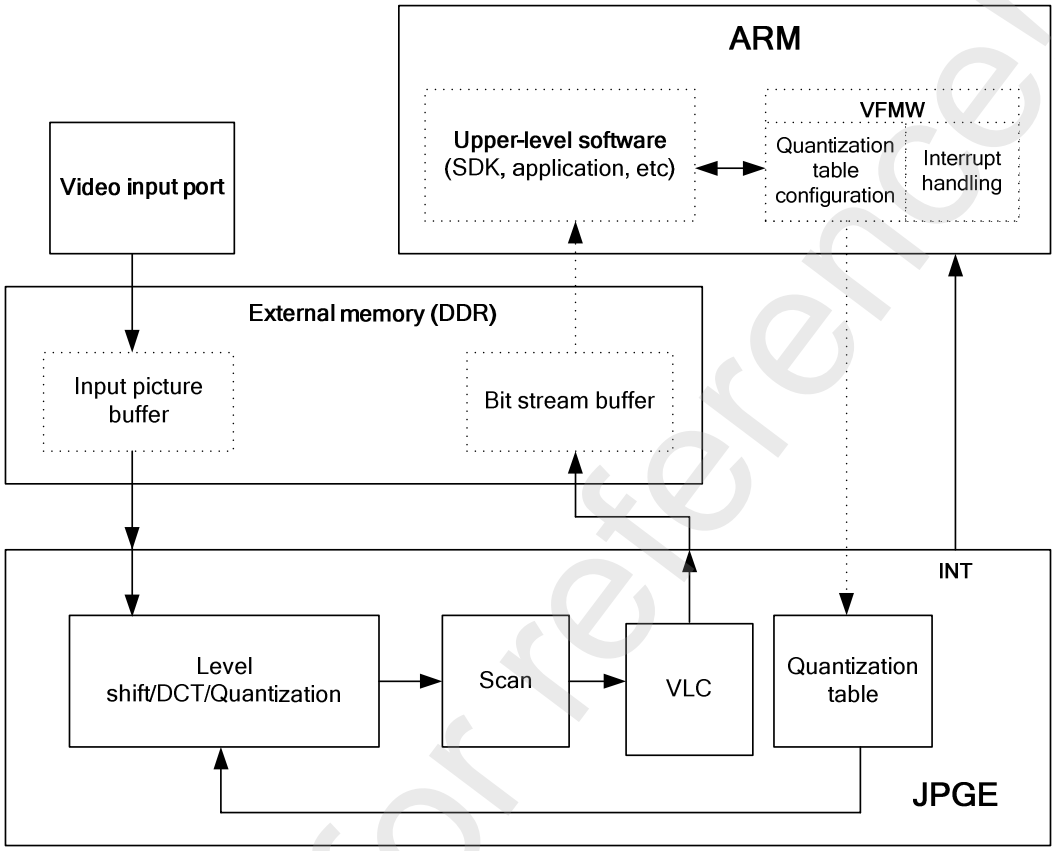
Before the JPGE is enabled for video encoding, the software allocates two types of buffers for the JPGE in the external DDR SDRAM:

- Input picture buffer

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the VICAP module.
- Stream buffer

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

Figure 6-2 Encoding functional block diagram of the JPGE



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7 Video and Graphics Processing

7.1 VPSS

7.1.1 Overview

The video processing subsystem (VPSS) implements video processing. It supports Gaussian 3D adaptive noise reduction (NR), video sharpening, video covering, demosaic, video cropping, scaling, single-component luminance processing, compression/decompression, mirroring, and flipping.

The VPSS has the following features:

- Processing of video sources with 2048-pixel width using a single frame in online or offline mode
- A maximum of three video output channels
- Gaussian 3D adaptive NR
- Video sharpening
- Output of eight video regions covered by solid quadrilaterals (the concave quadrilateral is converted into a triangle)
- Output of four regions with demosaic processing
- Video cropping of two output channels (channel 1 and channel 2)
- Input of compressed video data
- Output of compressed video data (only channel 0 and channel 1)
- Register configuration using the linked list in offline mode and register configuration using the APB in online mode
- Input and output data in the format of semi-planar 420, semi-planar 422, or single-component
- Outstanding configuration
- Low-power mode
- Low delay
- Single-component luminance processing

7.1.2 Features

The following describes the major features:

- Gaussian NR: The NR module removes the Gaussian noises from pictures by configuring parameters. Then pictures become smooth and the encoding bit rate is reduced.
- Scaling: Low-frequency filtering is supported when the input and output resolutions are different. In online mode, the large stream channel (channel 0) supports only 1:1 scaling, whereas other channels support zoom-out or 1:1 scaling and do not support zoom-in. In offline mode, only the large stream channel (channel 0) supports zoom-in (at most 16x zoom-in) or 1:1 scaling, whereas other channels support zoom-out (at most 15x zoom-out) or 1:1 scaling.

7.2 VGS

7.2.1 Overview

The video graphics system (VGS) implements video and graphics processing. The functions include on-screen display (OSD) overlaying, scaling, statistics of the region luminance sum, video cropping, video covering, rotation, color inversion and fast transfer of the graphics OSD, and lens distortion correction (LDC).

The VGS has the following features:

- Processing of video sources with the 2048-pixel width by using a single frame in offline mode
- One video output channel
- Overlaying of the OSD and video in one region
- OSD input format of ARGB1555, ARGB4444, or ARGB8888
- Configuration of register linked lists
- Linear storage for the input/output data
- Compressed storage of video data for the input/output
- Rotation by 90°, 180° or 270°
- (Vertical) LDC
- One video region covered by the solid or dashed quadrilateral (the concave quadrilateral is converted into a triangle)
- Video cropping
- Outstanding configuration
- Low-power mode
- Statistics of the region luminance sum
- Single-component luminance processing
- Graphics OSD scaling. The maximum width is 1024.
- Color inversion of the graphics OSD
- Fast transfer

7.2.2 Features

The following describes the major features:

- Video covering: A video region is covered by the solid or dashed quadrilateral (the concave quadrilateral is converted into a triangle).
- Scaling: Low-frequency filtering is supported when the input and output resolutions are different. At most 15x zoom-out and 16x zoom-in are supported.

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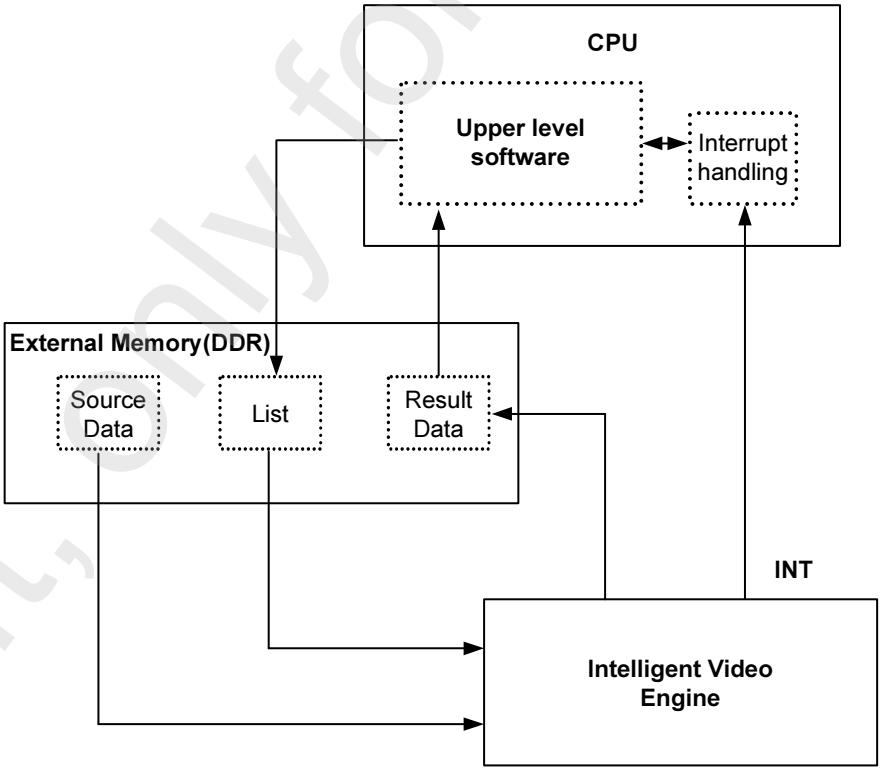
8 Intelligent Video Engine

8.1 IVE

8.1.1 Overview

The intelligent video engine (IVE) module is used to accelerate hardware processing. It provides a series of basic calculation functions and some time-consuming functions used in the intelligent analysis algorithm.

Figure 8-1 Position of the IVE in the system



8.1.2 Function Description

The IVE has the following features:

- DMA: Supports direct copying, alternative copying, and memory filling.
- Filter: Supports 5x5 template filtering.
- Color space conversion (CSC): Supports the color space conversion of YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV.
- FilterAndCSC: Combines 5x5 template filtering and CSC.
- Sobel: Supports the Sobel-like gradient calculation of 5x5 template.
- MagAndAng/Canny: Supports 5x5 template calculation and Canny edge extraction.
- Erode: Supports 5x5 template erode.
- Dilate: Supports 5x5 template dilate.
- Thresh\Thresh_S16\Thresh_U16: Supports image thresh processing.
- And\Or\Xor: Supports the AND, OR, or XOR operation on two images.
- Add\Sub: Deals with the weighted plus and minus of two images.
- Integ: Supports the integral calculation.
- Hist: Supports the histogram statistics.
- Map: Assigns values to images by using 256-level mapping.
- 16BitTo8Bit: Performs linear conversion from 16-bit data to 8-bit data.
- OrdStatFilter: Supports the sequence statistic filtering, including the median filtering, maximum filtering, and minimum filtering.
- NCC: Calculates the correlation coefficients of two images with the same size.
- CCL: Marks connected regions.
- GMM: Creates the GMM for a gray image and RGB image.
- NormGrad: Performs a normalized gradient calculation.
- GradFg: Supports the gradient foreground calculation.
- MatchBgModel\UpdateBgModel: Supports background match and background refresh.
- SAD: This function calculates the accumulated sum of the absolute pixel differences corresponding to two images by block.
- GMM2: Creates the GMM quickly for the gray scale image and RGB image.
- Supports separate soft reset.
- Supports 128-bit AXI bus and 32-bit APB.
- Supports linked-list interrupt, node interrupt, and timeout interrupt.
- Supports input formats including SP400, semi-planar 420 (SP420), semi-planar 422 (SP422), package, and planar.
- Supports output formats including SP 400, SP420, SP422, package, and planar.
- Supports non-16-byte-aligned read and write addresses for some operators.

8.1.3 Operating Mode

8.1.3.1 Input and Output Data Formats

The w and h in Figure 8-2 to Figure 8-12 indicate the width and height of images in pixels. Unless otherwise specified, the sequence for storing data is the same as that in the little endian

system. The following sections use word as the storage unit. In actual applications, the data alignment format varies with operators. The input and output format for operators described in section 8.1.3.2 "Supported Functions" are also different.

Figure 8-2 SP422 storage format

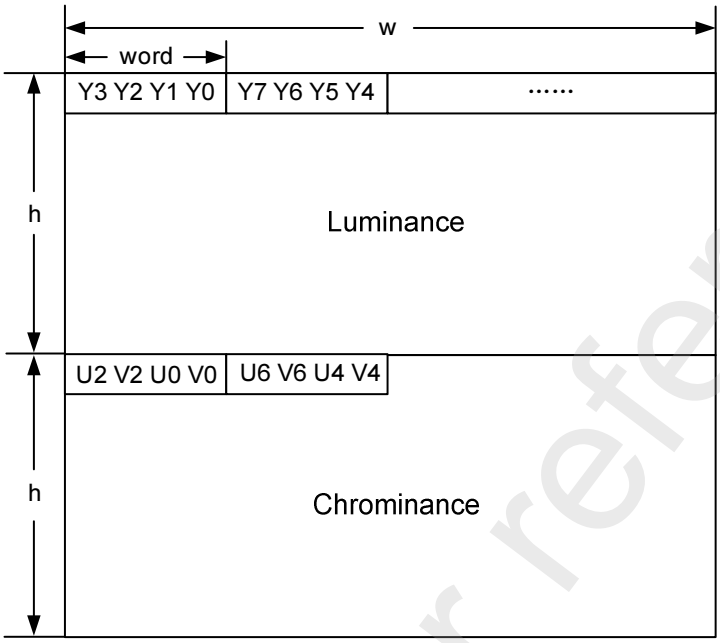


Figure 8-3 SP420 storage format

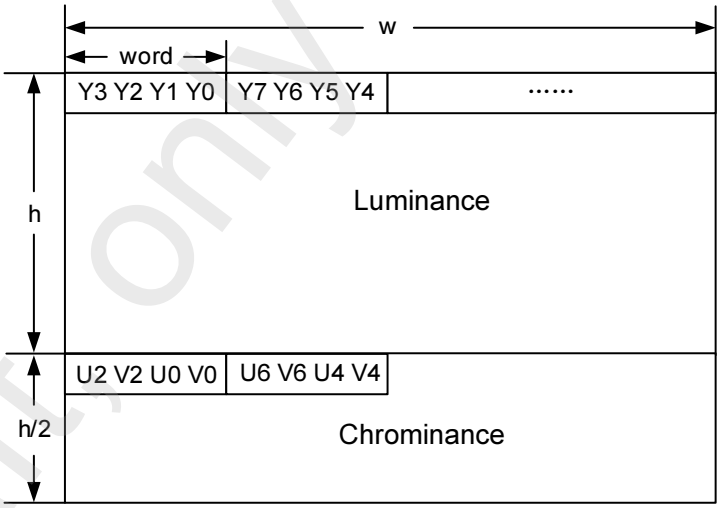


Figure 8-4 Storage format of the 8-bit single component data in the memory

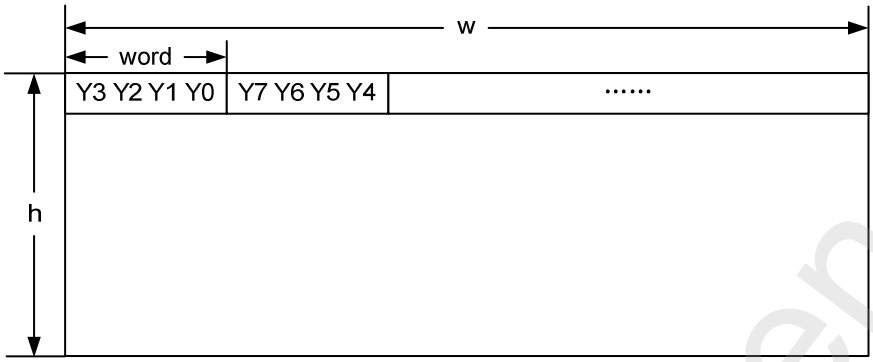


Figure 8-5 Package storage format

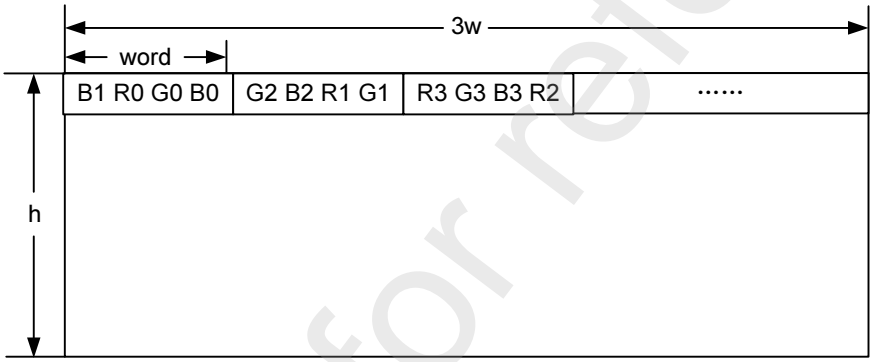


Figure 8-6 Planar storage format

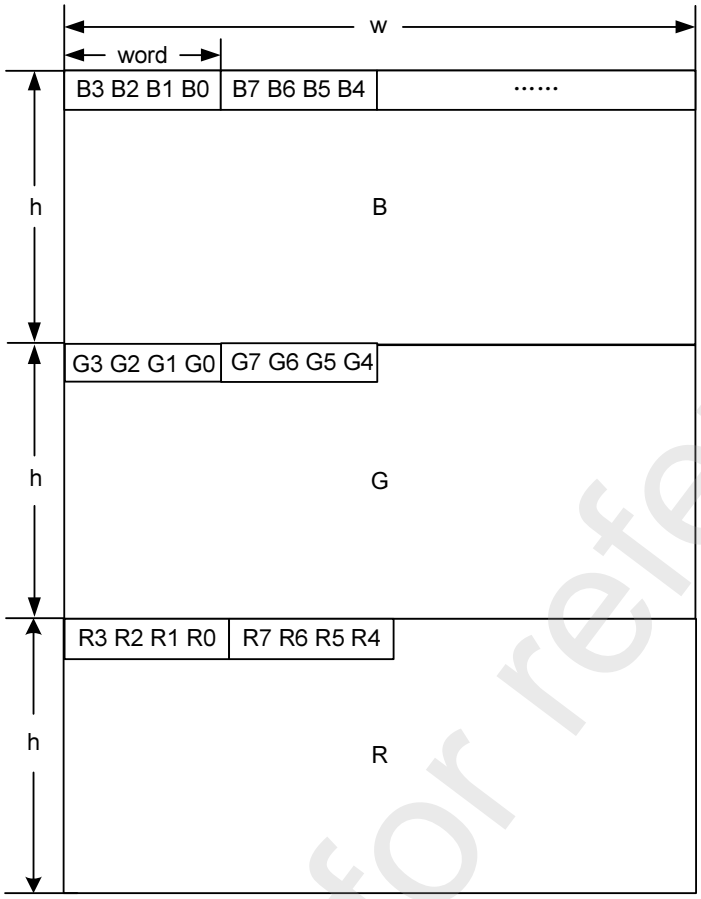


Figure 8-7 Storage format of the 16-bit single component data in the memory

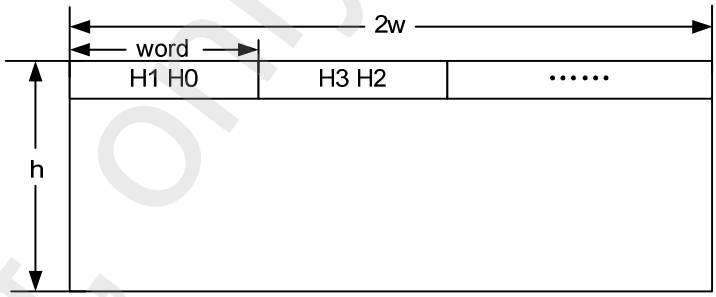


Figure 8-8 Storage format of the 32-bit single component data in the memory

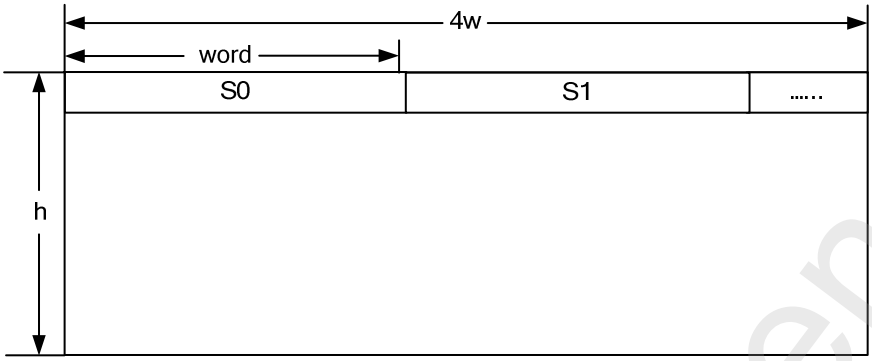


Figure 8-9 Storage format of the 64-bit single component data in the memory

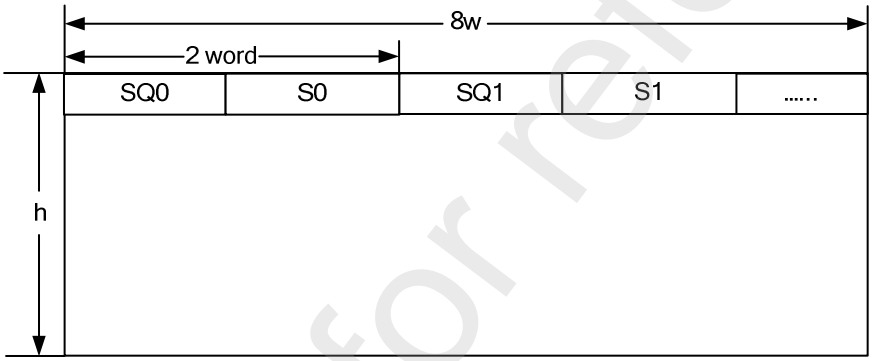


Figure 8-10 Storage format of NCC output data in the memory

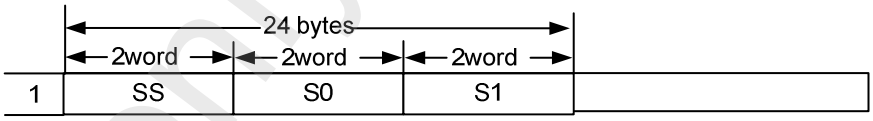
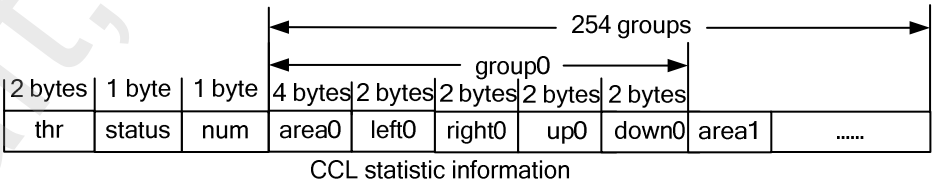
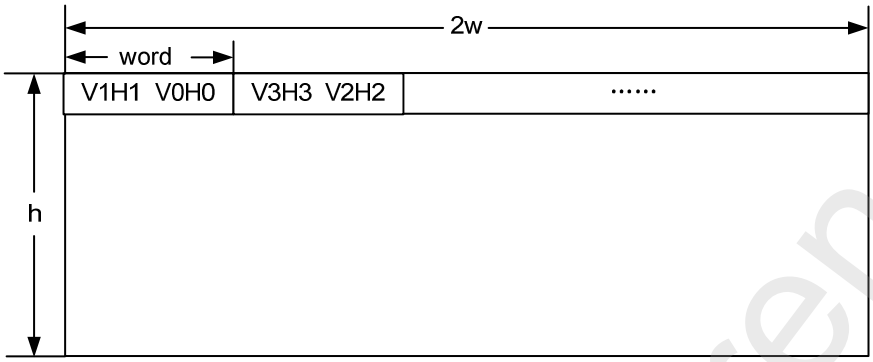


Figure 8-11 Storage format of CCL statistics in the memory (in sequence)



CCL statistic information

Figure 8-12 Storage format of 16-bit interleaving data (in the horizontal and vertical directions) in the memory



8.1.3.2 Supported Functions

NOTE

For details about the resolutions supported by operators described in this section, see the *HiIVE API Reference*.

DMA

1. Direct copy mode

This mode allows you to quickly transfer the data of rectangle regions. In this mode, the source data is transferred to the destination region through the internal fast channel, and directly overwrites the data of the destination region.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.

2. Alternative copy mode

This mode allows you to transfer the data of rectangle regions indirectly. In this mode, the source data with a specified size is transferred to the destination region at a specified distance in horizontal and vertical directions.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.
- Others: The width of the source data must be an integral multiple of the distance.

3. Memset mode (3 bytes)

This mode allows you to set the memory in rectangle regions, and fill the destination region by three bytes.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.

- Input and output formats: No input data is available. The output is 8-bit single component data, as shown in Figure 8-4.

4. Memset mode (8 bytes)

This mode allows you to set the memory in rectangle regions, with 8 byte as the unit for filling the target region.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: No input data is available. The output is 8-bit single component data, as shown in Figure 8-4.

Filter

The filter function allows the output of the source image after filtering it based on the 5x5 template.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- The following lists the three input and output formats:
  - Both the input and output are 8-bit single component data, as shown in Figure 8-4.
  - Both the input and output are SP420 data, as shown in Figure 8-3.
  - Both the input and output are SP422 data, as shown in Figure 8-2.

CSC

The CSC among YUV2RGB, YUV2HSV, YUV2LAB, and RGB2YUV is supported.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - SP420 > package; SP420 > planar
  - SP422 > package; SP422 > planar
  - Package > SP420; package > SP422
  - planar > SP420; planar > SP422

  Figure 8-3 and Figure 8-2 show the SP420 format and SP422 format respectively.

  Figure 8-5 shows the package format.

  Figure 8-6 shows the planar format.

FilterAndCSC

The FilterAndCSC function indicates that the YUV SP420/SP422 images are filtered based on the 5x5 template and then the color space is converted into YUV2RGB for output.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - SP420 > package; SP420 > planar
  - SP422 > package; SP422 > planar

Figure 8-3 and Figure 8-2 show the SP420 format and SP422 format respectively. Figure 8-5 shows the package format. Figure 8-6 shows the planar format.

Sobel

This function implements vertical and horizontal Sobel filtering based on the 5x5 template.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is an 8-bit single component image, as shown in Figure 8-4.
  - Only H or V is outputted, as shown in Figure 8-7.
  - Both H and V are outputted, as shown in Figure 8-7.

MagAndAng

The MagAndAng indicates that gradient magnitude and angle are calculated. It supports the thresh operation for TO_ZERO.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 8-5.
  - The output is the 16-bit single component amplitude image, as shown in Figure 8-7.
  - The output is the 8-bit single component angle image, as shown in Figure 8-4.

Dilate

This function implements dilation of a binary image based on the 5x5 template.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.

Erode

This function implements erosion of a binary image based on the 5x5 template.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.

Thresh

This function performs thresh processing for an image using specified thresh. Eight modes are available.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats: The input and output are 8-bit single component data, as shown in Figure 8-4.

And

This function implements the calculation for source data 2 and 1, and outputs the data to the destination region.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is an 8-bit single component data of source 1.
  - The input is an 8-bit single component data of source 2.
  - The output is the 8-bit single component destination data, as shown in Figure 8-4.

Sub

This function performs the subtraction of the data from sources 2 and 1, and outputs the data to the destination region.

- Resolution: The two input images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - An 8-bit single component minuend.
  - An 8-bit single component subtrahend.
  - The 8-bit single component destination data, as shown in Figure 8-4

Or

This function performs the Or calculation of the data from sources 2 and 1, and outputs the data to the destination region.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The two input images are 8-bit single component images.
  - The output is the 8-bit single component image, as shown in Figure 8-4.

Integral

This function performs the calculation of integral image and square sum integral image, and supports the output of sum integral image, square sum integral image, and the combination of the sum integral image and square sum integral image (the accumulated component sum occupied the lower 28-bit, and the accumulated component square sum occupied the upper 36-bit).

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 8-4.

- As shown in Figure 8-8, if a sum integral image is outputted, the output is a 32-bit single component image. As shown in Figure 8-9, if a square sum integral image is outputted or is outputted by combining with a sum integral image, the output is a 64-bit single component image.

Histogram

This function performs the 256-segment histogram statistics. The input is a single component, and the output is the statistics of a 32 bit wide 256-segment histogram.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 8-bit single component image, as shown in Figure 8-4.
  - The output is the 32-bit single component data of the statistic result, as shown in Figure 8-8.

Thresh_S16

This function implements thresh processing of signed 16-bit data to signed 8-bit data. It supports four comparison modes.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit single component data, as shown in Figure 8-7.
  - The output is the converted 8-bit single component data, as shown in Figure 8-4.

Thresh_U16

This function implements thresh processing of unsigned 16-bit data to unsigned 8-bit data. It supports two comparison modes.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit single component data, as shown in Figure 8-7.
  - The output is the converted 8-bit single component data, as shown in Figure 8-4.

16BitTo8Bit

This function implements linear conversion of 16-bit data to 8-bit data. It supports four comparison modes.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output formats:
  - The input is the 16-bit data, as shown in Figure 8-7.
  - The output is the converted 8-bit data, as shown in Figure 8-4.

OrdStatFilter

Supports median filtering, maximum value filtering, and minimum filtering in sequence based on a 3x3 template.

- Address alignment mode: Input and output strides must be 16-byte-aligned.

- Input and output formats: Both the input and output are 8-bit single component images, as shown in Figure 8-4.

Map

The source data is mapped by using the 256-segment 8-bit unsigned mapping table or 16-bit unsigned/signed mapping table, and the new data is output.

- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single component data, as shown in Figure 8-4.
  - The input is the 8-bit or 16-bit mapping table with a fixed length of 256 entries.
  - The output is the 8-bit single component data or 16-bit data after mapping, as shown Figure 8-4 and Figure 8-7.

Add

This function implements the sum of the weighted values of two gray images. The weight of the two images can be configured independently.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 8-4.
  - The output is the sum of data of 8-bit single component image, as shown Figure 8-4.

Xor

This function performs the Xor operation for two binary image data.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 8-4.
  - The output is the 8-bit single component data after performing the Xor operation, as shown in Figure 8-4.

NCC

This function calculates the cross correlation coefficient of two gray scale images of the same resolution.

- Resolution: The two inputted images should be of the same resolution.
- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the data of two 8-bit single component images, as shown in Figure 8-4.

- The output contains three types of data, namely the accumulative product of two images, accumulative product of square sum of image 1, and the accumulative product of square sum of image 2 (in sequence), as shown in Figure 8-10.

CCL

The eight or four connected regions of the binary image are marked.

- Resolution: Width x Height < 1024 x 1024.
- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component image, as shown in Figure 8-4.
  - The 16-bit output data indicates the minimum area of the output valid connected components.
  - The 8-bit output data indicates whether the area of the detected connected components is greater than the threshold.
  - The output is the coordinate and area of the circumscribed rectangle for each connected component, as shown in Figure 8-11. The original image is changed to an 8-bit single component image after the labeling of the connected components, as shown in Figure 8-4.

GMM

The GMM performs the inputted GMM background modeling for the gray images and RGB package images. Three or five Gauss models are supported.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component image or RGB package image, as shown in Figure 8-4 and Figure 8-5.
  - The input is the model data.
  - The output is the 8-bit single component foreground binary image, as shown in Figure 8-4.
  - The output is the updated model data.
  - The output is the background data and the corresponding input is an 8-bit single component image or RGB package image, as shown in Figure 8-4 and Figure 8-5.

CannyHysEdge

This function performs the threshold processing for the magnetic hysteresis, limited non-maximum values, outputted strong and weak edge image and the strong edge coordinate detected by the Canny edge:

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component angle image, as shown in Figure 8-4.
  - The input is a 16-bit single component amplitude image, as shown in Figure 8-7.
  - The output is an 8-bit single edge mark image, as shown in Figure 8-4.
  - The output is a 32-bit single component data stack, as shown in Figure 8-8.
  - The output is the number of the 32-bit stack.

NormGrad

This function performs the normalized gradient calculation. The gradient components are all normalized to eight bits.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single component data, as shown in Figure 8-4.
  - When out_fmt is set to 0x00, 0x01, or 0x02, the output is the 8-bit single component data, as shown in Figure 8-4. When out_fmt is set to 0x03, the output is the 16-bit interleaving data of H and V, as shown in Figure 8-12.

GradFg

This function calculates the gradient foreground based on the gradient of the background images and current frame images.

- Address alignment mode: Input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the background differential foreground images, as shown in Figure 8-4.
  - The input is the current gradient interleaving images.
  - The input is the background gradient interleaving images, as shown in Figure 8-12.
  - The output is gradient foreground images, as shown in Figure 8-4.

MatchBgModel

This function performs the background model matching based on CodeBook.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is an 8-bit single component current gray image.
  - The input is the foreground status flag (8-bit single component), as shown in Figure 8-4.
  - The input is the 24-byte model data.
  - The output is the background differential foreground image (8-bit single component).
  - The output is the frame differential images (8-bit single component)
  - The output is the forehead status flag (8-bit single component), as shown in Figure 8-4.
  - The output is the 24-byte model data.
  - The output is a 64-bit statistic value.

UpdateBgModel

This function performs the background model refresh based on CodeBook.

- Address alignment mode: The input and output addresses must be byte-aligned, and the input and output strides must be 16-byte-aligned.
- Input and output data formats:

- The input is the foreground status flag (8-bit single component), as shown in Figure 8-4.
- The input is the 24-byte model data.
- The output is the background differential foreground image (8-bit single component).
- The output is a background gray image (8-bit single component)
- The output is a gray image in the change state (8-bit single component)
- The output is a foreground image in the change state (8-bit single component), as shown in Figure 8-4.
- The output is the pixel life period in the change state (16-bit single component), as shown in Figure 8-7.
- The output is the 24-byte model data.
- The output is a 64-bit statistic value.

SAD

This function calculates the accumulated sum of the absolute pixel differences corresponding to two images by block.

- The resolution ranges from 64 x 64 to 1920 x 1080. The width and height of the image must be an integral multiple of the block size.
- Address alignment mode: The input and output addresses and strides must be byte-aligned.
- Input and output data formats:
  - The inputs are two 8-bit single-component images with the same resolution, as shown in Figure 8-4.
  - The results of dst1 and dst2 depend on the configured value of out_fmt:
    a. If out_fmt is set to **0x00**, dst1 indicates the SAD value (16-bit single component) and dst2 indicates the binary image (8-bit single component), as shown in Figure 8-7 and Figure 8-4 respectively.
    b. If out_fmt is set to **0x01**, dst1 indicates the SAD value (8-bit single component) and dst2 indicates the binary image (8-bit single component), as shown in Figure 8-4.
    c. If out_fmt is set to **0x02**, dst1 indicates the SAD value (16-bit single component), as shown in Figure 8-7.
    d. If out_fmt is set to **0x03**, dst1 indicates the SAD value (8-bit single component), as shown in Figure 8-4.
    e. If out_fmt is set to **0x04**, dst1 indicates the thresh result (8-bit single component), as shown in Figure 8-4.

GMM2

The GMM background modeling is implemented. The input can be the gray scale image or RGB package image. The number of Gaussian models can be 1−5.

- Address alignment mode: Input and output addresses and strides must be 16-byte-aligned.
- Input and output data formats:
  - The input is the 8-bit single-component image or RGB package image, as shown in Figure 8-4 and Figure 8-5.

- The input is the 16-bit pixel factor image. The upper eight bits of the pixel factor are the update duration and the lower eight bits are the sensitivity information, as shown in Figure 8-7.
- The input is the model data.
- The output is the 8-bit single-component foreground binary image, as shown in Figure 8-4.
- The output is the updated model data.
- The output is the background image, the type of which is the same as that of the input image.
- The output is the 8-bit model hitting information, as shown in Figure 8-4. The lower one bit indicates whether the model is hit or not, and the upper seven bits indicate the index of the hitting model.

8.1.4 Register Summary

Table 8-1 describes IVE registers.

Table 8-1 Summary of IVE registers (base address: 0x1123_0000)

Offset Address	Register	Description
0x0000	IVE_START	IVE start configuration register
0x0004	INT_EN	IVE interrupt enable register
0x0008	INT_RW	IVE clear interrupt register
0x000C	INT_STATUS	IVE interrupt status register
0x0010	LIST_POINTER	Linked list start address register
0x0014	IVE_STATUS	IVE working status register
0x0018	IVE_TASK_ID	ID register for the tasks processed by the IVE at the previous time
0x0030	NODE_CLK_VALUE	Register for the number of cycles consumed by the preceding node
0x0034	CLK_GT_EN	Clock gating of the IVE internal module
0x0040	NODE_DONE_CNT	Register for the number of processed nodes
0x0044	LIST_DONE_CNT	Register for the number of processed linked lists
0x0054	AXI_INFO	Read and write outstanding number register
0x0060	IVE_OVER_TIME_THR	Overtime interrupt threshold register
0x0064	IVE_OVER_TIME_CNT	Register for the dynamic counting number of the operator working cycle
0x0068	CHAIN_STAT_CLK_VALUE	Register for the number of cycles consumed by the preceding linked list

Offset Address	Register	Description
0x006C	CHAIN_CYCLE_CNT	Register for the counting number of the current linked list cycles

Contents

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9 Video Interfaces

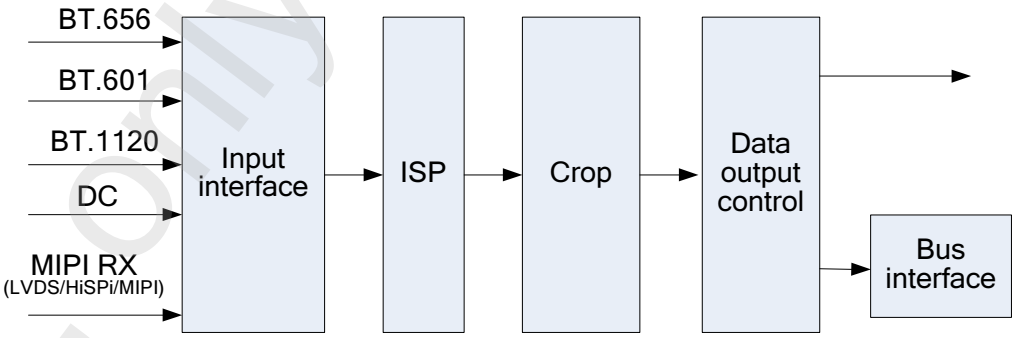
9.1 VICAP

9.1.1 Overview

The video capture (VICAP) module receives video data over the BT.656 interface, BT.601 interface, BT.1120 interface, digital camera (DC) interface, or mobile industry processor interface receiver (MIPI RX), and stores the data in the specified addresses of the memory or transmits the data to the video processing subsystem (VPSS). Note that the MIPI RX includes the MIPI, low-voltage differential signal (LVDS), and high-speed serial pixel interface (HiSPI). The VICAP module has a built-in image signal processor (ISP) that can directly receive external raw data (Bayer RGB data). Figure 9-1 shows the functional block diagram of the VICAP module.

The chip provides an internal VICAP module.

Figure 9-1 Functional block diagram of the VICAP module



9.1.2 Features

The VICAP module has the following features:

- Maximum input resolution of 2048 x 2048 and maximum 198MHz working clock.
- One external interface with maximum 16-bit width
- One internal interface and 1-channel video processing in interlaced or progressive input mode

- BT.656, BT.601, BT.1120, and DC digital interfaces
- MIPI and LVDS analog interfaces and HiSPi timing
- Flash trigger
- Shutter trigger
- Built-in ISP
- CROP
- Data output to the DDR in offline mode or to the VPSS in online mode
- Data output in single-component mode
- Output storage modes
  - Semi-planar YCbCr 4:2:2 mode
  - Semi-planar YCbCr 4:2:0 mode
  - Semi-planar YCbCr 4:0:0 mode
  - RAW mode

9.1.3 RAW Mode Function Description

9.1.3.1 Typical Applications

The VICAP module captures video data in multiple input timings and stores the captured data in the DDR or transmits data to the VPSS online. By using different function modes configured by the system, the VICAP module can be connected to different external VI interfaces.

The VICAP module can process 1-channel input video signal.

The VICAP module supports the following typical inputs:

- One 2M@60 fps input, 2F-WDR line mode, and one 2M@30 fps output
- One 2M@30 fps input, linear mode, and one 2M@30 fps output

9.1.3.2 Function Implementation

ITU-R BT.656 YCbCr4:2:2

1. Horizontal timing

Based on the ITU-R BT.656 protocol, sync signals are included in data streams. The special bytes start of active video (SAV) and end of active video (EAV) indicate the start and end of the active line data respectively. In video data streams, the header of the timing reference code indicates that the following byte is SAV or EAV. The timing reference code consists of FF 00 00. FF and 00 indicate the reserved bytes of the image encoding data, that is, non-image data. Table 9-1 shows the format of the ITU-R BT.656 line data.

Table 9-1 Format of the ITU-R BT.656 YCbCr 4:2:2 line data

Timing Reference Code				Line Blanking Region					Timing Reference Code				YCbCr 4:2:2 with 720 Active Pixels						
FF	00	00	EAV	80	10	…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	…	Cr718	Y719

The difference between the SAV and EAV depends on the special bit H. Both the SAV and EAV include the vertical blanking bit V and field indicator bit F. For details about the SAV and EAV, see Table 9-2.

Table 9-2 Formats of the SAV and EAV

Bit[7]	Bit[6] (F)	Bit[5] (V)	Bit[4] (H)	Bit[3:0] (P3–P0)
Fixed value 1	Field indicator bit 1st field: F = 0 2nd field: F = 1	Vertical blanking bit VBI: V = 1 Active video: V = 0	SAV: H = 0 EAV: H = 1	Check bits

The ITU-R BT.656 protocol defines valid SAV and EAV by using eight valid reserved bits. Four check bits can be used to correct 1-bit error and detect 2-bit errors. Table 9-3 describes the valid SAV and EAV values.

Table 9-3 Valid SAV and EAV values

Encoding	Binary Value	Field Number	Vertical Blanking Interval or Not
SAV	10000000	1	N/A
EAV	10011101	1	N/A
SAV	10101011	1	Yes
EAV	10110110	1	Yes
SAV	11000111	2	N/A
EAV	11011010	2	N/A
SAV	11101100	2	Yes
EAV	11110001	2	Yes

The four valid reserved bits (P0, P1, P2, and P3) provide the error correction function. They are determined by the F, V, and H bits. See Table 9-4.

Table 9-4 ITU-R BT.656 error-correcting codes

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0

F	V	H	P3	P2	P1	P0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

P0 = F^V^H

P1 = F^V

P2 = F^H

P3 = V^H

2. Vertical timing

The positions of the vertical timings are determined by bit F and bit V of the timing reference codes SAV and EAV. Figure 9-2 shows the vertical timing of the 525-line 60 field/s video system, and Figure 9-3 shows the vertical timing of the 625-line 50 field/s video system.

Figure 9-2 Vertical timing of the 525-line 60 field/s video system

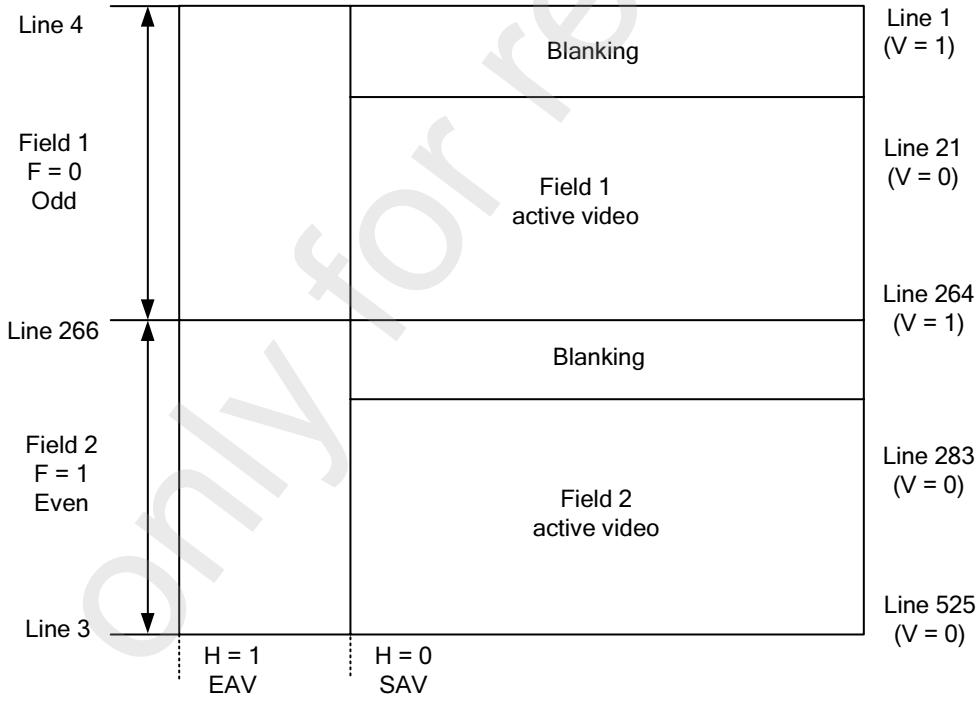
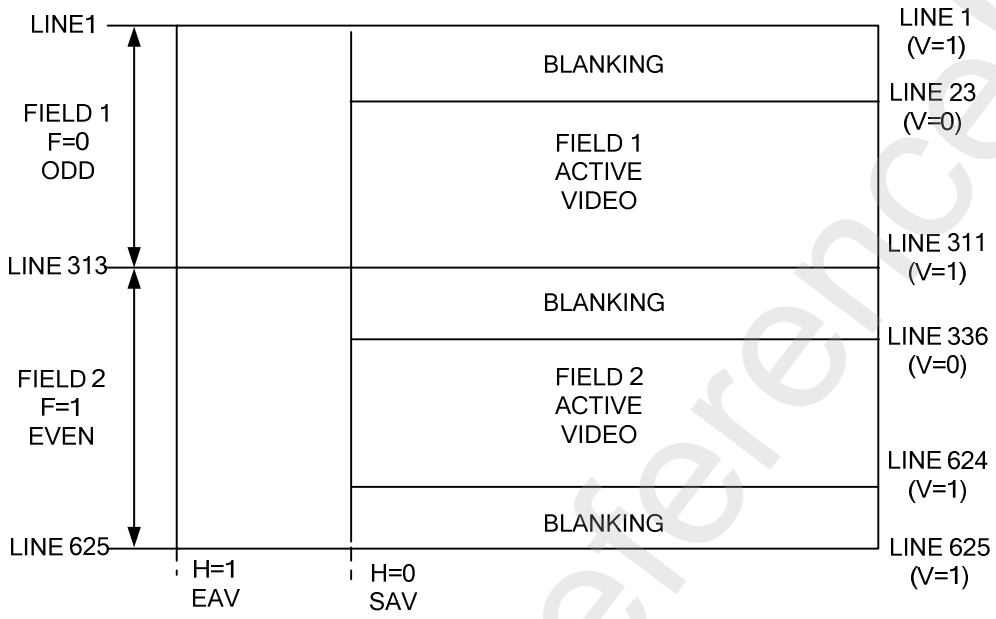


Figure 9-3 Vertical timing of the 625-line 50 field/s video system



NOTE

The VICAP module identifies vertical timings based on SAV and EAV regardless of the lines.

BT.1120 (HD) Interface Timings

The VICAP module supports the HD interface timings with separated Y/C inputs. In this case, two data ports are required. One is used to transfer luminance and the other one is used to transfer chrominance, as shown in Figure 9-4 and Figure 9-5.

Figure 9-4 Horizontal input timing of the HD interface

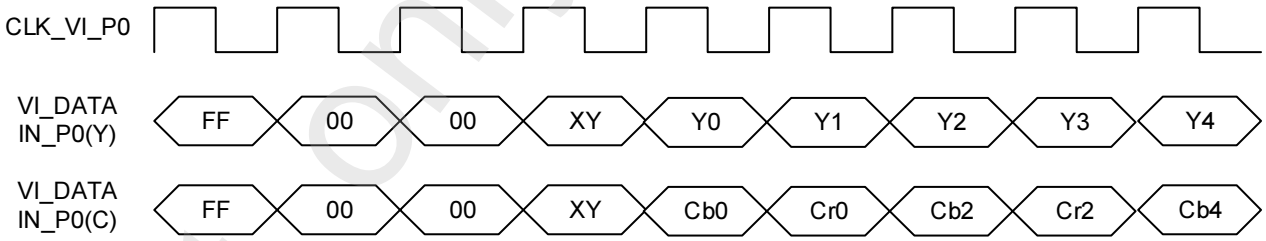
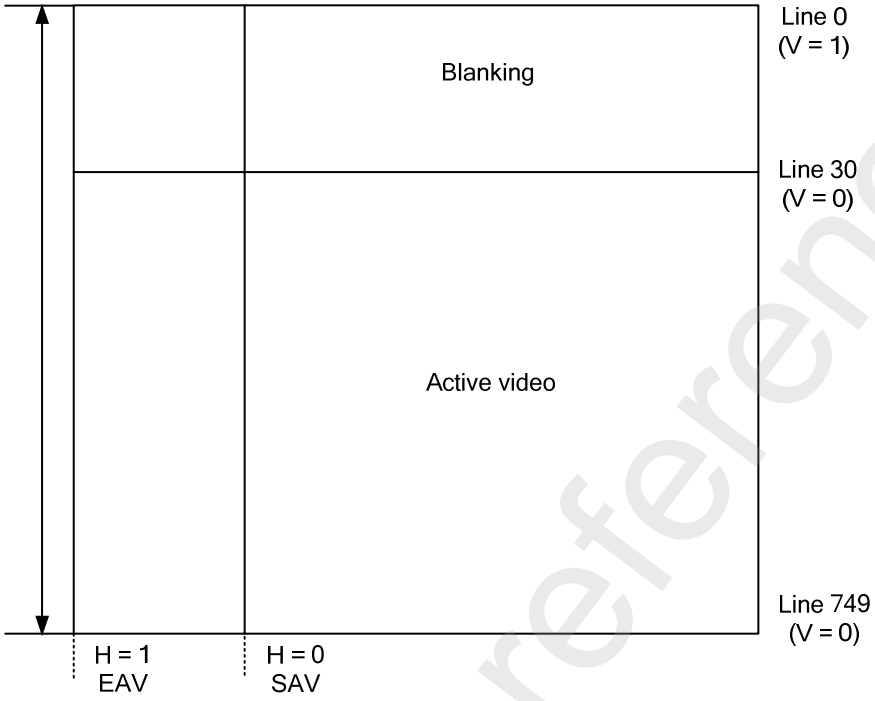


Figure 9-5 Vertical input timing of the HD interface

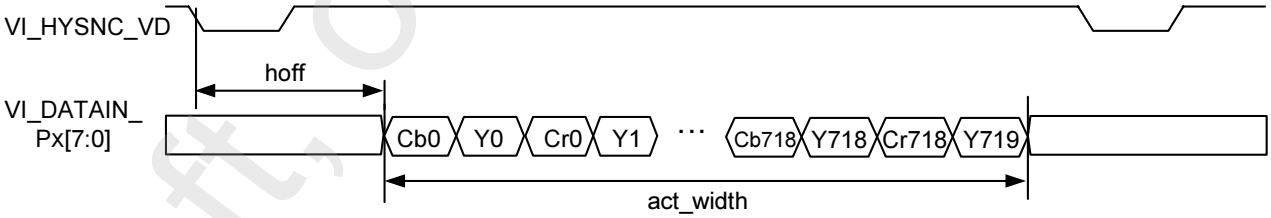


ITU-R BT.601 YCbCr4:2:2

1. Horizontal timing

The horizontal pulse indicates the start of a new line, as shown in Figure 9-6. After hoff clock cycles, an input signal passes the line front blanking region and enters the line active data region. The value of hoff is 244 in the NTSC 525-line system or 264 in the PAL 625-line system. After act_width clock cycles, the input signal passes the line active data region and enters the line back blanking region. The value of act_width can be configured, and the typical value is 720 or 704. In addition, the horizontal sync (HS) polarity is configurable.

Figure 9-6 ITU-R BT.601 horizontal timing



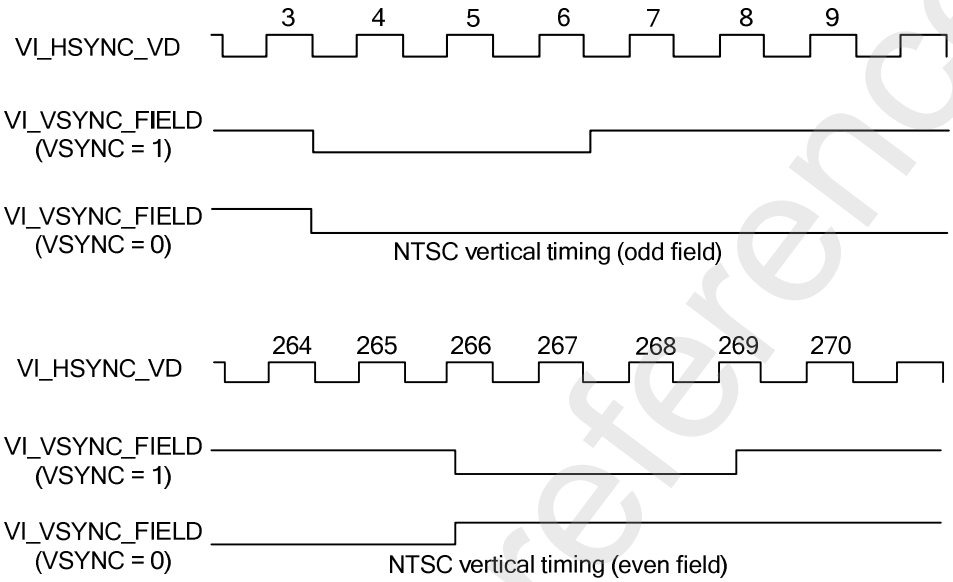
2. Vertical timings

Based on the ITU-R BT.601 recommendation, the signals VSYNC and FIELD are vertical sync (VS) signals. The VSYNC pulse or FIELD transition indicates the start of the odd field or even field. The VICAP module supports two vertical synchronization methods.

Figure 9-7 shows VI VS timings in the NTSC standard (525 lines), and Figure 9-8 shows VI VS timings in the PAL standard (625 lines). VI_HSYNC_VD indicates the HS pulse, and

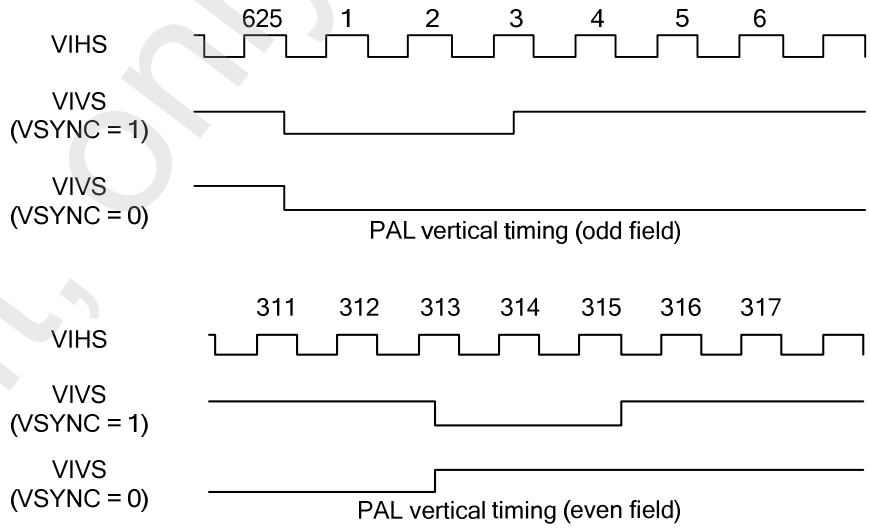
VI_VSYNC_FIELD indicates the VS pulse when VSYNC is 1 or field sync signal when VSYNC is 0.

Figure 9-7 VS timings in the NTSC standard



In NTSC interlaced scanning mode, the level of the VS signal in field 1 becomes low in the start position of line 4, retains low for three consecutive lines, and then becomes high in the start position of line 7. The VICAP module receives 240-line data from line 22 to line 261. The level of the VS signal in field 2 becomes low in the middle of line 266, retains low for three consecutive lines, and then becomes high in the middle of line 269. The VICAP module receives 240-line data from line 285 to line 524.

Figure 9-8 VS timings in the PAL standard



In PAL interlaced scanning mode, the level of the VS signal in field 1 becomes low in the start position of line 1, retains low for 2.5 consecutive lines, and then becomes high in the middle of line 3. The VICAP module receives 288-line data from line 24 to line 310. The level of the VS signal in field 2 becomes low in the middle of line 313, retains low for 2.5 consecutive lines, and then becomes high in the start position of line 316. The VICAP module receives 288-line data from line 336 to line 623.

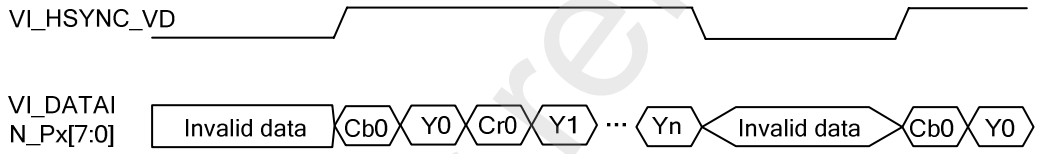
The preceding timings are typical BT.601 vertical timings. The number of lines from the start of the field to the active line, the number of field active lines, and VS polarity can be configured.

DC Interface Timings

1. Horizontal timing

When a DC is connected to the VICAP module, VI_HSYNC_VD is the data valid signal. The polarity of this signal is configurable. Figure 9-9 shows the DC horizontal timing.

Figure 9-9 DC horizontal timing



2. Vertical timing

The VICAP module supports the vertical pulse timing and vertical line active timing, as shown in Figure 9-10 and Figure 9-11. The VS polarity is configurable.

Figure 9-10 DC vertical pulse timing

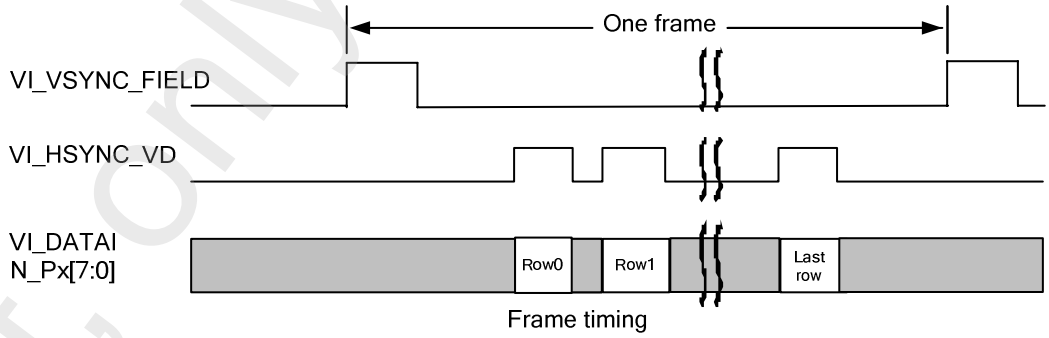
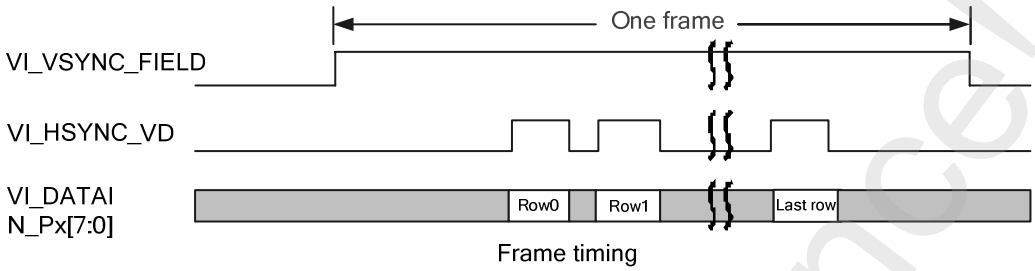


Figure 9-11 DC vertical line active timing

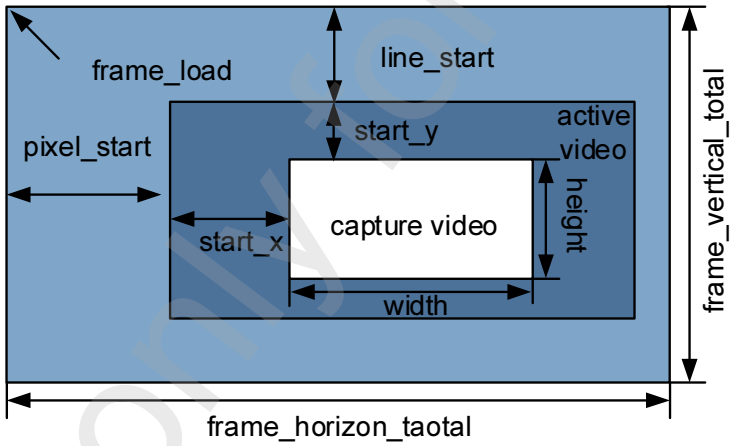


The preceding two timings are the same from the aspect of internal processing of the VICAP module. To be specific, the VICAP module considers the start of a frame after it detects a rising edge or a falling edge, and then detects the data active signal to check whether the current data is active.

9.1.3.3 Image Cropping

As shown in Figure 9-12, an active video starts from the end of the horizontal blanking region and vertical blanking region. The actual view range, however, is within the active video range.

Figure 9-12 Relationship between the active video area and the horizontal/vertical blanking regions



9.1.3.4 Image Storage Modes

The supported image storage modes include:

1. YUV data storage

- Semi-planar YCbCr storage mode

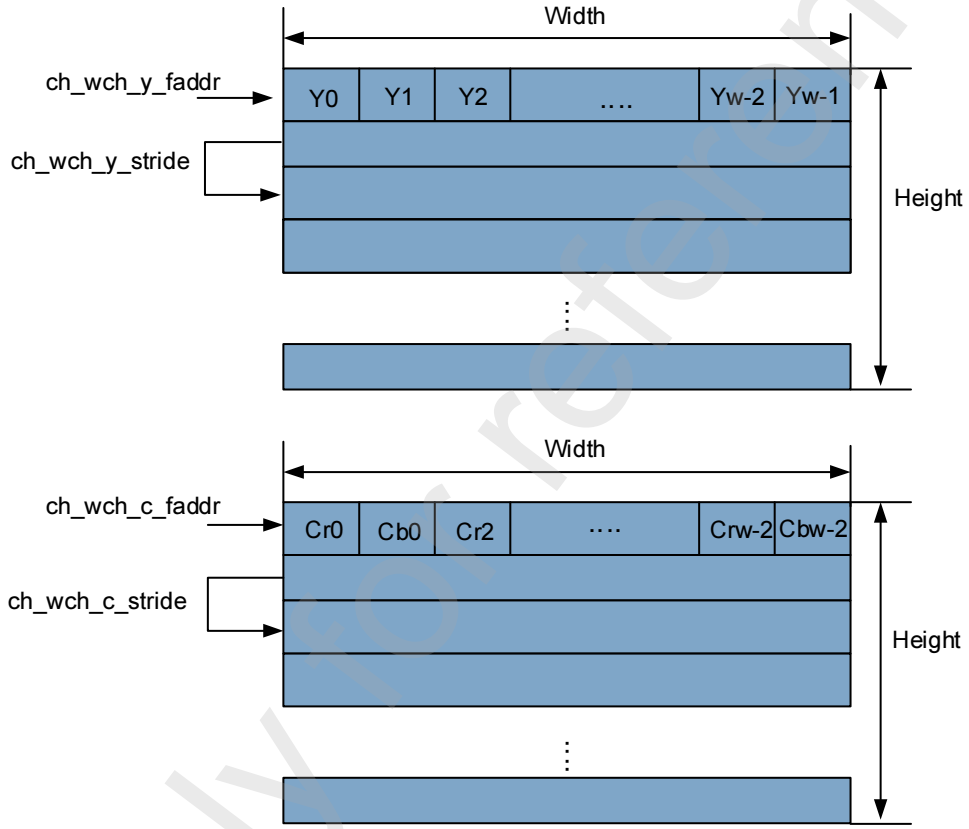
  After setting a view area, the system stores the read data in semi-planar mode. That is, the luminance component and the chrominance component are stored in the luminance space and chrominance space of the DDR respectively.

- For one line, the luminance component and chrominance component are stored separately and consecutively.

- For two consecutive lines, data is stored based on the **offset** parameter that defines the storage stride between the beginnings of two lines.
- The storage positions of the luminance component and chrominance component in the DDR are specified by the start address **base_addr**.

Figure 9-13 shows the mode of storing the YCbCr4:2:2 data captured by the VICAP module.

Figure 9-13 YCbCr4:2:2 storage mode

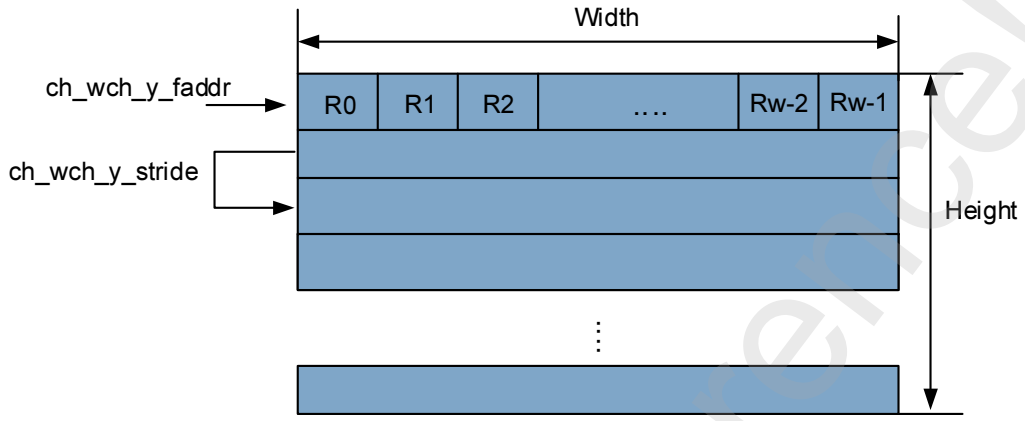


2. Raw data storage

- The raw data is stored in single-component mode.
- The raw data is consecutively stored in one line.
- For two consecutive lines, data is stored based on the **stride** parameter that defines the storage stride between the beginnings of two lines.
- The storage position of the DDR is specified by the start address **base_addr**.

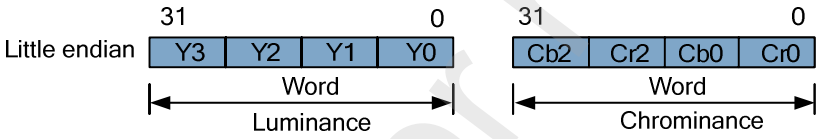
Figure 9-14 shows the mode of storing the raw data captured by the VICAP module.

Figure 9-14 Raw data storage mode



In the DDR, data is stored by word (32 bits). Four 8-bit pixels constitute a 32-bit word. See Figure 9-15.

Figure 9-15 Little-endian storage modes



The VICAP module supports the DDR that stores data in little-endian mode. The storage address is 16-byte-aligned.

9.1.4 Operating Mode

9.1.4.1 reg_newer Function

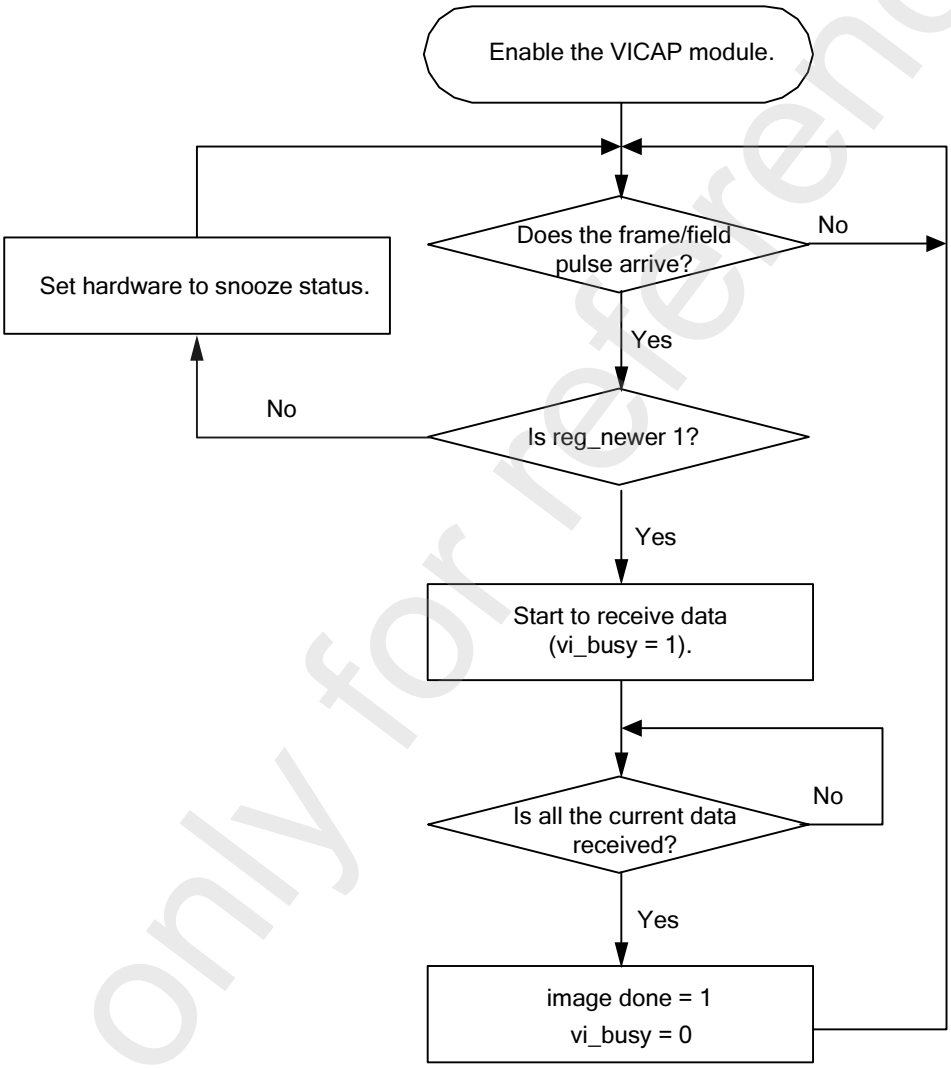
- Before enabling a channel of the VICAP module, the software must perform the following operations:
  - Configures the VICAP attribute register.
  - Writes 1 to the reg_newer bit to inform the VICAP module that the current register is ready.
- After the VICAP module is enabled, the VICAP logic starts to work. When a field or a frame arrives:
  - If reg_newer is 0, the VICAP module does not receive data. However, it sets the hardware status to snooze (the following hardware statuses are shown in Figure 9-16) and waits for the next field or frame.
  - If reg_newer is 1, the VICAP module starts receiving data, generates the register update interrupt (reg_update_int), and sets the hardware to busy state.
- After all the current data is received, the busy status of the hardware is cleared. When the next field or frame arrives:
  - If reg_newer is 0, the VICAP module does not receive the data of the next field or frame.

– If reg_newer is 1, the VICAP module receives the data of the next field or frame.

9.1.4.2 VICAP Hardware Workflow

Figure 9-16 shows the VICAP hardware workflow.

Figure 9-16 VICAP hardware workflow

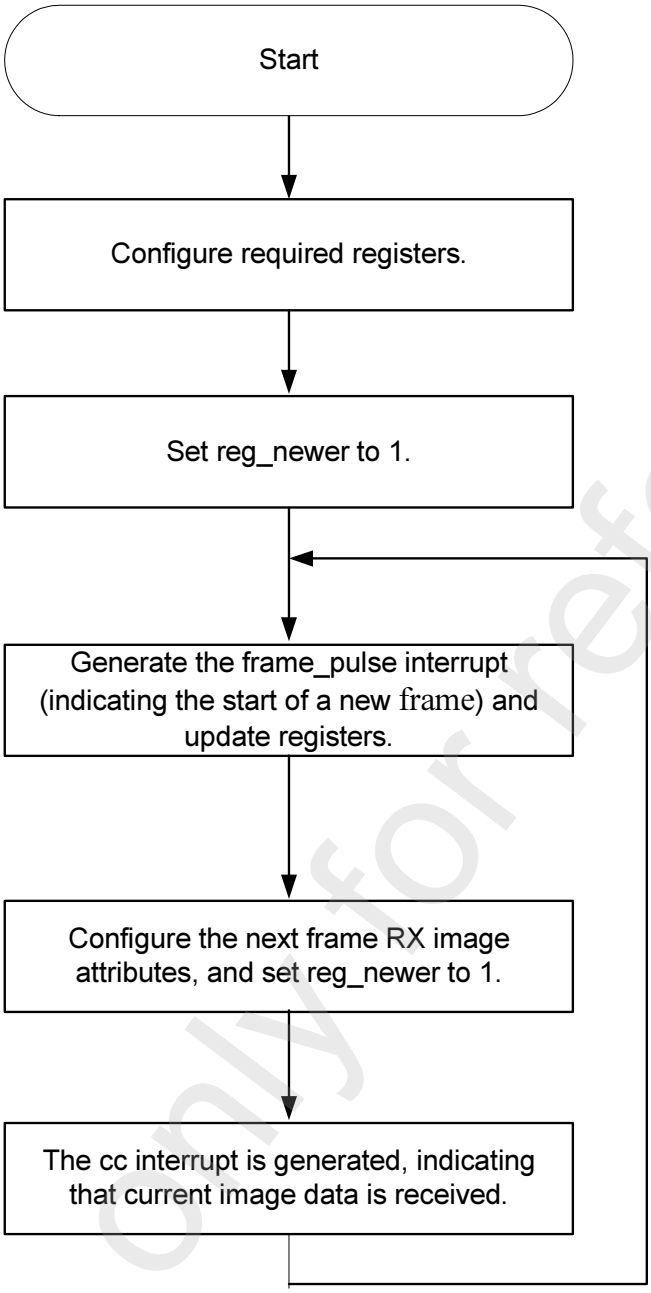


Each time after the VICAP module receives the data of a field or frame, it checks the reg_newer bit when the next field or frame arrives. If reg_newer is 1, software has updated or checked corresponding VICAP registers. In this case, the VICAP module automatically loads the register values configured by the software to the working register (this register is inaccessible to software), clears reg_newer, and starts to receive the data of the next field or frame. If reg_newer is 0, the VICAP module starts to receive data only when reg_newer is 1 and a new field or frame arrives.

9.1.4.3 Software Configuration Workflow

Figure 9-17 shows the software configuration process in interrupt mode.

Figure 9-17 Software Configuration



When the BT.656, BT.1120, MIPI Rx, or DC interface is used, timing registers do not need to be configured. If the BT.601 interface is used, timing registers including VS registers and HS registers need to be configured.

9.1.5 Register Summary

Table 9-5 describes VICAP registers.

Table 9-5 Summary of VICAP registers (base address: 0x1138_0000)

Offset Address	Register	Description	Page
0x0010	AXI_CFG	Bus configuration register	9-17
0x0050	ISP_SEL	ISP input data selection register	9-17
0x00F0	VICAP_INT	Interrupt indicator register	9-18
0x00F8	VICAP_INT_MASK	Interrupt mask register	9-20
0x0100	PT_INTF_MOD	Port mode register	9-21
0x0110	PT_OFFSET0	Component 0 offset register	9-22
0x0114	PT_OFFSET1	Component 1 offset register	9-22
0x0118	PT_OFFSET2	Component 2 offset register	9-23
0x0120	PT_BT656_CFG	BT.656 configuration register	9-23
0x0130	PT_UNIFY_TIMING_CFG	Timing configuration register	9-24
0x0134	PT_GEN_TIMING_CFG	Timing recovery module configuration register	9-26
0x0140	PT_UNIFY_DATA_CFG	Data configuration register	9-27
0x0144	PT_GEN_DATA_CFG	Data generation module configuration register	9-27
0x0148	PT_GEN_DATA_COEF	Data generation module coefficient register	9-29
0x014C	PT_GEN_DATA_INIT	Data generation module initial value configuration register	9-29
0x0150	PT_YUV444_CFG	YUV444 configuration register	9-30
0x0160	PT_FSTART_DLY	Port fstart interrupt delay register	9-30
0x0180	PT_INTF_HFB	Horizontal front blanking width register	9-30
0x0184	PT_INTF_HACT	Horizontal active width register	9-31
0x0188	PT_INTF_HBB	Horizontal back blanking width register	9-31
0x018C	PT_INTF_VFB	Vertical front blanking width register	9-32
0x0190	PT_INTF_VACT	Vertical active width register	9-32
0x0194	PT_INTF_VBB	Vertical back blanking width register	9-32
0x0198	PT_INTF_VBFB	Vertical bottom front blanking width register	9-33

Offset Address	Register	Description	Page
0x019C	PT_INTF_VBACT	Vertical bottom active width register	9-33
0x01A0	PT_INTF_VBBB	Vertical bottom back blanking width register	9-33
0x01A4	PT_ID_CFG	ID configuration register	9-34
0x01B0	PT_FLASH_CFG	Flash configuration register	9-35
0x01C0	PT_FLASH_CYC0	Flash timing 0 width register	9-36
0x01C4	PT_FLASH_CYC1	Flash timing 1 width register	9-36
0x01D0	PT_SHUTTER_CYC0	Shutter timing 0 width register	9-36
0x01D4	PT_SHUTTER_CYC1	Shutter timing 1 width register	9-37
0x01D8	PT_SHUTTER_CYC2	Shutter timing 2 width register	9-37
0x01DC	PT_SHUTTER_CYC3	Shutter timing 3 width register	9-37
0x01E0	PT_STATUS	Port status register	9-38
0x01E4	PT_BT656_STATUS	BT.656 status register	9-38
0x01EC	PT_SIZE	Input image active region size register	9-39
0x01F0	PT_INT	Port interrupt indicator register	9-39
0x01F8	PT_INT_MASK	Port interrupt mask register	9-40
0x0200	DES_CTRL	DES (RAW data write) control register	9-41
0x02F0	DES_INT	DES (RAW data write) raw interrupt register	9-42
0x02F8	DES_MASK	DES (RAW data write) interrupt mask register	9-43
0x0600	SRC_CTRL	SRC (RAW data write) control register	9-43
0x06F0	SRC_INT	SRC (RAW data read) raw interrupt register	9-44
0x06F8	SRC_MASK	SRC (RAW data read) interrupt mask register	9-45
0x1000	CH_CTRL	Channel control register	9-46
0x1004	CH_REG_NEWER	Capture control register	9-47

Offset Address	Register	Description	Page
0x1034	CH_DLY_CFG	Channel input image start interrupt delay configuration register	9-48
0x1080	CH_WCH_Y_CFG	Y component configuration register for the WCH module	9-48
0x1084	CH_WCH_Y_SIZE	Y component storage size register for the WCH module	9-49
0x1090	CH_WCH_Y_FADDR	Y component storage base address register for the WCH module	9-50
0x1094	CH_WCH_Y_HADDR	Y component header information storage base address register for the WCH module	9-50
0x1098	CH_WCH_Y_STRIDE	Y component line offset register for the WCH module	9-51
0x10A0	CH_WCH_C_CFG	C component configuration register for the WCH module	9-51
0x10A4	CH_WCH_C_SIZE	C component storage size register for the WCH module	9-52
0x10B0	CH_WCH_C_FADDR	C component storage base address register for the WCH module	9-53
0x10B4	CH_WCH_C_HADDR	C component header information storage base address register for the WCH module	9-53
0x10B8	CH_WCH_C_STRIDE	C component line offset register for the WCH module	9-53
0x10E8	CH_Y_OUT_SIZE	Luminance channel output image active region size indicator register	9-54
0x10EC	CH_C_OUT_SIZE	Chrominance channel output image active size indicator register	9-54
0x10F0	CH_INT	Channel raw interrupt register	9-55
0x10F8	CH_INT_MASK	Channel interrupt mask register	9-56
0x1100	CH_Y_CROP_CFG	Channel luminance crop enable register	9-56
0x1110	CH_Y_CROP0_START	Crop start position register for channel luminance region 0	9-57
0x1114	CH_Y_CROP0_SIZE	Crop size register for channel luminance region 0	9-57
0x1120	CH_C_CROP_CFG	Channel chrominance crop enable register	9-58

Offset Address	Register	Description	Page
0x1130	CH_C_CROP0_START	Crop start position register for channel chrominance region 0	9-58
0x1134	CH_C_CROP0_SIZE	Crop size register for channel chrominance region 0	9-59
0x2000	BAS_CTRL	BAS control register	9-59
0x2004	BAS_REG_NEWER	Capture control register	9-60
0x2008	BAS_MODE	BAS mode register	9-61
0x2010	BAS_ID_CFG	BAS RX ID selection register	9-61

9.1.6 Register Description

AXI_CFG

AXI_CFG is a bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0010	AXI_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				r_outstanding	reserved	w_outstanding	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	r_outstanding	Number of read request outstandings Value range: [1, 8]
[11:8]	RO	reserved	Reserved
[7:4]	RW	w_outstanding	Number of write request outstandings Value range: [1, 8]
[3:0]	RO	reserved	Reserved

ISP_SEL

ISP_SEL is an ISP input data selection register.

Offset Address	Register Name	Total Reset Value
0x0050	ISP_SEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															af_sel	reserved								isp_be_sel				reserved	isp_fe_sel		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	af_sel	AF input data select 0: The AF connects to ISP_FE. 1: The AF connects to ISP_BE. Other values: reserved
[15:7]	RO	reserved	Reserved
[6:4]	RW	isp_be_sel	ISP_BE input data select 000: ISP_BE connects to ISP_FE (for the raw input). 001: ISP_BE connects to LINE_BUF (for the YUV input). Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	isp_fe_sel	ISP_FE input data select 000: ISP_FE connects to LINE_BUF (for the raw input). 001: ISP_FE connects to SRC0. 010: reserved. 011: reserved. 100: ISP_FE connects to SRC3. Other values: reserved

VICAP_INT

VICAP_INT is an interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x00F0	VICAP_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													int_af	int_isp_be	int_isp_fe	reserved					int_bas	int_buf	int_src3	reserved			int_src0	reserved			int_des0	int_ch	int_pt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RO	int_af	AF interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[17]	RO	int_isp_be	ISP_BE interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	int_isp_fe	ISP_FE interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[15:11]	RO	reserved	Reserved
[10]	RO	int_bas	BAS interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	int_buf	LINE_BUF interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	int_src3	SRC3 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[7:6]	RO	reserved	Reserved
[5]	RO	int_src0	SRC0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[4:3]	RO	reserved	Reserved
[2]	RO	int_des0	DES0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

[1]	RO	int_ch	Channel interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_pt	Port interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

VICAP_INT_MASK

VICAP_INT_MASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x00F8	VICAP_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													int_af	int_isp_be	int_isp_fe	reserved					int_bas	int_buf	int_src3	reserved			int_src0	reserved			int_des0	int_ch	int_pt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	int_af	AF interrupt enable 0: masked 1: enabled
[17]	RW	int_isp_be	ISP_BE interrupt enable 0: masked 1: enabled
[16]	RW	int_isp_fe	ISP_FE interrupt enable 0: masked 1: enabled
[15:11]	RO	reserved	Reserved
[10]	RW	int_bas	BAS interrupt enable 0: masked 1: enabled
[9]	RW	int_buf	LINE_BUF interrupt enable 0: masked 1: enabled

[8]	RW	int_src3	SRC3 interrupt enable 0: masked 1: enabled
[7:6]	RO	reserved	Reserved
[5]	RW	int_src0	SRC0 interrupt enable 0: masked 1: enabled
[4:3]	RO	reserved	Reserved
[2]	RW	int_des0	DES0 interrupt enable 0: masked 1: enabled
[1]	RW	int_ch	Channel interrupt enable 0: masked 1: enabled
[0]	RW	int_pt	Port interrupt enable 0: masked 1: enabled

PT_INTF_MOD

PT_INTF_MOD is a port mode register.

Offset Address	Register Name	Total Reset Value
0x0100	PT_INTF_MOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Port enable 0: disabled 1: enabled
[30:1]	RO	reserved	Reserved
[0]	RW	mode	Timing mode 0: external sync 1: BT.656

PT_OFFSET0

PT_OFFSET0 is a component 0 offset register.

Offset Address	Register Name	Total Reset Value
0x0110	PT_OFFSET0	0xFFF0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 0 mask
[15]	RW	rev	Whether the data line is reversed 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 0 offset

PT_OFFSET1

PT_OFFSET1 is a component 1 offset register.

Offset Address	Register Name	Total Reset Value
0x0114	PT_OFFSET1	0xFFF0_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 1 mask
[15]	RW	rev	Whether the data line is reversed 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 1 offset

PT_OFFSET2

PT_OFFSET2 is a component 2 offset register.

Offset Address	Register Name	Total Reset Value
0x0118	PT_OFFSET2	0xFFF0_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mask																rev	reserved											offset			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	mask	Component 2 mask
[15]	RW	rev	Whether the data line is reversed 0: no 1: yes
[14:6]	RO	reserved	Reserved
[5:0]	RW	offset	Component 2 offset

PT_BT656_CFG

PT_BT656_CFG is a BT.656 configuration register.

Offset Address	Register Name	Total Reset Value
0x0120	PT_BT656_CFG	0x0000_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																				field_inv	vsync_inv	hsync_inv	reserved				mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31]	RW	enable	BT.656 enable 0: disabled 1: enabled
[30:11]	RO	reserved	Reserved
[10]	RW	field_inv	field reverse control 0: not reversed 1: reversed

[9]	RW	vsync_inv	vsync reverse control 0: not reversed 1: reversed
[8]	RW	hsync_inv	hsync reverse control 0: not reversed 1: reversed
[7:4]	RO	reserved	Reserved
[3:0]	RW	mode	Mode select mode[0] 0: hsync is not an active signal. 1: hsync is an active signal. mode[1] 0: The hsync output is active low. 1: The hsync output is active high. mode[3:2] 00: Component 0 is parsed. 01: Component 1 is parsed. 10: Component 2 is parsed. 11: reserved

PT_UNIFY_TIMING_CFG

PT_UNIFY_TIMING_CFG is a timing configuration register.

Offset Address	Register Name	Total Reset Value
0x0130	PT_UNIFY_TIMING_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					field_inv	field_sel		reserved				vsync_mode	vsync_inv	vsync_sel		reserved	hsync_mode			hsync_and		hsync_inv	hsync_sel	reserved					de_inv	de_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RW	field_inv	Field inverse (level-1 field processing) 0: not inverted 1: inverted

[25:24]	RW	field_sel	Field source select (level-0 field processing) 00: input field 01: input vsync 10: detected based on the relationship between vsync and hsync 11: fixed at 0
[23:21]	RO	reserved	Reserved
[20:19]	RW	vsync_mode	vsync processing mode (level-2 vsync processing) 00: not processed 01: detect the rising edge 10: detect the rising edge and falling edge 11: reserved
[18]	RW	vsync_inv	vsync inversion (level-1 vsync processing) 0: not inverted 1: inverted
[17:16]	RW	vsync_sel	vsync source select (level-0 vsync processing) 00: input vsync 01: input field 10: fixed at 0 11: reserved
[15]	RO	reserved	Reserved
[14:13]	RW	hsync_mode	hsync processing mode (level-3 hsync processing) 0: not processed 1: detect the rising edge
[12:11]	RW	hsync_and	Whether hsync is operated with the result of level-1 vsync processing (level-2 hsync processing) 00: not processed 01: ANDed 10: exclusive ORed 11: reserved
[10]	RW	hsync_inv	hsync inversion (level-1 hsync processing) 0: not inverted 1: inverted
[9:8]	RW	hsync_sel	hsync source select (level-0 hsync processing) 00: input hsync 01: input de 10: fixed at 0 11: reserved
[7:3]	RO	reserved	Reserved

[2]	RW	de_inv	de inversion (level-1 de processing) 0: not inverted 1: inverted
[1:0]	RW	de_sel	de source select (level-0 de processing) 00: input de 01: result of level-2 hsync processing 10: fixed at 1 11: fixed at 0

PT_GEN_TIMING_CFG

PT_GEN_TIMING_CFG is a timing recovery module configuration register.

Offset Address	Register Name	Total Reset Value
0x0134	PT_GEN_TIMING_CFG	0x4000_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	mode	reserved																											vsync_mode	hsync_mode	reserved
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31]	RW	enable	Timing recovery enable (timings are recovered based on timing parameters) 0: disabled 1: enabled
[30]	RW	mode	Timing recovery mode (timings are recovered based on timing parameters) 0: Timings are generated based on the input valid signal of PT. 1: Timings are internally calculated and generated.
[29:3]	RO	reserved	Reserved
[2]	RW	vsync_mode	vsync recovery 0: not recovered 1: recovered
[1]	RW	hsync_mode	hsync recovery 0: not recovered 1: recovered
[0]	RO	reserved	Reserved

PT_UNIFY_DATA_CFG

PT_UNIFY_DATA_CFG is a data configuration register.

Offset Address	Register Name	Total Reset Value
0x0140	PT_UNIFY_DATA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																											uv_seq	yc_seq	comp_num		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Data separation enable 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved
[3]	RW	uv_seq	CbCr sequence 0: CbCr 1: CrCb
[2]	RW	yc_seq	YC sequence 0: CY 1: YC
[1:0]	RW	comp_num	Data component select 00: component 1 01: component 2 10: component 3 11: reserved

PT_GEN_DATA_CFG

PT_GEN_DATA_CFG is a data generation module configuration register.

Offset Address	Register Name	Total Reset Value
0x0144	PT_GEN_DATA_CFG	0x0000_00E9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																							data0_move	data1_move	data2_move	vsync_reset	hsync_reset	vsync_move	hsync_move	de_move	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1

Bits	Access	Name	Description
[31]	RW	enable	Data generation enable. Data is generated based on the data generation parameter. 0: disabled 1: enabled
[30:8]	RO	reserved	Reserved
[7]	RW	data0_move	Whether data 0 is incremented progressively 0: no 1: yes
[6]	RW	data1_move	Whether data 1 is incremented progressively 0: no 1: yes
[5]	RW	data2_move	Whether data 2 is incremented progressively 0: no 1: yes
[4]	RW	vsync_reset	Whether to reset data based on the VS signal 0: not reset 1: reset
[3]	RW	hsync_reset	Whether to reset data based on the HS signal 0: not reset 1: reset
[2]	RW	vsync_move	Whether data is incremented progressively based on the VS signal 0: no 1: yes
[1]	RW	hsync_move	Whether data is incremented progressively based on the HS signal 0: no 1: yes

[0]	RW	de_move	Whether data is incremented progressively based on the de signal 0: no 1: yes

PT_GEN_DATA_COEF

PT_GEN_DATA_COEF is a data generation module coefficient register.

Offset Address	Register Name	Total Reset Value
0x0148	PT_GEN_DATA_COEF	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	inc_frame								step_frame								inc_space								step_space							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	inc_frame	Incremental value between data frames. The incremental values are accumulated in the upper eight bits of data.
[23:16]	RW	step_frame	Interval for data frame increment. The configured value is the actual value minus 1. The value 0 indicates the increment by frame.
[15:8]	RW	inc_space	Incremental value between data pixels. The incremental values are accumulated in the upper 10 bits of data.
[7:0]	RW	step_space	Interval for data pixel increment. The value 0 indicates the increment by pixel.

PT_GEN_DATA_INIT

PT_GEN_DATA_INIT is a data generation module initial value configuration register.

Offset Address	Register Name	Total Reset Value
0x014C	PT_GEN_DATA_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								data2								data1								data0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	data2	Initial V/B value
[15:8]	RW	data1	Initial U/G value

[7:0]	RW	data0	Initial Y/R value

PT_YUV444_CFG

PT_YUV444_CFG is a YUV444 configuration register.

Offset Address	Register Name	Total Reset Value
0x0150	PT_YUV444_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved																														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	YUV enable for converting YUV422 signals into YUV444 signals 0: disabled 1: enabled
[30:0]	RO	reserved	Reserved

PT_FSTART_DLY

PT_FSTART_DLY is a port fstart interrupt delay register.

Offset Address	Register Name	Total Reset Value
0x0160	PT_FSTART_DLY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fstart_dly																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fstart_dly	fstart interrupt delay time, in the unit of the port clock

PT_INTF_HFB

PT_INTF_HFB is a horizontal front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0180	PT_INTF_HFB	0x0000_0058

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hfb	Horizontal front blanking width

PT_INTF_HACT

PT_INTF_HACT is a horizontal active width register.

Offset Address	Register Name	Total Reset Value
0x0184	PT_INTF_HACT	0x0000_0780

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hact																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hact	Horizontal active width (in clock cycle)

PT_INTF_HBB

PT_INTF_HBB is a horizontal back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0188	PT_INTF_HBB	0x0000_00C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																hbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	hbb	Horizontal back blanking width

PT_INTF_VFB

PT_INTF_VFB is a vertical front blanking width register.

Offset Address	Register Name	Total Reset Value
0x018C	PT_INTF_VFB	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vfb	Vertical front blanking width

PT_INTF_VACT

PT_INTF_VACT is a vertical active width register.

Offset Address	Register Name	Total Reset Value
0x0190	PT_INTF_VACT	0x0000_0438

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vact	Vertical active width

PT_INTF_VBB

PT_INTF_VBB is a vertical back blanking width register.

Offset Address	Register Name	Total Reset Value
0x0194	PT_INTF_VBB	0x0000_0029

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	vbb	Vertical back blanking width

PT_INTF_VBFB

PT_INTF_VBFB is a vertical bottom front blanking width register.

Offset Address	Register Name	Total Reset Value
0x0198	PT_INTF_VBFB	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbfb	Vertical bottom front blanking width

PT_INTF_VBACT

PT_INTF_VBACT is a vertical bottom active width register.

Offset Address	Register Name	Total Reset Value
0x019C	PT_INTF_VBACT	0x0000_0438

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbact															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbact	Vertical bottom active width

PT_INTF_VBBB

PT_INTF_VBBB is a vertical bottom back blanking width register.

Offset Address	Register Name	Total Reset Value
0x01A0	PT_INTF_VBBB	0x0000_0029

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbbb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	vbbb	Vertical bottom back blanking width

PT_ID_CFG

PT_ID_CFG is an ID configuration register.

Offset Address	Register Name	Total Reset Value
0x01A4	PT_ID_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	mode	reset	reserved																							id_det		id_max		id			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	ID generation enable 0: disabled 1: enabled
[30]	RW	mode	ID generation mode 0: automatic mode (the ID automatically increases for each frame) 1: non-automatic mode (the ID depends on the configured value)
[29]	WO	reset	In automatic mode, setting this field to 1 restores the ID of the next frame to the initial value. This field is automatically cleared after restoration.
[28:6]	RO	reserved	Reserved
[5:4]	RW	id_det	ID of the frame whose width and height are detected
[3:2]	RW	id_max	Maximum ID in automatic mode
[1:0]	RW	id	Initial ID in automatic mode or generated ID in non-automatic mode

PT_FLASH_CFG

PT_FLASH_CFG is a flash configuration register.

Offset Address	Register Name	Total Reset Value
0x01B0	PT_FLASH_CFG	0x1000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_sel				reserved									shutter_times	shutter_phase	shutter_en	reserved															flash_phase	flash_en
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	id_sel	Trigger frame ID 0x1: triggered by using the start interrupt of the frame whose ID is 0 0x2: triggered by using the start interrupt of the frame whose ID is 1 0x4: triggered by using the start interrupt of the frame whose ID is 2 0x8: triggered by using the start interrupt of the frame whose ID is 3
[27:19]	RO	reserved	Reserved
[18]	RW	shutter_times	Shutter pulse times 0: twice 1: once
[17]	RW	shutter_phase	Shutter signal reverse 0: not reversed 1: reversed
[16]	WO	shutter_en	Shutter trigger enable. This field is automatically cleared. 0: disable 1: enable
[15:2]	RO	reserved	Reserved
[1]	RW	flash_phase	Flash signal reverse 0: not reversed 1: reversed
[0]	WO	flash_en	Flash trigger enable. This field is automatically cleared. 0: disable 1: enable

PT_FLASH_CYC0

PT_FLASH_CYC0 is a flash timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01C0	PT_FLASH_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 0 (in VICAP clock). The configured value is the actual value minus 1.

PT_FLASH_CYC1

PT_FLASH_CYC1 is a flash timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01C4	PT_FLASH_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of flash timing 1 (in VICAP clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC0

PT_SHUTTER_CYC0 is a shutter timing 0 width register.

Offset Address	Register Name	Total Reset Value
0x01D0	PT_SHUTTER_CYC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 0 (in VICAP clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC1

PT_SHUTTER_CYC1 is a shutter timing 1 width register.

Offset Address	Register Name	Total Reset Value
0x01D4	PT_SHUTTER_CYC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 1 (in VICAP clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC2

PT_SHUTTER_CYC2 is a shutter timing 2 width register.

Offset Address	Register Name	Total Reset Value
0x01D8	PT_SHUTTER_CYC2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 2 (in VICAP clock). The configured value is the actual value minus 1.

PT_SHUTTER_CYC3

PT_SHUTTER_CYC3 is a shutter timing 3 width register.

Offset Address	Register Name	Total Reset Value
0x01DC	PT_SHUTTER_CYC3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cyc																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cyc	Duration of shutter timing 3 (in VICAP clock). The configured value is the actual value minus 1.

PT_STATUS

PT_STATUS is a port status register.

Offset Address	Register Name	Total Reset Value
0x01E0	PT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										id		field	vsync	hsync	de
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RO	id	Port output ID
[3]	RO	field	Field output over the port
[2]	RO	vsync	vsync signal output over the port
[1]	RO	hsync	hsync signal over the port
[0]	RO	de	de signal output over the port

PT_BT656_STATUS

PT_BT656_STATUS is a BT.656 status register.

Offset Address	Register Name	Total Reset Value
0x01E4	PT_BT656_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																seav								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	seav	Synchronization code
[7:0]	RO	reserved	Reserved

PT_SIZE

PT_SIZE is an input image active region size indicator register.

Offset Address	Register Name	Total Reset Value
0x01EC	PT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Height of the image active region
[15:0]	RO	width	Width of the image active region

PT_INT

PT_INT is a port interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x01F0	PT_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err	width_err	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	WC	height_err	Status of the image height change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	width_err	Status of the image width change interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

PT_INT_MASK

PT_INT_MASK is a port interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	PT_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													height_err	width_err	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	height_err	Image height change interrupt enable 0: masked 1: enabled

[1]	RW	width_err	Image width change interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Frame start interrupt enable 0: masked 1: enabled

DES_CTRL

DES_CTRL is a DES (RAW data write) control register.

Offset Address	Register Name	Total Reset Value
0x0200	DES_CTRL	0x0002_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reg_newer_mode	reserved										finish_mode	reserved											bit_width							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	DES enable 0: disabled 1: enabled
[30]	RW	reg_newer_mode	Enable mode control 0: Timings are output when the reg_newer register is set to 1 and the module is enabled. 1: Timings are output when the module is enabled.
[29:18]	RO	reserved	Reserved
[17]	RW	finish_mode	Finish interrupt report time control 0: reported immediately 1: reported at the start of the next frame
[16:6]	RO	reserved	Reserved

[5:0]	RW	bit_width	Width of the data written by the DES 0x08: 8 bits 0x0A: 10 bits 0x0C: 12 bits 0x0E: 14 bits 0x10: 16 bits Other values: reserved

DES_INT

DES_INT is a DES (RAW data write) raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x02F0	DES_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

[0]	WC	fstart	Status of the frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

DES_MASK

DES_MASK is a DES (RAW data write) interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x02F8	DES_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	update_cfg	Register update interrupt enable 0: masked 1: enabled
[3]	RW	field_throw	Frame loss interrupt enable 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Frame start interrupt enable 0: masked 1: enabled

SRC_CTRL

SRC_CTRL is an SRC (RAW data write) control register.

Offset Address	Register Name	Total Reset Value
0x0600	SRC_CTRL	0x0002_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reg_newer_mode	reserved												finish_mode	reserved													bit_width			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	SRC enable 0: disabled 1: enabled 0x600−0x6FF: address space of the SRC0 register 0x900−0x9FF: address space of the SRC3 register
[30]	RW	reg_newer_mode	Enable mode control 0: Timings are output when the reg_newer register is set to 1 and the module is enabled. 1: Timings are output when the module is enabled.
[29:18]	RO	reserved	Reserved
[17]	RW	finish_mode	Finish interrupt report time control 0: reported immediately 1: reported at the start of the next frame
[16:6]	RO	reserved	Reserved
[5:0]	RW	bit_width	Data bit width 0x08: 8 bits 0x0A: 10 bits 0x0C: 12 bits 0x0E: 14 bits 0x10: 16 bits Other values: reserved

SRC_INT

SRC_INT is an SRC (RAW data read) raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x06F0	SRC_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dcmp_wrong	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	WC	dcmp_wrong	Status of the decompress error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

SRC_MASK

SRC_MASK is an SRC (RAW data read) interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x06F8	SRC_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										dcmp_wrong	update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	dcmp_wrong	Decompress error interrupt enable 0: masked 1: enabled
[4]	RW	update_cfg	Register update interrupt enable 0: masked 1: enabled
[3]	RW	field_throw	Frame loss interrupt enable 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Frame start interrupt enable 0: masked 1: enabled

CH_CTRL

CH_CTRL is a channel control register.

Offset Address	Register Name	Total Reset Value
0x1000	CH_CTRL	0x0003_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reg_newer_mode	reserved												finish_mode	online_out_en	reserved															mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	Channel enable 0: disabled 1: enabled
[30]	RW	reg_newer_mode	Enable mode control 0: Timings are output when the reg_newer register is set to 1 and the module is enabled. 1: Timings are output when the module is enabled.
[29:18]	RO	reserved	Reserved
[17]	RW	finish_mode	Finish interrupt report time control 0: reported immediately 1: reported at the start of the next frame
[16]	RW	online_out_en	Online timing output enable control 0: disabled 1: enabled
[15:2]	RO	reserved	Reserved
[1:0]	RW	mode	Channel mode 00: normal mode 01: single-component (luminance) mode 10: single-component (chrominance) mode Other values: reserved

CH_REG_NEWER

CH_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x1004	CH_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	reg_newer	Channel update. This bit is automatically cleared for each frame.

CH_DLY_CFG

CH_DLY_CFG is a channel input image start interrupt delay configuration register.

Offset Address	Register Name	Total Reset Value
0x1034	CH_DLY_CFG	0x0010_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_dly_cfg																reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	v_dly_cfg	Number of delayed vertical lines
[15:0]	RO	reserved	Reserved

CH_WCH_Y_CFG

CH_WCH_Y_CFG is a Y component configuration register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1080	CH_WCH_Y_CFG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved													bit_width		reserved											flip	mirror	head_tword	cmp_mode	cmp_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable 0: disabled 1: enabled
[30:18]	RO	reserved	Reserved
[17:16]	RW	bit_width	Data width 00: 8 bits 10: 16 bits Other values: reserved
[15:5]	RO	reserved	Reserved
[4]	RW	flip	Channel flip enable 0: disabled 1: enabled
[3]	RW	mirror	Channel mirror enable 0: disabled 1: enabled
[2]	RW	head_tword	Header information stride 0: 128 bits (128 bits/line) 1: 256 bits (256 bits/line)
[1]	RW	cmp_mode	Compressed segment length 0: 128 pixels 1: 256 pixels
[0]	RW	cmp_en	Compression enable 0: disabled 1: enabled

CH_WCH_Y_SIZE

CH_WCH_Y_SIZE is a Y component storage size register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1084	CH_WCH_Y_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored image. The configured value is the actual value minus 1.

CH_WCH_Y_FADDR

CH_WCH_Y_FADDR is a Y component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1090	CH_WCH_Y_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the Y component

CH_WCH_Y_HADDR

CH_WCH_Y_HADDR is a Y component header information storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1094	CH_WCH_Y_HADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	haddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	haddr	Base address for storing the Y component header information

CH_WCH_Y_STRIDE

CH_WCH_Y_STRIDE is a Y component line offset register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x1098	CH_WCH_Y_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the Y component

CH_WCH_C_CFG

CH_WCH_C_CFG is a C component configuration register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10A0	CH_WCH_C_CFG	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reserved														bit_width	reserved											flip	mirror	head_tword	cmp_mode	cmp_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31]	RW	enable	CH write channel enable 0: disabled 1: enabled

[30:18]	RO	reserved	Reserved
[17:16]	RW	bit_width	Data width 00: 8 bits 10: 16 bits Other values: reserved
[15:5]	RO	reserved	Reserved
[4]	RW	flip	Channel flip enable 0: disabled 1: enabled
[3]	RW	mirror	Channel mirror enable 0: disabled 1: enabled
[2]	RW	head_tword	Header information stride 0: 128 bits (128 bits/line) 1: 256 bits (256 bits/line)
[1]	RW	cmp_mode	Compressed segment length 0: 128 pixels 1: 256 pixels
[0]	RW	cmp_en	Compression enable 0: disabled 1: enabled

CH_WCH_C_SIZE

CH_WCH_C_SIZE is a C component storage size register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10A4	CH_WCH_C_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the stored image. The configured value is the actual value minus 1.

[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the stored image. The configured value is the actual value minus 1.

CH_WCH_C_FADDR

CH_WCH_C_FADDR is a C component storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B0	CH_WCH_C_FADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	faddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	faddr	Base address for storing the C component

CH_WCH_C_HADDR

CH_WCH_C_HADDR is a C component header information storage base address register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B4	CH_WCH_C_HADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	haddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	haddr	Base address for storing the C component header information

CH_WCH_C_STRIDE

CH_WCH_C_STRIDE is a C component line offset register for the WCH module.

Offset Address	Register Name	Total Reset Value
0x10B8	CH_WCH_C_STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	stride	Stride (in byte) for storing the C component

CH_Y_OUT_SIZE

CH_Y_OUT_SIZE is a luminance channel output image active region size indicator register.

Offset Address	Register Name	Total Reset Value
0x10E8	CH_Y_OUT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Image height
[15:0]	RO	width	Image width

CH_C_OUT_SIZE

CH_C_OUT_SIZE is a chrominance channel output image active region size indicator register.

Offset Address	Register Name	Total Reset Value
0x10EC	CH_C_OUT_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	height	Image height
[15:0]	RO	width	Image width

CH_INT

CH_INT is a channel raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x10F0	CH_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fstart_dly	reserved											update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	WC	fstart_dly	Status of the delayed frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[14:5]	RO	reserved	Reserved
[4]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	field_throw	Status of the frame loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	buf_ovf	Status of the internal FIFO overflow error interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	cc_int	Status of the capture completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

CH_INT_MASK

CH_INT_MASK is a channel interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x10F8	CH_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fstart_dly	reserved										update_cfg	field_throw	buf_ovf	cc_int	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RW	fstart_dly	Delayed frame start interrupt enable 0: masked 1: enabled
[14:5]	RO	reserved	Reserved
[4]	RW	update_cfg	Register update interrupt enable 0: masked 1: enabled
[3]	RW	field_throw	Frame loss interrupt enable 0: masked 1: enabled
[2]	RW	buf_ovf	Internal FIFO overflow error interrupt enable 0: masked 1: enabled
[1]	RW	cc_int	Capture completion interrupt enable 0: masked 1: enabled
[0]	RW	fstart	Frame start interrupt enable 0: masked 1: enabled

CH_Y_CROP_CFG

CH_Y_CROP_CFG is a channel luminance crop enable register.

Offset Address	Register Name	Total Reset Value
0x1100	CH_Y_CROP_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								n0_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	CROP enable 0: disabled 1: enabled

CH_Y_CROP0_START

CH_Y_CROP0_START is a channel luminance crop start position register.

Offset Address	Register Name	Total Reset Value
0x1110	CH_Y_CROP0_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved			y_start		reserved		x_start	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which the image starts to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which the image starts to be captured

CH_Y_CROP0_SIZE

CH_Y_CROP0_SIZE is a channel luminance crop size register.

Offset Address	Register Name	Total Reset Value
0x1114	CH_Y_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained image. The configured value is the actual value minus 1.

CH_C_CROP_CFG

CH_C_CROP_CFG is a channel chrominance crop enable register.

Offset Address	Register Name	Total Reset Value
0x1120	CH_C_CROP_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															n0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	n0_en	CROP enable 0: disabled 1: enabled

CH_C_CROP0_START

CH_C_CROP0_START is a channel chrominance crop start position register.

Offset Address	Register Name	Total Reset Value
0x1130	CH_C_CROP0_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				y_start												reserved				x_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	y_start	ID of the line from which the image starts to be captured
[15:13]	RO	reserved	Reserved
[12:0]	RW	x_start	ID of the pixel from which the image starts to be captured

CH_C_CROP0_SIZE

CH_C_CROP0_SIZE is a channel chrominance crop size register.

Offset Address	Register Name	Total Reset Value
0x1134	CH_C_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height (in line) of the obtained image. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width (in pixel) of the obtained image. The configured value is the actual value minus 1.

BAS_CTRL

BAS_CTRL is a BAS control register.

Offset Address	Register Name	Total Reset Value
0x2000	BAS_CTRL	0xC000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	enable	reg_newer_mode	reserved																													
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	enable	BAS enable 0: disabled 1: enabled
[30]	RW	reg_newer_mode	Enable mode control 0: Timings are output when the reg_newer register is set to 1 and the module is enabled. 1: Timings are output when the module is enabled.
[29:0]	-	reserved	Reserved

BAS_REG_NEWER

BAS_REG_NEWER is a capture control register.

Offset Address	Register Name	Total Reset Value
0x2004	BAS_REG_NEWER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															reg_newer
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	reg_newer	DES update register. It is set to 0 for each frame. 0: not updated (discard the frame) 1: updated

BAS_MODE

BAS_MODE is a BAS mode register (instant register).

Offset Address	Register Name	Total Reset Value
0x2008	BAS_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	mode	Mode control register 0: WDR line mode or linear mode 1: WDR frame mode

BAS_ID_CFG

BAS_ID_CFG is a BAS RX ID selection register (instant register).

Offset Address	Register Name	Total Reset Value
0x2010	BAS_ID_CFG	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												id_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved
[3:0]	RW	id_sel	id_sel ID selection 0: Data with this ID is filtered. 1: Data with this ID is received. bit[0]: data with ID 0 bit[1]: data with ID 1 bit[2]: data with ID 2 bit[3]: data with ID 3

9.2 VDP

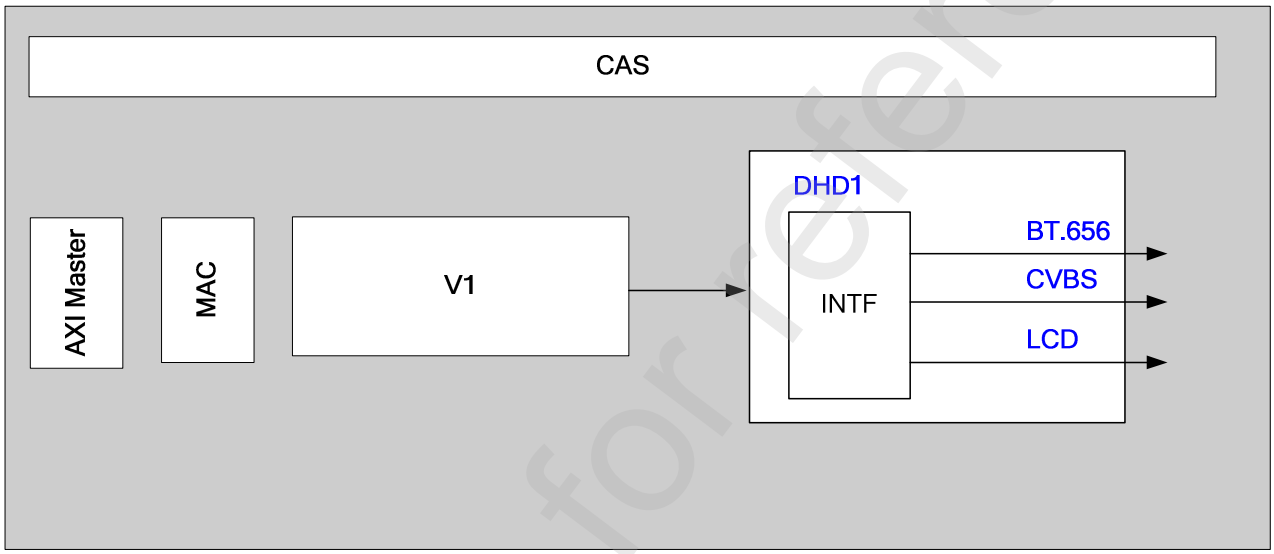
9.2.1 Overview

The video display processor (VDP) actively reads video data from the memory and transmits the video data through the display channel.

9.2.2 Architecture

Figure 9-18 shows the block diagram of the VDP.

Figure 9-18 Block diagram of the VDP



The following describes the major concepts:

- Surface: data path of bus inputs. The surface reads and processes the bus data of a single layer (V1).
- Display channel: It includes the HD display channel DHD1.
- Memory access controller (MAC): Each module reads data from the memory over the AXI bus. The MAC arbitrates the requests from all surfaces.
- Control and status (CAS): It configures registers over the APB and reports the status of other modules to the CPU.

The VDP registers are classified into:

- Global registers

  Include the bus configuration registers, interrupt registers, and version register.
- Surface registers

  Include the video layer configuration registers.
- Display channel registers

  Include the DHD1 configuration registers.

The VDP has the following features:

- Digital output interfaces, which support ITU-R BT.656 outputs and LCD 565 serial outputs.
- Analog output interface, which supports the CVBS output
- Video layer (V1)
- One video channel. It has a separate vertical timing interrupt (indicating the end of a frame) and a low bandwidth interrupt.

9.2.3 Operating Mode

9.2.3.1 Clock Configurations

Interfaces of the VDP module can be configured to output the clock source VPLL.

For details, see the description of the PERI_CRG13 for 3.2.7 section.

9.2.3.2 Reset

The VDP supports a hard reset signal and a soft reset signal.

CAUTION

Before soft-resetting the AXI bus, do as follows:

- Disable all layers.
- Configure the bus reset request after the next frame interrupt is detected.

9.2.3.3 Bus Configurations

AXI Master

The VDP provides one master interface to improve bus access efficiency.

The VDP supports the AXI master. The data read/write requests of V1 can be implemented by using the master.

APB Register Configuration

The VDP registers are read and written over the APB interface. The base address for VDP registers is 0x1140_0000, the register addressing space is 64 KB, and the address offset range is 0x0000–0xFFFF.

Outstanding Configuration

The depth of the AXI master outstanding ranges from 0 to 7. When the outstanding depth is set to 0, the AXI master does not operate the bus.

9.2.3.4 Digital Output Interfaces

The VDP supports two digital interface serial output modes: ITU-R BT.656 and LCD RGB.

9.2.3.5 Analog Output Interface

The VDP supports the CVBS analog interface output.

9.2.3.6 Interrupts

VDP interrupts are classified into:

- Vertical timing interrupt
- Low bandwidth interrupt

Vertical Timing Interrupt

The position of generating the vertical timing interrupt can be configured.

- The VDP supports one vertical timing interrupt, indicating the end of a frame or field.
- The interrupt can be generated by frame or field.
- In progressive display mode, the vertical timing interrupt must be generated by frame.
- In interlaced display mode, the vertical timing interrupt can be generated by frame or field. You are advised to set the interrupt generation mode to generation by field for HD and generation by frame for SD.
- Interrupt mask can be configured.
- The threshold for the vertical timing interrupt can be configured.
- The interrupt source can be separately enabled or disabled. Writing 1 clears the interrupt.

Low Bandwidth Interrupt

The VDP allows the low bandwidth status to be reported by using an interrupt.

- The VDP supports one low bandwidth interrupt, indicating low bandwidth of a frame or field.
- The interrupt can be masked.
- The interrupt source can be separately enabled or disabled. Writing 1 clears the interrupt.

9.2.4 Function Description

9.2.4.1 Video Layer

Features

The video layer has the following features:

- Input pixel formats of semi-planar420, semi-planar422, and Semi-planar400
- Minimum input resolution of 32 x 32 and maximum input resolution of 720 x 576
- Minimum output resolution of 32 x 32 and maximum output resolution of 720 x 576
- A multiple of 2 for the input horizontal resolution
- A multiplier of 4 for the interlaced 420 input vertical resolution and a multiple of 2 for the other input vertical resolutions
- Interlaced mode and progressive mode
- User-defined source luminance and chrominance start addresses, 2-byte-aligned

- User-defined source luminance and chrominance stride, 16-byte-aligned
- Vertical chrominance up sampling, replication mode
- Horizontal chrominance up sampling, replication mode
- Color space conversion (CSC) and adjustment of contrast, hue, and saturation
- User-defined display position, anywhere on the screen
- User-defined global alpha ranging from 0 to 255

420-422 (Vertical Chrominance Up Sampling)

When YUV420 data is input, 2x vertical scaling must be performed on the chrominance to convert the data format into YUV422. V1 converts the data format in replication mode.

422-444 (Horizontal Chrominance Up Sampling)

Horizontal chrominance up sampling converts the YUV422 data format into YUV444 in replication mode.

CSC

- CSC between YCbCr BT601 and BT709
- Adjustment of luminance, hue, and saturation

9.2.4.2 Display Channel

Video Channel Features

- DHD1 can function as an output channel.
- Only one output timing is supported in an application scenario.
- The following typical output timings are supported: 576p, 576i.

Timing Configuration

The VDP output interfaces support typical and non-typical timings to connect to different interfaces.

CAUTION

Interfaces must be disabled before timing parameters are configured and be enabled after configuration.

9.2.4.3 SD Output Interface BT.656

Features

- 10 bits to 8 bits dither
- YCbCr444-to-YCbCr422 horizontal chrominance down sampling (DFIR)
- Clipping for data clamp (Y 16−235 and C 16−240 according to the interface protocol)
- Typical output timings of NTSC and PAL

9.2.4.4 LCD Output Interface RGB

Features

- RGB565 serial output
- Maximum 27 MHz output clock

9.2.4.5 SD Analog Output Interface CVBS

Features

- Data clamping clip. According to the interface protocol, Y clamping ranges from 16 to 235, and C clamping ranges from 16 to 240.
- Typical output timing: NTSC and PAL

  27 MHz typical output clock

9.2.5 Register Summary

Table 9-6 describes VDP registers.

Table 9-6 Summary of VDP registers (base address: 0x1140_0000)

Offset Address	Register	Description	Page
0x0000	VOCTRL	VO control register	9-69
0x0004	VOINTSTA	VO interrupt status register (read-only)	9-69
0x0008	VOMSKINTSTA	VO masked interrupt status register	9-70
0x000C	VOINTMSK	VDP interrupt mask register	9-71
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Offset Address	Register	Description	Page
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0xC408	DHD1_HSYNC1	Horizontal sync configuration register in interlaced or progressive output mode	9-87
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0xC410	DHD1_VPLUS	Bottom field vertical sync timing register in interlaced output mode (non-instant register)	9-87
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Offset Address	Register	Description	Page
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0xC4F0	DHD1_STATE	DHD1 status register	9-89
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0xD214	BT_CLIP0_H	BT.656 clip highest threshold register (instant register)	9-90
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0xD284	BT_DITHER0_COEF 0	BT.656 dither coefficient 0 register	9-92
0xD288	BT_DITHER0_COEF 1	BT.656 dither coefficient 1 register	9-92
0xD400	LCD_CTRL	LCD control register	9-92
0xD408	LCD_SYNC_INV	Sync signal polarity configuration register when the LCD external sync timing is input	9-93
0xF200	DATE_COEFF0	Standard parameter configuration register	9-94
0xF254	DATE_COEFF21	Output matrix control register	9-98
0xF258	DATE_COEFF22	Discrete time oscillator (DTO) initial phase configuration register	9-98
0xF25C	DATE_COEFF23	VIDEO_OUT delay configuration register	9-99
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0xF298	DATE_COEFF38	Up-sampling filtering coefficient 2 register	9-100
0xF29C	DATE_COEFF39	Up-sampling filtering coefficient 3 register	9-101
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0xF2A4	DATE_COEFF41	Up-sampling filtering coefficient 5 register	9-101
0xF2A8	DATE_COEFF42	Up-sampling filtering coefficient 6 register	9-102
0xF2C0	DATE_DACDET1	DAC automatic detection register 1	9-102
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Offset Address	Register	Description	Page
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9.2.6 Register Description

VOCTRL

VOCTRL is a VO control register. It is used to configure the arbitration mode of surface bus requests.

Offset Address	Register Name	Total Reset Value
0x0000	VOCTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vo_ck_gt_en	reserved																											m0_arb_mode			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	vo_ck_gt_en	VDP clock gating enable 0: disabled 1: enabled
[30:4]	RO	reserved	Reserved
[3:0]	RW	m0_arb_mode	Arbitration mode of data requests of internal surface buses of VO MAC0 0x0: polling Other values: reserved

VOINTSTA

VOINTSTA is a VO interrupt status register (read-only).

Offset Address	Register Name	Total Reset Value
0x0004	VOINTSTA	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dhd1uf_int	reserved	reserved	dhd1vtthd1_int	reserved	reserved	reserved	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	dhd1uf_int	DHD1 low-bandwidth alarm interrupt 0: An interrupt is reported. 1: No interrupt is reported.
[6]	RO	reserved	Reserved
[5]	RO	reserved	Reserved
[4]	RO	dhd1vtthd1_int	DHD1 vertical timing interrupt 1 0: An interrupt is reported. 1: No interrupt is reported.
[3]	RO	reserved	Reserved
[2]	RO	reserved	Reserved
[1]	RO	reserved	Reserved
[0]	RO	reserved	Reserved

VOMSKINTSTA

VOMSKINTSTA is a VO masked interrupt status register. Writing 1 clears this register.

Offset Address	Register Name	Total Reset Value
0x0008	VOMSKINTSTA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			vdac0_unload_int	reserved				dhd1uf_clr	reserved	reserved	dhd1vtthd1_clr	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	vdac0_unload_int	DAC0 offload interrupt 0: An interrupt is reported. 1: No interrupt is reported.
[11:8]	RO	reserved	Reserved
[7]	WC	dhd1uf_clr	DHD1 low-bandwidth alarm interrupt 0: An interrupt is reported. 1: No interrupt is reported.
[6]	RO	reserved	Reserved
[5]	RO	reserved	Reserved
[4]	WC	dhd1vtthd1_clr	DHD1 vertical timing interrupt 1 0: An interrupt is reported. 1: No interrupt is reported.
[3:0]	RO	reserved	Reserved

VOINTMSK

VOINTMSK is a VDP interrupt mask register.

CAUTION

VOINTMSK corresponds to VOINTSTA. If a bit is 1, the corresponding interrupt is enabled; if a bit is 0, the corresponding interrupt is masked.

Offset Address	Register Name	Total Reset Value
0x000C	VOINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								dhd1uf_intmsk	reserved	reserved	dhd1vtthd1_intmsk	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	dhd1uf_intmsk	Mask for the DHD1 low-bandwidth alarm interrupt 0: masked 1: enabled
[6]	RO	reserved	Reserved
[5]	RO	reserved	Reserved
[4]	RW	dhd1vtthd1_intmsk	Mask for DHD1 vertical timing interrupt 1 0: masked 1: enabled
[3:0]	RO	reserved	Reserved

VOAXICTRL

VOAXICTRL is a VO AXI bus configuration register.

Offset Address	Register Name	Total Reset Value
0x0034	VOAXICTRL	0x0111_0111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												m0_outstd_rid0			
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	m0_outstd_rid0	Read ID0 outstanding of AXI master 0. The value ranges from 1 to 7.

VO_MUX

VO_MUX is a VO interface multiplexing register.

Offset Address	Register Name	Total Reset Value
0x0100	VO_MUX	0x0001_6540

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	digital_sel				reserved	reserved																										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	digital_sel	Digital interface data select 0x1: BT.656 0x2: LCD Other values: reserved
[27]	RW	reserved	Reserved
[26:0]	RO	reserved	Reserved

VO_DAC_CTRL

VO_DAC_CTRL is a VO DAC control register.

Offset Address	Register Name	Total Reset Value
0x0120	VO_DAC_CTRL	0x2000_4000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									envbg	pdchopper	enextref	enctr				dac_reg_rev															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	envbg	VBG reference voltage enable 0: disabled 1: enabled

[21]	RW	pdchopper	VBG Chopper enable 0: enabled 1: disabled
[20]	RW	enextref	VBG output test enable 0: The interval VBG is used, and the VBG is not output to the test pin. 1: The VBG is output for testing.
[19:16]	RW	enctr	VBG output test enable 0: The interval VBG is used, and the VBG is not output to the test pin. 1: The VBG is output for testing.
[15:0]	RW	dac_reg_rev	Reserved

VO_DAC_0_CTRL

VO_DAC_0_CTRL is a VO DAC 0 channel control register.

Offset Address	Register Name	Total Reset Value
0x0134	VO_DAC_0_CTRL	0x1000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dac0en	reserved																							dac0gc					reserved		cablectr0
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dac0en	DAC enable 0: disabled 1: enabled
[30:10]	RO	reserved	Reserved
[9:4]	RW	dac0gc	DAC output amplitude control The full-scale output voltage ranges from 0.52 V to 1.37 V. The output amplitude is divided into 64 orders for adjustment. The adjustment precision is 1%. The formula is as follows: Ifs = 13.9 + GAIN x 0.358 (m A) 000000: 0.52 V ... 111111: 1.37 V
[3:2]	RO	reserved	Reserved

[1:0]	RW	cablectr0	VREF_CABLE reference voltage adjustment of the DAC 00: normal (default) 01: –10% 10: –20% 11: +10%

VO_DAC_STAT0

VO_DAC_STAT0 is a VO DAC status 0 register.

Offset Address	Register Name	Total Reset Value
0x0140	VO_DAC_STAT0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			cableout0	reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	cableout0	cableout0 feedback signal
[15:0]	RO	reserved	Reserved

V1_CTRL

V1_CTRL is a V1 configuration register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1000	V1_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_en	reserved									precharge_en	precharge_mode	reserved				lm_rmode		chm_rmode		reserved								ifmt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	surface_en	Surface enable (non-instant) 0: disabled 1: enabled
[30:22]	RO	reserved	Reserved
[21]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled
[20]	RW	precharge_mode	Pre-charge mode of the FDR FIFO 0: hardware mode. Hardware automatically enters the pre-charge status on the frame trailer. 1: software mode. Software determines whether to enter or exit the pre-charge status.
[19:16]	RO	reserved	Reserved
[15:14]	RW	lm_rmode	Luminance read mode 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[13:12]	RW	chm_rmode	Chrominance read mode 00: The read mode is bound to the interface. 01: The frame buffer data is read in progressive mode. 10: The top field is read in interlaced mode. 11: The bottom field is read in interlaced mode.
[11:4]	RO	reserved	Reserved

[3:0]	RW	ifmt	Format of the input data 0x1: Semi-planar YCbCr400 0x3: Semi-planar YCbCr420 0x4: Semi-planar YCbCr422 Other values: reserved

V1_UPD

V1_UPD is a V1 channel update enable register.

Offset Address	Register Name	Total Reset Value
0x1004	V1_UPD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							regup
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After the registers are updated, this bit is automatically cleared by the hardware.

V1_IRESO

V1_IRESO is a V1 input resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1028	V1_IRESO	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			ih			iw	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	ih	Height (in line). The configured value is the actual height minus 1. The frame height is referenced and its unit is line.
[11:0]	RW	iw	Width (in pixel). The configured value is the actual width minus 1.

V1_ORESO

V1_ORESO is a V1 output resolution register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x102C	V1_ORESO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oh												ow											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	oh	Height (in line). The configured value is the actual height minus 1. The frame height is referenced and its unit is line.
[11:0]	RW	ow	Width (in pixel). The configured value is the actual width minus 1.

V1_CBMPARA

V1_CBMPARA is a V1 overlay parameter register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1038	V1_CBMPARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								galpha							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	galpha	Overlay global alpha value. The value ranges from 0 to 255. The value 255 indicates opaque, and the value 0 indicates completely transparent.

V1_DFPOS

V1_DFPOS is a V1 surface start position (in the display window) register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1060	V1_DFPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_yfpos												disp_xfpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_yfpos	Start coordinates of the display column The frame height is referenced and its unit is line.
[11:0]	RW	disp_xfpos	Start coordinates of the display row

V1_DLPOS

V1_DLPOS is a V1 surface end position (in the display window) register (non-instant register).

Offset Address	Register Name	Total Reset Value
0x1064	V1_DLPOS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								disp_ylpos												disp_xlpos											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:12]	RW	disp_ylpos	End coordinates of the display column The frame height is referenced and its unit is line.
[11:0]	RW	disp_xlpos	End coordinates of the display row

V1_CSC_IDC

V1_CSC_IDC is a V1 CSC input DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1080	V1_CSC_IDC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									csc_en	cscidc1														cscidc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_en	CSC enable 0: disabled 1: enabled
[21:11]	RW	cscidc1	DC parameter of the input U/G component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc0	DC parameter of the input V/B component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_ODC

V1_CSC_ODC is a V1 CSC output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1084	V1_CSC_ODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									csc_sign_mode	cscodc1														cscodc0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22]	RW	csc_sign_mode	CSC output mode 0: The CSC output is a 10-bit unsigned number. 1: The CSC output is a 12-bit signed number.
[21:11]	RW	cscodc1	DC parameter of the output U/G component. The MSB is the signed bit. The value is expressed as a two's complement.

[10:0]	RW	cscodc0	DC parameter of the output Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_IODC

V1_CSC_IODC is a V1 CSC input/output DC component register (instant register).

Offset Address	Register Name	Total Reset Value
0x1088	V1_CSC_IODC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cscodc2												cscidc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:11]	RW	cscodc2	DC parameter of the output V/B component. The MSB is the signed bit. The value is expressed as a two's complement.
[10:0]	RW	cscidc2	DC parameter of the input Y/R component. The MSB is the signed bit. The value is expressed as a two's complement.

V1_CSC_P0

V1_CSC_P0 is a V1 CSC parameter 0 register (instant register).

Offset Address	Register Name	Total Reset Value
0x108C	V1_CSC_P0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	cscp01															reserved	cscp00														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp01	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp00	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P1

V1_CSC_P1 is a V1 CSC parameter 1 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1090	V1_CSC_P1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp10												reserved				cscp02											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp10	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp02	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P2

V1_CSC_P2 is a V1 CSC parameter 2 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1094	V1_CSC_P2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp12												reserved				cscp11											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp12	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp11	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P3

V1_CSC_P3 is a V1 CSC parameter 3 register (instant register).

Offset Address	Register Name	Total Reset Value
0x1098	V1_CSC_P3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cscp21												reserved				cscp20											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	cscp21	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.
[15]	RO	reserved	Reserved
[14:0]	RW	cscp20	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_CSC_P4

V1_CSC_P4 is a V1 CSC parameter 4 register (instant register).

Offset Address	Register Name	Total Reset Value
0x109C	V1_CSC_P4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cscp22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:0]	RW	cscp22	Data format: a 1-bit sign part, a 4-bit integer part, and an 8-bit decimal part. The value is expressed as a two's complement.

V1_P0LADDR

V1_P0LADDR is a V1 luminance address register.

Offset Address	Register Name	Total Reset Value
0x1204	V1_P0LADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Luminance start address for the video layer

V1_P0CADDR

V1_P0CADDR is a V1 chrominance address register.

Offset Address	Register Name	Total Reset Value
0x1208	V1_P0CADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	surface_addr	Chrominance start address for the video layer

V1_P0STRIDE

V1_P0STRIDE is a V1 stride register.

Offset Address	Register Name	Total Reset Value
0x120C	V1_P0STRIDE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	surface_cstride																surface_stride															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	surface_cstride	Stride of the chrominance buffer of the video layer (valid in semi-planar format), 128-bit alignment
[15:0]	RW	surface_stride	Stride of the video layer buffer (luminance stride in semi-planar format), 128-bit alignment

DHD1_CTRL

DHD1_CTRL is a DHD1 global control register.

CAUTION

All bits of this register must be configured before or when DHD0_CTRL.intf_en is configured; otherwise, the configurations do not take effect.

Offset Address	Register Name	Total Reset Value
0xC400	DHD1_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	intf_en	cbar_en	cbar_sel	reserved	reserved								reserved								precharge_en	precharge_mode	reserved			iop	reserved				regup	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	intf_en	Display interface enable (instant). Data is output over the interface only when this field is enabled. 0: disabled 1: enabled
[30]	RW	cbar_en	Color bar enable. The color bar is output over the interface when this field is enabled. 0: disabled 1: enabled
[29]	RW	cbar_sel	Color space select for the output color bar (instant) 0: VGA 1: YPbPr
[28]	RO	reserved	Reserved.
[27:20]	RW	reserved	Reserved.
[19:11]	RO	reserved	Reserved.
[10]	RW	precharge_en	Pre-charge enable. This field is valid when the precharge_mode field is 1 (software mode). 0: disabled 1: enabled

[9]	RW	precharge_mode	Pre-charge mode of AFIFO 0: hardware mode. Hardware automatically enters the pre-charge status in the vertical blanking region. 1: software mode. Software determines whether to enter or exit the pre-charge status.
[8:5]	RO	reserved	Reserved
[4]	RW	iop	Display mode (non-instant) 0: interlaced display 1: progressive display
[3:1]	RO	reserved	Reserved
[0]	WC	regup	Surface register update. After the registers at this layer are configured, the registers are updated when the value 1 is written to this bit. After the registers are updated, this bit is automatically cleared by the hardware.

DHD1_VSYNC

DHD1_VSYNC is a top field vertical sync timing register in interlaced output mode or frame vertical sync timing register in progressive output mode. This register is a non-instant register.

Offset Address	Register Name	Total Reset Value
0xC404	DHD1_VSYNC	0x0011_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vfb								vbb								vact											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:20]	RW	vfb	In interlaced output mode: top vertical front blanking (TVFB) In progressive output mode: vertical front blanking (VFB) The configured value is the actual value minus 1.
[19:12]	RW	vbb	In interlaced output mode: top vertical back blanking (TVBB) In progressive output mode: vertical back blanking (VBB)+vertical pulse width (VPW) The configured value is the actual value minus 1.
[11:0]	RW	vact	In interlaced output mode: height of an active picture on the top field In progressive output mode: height of an active picture in a frame. The configured value is the actual value minus 1.

DHD1_HSYNC1

DHD1_HSYNC1 is a horizontal sync configuration register in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC408	DHD1_HSYNC1	0x00BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hbb																hact															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hbb	Horizontal back blanking (HBB), in pixel The configured value is the actual value minus 1.
[15:0]	RW	hact	Number of horizontal pixels in an active region The configured value is the actual value minus 1.

DHD1_HSYNC2

DHD1_HSYNC2 is a horizontal sync configuration register in interlaced or progressive output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC40C	DHD1_HSYNC2	0x0000_020F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hmid																hfb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	hmid	Bottom vertical sync active pixel (active region) The configured value is the actual value minus 1.
[15:0]	RW	hfb	HFB, in pixel The configured value is the actual value minus 1.

DHD1_VPLUS

DHD1_VPLUS is a bottom field vertical sync timing in interlaced output mode (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC410	DHD1_VPLUS	0x0021_321B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bvfb								bvbb								bvact											
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:20]	RW	bvfb	Bottom vertical front blanking (BVFB) in interlaced output mode The configured value is the actual value minus 1.
[19:12]	RW	bvbb	Bottom vertical back blanking (BVBB)+VPW in interlaced output mode The configured value is the actual value minus 1.
[11:0]	RW	bvact	Height of an active picture in the bottom field in interlaced output mode The configured value is the actual value minus 1.

DHD1_PWR

DHD1_PWR is a sync signal pulse width register (non-instant register).

Offset Address	Register Name	Total Reset Value
0xC414	DHD1_PWR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								vpw								hpw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	vpw	VPW. The configured value is the actual value minus 1.
[15:0]	RW	hpw	Horizontal pulse width (HPW). The configured value is the actual value minus 1.

DHD1_VTTHD

DHD1_VTTHD is a vertical timing threshold register (instant register).

CAUTION

It can be used to set two thresholds for generating two interrupts separately.

Offset Address	Register Name	Total Reset Value
0xC41C	DHD1_VTTHD	0x0001_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15	14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				thd1_mode	reserved	vtmgthd1		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15]	RW	thd1_mode	Mode of generating threshold 1 0: frame mode. The threshold count is by frame. 1: field mode. The threshold count is by field during interlaced displaying.
[14:13]	RO	reserved	Reserved
[12:0]	RW	vtmgthd1	Vertical timing threshold 1. When the vertical timing counter reaches this threshold, the VOINTSTA[dhdvtthd_int1] interrupt is triggered.

DHD1_STATE

DHD1_STATE is a DHD1 status register.

Offset Address	Register Name	Total Reset Value
0xC4F0	DHD1_STATE	0x0000_0006

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved		count_int		vcnt				bottom_field	vblank	vback_blank
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	1	1	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:16]	RO	count_int	DHD1 interrupt count. The count value is increased by 1 each time a vertical timing interrupt is reported.
[15:3]	RO	vcnt	Active display line count of DHD1
[2]	RO	bottom_field	DHD1 top/bottom field indicator 0: top field 1: bottom field
[1]	RO	vblank	DHD1 blanking region indicator 0: active region 1: blanking region
[0]	RO	vback_blank	DHD1 back blanking region indicator 0: non-back blanking region 1: blanking region

BT_CLIP0_L

BT_CLIP0_L is a BT.656 clip lowest threshold register (instant register).

Offset Address	Register Name	Total Reset Value
0xD210	BT_CLIP0_L	0x0100_4010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_cl2								clip_cl1								clip_cl0											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	clip_cl2	Lowest threshold Y/R of component 2, unsigned integer
[19:10]	RW	clip_cl1	Lowest threshold Cb/G of component 1, unsigned integer
[9:0]	RW	clip_cl0	Lowest threshold Cr/B of component 0, unsigned integer

BT_CLIP0_H

BT_CLIP0_H is a BT.656 clip highest threshold register (instant register). For example, the output data needs to be clipped in BT.656 output mode.

Offset Address	Register Name	Total Reset Value
0xD214	BT_CLIP0_H	0x0EB3_C0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_ch2								clip_ch1								clip_ch0											
Reset	0	0	0	0	1	1	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	clip_ch2	Highest threshold Y/R of component 2, unsigned integer
[19:10]	RW	clip_ch1	Highest threshold Cb/G of component 1, unsigned integer
[9:0]	RW	clip_ch0	Highest threshold Cr/B of component 0, unsigned integer

BT_DITHER0_CTRL

BT_DITHER0_CTRL is a BT.656 dither control register.

Offset Address	Register Name	Total Reset Value
0xD280	BT_DITHER0_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_md			reserved																												
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RW	dither_md	Dither mode select 000: 12-bit inputs, 10-bit outputs, no dithering, and direct bit truncation 001: 12-bit inputs, 10-bit outputs, and time-domain dithering 010: 12-bit inputs, 10-bit outputs, and spatial-domain dithering 011: 12-bit inputs, 8-bit outputs, and time-domain and spatial-domain dithering 100: 12-bit inputs, 10-bit outputs, and round off 101: 12-bit inputs, 8-bit outputs, and round off Other values: reserved
[28:0]	RO	reserved	Reserved

BT_DITHER0_COEF0

BT_DITHER0_COEF0 is BT.656 dither coefficient register 0.

Offset Address	Register Name	Total Reset Value
0xD284	BT_DITHER0_COEF0	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef3								dither_coef2								dither_coef1								dither_coef0							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef3	Coefficient 3 for time-domain dithering
[23:16]	RW	dither_coef2	Coefficient 2 for time-domain dithering
[15:8]	RW	dither_coef1	Coefficient 1 for time-domain dithering
[7:0]	RW	dither_coef0	Coefficient 0 for time-domain dithering

BT_DITHER0_COEF1

BT_DITHER0_COEF1 is BT.656 dither coefficient register 1.

Offset Address	Register Name	Total Reset Value
0xD288	BT_DITHER0_COEF1	0xDD66_4400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dither_coef7								dither_coef6								dither_coef5								dither_coef4							
Reset	1	1	0	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dither_coef7	Coefficient 7 for time-domain dithering
[23:16]	RW	dither_coef6	Coefficient 6 for time-domain dithering
[15:8]	RW	dither_coef5	Coefficient 5 for time-domain dithering
[7:0]	RW	dither_coef4	Coefficient 4 for time-domain dithering

LCD_CTRL

LCD_CTRL is an LCD control register.

Offset Address	Register Name	Total Reset Value
0xD400	LCD_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		lcd_serial_mode	lcd_serial_perd	reserved	lcd_data_inv	reserved																									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RW	lcd_serial_mode	LCD serial mode 0: reserved 1: serial mode
[28]	RW	lcd_serial_perd	Number of cycles of the LCD serial output single-pixel clock 0: three cycles 1: four cycles
[27]	RW	reserved	Reserved
[26]	RW	lcd_data_inv	LCD output line sequence 0: from upper bits to lower bits (bit 15 to bit 0) 1: from lower bits to upper bits (bit 0 to bit 15)
[25:0]	RO	reserved	Reserved

LCD_SYNC_INV

LCD_SYNC_INV is a sync signal polarity configuration register when the LCD external sync timing is input.

CAUTION

This register takes effect immediately after configuration. That is, the polarity of the corresponding sync signal is affected immediately after a bit is configured.

Offset Address	Register Name	Total Reset Value
0xD408	LCD_SYNC_INV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												f_inv	vs_inv	hs_inv	dv_inv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	f_inv	Parity field indicator signal output reverse-phase enable (instant register) 0: disabled 1: enabled
[2]	RW	vs_inv	Vertical sync pulse output reverse-phase enable (instant register) 0: disabled 1: enabled
[1]	RW	hs_inv	Horizontal sync pulse output reverse-phase enable (instant register) 0: disabled 1: enabled
[0]	RW	dv_inv	Data validity signal output reverse-phase enable (instant register) 0: disabled 1: enabled

DATE_COEFF0

DATE_COEFF0 is a standard parameter configuration register.

Offset Address	Register Name	Total Reset Value
0xF200	DATE_COEFF0	0x5284_14FC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clpf_sel		dis_ire	reserved	pal_half_en	pbpr_lpf_en	scanline	rgb_en	vbi_lpf_en	reserved	style_sel			sync_mode_sel			sync_mode_scart	length_sel	agc_amp_sel	luma_dl				reserved	oversam_en		lunt_en	oversam2_en	chlp_en	sylp_en	chgain_en	reserved
Reset	0	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:30]	RW	clpf_sel	Bandwidth of the chrominance low-pass filter 00: 1.1 MHz (NTSC) 01: 1.3 MHz (PAL) 10: 1.6 MHz (for test) 11: reserved
[29]	RW	dis_ire	For the (M) NTSC and (M, N) PAL standards, the black level is 7.5 IRE higher than the blanking level; for other standards, the black level is equal to the blanking level. This bit controls whether the black level is 7.5 IRE higher than the blanking level. 0: The black level is 7.5 IRE higher than the blanking level. 1: The black level is equal to the blanking level.
[28]	-	reserved	Reserved
[27]	RW	pal_half_en	PAL half line reduction enable 0: disabled 1: enabled
[26]	RW	pbpr_lpf_en	Component chrominance low-pass filtering enable 0: disabled 1: enabled
[25]	RW	scanline	Number of scanned lines in each frame based on standards. For the (M) NTSC, NTSC-J, and (M) PAL standards, each line contains 525 lines; for the (B, D, J, H, I) PAL, (N) PAL, and (Nc) PAL standards, each frame contains 625 lines. 0: 525 lines in a frame 1: 625 lines in a frame

[24]	RW	rgb_en	When intf_sel is set to 100, this bit determines whether the component signal is RGB or YPbPr. 0: YPbPr 1: RGB
[23]	RW	vbi_lpf_en	VBI data low-pass filtering enable 0: no filtering 1: filtering
[22]	RW	reserved	Reserved
[21:18]	RW	style_sel	CVBS/S-Video output signal standard when this bit works with the scanline bit When the scanline bit is 0 (525 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (M) NTSC standard 0x2: NTSC-J standard 0x4: (M) PAL standard When the scanline bit is 1 (625 scanned lines in a frame), the definition of the style_sel bit is as follows: 0x1: (B, D, G, H, I) PAL standard 0x2: (N) PAL standard 0x4: (Nc) PAL standard Other values: reserved
[17:16]	RW	sync_mode_sel	bit[17]: specifies whether there are sync signals in three channels during component output. This bit takes effect only when the sync_mode_scart bit is set to 0. bit[17] is valid only when intf_sel is set to 100 (component output enabled). The definition of bit[17] is as follows: 0: Only one channel contains sync signals during component output. 1: Three channels contain sync signals during component output. When bit[17] is set to 0, the sync channel must be the Y channel for YPbPr output or G channel for RGB output. bit[16]: specifies whether there are blanking radixes during RGB output. bit[16] is valid only when intf_sel is set to 100 and rgb_en is set to 1. The definition of bit[16] is as follows: 0: There are no blanking radixes during RGB output. 1: There are blanking radixes during RGB output.
[15]	RW	sync_mode_scart	Overlay sync control for the components of three channels 0: Component sync output is configured based on sync_mode_sel bit[1]. 1: The components of the three channels are not overlaid and synchronized. In this case, sync_mode_sel bit[1] must be set to 0.

[14]	RW	length_sel	Active width of each video line (in pixel) 0: output according to the line active pixel width in BT.601 mode. 1: output according to the line active pixel width in BT.470 mode When this bit is set to 0, the active width of the line is 720 pixels. When this bit is set to 1, the active width of the line is 704 pixels for the 625-line standard or 712 pixels for the 525-line standard. Currently, the BT.601 mode and BT.470 mode cannot be dynamically switched. You can change the mode only after reset. The BT.601 mode is recommended, and this mode is the default mode after power-on reset.
[13]	RW	agc_amp_sel	AGC pulse select 0: The AGC pulse is generated based on the on-chip default value (recommended). 1: The AGC pulse is generated based on the off-chip configuration.
[12:9]	RW	luma_dl	Lead or lag-behind offset of the chrominance signal relative to the luminance signal, in the unit of half a pixel width bit[12]: offset direction of the chrominance signal relative to the luminance signal. 0: The chrominance signal lags behind the luminance signal. 1: The chrominance signal leads the luminance signal. bit[11:9]: absolute offset of the chrominance signal relative to the luminance signal. The value is in binary format and ranges from 0 to 7. 000: The chrominance signal is aligned with the luminance signal. No adjustment is required. 001−111: The chrominance signal leads or lags behind the luminance signal by one to seven units.
[8]	-	reserved	Reserved
[7:6]	RW	oversam_en	Level-1 over-sampling enable. Both luminance over-sampling and chrominance over-sampling are controlled. bit[7]: luminance over-sampling enable 0: disabled 1: enabled bit[6]: chrominance over-sampling enable 0: disabled 1: enabled
[5]	RW	lunt_en	Luminance notch enable 0: disabled 1: enabled
[4]	RW	oversam2_en	Level-2 over-sampling enable. Both the luminance channel and chrominance channel are controlled. 0: disabled 1: enabled

[3]	RW	chlp_en	Chrominance low-pass filtering enable 0: disabled 1: enabled
[2]	RW	sylp_en	Sync low-pass filtering enable 0: disabled 1: enabled
[1]	RW	chgain_en	Chrominance gain enable 0: disabled 1: enabled
[0]	RW	reserved	Reserved

DATE_COEFF21

DATE_COEFF21 is an output matrix control register.

Offset Address	Register Name	Total Reset Value
0xF254	DATE_COEFF21	0x0065_1432

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dac0_in_sel	
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2:0]	RW	dac0_in_sel	DAC0 output mode 001: CVBS Other values: reserved

DATE_COEFF22

DATE_COEFF22 is a DTO initial phase configuration register.

Offset Address	Register Name	Total Reset Value
0xF258	DATE_COEFF22	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								video_phase_delta							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RW	video_phase_delta	DTO initial phase

DATE_COEFF23

DATE_COEFF23 is a VIDEO_OUT delay configuration register.

Offset Address	Register Name	Total Reset Value
0xF25C	DATE_COEFF23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														dac0_out_dly	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2:0]	RW	dac0_out_dly	DAC0 output delay cycle The value is measured by a 54 MHz clock cycle, and the value *n* indicates *n* delay cycles.

DATE_COEFF24

DATE_COEFF24 is a color burst start position register.

Offset Address	Register Name	Total Reset Value
0xF260	DATE_COEFF24	0x0001_2C99

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	burst_start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31:0]	RW	burst_start	Color burst start position

DATE_COEFF37

DATE_COEFF37 is an up-sampling filtering coefficient 1 register.

Offset Address	Register Name	Total Reset Value
0xF294	DATE_COEFF37	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y1_coeff3								fir_y1_coeff2								fir_y1_coeff1								fir_y1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31:24]	RW	fir_y1_coeff3	Coefficient 13 for luminance up-sampling and filtering
[23:16]	RW	fir_y1_coeff2	Coefficient 12 for luminance up-sampling and filtering
[15:8]	RW	fir_y1_coeff1	Coefficient 11 for luminance up-sampling and filtering
[7:0]	RW	fir_y1_coeff0	Coefficient 10 for luminance up-sampling and filtering

DATE_COEFF38

DATE_COEFF38 is an up-sampling filtering coefficient 2 register.

Offset Address	Register Name	Total Reset Value
0xF298	DATE_COEFF38	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff1																fir_y2_coeff0															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff1	Coefficient 21 for luminance up-sampling and filtering
[15:0]	RW	fir_y2_coeff0	Coefficient 20 for luminance up-sampling and filtering

DATE_COEFF39

DATE_COEFF39 is an up-sampling filtering coefficient 3 register.

Offset Address	Register Name	Total Reset Value
0xF29C	DATE_COEFF39	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_y2_coeff3																fir_y2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RW	fir_y2_coeff3	Coefficient 23 for luminance up-sampling and filtering
[15:0]	RW	fir_y2_coeff2	Coefficient 22 for luminance up-sampling and filtering

DATE_COEFF40

DATE_COEFF40 is an up-sampling filtering coefficient 4 register.

Offset Address	Register Name	Total Reset Value
0xF2A0	DATE_COEFF40	0x19EF_0CF9

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c1_coeff3								fir_c1_coeff2								fir_c1_coeff1								fir_c1_coeff0							
Reset	0	0	0	1	1	0	0	1	1	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	1	0	0	1

Bits	Access	Name	Description
[31:24]	RW	fir_c1_coeff3	Coefficient 13 for chrominance up-sampling and filtering
[23:16]	RW	fir_c1_coeff2	Coefficient 12 for chrominance up-sampling and filtering
[15:8]	RW	fir_c1_coeff1	Coefficient 11 for chrominance up-sampling and filtering
[7:0]	RW	fir_c1_coeff0	Coefficient 10 for chrominance up-sampling and filtering

DATE_COEFF41

DATE_COEFF41 is an up-sampling filtering coefficient 5 register.

Offset Address	Register Name	Total Reset Value
0xF2A4	DATE_COEFF41	0x003A_FFDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c2_coeff1																fir_c2_coeff0															
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff1	Coefficient 21 for chrominance up-sampling and filtering
[15:0]	RW	fir_c2_coeff0	Coefficient 20 for chrominance up-sampling and filtering

DATE_COEFF42

DATE_COEFF42 is an up-sampling filtering coefficient 6 register.

Offset Address	Register Name	Total Reset Value
0xF2A8	DATE_COEFF42	0x0148_FF97

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fir_c2_coeff3																fir_c2_coeff2															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RW	fir_c2_coeff3	Coefficient 23 for chrominance up-sampling and filtering
[15:0]	RW	fir_c2_coeff2	Coefficient 22 for chrominance up-sampling and filtering

DATE_DACDET1

DATE_DACDET1 is DAC automatic detection register 1.

Offset Address	Register Name	Total Reset Value
0xF2C0	DATE_DACDET1	0x000D_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								det_line								reserved				vdac_det_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	det_line	Line of the detected level
[15:10]	-	reserved	Reserved

[9:0]	RW	vdac_det_high	Detected level

DATE_DACDET2

DATE_DACDET2 is DAC automatic detection register 2.

Offset Address	Register Name	Total Reset Value
0xF2C4	DATE_DACDET2	0x0030_0118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	vdac_det_en	reserved							det_pixel_wid								reserved								det_pixel_sta							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0

Bits	Access	Name	Description
[31]	RW	vdac_det_en	DAC automatic detection enable 0: disabled 1: enabled
[30:27]	-	reserved	Reserved
[26:16]	RW	det_pixel_wid	Level width
[15:11]	-	reserved	Reserved
[10:0]	RW	det_pixel_sta	Start position of a line

DATE_COEFF56

DATE_COEFF56 is an over-sampling round-off register.

Offset Address	Register Name	Total Reset Value
0xF2E0	DATE_COEFF56	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															oversam2_round_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	oversam2_round_en	Round-off enable during 2x up-sampling 0: disabled 1: enabled

DATE_COEFF57

DATE_COEFF57 is a CVBS gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E4	DATE_COEFF57	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cvbs_gain_en	reserved							ycvbs_gain								u_gain								v_gain							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	cvbs_gain_en	CVBS gain enable 0: disabled 1: enabled
[30:24]	-	reserved	Reserved
[23:16]	RW	ycvbs_gain	Gain control of the luminance component Y
[15:8]	RW	u_gain	Gain control of the chrominance component U
[7:0]	RW	v_gain	Gain control of the chrominance component V

DATE_COEFF58

DATE_COEFF58 is a component gain control register.

Offset Address	Register Name	Total Reset Value
0xF2E8	DATE_COEFF58	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	comp_gain_en	reserved							ycomp_gain								pb_gain								pr_gain							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	comp_gain_en	Component gain enable 0: disabled 1: enabled
[30:24]	-	reserved	Reserved
[23:16]	RW	ycomp_gain	Gain control of the luminance component Y
[15:8]	RW	pb_gain	Gain control of the chrominance component U
[7:0]	RW	pr_gain	Gain control of the chrominance component V

DATE_COEFF59

DATE_COEFF59 is a clip control bit register.

Offset Address	Register Name	Total Reset Value
0xF2EC	DATE_COEFF59	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cb_gain_polar	reserved			cr_os_clip_fullrange	cb_os_clip_fullrange	reserved		v_os_clip_fullrange	u_os_clip_fullrange	reserved			y_os_clip_fullrange	reserved		clpf_clip_fullrange	ynotch_clip_fullrange
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved

[16]	RW	cb_gain_polar	Chrominance subcarrier polarity control 0: negative gain 1: positive gain
[15:14]	-	reserved	Reserved
[13]	RW	cr_os_clip_fullrange	Cr component clip enable on the up-sampling module 0: disabled 1: enabled
[12]	RW	cb_os_clip_fullrange	Cb component clip enable on the up-sampling module 0: disabled 1: enabled
[11:10]	-	reserved	Reserved
[9]	RW	v_os_clip_fullrange	V component clip enable on the up-sampling module 0: disabled 1: enabled
[8]	RW	u_os_clip_fullrange	U component clip enable on the up-sampling module 0: disabled 1: enabled
[7:5]	-	reserved	Reserved
[4]	RW	y_os_clip_fullrange	Y component clip enable on the up-sampling module 0: disabled 1: enabled
[3:2]	-	reserved	Reserved
[1]	RW	clpf_clip_fullrange	Chrominance low-pass module clip enable 0: disabled 1: enabled
[0]	RW	ynotch_clip_fullrange	Luminance notch module clip enable. 0: disabled 1: enabled

9.3 MIPI RX

9.3.1 Overview

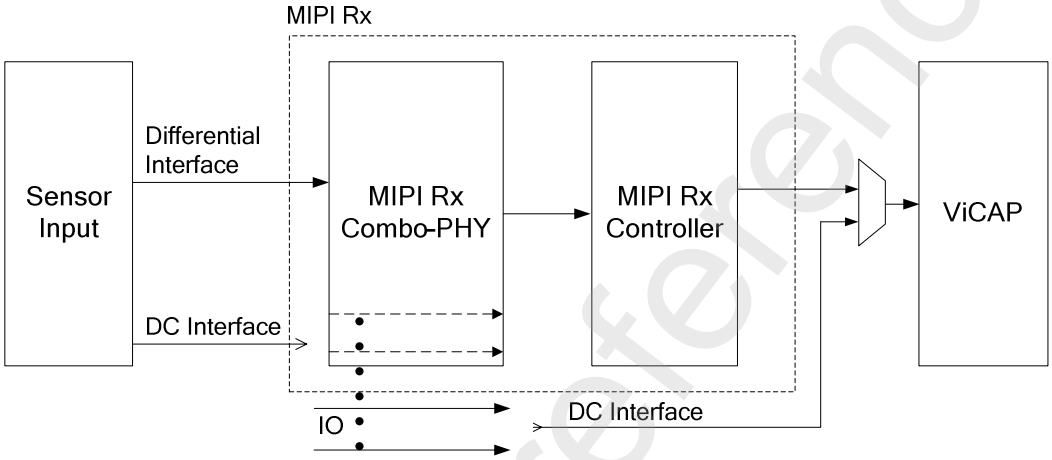
The MIPI RX receives LVDSs that carry raw video data (Bayer RGB data), converts the signals into the digital camera (DC) timing, and transfers it to the downstream VICAP module.

The MIPI RX supports serial video signal inputs such as the MIPI D-PHY, LVDS, and HiSPI. The serial video interfaces provide more bandwidth to enhance transmission stability. The

MIPI RX is also compatible with the DC video interface, supports the 3.3 V/1.8 V DC parallel input, and requires a less number of chip pins while providing better compatibility.

The MIPI RX consists of the combo-PHY and controller. Figure 9-19 shows the MIPI RX workflow and its position in the system.

Figure 9-19 MIPI RX workflow and its position in the system



9.3.2 Features

The MIPI RX has the following features:

- MIPI D-PHY interface with at most four lanes, up to 1 Gbit/s per lane
- LVDS/Sub-LVDS/HiSPI interface with at most four lanes, up to 1 Gbit/s per lane
- CMOS parallel 1.8 V/3.3 V input
- Raw8, raw10, raw12, raw14, or raw16 data parsing
- 2-frame WDR and multiple WDR timings
- Endian mode configuration for LVDS or HiSPI mode pixel or synchronization code
- Configuration of channel quantity and sequence

9.3.3 Function Description

9.3.3.1 Typical Applications

The MIPI RX is a collection unit that supports multiple differential video input interfaces. It is used for converting interface timings. It can receive data through the MIPI, LVDS, sub-LVDS, HiSPI, or DC interface. Depending on the function configuration, the MIPI RX allows data transmission at various rates and transmission of images in various resolutions, and supports multiple image sensors.

The MIPI RX supports at most 1-link/4-lane MIPI input and 1-link/4-lane LVDS/sub-LVDS/HiSPI input. The input pins can be multiplexed to support single-ended DC or BT.1120 channel inputs, thereby providing better compatibility with fewer chip pins.

Table 9-7 lists the interfaces supported by the MIPI RX.

Table 9-7 Interfaces supported by the MIPI RX

Interface Type	Common Mode Voltage	Differential Mode Voltage	Maximum Clock Frequency	Maximum Data Rate per Lane
D-PHY	200 mV	200 mV	500 MHz	1 Gbit/s
Sub-LVDS	900 mV	150 mV	500 MHz	1 Gbit/s
LVDS	1.25 V	350 mV	500 MHz	1 Gbit/s
HiSPI (HiVCM)	900 mV	280 mV	500 MHz	1 Gbit/s
HiSPI (SLVS)	200 mV	200 mV	500 MHz	1 Gbit/s
CMOS parallel	1.8 V	1.8 V	100 MHz	100 Mbit/s
CMOS parallel	3.3 V	3.3 V	100 MHz	100 Mbit/s

The MIPI RX only converts the interface timings, and does not process image data formats. It supports any resolution and frame rate as long as the bandwidth requirement is met. The MIPI RX bandwidth is limited by the interface data rate and internal processing speed of the Combo PHY. The Combo PHY interface supports the maximum interface rate of 1 Gbit/s per lane and maximum internal processing speed of 250 megapixels/s.

NOTE

The maximum bandwidth supported by the Combo PHY interface is (1 Gbit/s x number of lanes). The maximum internal processing capability is (250 megapixels x pixel bit width). In the actual application, the maximum operating rate of the MIPI RX is limited by the smaller value between the maximum bandwidth and the maximum internal processing capability.

9.3.3.2 Function Implementation

Data Format of the MIPI Interface

MIPI specifications are developed and maintained by different working groups and cover diverse application requirements for use in different fields. The MIPI RX supports the D-PHY ver1.0 and CSI-2 ver1.0. D-PHY ver1.0 stipulates the rules of transmission at the physical layer, and CSI-2 ver1.0 stipulates the format and protocol of camera output data packets.

(1) D-PHY

D-PHY is a high-speed physical layer standard released by the MIPI Alliance. The standard stipulates the physical specifications and transmission protocols at the physical layer for hosts and peripherals. D-PHY uses the LVDS technology with 200 mV source synchronization. The data rate of each channel ranges from 80 Mbit/s to 1000 Mbit/s. D-PHY can work in either low-power (LP) or high-speed (HS) mode.

(2) CSI-2

CSI-2 is a camera data protocol that stipulates the data packet format used for communication between hosts and peripherals.

CSI-2 supports image application in different pixel formats, and the smallest unit for data transmission is byte. An appropriate number of data channels can be selected to attain enhanced CSI-2 performance. CSI-2 specifies how the TX end packetizes pixel data into

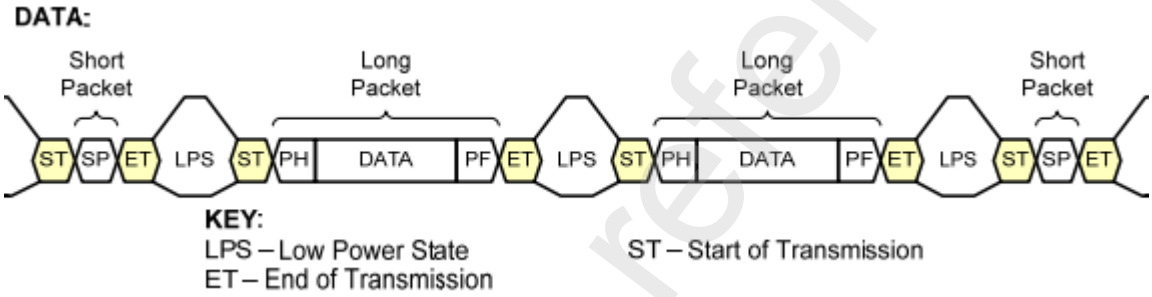
bytes and how multiple data channels are allocated and managed. Byte data is organized in data packets, which are transmitted between the start of transmission (SoT) and the end of transmission (EoT). The RX end parses the data packets based on the applicable protocol and restores the pixel data.

The MIPI RX can parse pixel data in RAW8, RAW10, RAW12, RAW14 or RAW16 format.

CSI-2 data packets can be long or short and contain parity codes for parity check and error correction.

Both long and short packets are transmitted between the SoT and EoT. D-PHY works in LP mode in gaps of data transmission. Figure 9-20 shows the mechanism for transmitting CSI-2 data packets. PH and PF mean packet header and packet footer, respectively.

Figure 9-20 CSI-2 data packet transmission mechanism



Long packets are used to transmit effective pixel data in five parts: Data ID, Word Count, ECC, Payload, and Checksum.

Data ID comprises Virtual Channel and Data Type. Virtual Channel controls the channel used for transmission and can specify channel multiplexing so that different channels will transmit different data. Data Type specifies the type of data.

Word Count indicates the amount of data to be received by the RX end.

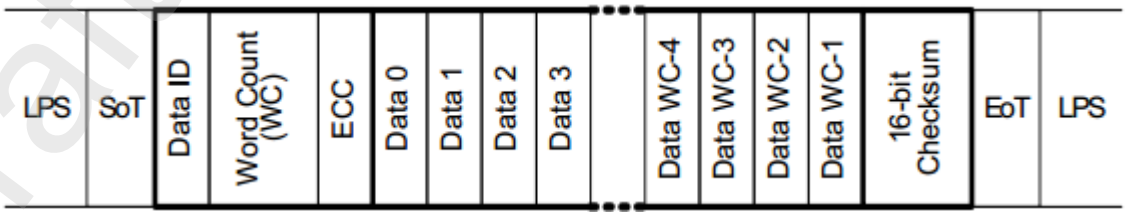
ECC is 8-bit error correction code that can be used to detect and correct errors in Data Type and Word Count.

Payload is the pixel data to be transmitted.

Checksum is generated by a linear feedback shift register and is used to check payload data.

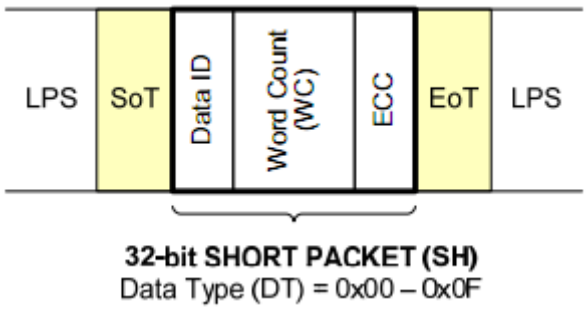
Figure 9-21 shows the format of a long packet.

Figure 9-21 CSI-2 long packet format



Short packets are used to transmit synchronization information in three parts: Data ID, Word Count, and ECC. Figure 9-22 shows its format.

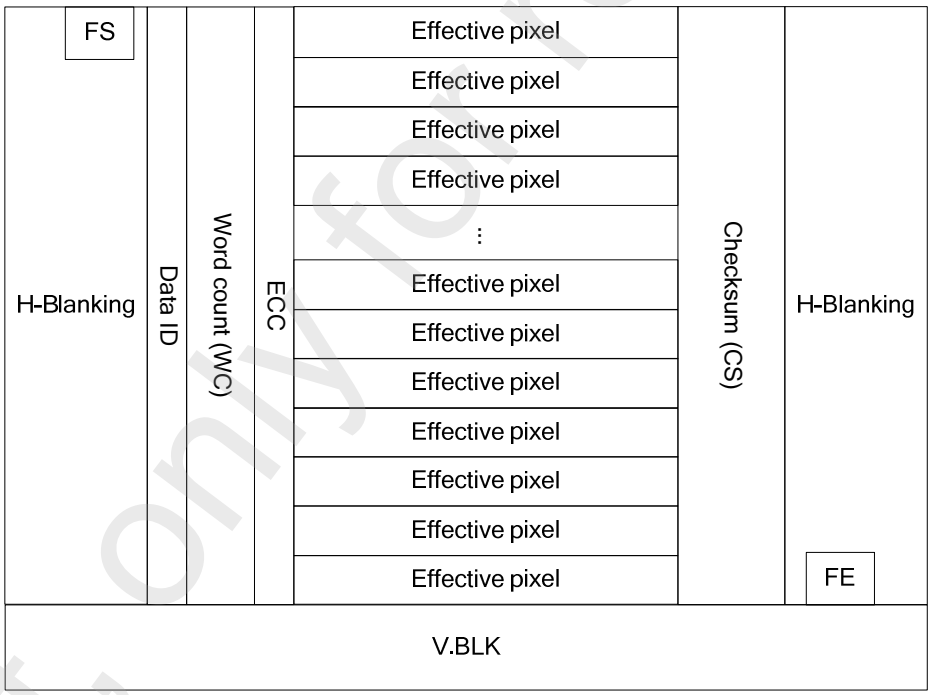
Figure 9-22 CSI-2 short packet format



Linear Mode of the MIPI Interface

Figure 9-23 shows the video transfer format in linear mode of the MIPI interface. FS indicates the start of the frame, and FE indicates the end of the frame. The 32-bit data packet in each line consists of the virtual channel and data type information of the current line.

Figure 9-23 Image data format of the MIPI interface



WDR Modes of the MIPI Interface

The MIPI RX supports three WDR modes of the MIPI interface.

- MIPI WDR mode 1: The virtual channel (VC) is used to distinguish the long exposure data and short exposure data.
- MIPI WDR mode 2: The data type (DT) is used to distinguish the long exposure data and short exposure data.

- MIPI WDR mode 3: Data is transferred in DOL WDR mode.

Figure 9-24 shows data transfer in WDR mode that uses the VC. The short FS and FE packets as well as long data packets contain the VC information. The MIPI RX controller detects the long/short exposure data based on the VC information in the short/long packet, adds a 2-bit signal flag to each line of data, and outputs the data, signal flag, and DC timing to the VICAP module, where demultiplexing is implemented.

Figure 9-24 Data transfer in WDR mode of the MIPI interface (the VC is used)

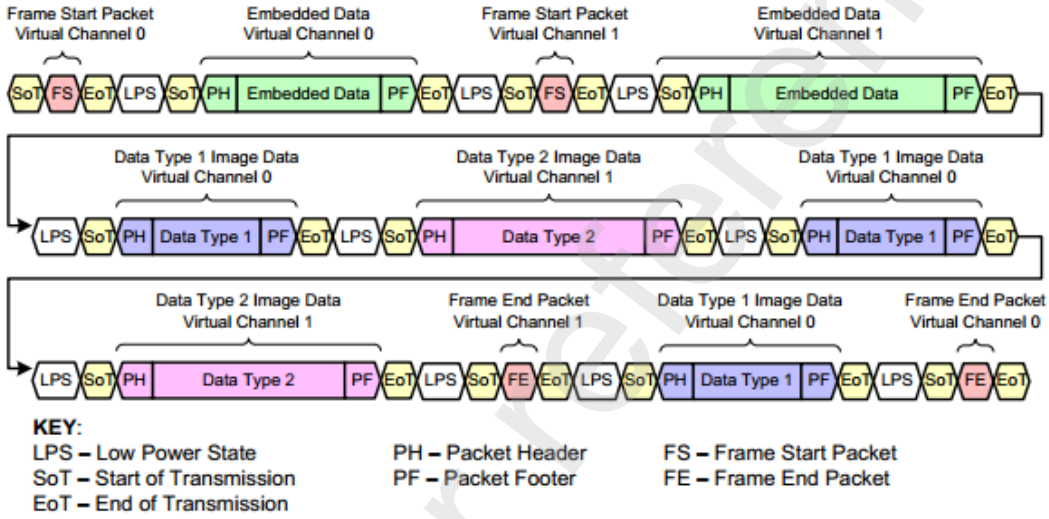


Figure 9-25 shows data transfer in WDR mode that uses the DT. The frame with different exposure lengths uses one group of short FS and FE packets. The header of the long packet contains the DT information. The bit width of the DT0 raw data may be different from that of the DT1 raw data. The MIPI RX controller distinguishes the long and short exposure data based on the DT information, adds a 2-bit signal flag to each line of data, and outputs the data, signal flag, and DC timing to the VICAP module, where demultiplexing is implemented.

Figure 9-25 Data transfer in WDR mode of the MIPI interface (the DT is used)

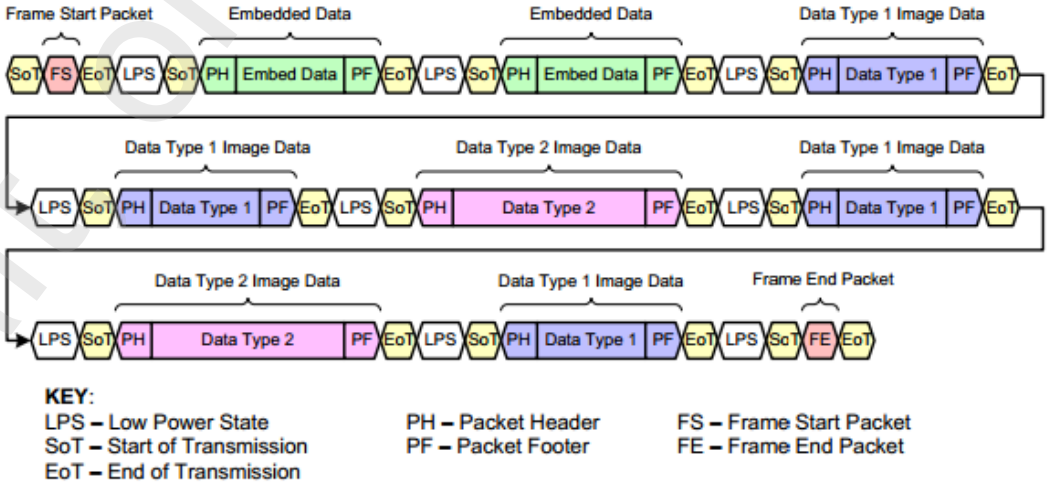
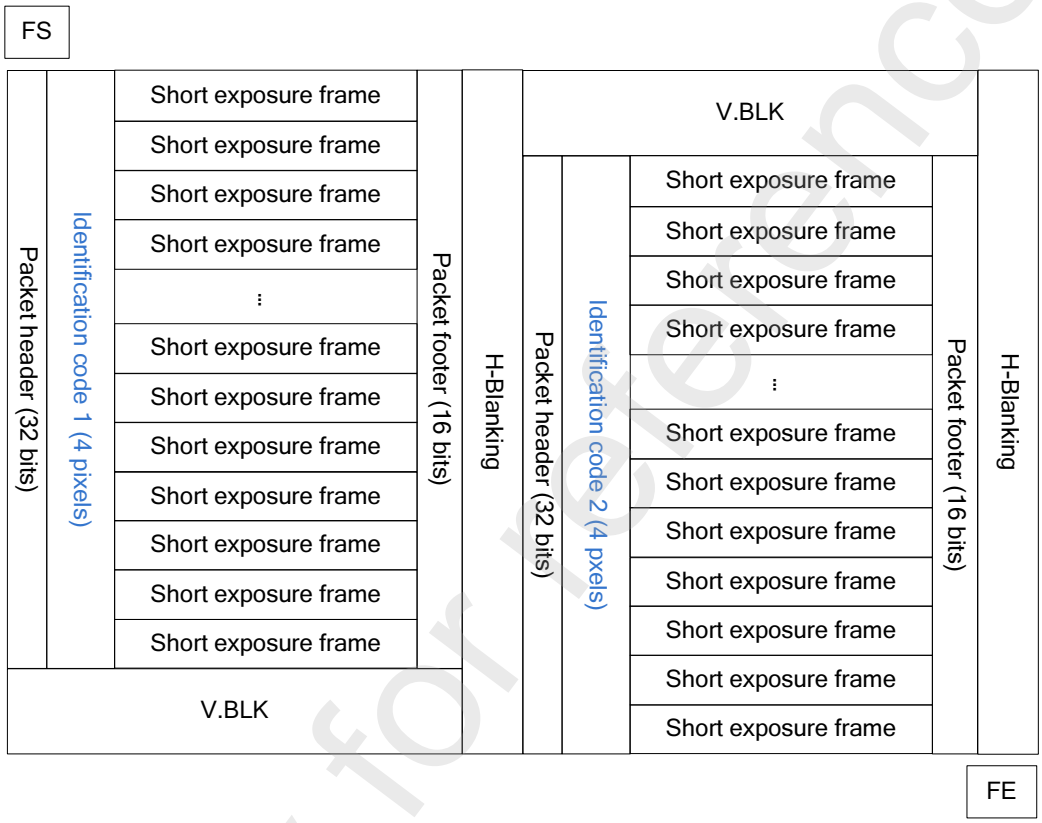


Figure 9-26 shows data transfer in DOL WDR mode of the MIPI interface. The long and short exposure data uses one group of short FS and FE packets. The first four pixels in each line are the identification codes for distinguishing the long exposure data and short exposure data.

Figure 9-26 Data transfer in DOL WDR mode of the MIPI interface



NOTE

The image sensor supports the frame interleaved WDR mode and line interleaved WDR mode. The timings and data formats for the two modes are the same. This section takes the line interleaved WDR mode as an example.

Input Data Format of the LVDS Interface

The LVDS is widely used in front-end cameras. It identifies data of the blanking region and active region by synchronization code.

NOTE

For the LVDS, there are only the electrical transfer specifications but no standard protocols on the timing and data format. The sub-LVDS is a differential signal technology with ultra-low voltage swing. The common mode/differential mode voltage of the sub-LVDS is lower than that of the LVDS. Compared with the LVDS, the sub-LVDS is more suitable for image sensor applications. The sub-LVDS can be considered as one type of LVDS. In the following sections, sub-LVDS is also called LVDS.

The Combo PHY interface of the MIPI RX converts the differential serial data into parallel data. Then the MIPI RX controller splits and combines the parallel data, extracts the synchronization code, and parses the pixel data.

In LVDS transmission mode, frame or line synchronization signals are integrated into data streams. In data streams, SOF and EOF indicate the start and end of a frame, whereas SOL and EOL indicate the start and end of a line. In a data stream, each of SOF, EOF, SOL, and EOL consists of four fields, and the bit width and pixel data of each field are consistent. The first three fields are fixed reference codes, and the fourth field is used to identify the start of end of a frame or line. Table 9-8 illustrates the LVDS synchronization code format.

Table 9-8 LVDS synchronization code format

Field	Bit Width	Synchronization Code			
		SOL/SAV (Valid Line)	EOL/EAV (Valid Line)	SOF/SAV (Invalid Line)	EOF/EAV (Invalid Line)
First code	8 bits	FFh	FFh	FFh	FFh
	10 bits	3FFh	3FFh	3FFh	3FFh
	12 bits	FFFh	FFFh	FFFh	FFFh
	14 bits	3FFFh	3FFFh	3FFFh	3FFFh
	16 bit	FFFFh	FFFFh	FFFFh	FFFFh
Second code	8 bits	00h	00h	00h	00h
	10 bits	000h	000h	000h	000h
	12 bits	000h	000h	000h	000h
	14 bits	0000h	0000h	0000h	0000h
	16 bit	0000h	0000h	0000h	0000h
Third code	8 bits	00h	00h	00h	00h
	10 bits	000h	000h	000h	000h
	12 bits	000h	000h	000h	000h
	14 bits	0000h	0000h	0000h	0000h
	16 bit	0000h	0000h	0000h	0000h
Fourth code	8 bits	XXh	XXh	XXh	XXh
	10 bits	XXXh	XXXh	XXXh	XXXh
	12 bits	XXXh	XXXh	XXXh	XXXh
	14 bits	XXXXh	XXXXh	XXXXh	XXXXh
	16 bit	XXXXh	XXXXh	XXXXh	XXXXh

NOTE

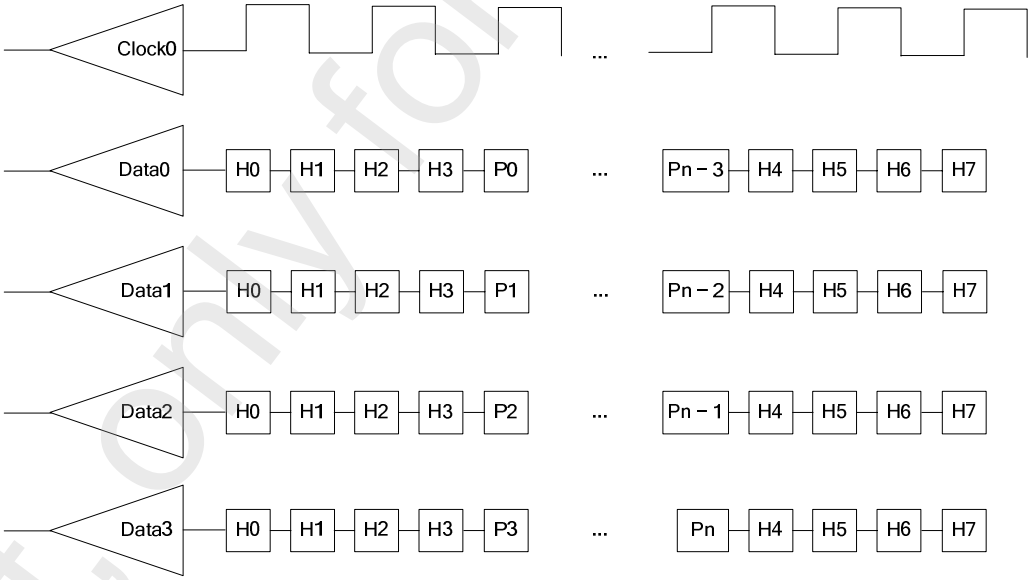
The first three fields of the synchronization code are fixed, and the fourth field identifies the start or end of a frame or line. The value of the fourth field is specified by image sensor vendors and therefore it varies according to vendors. Table 9-9 describes an implementation mode.

Table 9-9 Sample of the fourth field of the LVDS synchronization code

Field	Bit Width	Synchronization code			
		SAV(Valid line)	EAV(Valid line)	SAV(Invalid line)	EAV(Invalid line)
Fourth code	8 bits	80h	9Dh	ABh	B6h
	10 bits	200h	274h	2ACh	2D8h
	12 bits	800h	9D0h	AB0h	B60h
	14 bits	2000h	2740h	2AC0h	2D80h
	16 bit	8000h	9D00h	AB00h	B600h

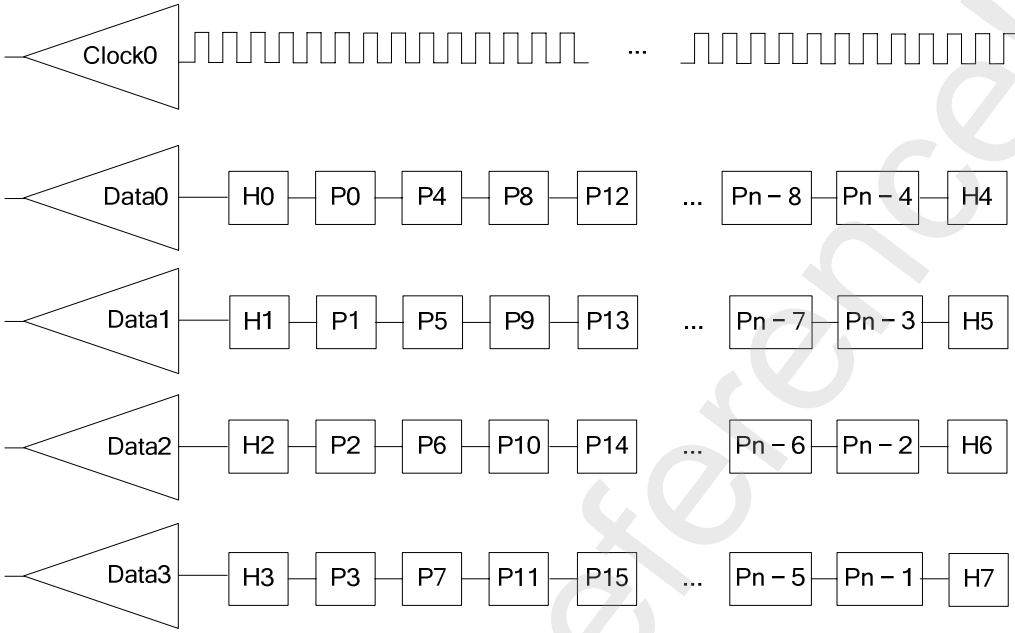
Figure 9-27 shows how LVDS synchronization code and pixel data are transmitted on each of the four channels. H indicates the synchronization code, and P indicates pixel. The bit widths of H and P are consistent with that of a single output pixel of the image sensor. In each data channel, the synchronization code with four-pixel bit width is transmitted before pixel data. The distribution of pixel data is related to the number of channels. Data is transmitted in series, and the endian mode is configurable in the MIPI RX.

Figure 9-27 LVDS synchronization code and image transfer mode 1



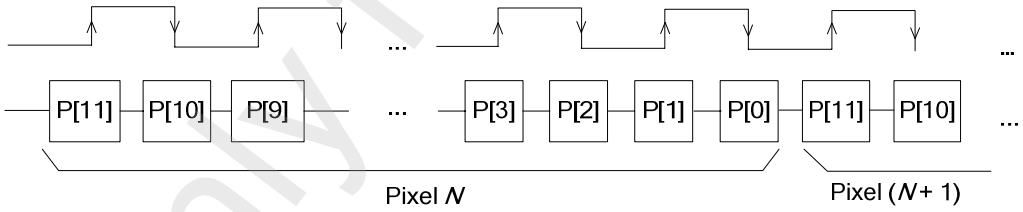
In another LVDS transfer mode, the four fields of the synchronization code are allocated to and transmitted in different channels. As shown in Figure 9-28, H0 to H3 are simultaneously transmitted in four data channels. The transfer mode of the pixel data in Figure 9-28 is the same as that in Figure 9-27.

Figure 9-28 LVDS synchronization code and image transfer mode 2



The synchronization codes and pixel data are transmitted in serial mode, and the data endian mode is configurable in the MIPI RX. Figure 9-29 shows the timing in which the image sensor outputs a single pixel by taking the raw12 data and big-endian mode as an example.

Figure 9-29 LVDS timing of a single pixel



Linear Mode of the LVDS Interface

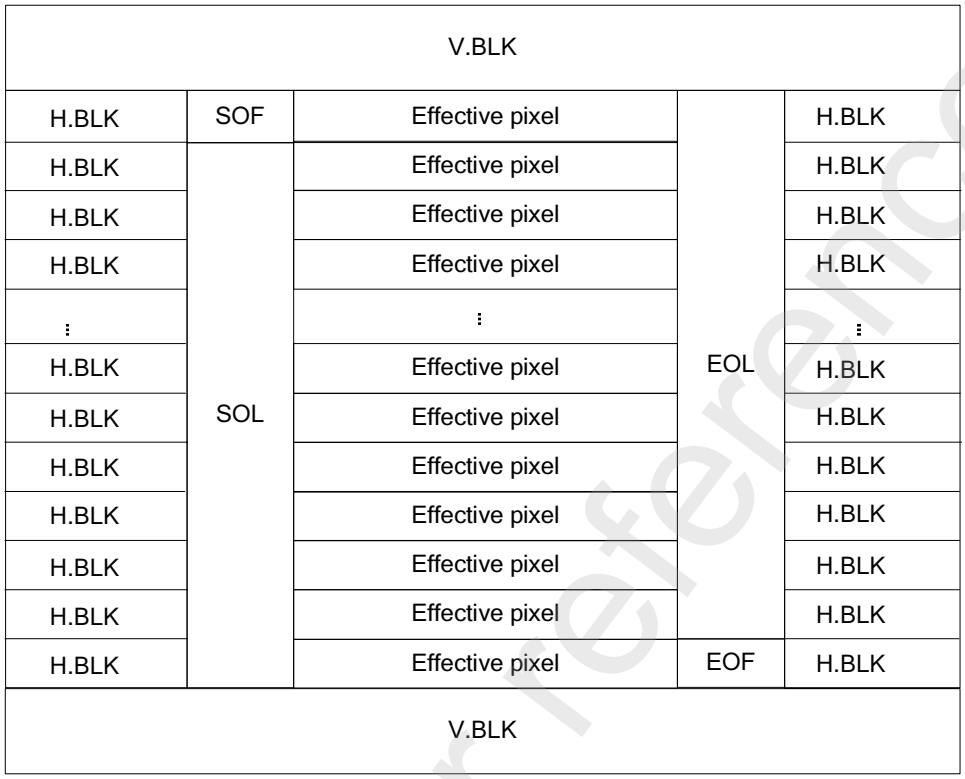
Two LVDS synchronization modes are available. In one mode, SAV (Invalid) and EAV (Invalid) identify invalid data of the blanking region whereas SAV (Valid) and EAV (Valid) identify pixel data of the active region. Figure 9-30 shows this synchronization mode.

Figure 9-30 LVDS synchronization mode 1

<table>
<tr><td>H.BLK</td><td rowspan="3">SAV
(invalid line)</td><td>V.BLK</td><td rowspan="3">EAV
(invalid line)</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>V.BLK</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>V.BLK</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td rowspan="13">SAV
(valid line)</td><td>Effective pixel</td><td rowspan="13">EAV
(valid line)</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective pixel</td><td>H.BLK</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H.BLK</td><td>Effective pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>Effective pixel</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td rowspan="4">SAV
(invalid line)</td><td>V.BLK</td><td rowspan="4">EAV
(invalid line)</td><td>H.BLK</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>H.BLK</td><td>V.BLK</td><td>H.BLK</td></tr>
<tr><td>H.BLK</td><td>V.BLK</td><td>H.BLK</td></tr>
</table>

In the other mode, SOF identifies the start of the first line in the active region, EOF identifies the end of the last line in the active region, and SOL and EOL identify the start and end of the other lines in the active region. Figure 9-31 shows this synchronization mode.

Figure 9-31 LVDS synchronization mode 2



WDR Modes of the LVDS Interface

The MIPI RX supports three WDR transfer modes of the LVDS interface.

- LVDS WDR mode 1: a WDR mode with the SOF-EOF flag. In this mode, the long and short exposure frames have independent synchronization codes.
- LVDS WDR mode 2: a DOL WDR mode with the SAV-EAV flag. In this mode, the synchronization code consists of four fields, and the long and short exposure frames have independent synchronization codes.
- LVDS WDR mode 3: a DOL WDR mode with the SAV-EAV flag. In this mode, the synchronization code consists of five fields, and the long and short exposure frames have independent synchronization codes.

The MIPI RX compares the received synchronization code value with the preconfigured value in the register based on the mode configuration, determines whether the received image frame is a long exposure frame or a short exposure frame based on the comparison result, identifies the image frame type in a specific way, and implements demultiplexing in the VICAP module.

Figure 9-32 shows the LVDS WDR mode 1. The type of the synchronization code for the long exposure video data is different from that of the synchronization code for the short exposure video data. Data with different exposure lengths is distinguished by using the synchronization code.

Figure 9-32 LVDS WDR mode 1 (two frames)

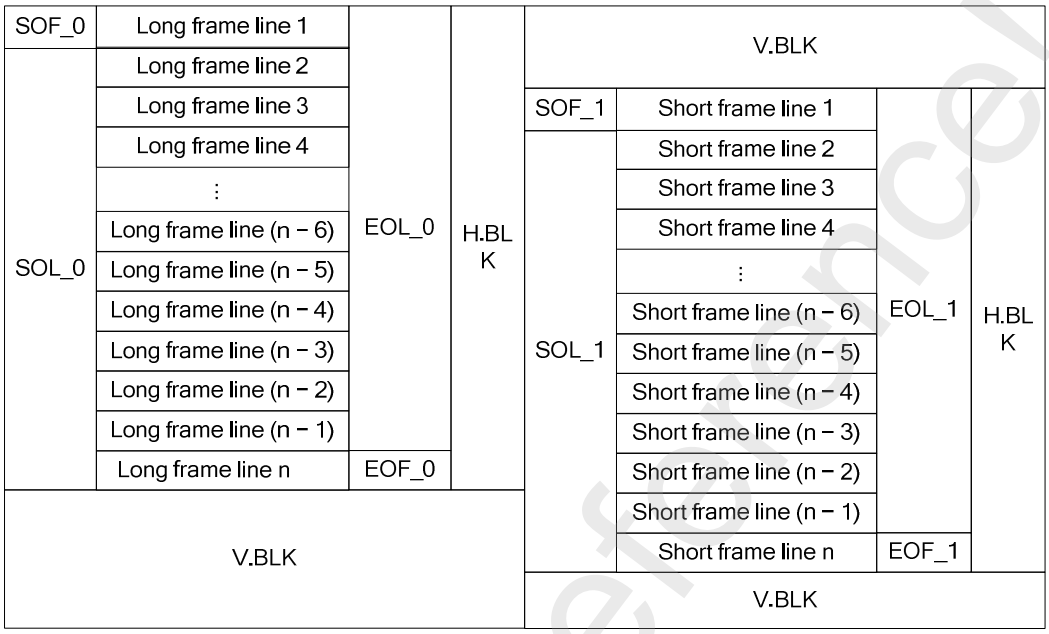
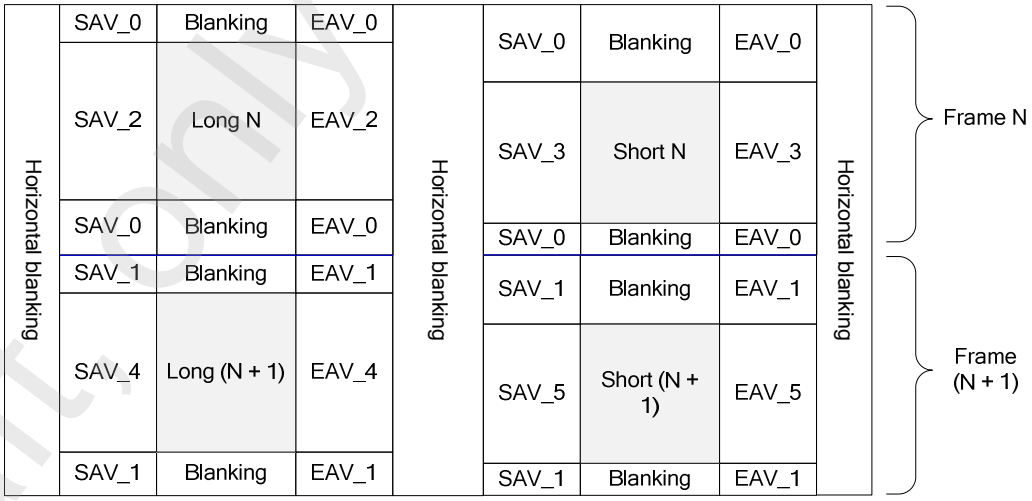


Figure 9-33 shows the LVDS WDR mode 2. In this mode, the SAV-EAV is used for synchronization, the long and short exposure frames have independent synchronization codes, and the synchronization code of frame *N* is different from that of frame (*N* + 1).

The LVDS WDR mode 3 is similar to LVDS WDR mode 2 except that the synchronization code in mode 3 consists of five fields.

Figure 9-33 LVDS WDR mode 2 (two frames)



HiSPI Data Format

HiSPI, formulated by Aptina, includes the HiSPI physical layer protocol and HiSPI specification. The HiSPI physical layer protocol stipulates the electrical specifications and timing parameters, whereas the HiSPI specification defines the data packetizing modes.

The HiSPI specification stipulates two physical layer electric standards (HiVCM and SLVS) and four data transmission modes (Packetized-SP, Streaming-SP, Streaming-S, and ActiveStart-SP8).

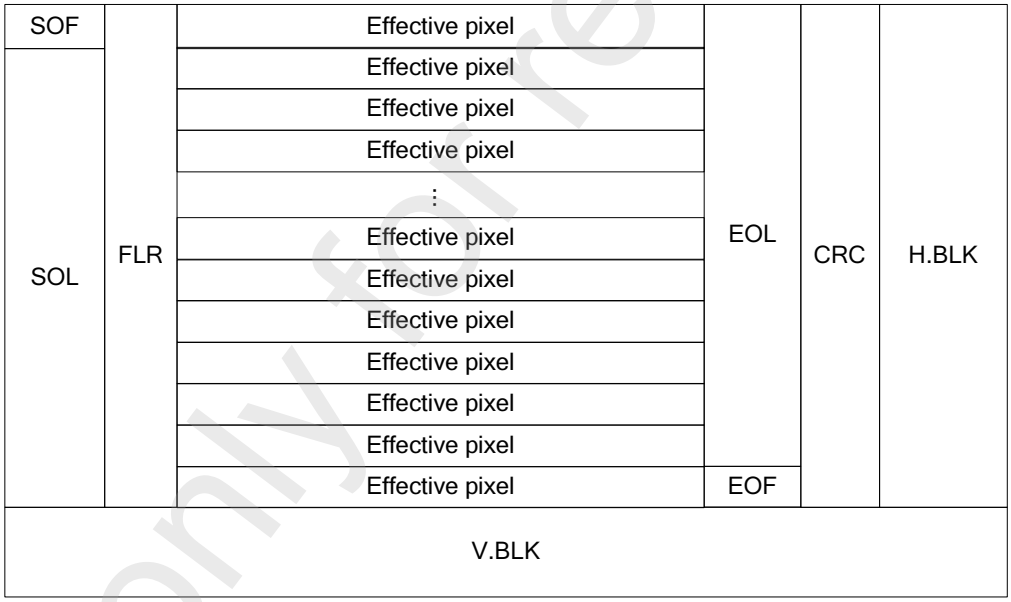
The MIPI RX supports the HiVCM and SLVS electric standards and supports the Packetized-SP and Streaming-SP mode.

HiSPI Linear Mode

In Packetized-SP mode, the image sensor identifies the start of the first line in the active region by using the SOF, the end of the last line in the active region by using the EOF, and the start as well end of other lines in the active region by using SOL and EOL respectively. This synchronization method is similar to that in Figure 9-31 except that CRC and FLR can be added to data packets in Packetized-SP mode. Figure 9-34 shows the data format in HiSPI Packetized-SP mode.

The MIPI RX can check whether the matching of SOF-EOF and SOL-EOL is correct. However, it does not process the CRC and FLR data.

Figure 9-34 Data format in HiSPI Packetized-SP mode



The other three HiSPI transfer modes (Streaming-SP, Streaming-S, and ActiveStart-SP8) are similar to the Packetized-SP mode except that they differ in the calibration mode of the synchronization code. Table 9-10 describes the differences between the four HiSPI transfer modes. SOF and EOF indicate the start and end of the frame in the active region respectively; SOL and EOL indicate the start and end of the line in the active region respectively; SAV indicates the start of the line in the blanking region.

Table 9-10 HiSPI transfer modes

Synchronization Code	Packetized-SP	Streaming-SP	Streaming-S	ActiveStart-SP8
SOF	Required	Required	Unsupported	Required
SOL	Required	Required	Required	Required

Synchronization Code	Packetized-SP	Streaming-SP	Streaming-S	ActiveStart-SP8
EOF	Required	Unsupported	Unsupported	Unsupported
EOL	Required	Unsupported	Unsupported	Unsupported
SAV	Unsupported	Required	Required	Unsupported

The MIPI RX supports the preceding four modes. All the four fields of a synchronization code can be transmitted in each channel (as shown in Figure 9-27), or the four fields can be allocated to and transmitted in different channels (as shown in Figure 9-28).

HiSPI WDR Mode

The synchronization code in HiSPI WDR mode is the same as that in linear mode. There are blanking regions between the long exposure data and short exposure data. The first several lines of short exposure data are not the active pixel region and are stuffed with fixed values. Figure 9-35 shows the timing in HiSPI WDR mode.

Figure 9-35 HiSPI WDR mode

<table>
<tr><td>SOF</td><td>Long frame line 1</td><td rowspan="13">EOL</td><td rowspan="13">H.BLK</td><td rowspan="13">SOL</td><td rowspan="2">T2 padding</td><td rowspan="13">EOL</td><td rowspan="13">H.BLK</td></tr>
<tr><td rowspan="12">SOL</td><td>Long frame line 2</td></tr>
<tr><td>Long frame line 3</td><td>Short frame line 1</td></tr>
<tr><td>Long frame line 4</td><td>Short frame line 2</td></tr>
<tr><td>⋮</td><td>Short frame line 3</td></tr>
<tr><td>Long frame line (n − 3)</td><td>Short frame line 4</td></tr>
<tr><td>Long frame line (n − 2)</td><td>⋮</td></tr>
<tr><td>Long frame line (n − 1)</td><td>Short frame line (n − 3)</td></tr>
<tr><td>Long frame line n</td><td>Short frame line (n − 2)</td></tr>
<tr><td rowspan="2">T1 padding</td><td>Short frame line (n − 1)</td></tr>
<tr><td>Short frame line n</td><td>EOF</td></tr>
<tr><td>SOV</td><td>V.BLK</td><td>EOV</td><td></td><td>SOV</td><td>V.BLK</td><td>EOV</td><td></td></tr>
</table>

9.3.4 Operating Mode of the MIPI RX Controller

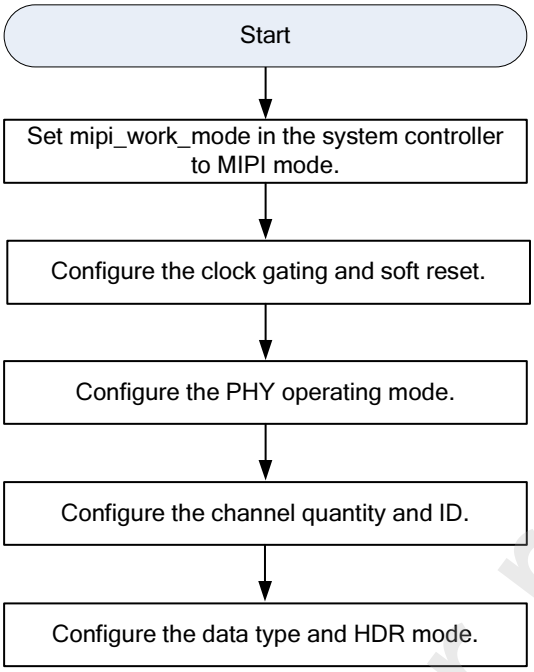
The MIPI RX controller supports the MIPI, LVDS, and HiSPI modes. The software configuration in each mode contains two parts: controller and combo-PHY.

9.3.4.1 MIPI Mode Configuration Process

In MIPI mode, the required channel quantity, data type, and WDR mode for data transmission as well as PHY operating mode need to be configured. The frame or line synchronization information in MIPI mode is contained in the data packet. The controller parses the data

packet and restores the pixel data. Figure 9-36 shows the software configuration process in MIPI mode.

Figure 9-36 MIPI RX configuration process in MIPI mode

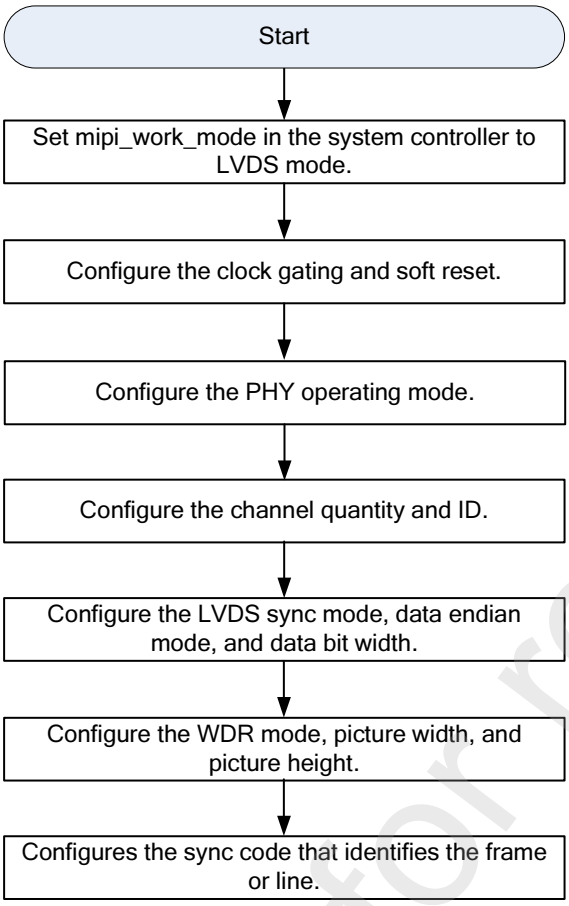


9.3.4.2 LVDS and HiSPI Mode Configuration Process

In LVDS/HiSPi mode, configure the type of raw data, endian mode, synchronization mode, WDR mode and image size registers. In LVDS mode, a synchronization code is used to identify frame or line synchronization information. Depending on the type of raw data, the synchronization code can be 8, 10, 12, 14, or 16 bits.

Figure 9-37 shows the software configuration process in LVDS and HiSPI modes.

Figure 9-37 MIPI RX configuration process in LVDS and HiSPI modes



9.3.5 MIPI RX Register Summary

Table 9-11 describes the MIPI RX registers.

Table 9-11 Summary of MIPI RX registers (base address: 0x1130_0000)

Offset Address	Register	Description	Page
0x0000	PHY_MODE_LINK0	Link 0 PHY operating mode register	9-130
0x0004	PHY_SKEW_LINK0	Link 0 PHY channel delay adjustment register	9-132
0x0008	PHY_EN_LINK0	Link 0 PHY channel enable register	9-132
0x0018	PHY_DATA_LINK0	Link 0 PHY output parallel data register	9-134
0x001C	PHY_PH_MIPI_LINK0	Link 0 MIPI data packet header register	9-134
0x0020	PHY_DATA_MIPI_LINK0	Link 0 MIPI mode data register	9-135

Offset Address	Register	Description	Page
0x0024	PHY_SYNC_DCT_LINK0	Link 0 PHY LVDS mode synchronization header detection control register	9-135
0x0030	PHY_SYNC_CODE0_LINK0	Link 0 PHY LVDS mode lane0 synchronization header register	9-136
0x0034	PHY_SYNC_CODE1_LINK0	Link 0 PHY LVDS mode lane1 synchronization header register	9-137
0x0038	PHY_SYNC_CODE2_LINK0	Link 0 PHY LVDS mode lane2 synchronization header register	9-137
0x003C	PHY_SYNC_CODE3_LINK0	Link 0 PHY LVDS mode lane3 synchronization header register	9-137
0x01F0	MIPI_CIL_INT_RAW_LINK0	Link 0 MIPI CIL raw interrupt status register	9-138
0x01F4	MIPI_CIL_INT_LINK0	Link 0 MIPI CIL interrupt status register	9-139
0x01F8	MIPI_CIL_INT_MSK_LINK0	Link 0 MIPI CIL interrupt mask register	9-141
0x0800	CHN0_PHY_EN	CHN0 PHY enable register	9-142
0x0808	CHN0_MEM_CTRL	CHN0 Memory control register	9-143
0x080C	CHN0_LANE_EN	CHN0 Lane enable register	9-143
0x0810	CHN0_PHYCFG_MODE	CHN0 PHY configuration mode register	9-144
0x0814	CHN0_PHYCFG_EN	CHN0 PHY configuration enable register	9-145
0x0818	CHN0_CLR_EN	CHN0 forced setting enable register	9-145
0x081C	CHN0_CIL_CTRL	CHN0 CIL control register	9-146
0x0EF0	MIPI_CHN0_INT_RAW	MIPI channel 0 raw interrupt status register	9-147
0x0EF4	MIPI_CHN0_INT	MIPI channel 0 interrupt status register	9-147
0x0EF8	MIPI_CHN0_INT_MSK	MIPI channel 0 interrupt mask register	9-148
0x1004	MIPI0_LANES_NUM	MIPI 0 enabled data channel quantity register	9-149
0x100C	MIPI0_MAIN_INT_ST	MIPI 0 global interrupt status register	9-150
0x1010	MIPI0_DI_1	MIPI 0 controller data ID 1 register	9-151
0x1014	MIPI0_DI_2	MIPI 0 controller data ID 2 register	9-153

Offset Address	Register	Description	Page
0x1060	MIPI0_PKT_INTR_ST	MIPI 0 packet interrupt status register	9-154
0x1064	MIPI0_PKT_INTR_MSK	MIPI 0 packet interrupt mask register	9-155
0x1070	MIPI0_PKT_INTR2_ST	MIPI 0 packet interrupt status 2 register	9-156
0x1074	MIPI0_PKT_INTR2_MSK	MIPI 0 packet interrupt mask 2 register	9-158
0x1080	MIPI0_FRAME_INTR_ST	MIPI 0 frame interrupt status register	9-159
0x1084	MIPI0_FRAME_INTR_MSK	MIPI 0 frame interrupt mask register	9-161
0x1090	MIPI0_LINE_INTR_ST	MIPI 0 line interrupt status register	9-162
0x1094	MIPI0_LINE_INTR_MSK	MIPI 0 line interrupt mask register	9-165
0x1100	MIPI0_USERDEF_DT	MIPI 0 pixel bit width configuration register for the user-defined data type	9-166
0x1104	MIPI0_USER_DEF	MIPI 0 user-defined data type enable configuration register	9-168
0x1108	MIPI0_CTRL_MODE_HS	MIPI 0 operating mode enable register	9-169
0x1200	MIPI0_DOL_ID_CODE0	MIPI 0 DOL mode frame identification 0 register	9-169
0x1204	MIPI0_DOL_ID_CODE1	MIPI 0 DOL mode frame identification 1 register	9-170
0x1208	MIPI0_DOL_ID_CODE2	MIPI 0 DOL mode frame identification 2 register	9-170
0x1230	MIPI0_CTRL_MODE_PIXEL	MIPI 0 output operating mode enable register	9-170
0x1240	MIPI0_DUMMY_PIX_REG	MIPI 0 dummy line pixel value register	9-171
0x1250	MIPI0_IMGSIZE0_STATIS	MIPI 0 VC 0 transferred image size register	9-172
0x1254	MIPI0_IMGSIZE1_STATIS	MIPI 0 VC 1 transferred image size register	9-172
0x1258	MIPI0_IMGSIZE2_STATIS	MIPI 0 VC 2 transferred image size register	9-173
0x125C	MIPI0_IMGSIZE3_STATIS	MIPI 0 VC 3 transferred image size register	9-173
0x12F0	MIPI0_CTRL_INT_RAW	MIPI 0 read data error raw interrupt status register	9-173

Offset Address	Register	Description	Page
0x12F4	MIPI0_CTRL_INT	MIPI 0 read data error interrupt status register	9-174
0x12F8	MIPI0_CTRL_INT_MSK	MIPI 0 read data error interrupt mask register	9-175
0x1300	LVDS0_WDR	LVDS WDR control register	9-176
0x1304	LVDS0_CTRL	LVDS control register	9-178
0x1308	LVDS0_DOLSCD_HBLK	LVDS SCD control register	9-179
0x130C	LVDS0_IMGSIZE	LVDS image size register	9-180
0x1320	LVDS0_LANE0_SOF_01	Lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode	9-180
0x1324	LVDS0_LANE0_SOF_23	Lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode	9-181
0x1328	LVDS0_LANE0_EOF_01	Lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode	9-181
0x132C	LVDS0_LANE0_EOF_23	Lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode	9-182
0x1330	LVDS0_LANE0_SOL_01	Lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode	9-182
0x1334	LVDS0_LANE0_SOL_23	Lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode	9-183
0x1338	LVDS0_LANE0_EOL_01	Lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode	9-183
0x133C	LVDS0_LANE0_EOL_23	Lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode	9-184
0x1340	LVDS0_LANE1_SOF_01	Lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode	9-184
0x1344	LVDS0_LANE1_SOF_23	Lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode	9-185

Offset Address	Register	Description	Page
0x1348	LVDS0_LANE1_EOF_01	Lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode	9-185
0x134C	LVDS0_LANE1_EOF_23	Lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode	9-186
0x1350	LVDS0_LANE1_SOL_01	Lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode	9-186
0x1354	LVDS0_LANE1_SOL_23	Lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode	9-187
0x1358	LVDS0_LANE1_EOL_01	Lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode	9-187
0x135C	LVDS0_LANE1_EOL_23	Lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode	9-188
0x1360	LVDS0_LANE2_SOF_01	Lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode	9-188
0x1364	LVDS0_LANE2_SOF_23	Lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode	9-189
0x1368	LVDS0_LANE2_EOF_01	Lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode	9-189
0x136C	LVDS0_LANE2_EOF_23	Lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode	9-190
0x1370	LVDS0_LANE2_SOL_01	Lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode	9-190
0x1374	LVDS0_LANE2_SOL_23	Lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode	9-191
0x1378	LVDS0_LANE2_EOL_01	Lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode	9-191
0x137C	LVDS0_LANE2_EOL_23	Lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode	9-192

Offset Address	Register	Description	Page
0x1380	LVDS0_LANE3_SOF_01	Lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode	9-192
0x1384	LVDS0_LANE3_SOF_23	Lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode	9-193
0x1388	LVDS0_LANE3_EOF_01	Lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode	9-193
0x138C	LVDS0_LANE3_EOF_23	Lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode	9-194
0x1390	LVDS0_LANE3_SOL_01	Lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode	9-194
0x1394	LVDS0_LANE3_SOL_23	Lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode	9-195
0x1398	LVDS0_LANE3_EOL_01	Lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode	9-195
0x139C	LVDS0_LANE3_EOL_23	Lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode	9-196
0x13A0	LVDS0_LANE0_NXT_SOF_01	Lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-196
0x13A4	LVDS0_LANE0_NXT_SOF_23	Lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-197
0x13A8	LVDS0_LANE0_NXT_EOF_01	Lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-197
0x13AC	LVDS0_LANE0_NXT_EOF_23	Lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-198
0x13B0	LVDS0_LANE0_NXT_SOL_01	Lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-198
0x13B4	LVDS0_LANE0_NXT_SOL_23	Lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode	9-199

Offset Address	Register	Description	Page
0x13B8	LVDS0_LANE0_NXT_EOL_01	Lane 0 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-199
0x13BC	LVDS0_LANE0_NXT_EOL_23	Lane 0 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-200
0x13C0	LVDS0_LANE1_NXT_SOF_01	Lane 1 SOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-200
0x13C4	LVDS0_LANE1_NXT_SOF_23	Lane 1 SOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-201
0x13C8	LVDS0_LANE1_NXT_EOF_01	Lane 1 EOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-201
0x13CC	LVDS0_LANE1_NXT_EOF_23	Lane 1 EOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-202
0x13D0	LVDS0_LANE1_NXT_SOL_01	Lane 1 SOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-202
0x13D4	LVDS0_LANE1_NXT_SOL_23	Lane 1 SOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-203
0x13D8	LVDS0_LANE1_NXT_EOL_01	Lane 1 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-203
0x13DC	LVDS0_LANE1_NXT_EOL_23	Lane 1 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-204
0x13E0	LVDS0_LANE2_NXT_SOF_01	Lane 2 SOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-204
0x13E4	LVDS0_LANE2_NXT_SOF_23	Lane 2 SOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-205
0x13E8	LVDS0_LANE2_NXT_EOF_01	Lane 2 EOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-205
0x13EC	LVDS0_LANE2_NXT_EOF_23	Lane 2 EOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-206

Offset Address	Register	Description	Page
0x13F0	LVDS0_LANE2_NXT_SOL_01	Lane 2 SOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-206
0x13F4	LVDS0_LANE2_NXT_SOL_23	Lane 2 SOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-207
0x13F8	LVDS0_LANE2_NXT_EOL_01	Lane 2 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-207
0x13FC	LVDS0_LANE2_NXT_EOL_23	Lane 2 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-208
0x1400	LVDS0_LANE3_NXT_SOF_01	Lane 3 SOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-208
0x1404	LVDS0_LANE3_NXT_SOF_23	Lane 3 SOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-209
0x1408	LVDS0_LANE3_NXT_EOF_01	Lane 3 EOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-209
0x140C	LVDS0_LANE3_NXT_EOF_23	Lane 3 EOF synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-210
0x1410	LVDS0_LANE3_NXT_SOL_01	Lane 3 SOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-210
0x1414	LVDS0_LANE3_NXT_SOL_23	Lane 3 SOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-211
0x1418	LVDS0_LANE3_NXT_EOL_01	Lane 3 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-211
0x141C	LVDS0_LANE3_NXT_EOL_23	Lane 3 EOL synchronization code configuration register for frame (*N* + 1) in LVDS or HiSPI mode	9-212
0x1420	LVDS0_LI_WORD0	LVDS DOL mode frame 0 LI register	9-212
0x1424	LVDS0_LI_WORD1	LVDS DOL mode frame 1 LI register	9-213
0x1428	LVDS0_LI_WORD2	LVDS DOL mode frame 2 LI register	9-213
0x142C	LVDS0_LI_WORD3	LVDS DOL mode frame 3 LI register	9-214

Offset Address	Register	Description	Page
0x1500	LVDS0_IMGSIZE0_STATIS	LVDS LEF image size statistics register	9-214
0x1504	LVDS0_IMGSIZE1_STATIS	LVDS SEF1 image size statistics register	9-214
0x1508	LVDS0_IMGSIZE2_STATIS	LVDS SEF2 image size statistics register	9-215
0x150C	LVDS0_IMGSIZE3_STATIS	LVDS SEF3 image size statistics register	9-215
0x15F0	LVDS0_CTRL_INT_RAW	LVDS read data raw interrupt status register	9-216
0x15F4	LVDS0_CTRL_INT	LVDS read data interrupt status register	9-217
0x15F8	LVDS0_CTRL_INT_MSK	LVDS read data interrupt mask register	9-218
0x1600	ALIGN0_LANE_ID	Link 0 lane priority configuration register	9-219
0x16F0	ALIGN0_INT_RAW	MIPI_ALIGN raw interrupt status register	9-220
0x16F4	ALIGN0_INT	MIPI_ALIGN interrupt status register	9-221
0x16F8	ALIGN0_INT_MSK	MIPI_ALIGN interrupt mask register	9-222

9.3.6 MIPI Register Description

PHY_MODE_LINK0

PHY_MODE_LINK0 is a link 0 PHY operating mode register.

Offset Address	Register Name	Total Reset Value
0x0000	PHY_MODE_LINK0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	phy0_rg_mipi_mode	reserved	phy0_rg_ext_clk_en	reserved	phy0_rg_faclk_en	reserved	phy0_rg_en_lp	reserved	phy0_rg_en_cmos	reserved	phy0_rg_en_clk	phy0_rg_en_d
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24]	RW	phy0_rg_mipi_mode	MIPI/LVDS input mode select. This field is set to 0 when the PHY works in LVDS mode and the common voltage is greater than 1.25 V. 0: The common voltage is higher than 1.25 V. 1: The common voltage is 1.25 V or lower.
[23:21]	RO	reserved	Reserved
[20]	RW	phy0_rg_ext_clk_en	Differential clock source select 0: PAD input differential clock. 1: differential clock of other links.
[19:17]	RO	reserved	Reserved
[16]	RW	phy0_rg_faclk_en	Phase of the associated clock for the PHY output data 0: Data is output at the rising edge of the clock. 1: Data is output at the falling edge of the clock.
[15:13]	RO	reserved	Reserved
[12]	RW	phy0_rg_en_lp	PHY LP mode enable. The LP mode is enabled in MIPI mode and disabled in other modes. 0: disabled 1: enabled
[11:9]	RO	reserved	Reserved
[8]	RW	phy0_rg_en_cmos	PHY CMOS mode enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	phy0_rg_en_clk	Clock lane enable 0: disabled 1: enabled

[3:0]	RW	phy0_rg_en_d	Data lane enable 0: disabled 1: enabled

PHY_SKEW_LINK0

PHY_SKEW_LINK0 is a link 0 PHY channel delay adjustment register.

Offset Address	Register Name	Total Reset Value
0x0004	PHY_SKEW_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												phy0_d3_skew				reserved	phy0_d2_skew			reserved	phy0_d1_skew			reserved	phy0_d0_skew			reserved	phy0_clk_skew		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	phy0_d3_skew	Timing delay adjustment for data lane 3. The phase is delayed by about 62.5 ps each time the register value is incremented by 1.
[15]	RO	reserved	Reserved
[14:12]	RW	phy0_d2_skew	Timing delay adjustment for data lane 2. The phase is delayed by about 62.5 ps each time the register value is incremented by 1.
[11]	RO	reserved	Reserved
[10:8]	RW	phy0_d1_skew	Timing delay adjustment for data lane 1. The phase is delayed by about 62.5 ps each time the register value is incremented by 1.
[7]	RO	reserved	Reserved
[6:4]	RW	phy0_d0_skew	Timing delay adjustment for data lane 0. The phase is delayed by about 62.5 ps each time the register value is incremented by 1.
[3]	RO	reserved	Reserved
[2:0]	RW	phy0_clk_skew	Timing delay adjustment for the clock lane. The phase is delayed by about 62.5 ps each time the register value is incremented by 1.

PHY_EN_LINK0

PHY_EN_LINK0 is a link 0 PHY channel enable register.

Offset Address	Register Name	Total Reset Value
0x0008	PHY_EN_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							phy0_clk_term_en	phy0_d3_term_en	phy0_d2_term_en	phy0_d1_term_en	phy0_d0_term_en	phy0_da_d3_valid	phy0_da_d2_valid	phy0_da_d1_valid	phy0_da_d0_valid
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	phy0_clk_term_en	Termination matched impedance enable for the clock lane 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[7]	RW	phy0_d3_term_en	Termination matched impedance enable for data lane 3 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[6]	RW	phy0_d2_term_en	Termination matched impedance enable for data lane 2 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[5]	RW	phy0_d1_term_en	Termination matched impedance enable for data lane 1 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[4]	RW	phy0_d0_term_en	Termination matched impedance enable for data lane 0 0: The internal matched resistor is disabled. 1: The internal matched resistor is enabled.
[3]	RW	phy0_da_d3_valid	High-speed mode enable for data lane 3 0: disabled 1: enabled
[2]	RW	phy0_da_d2_valid	High-speed mode enable for data lane 2 0: disabled 1: enabled
[1]	RW	phy0_da_d1_valid	High-speed mode enable for data lane 1 0: disabled 1: enabled

[0]	RW	phy0_da_d0_valid	High-speed mode enable for data lane 0 0: disabled 1: enabled

PHY_DATA_LINK0

PHY_DATA_LINK0 is a link 0 PHY output parallel data register.

Offset Address	Register Name	Total Reset Value
0x0018	PHY_DATA_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_data3_mipi								phy0_data2_mipi								phy0_data1_mipi								phy0_data0_mipi							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	phy0_data3_mipi	Data received by data lane 3
[23:16]	RO	phy0_data2_mipi	Data received by data lane 2
[15:8]	RO	phy0_data1_mipi	Data received by data lane 1
[7:0]	RO	phy0_data0_mipi	Data received by data lane 0

PHY_PH_MIPI_LINK0

PHY_PH_MIPI_LINK0 is a link 0 MIPI data packet header register.

Offset Address	Register Name	Total Reset Value
0x001C	PHY_PH_MIPI_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	phy0_ph3_mipi								phy0_ph2_mipi								phy0_ph1_mipi								phy0_ph0_mipi							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	phy0_ph3_mipi	Data packet header received by data lane 3
[23:16]	RO	phy0_ph2_mipi	Data packet header received by data lane 2
[15:8]	RO	phy0_ph1_mipi	Data packet header received by data lane 1
[7:0]	RO	phy0_ph0_mipi	Data packet header received by data lane 0

PHY_DATA_MIPI_LINK0

PHY_DATA_MIPI_LINK0 is a link 0 MIPI mode data register.

Offset Address	Register Name	Total Reset Value
0x0020	PHY_DATA_MIPI_LINK0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	phy0_data3_mipi_hs		phy0_data2_mipi_hs		phy0_data1_mipi_hs		phy0_data0_mipi_hs	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	phy0_data3_mipi_hs	MIPI data for data lane 3
[23:16]	RO	phy0_data2_mipi_hs	MIPI data for data lane 2
[15:8]	RO	phy0_data1_mipi_hs	MIPI data for data lane 1
[7:0]	RO	phy0_data0_mipi_hs	MIPI data for data lane 0

PHY_SYNC_DCT_LINK0

PHY_SYNC_DCT_LINK0 is a link 0 PHY LVDS mode synchronization header detection control register.

Offset Address	Register Name	Total Reset Value
0x0024	PHY_SYNC_DCT_LINK0	0x0000_0101

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7	6 5 4	3	2 1 0
Name	reserved						cil0_code_big_endian	reserved	cil0_split_mode	reserved	cil0_raw_type
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1	0	0 0 0	0	0 0 1

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved

[8]	RW	cil0_code_big_endian	Serial bit transmission sequence for the synchronization code (sync_code) of the raw data to be transmitted in LVDS or HiSPI mode 0: LSB. The lower bits are transmitted first. The serial data sequence of the received synchronization code is bit 0, bit 1, ..., and bit 11. 1: MSB. The upper bits are transmitted first. The serial data sequence of the received synchronization code is bit 11, bit 10, ..., and bit 0.
[7]	RO	reserved	Reserved
[6:4]	RW	cil0_split_mode	Transfer type for the synchronization code in LVDS or HiSPI mode 000: per lane mode 011: Split 2 lane mode 111: Split 4 lane mode Other values: reserved
[3]	RO	reserved	Reserved
[2:0]	RW	cil0_raw_type	Type of the raw data to be transmitted in LVDS or HiSPI mode 001: 8-bit raw data 010: 10-bit raw data 011: 12-bit raw data 100: 14-bit raw data 101: 16-bit raw data Other values: reserved

PHY_SYNC_CODE0_LINK0

PHY_SYNC_CODE0_LINK0 is link 0 PHY LVDS mode lane0 synchronization header register.

Offset Address	Register Name	Total Reset Value
0x0030	PHY_SYNC_CODE0_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_0																cil0_sof0_word4_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_0	Lane 0 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil0_sof0_word4_0	Lane 0 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE1_LINK0

PHY_SYNC_CODE1_LINK0 is link 0 PHY LVDS mode lane1 synchronization header register.

Offset Address	Register Name	Total Reset Value
0x0034	PHY_SYNC_CODE1_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_1																cil0_sof0_word4_1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_1	Lane 1 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil0_sof0_word4_1	Lane 1 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE2_LINK0

PHY_SYNC_CODE2_LINK0 is link 0 PHY LVDS mode lane2 synchronization header register.

Offset Address	Register Name	Total Reset Value
0x0038	PHY_SYNC_CODE2_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_2																cil0_sof0_word4_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_2	Lane 2 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil0_sof0_word4_2	Lane 2 SOF synchronization code (for frame *N*)

PHY_SYNC_CODE3_LINK0

PHY_SYNC_CODE3_LINK0 is link 0 PHY LVDS mode lane3 synchronization header register.

Offset Address	Register Name	Total Reset Value
0x003C	PHY_SYNC_CODE3_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cil0_sof1_word4_3																cil0_sof0_word4_3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	cil0_sof1_word4_3	Lane 3 SOF synchronization code (for frame *N* + 1)
[15:0]	RW	cil0_sof0_word4_3	Lane 3 SOF synchronization code (for frame *N*)

MIPI_CIL_INT_RAW_LINK0

MIPI_CIL_INT_RAW_LINK0 is a link 0 MIPI CIL raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x01F0	MIPI_CIL_INT_RAW_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				err0_timeout_ck_raw	err0_timeout_d3_raw	err0_timeout_d2_raw	err0_timeout_d1_raw	err0_timeout_d0_raw	reserved				err0_escape_ck_raw	err0_escape_d3_raw	err0_escape_d2_raw	err0_escape_d1_raw	err0_escape_d0_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	WC	err0_timeout_ck_raw	Status of the raw FSM timeout interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[11]	WC	err0_timeout_d3_raw	Status of the raw FSM timeout interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[10]	WC	err0_timeout_d2_raw	Status of the raw FSM timeout interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[9]	WC	err0_timeout_d1_raw	Status of the raw FSM timeout interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[8]	WC	err0_timeout_d0_raw	Status of the raw FSM timeout interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	WC	err0_escape_ck_raw	Status of the raw escape sequence interrupt for the clock lane 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	WC	err0_escape_d3_raw	Status of the raw escape sequence interrupt for data lane 3 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	err0_escape_d2_raw	Status of the raw escape sequence interrupt for data lane 2 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	err0_escape_d1_raw	Status of the raw escape sequence interrupt for data lane 1 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	err0_escape_d0_raw	Status of the raw escape sequence interrupt for data lane 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.

MIPI_CIL_INT_LINK0

MIPI_CIL_INT_LINK0 is a link 0 MIPI CIL interrupt status register.

Offset Address	Register Name	Total Reset Value
0x01F4	MIPI_CIL_INT_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err0_timeout_ck_st	err0_timeout_d3_st	err0_timeout_d2_st	err0_timeout_d1_st	err0_timeout_d0_st	reserved				err0_escape_ck_st	err0_escape_d3_st	err0_escape_d2_st	err0_escape_d1_st	err0_escape_d0_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	err0_timeout_ck_st	Status of the FSM timeout interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RO	err0_timeout_d3_st	Status of the FSM timeout interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	err0_timeout_d2_st	Status of the FSM timeout interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	err0_timeout_d1_st	Status of the FSM timeout interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	err0_timeout_d0_st	Status of the FSM timeout interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.
[7:5]	RO	reserved	Reserved
[4]	RO	err0_escape_ck_st	Status of the escape sequence interrupt for the clock lane 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err0_escape_d3_st	Status of the escape sequence interrupt for data lane 3 0: No interrupt is generated. 1: An interrupt is generated.

[2]	RO	err0_escape_d2_st	Status of the escape sequence interrupt for data lane 2 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	err0_escape_d1_st	Status of the escape sequence interrupt for data lane 1 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	err0_escape_d0_st	Status of the escape sequence interrupt for data lane 0 0: No interrupt is generated. 1: An interrupt is generated.

MIPI_CIL_INT_MSK_LINK0

MIPI_CIL_INT_MSK_LINK0 is a link 0 MIPI CIL interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x01F8	MIPI_CIL_INT_MSK_LINK0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			err0_timeout_ck_msk	err0_timeout_d3_msk	err0_timeout_d2_msk	err0_timeout_d1_msk	err0_timeout_d0_msk	reserved				err0_escape_ck_msk	err0_escape_d3_msk	err0_escape_d2_msk	err0_escape_d1_msk	err0_escape_d0_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	err0_timeout_ck_msk	Enable of the FSM timeout interrupt for the clock lane 0: masked 1: enabled
[11]	RW	err0_timeout_d3_msk	Enable of the FSM timeout interrupt for data lane 3 0: masked 1: enabled
[10]	RW	err0_timeout_d2_msk	Enable of the FSM timeout interrupt for data lane 2 0: masked 1: enabled

[9]	RW	err0_timeout_d1_msk	Enable of the FSM timeout interrupt for data lane 1 0: masked 1: enabled
[8]	RW	err0_timeout_d0_msk	Enable of the FSM timeout interrupt for data lane 0 0: masked 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	err0_escape_ck_msk	Enable of the escape sequence interrupt for the clock lane 0: masked 1: enabled
[3]	RW	err0_escape_d3_msk	Enable of the escape sequence interrupt for data lane 3 0: masked 1: enabled
[2]	RW	err0_escape_d2_msk	Enable of the escape sequence interrupt for data lane 2 0: masked 1: enabled
[1]	RW	err0_escape_d1_msk	Enable of the escape sequence interrupt for data lane 1 0: masked 1: enabled
[0]	RW	err0_escape_d0_msk	Enable of the escape sequence interrupt for data lane 0 0: masked 1: enabled

CHN0_PHY_EN

CHN0_PHY_EN is a CHN0 PHY enable register.

Offset Address	Register Name	Total Reset Value
0x0800	CHN0_PHY_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															phy0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RW	phy0_en	PHY 0 enable 0: disabled 1: enabled

CHN0_MEM_CTRL

CHN0_MEM_CTRL is a CHN0 memory control register.

Offset Address	Register Name	Total Reset Value
0x0808	CHN0_MEM_CTRL	0x0000_0331

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			mem_ck_gt	reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	mem_ck_gt	CHN0 memory clock gating enable 0: disabled 1: enabled. The memory port clock is not inverted when the memory is not read or written.
[11:0]	RO	reserved	Reserved

CHN0_LANE_EN

CHN0_LANE_EN is a CHN0 lane enable register.

Offset Address	Register Name	Total Reset Value
0x080C	CHN0_LANE_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												lane3_en	lane2_en	lane1_en	lane0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved

[3]	RW	lane3_en	Lane 3 enable 0: disabled 1: enabled
[2]	RW	lane2_en	Lane 2 enable 0: disabled 1: enabled
[1]	RW	lane1_en	Lane 1 enable 0: disabled 1: enabled
[0]	RW	lane0_en	Lane 0 enable 0: disabled 1: enabled

CHN0_PHYCFG_MODE

CHN0_PHYCFG_MODE is a CHN0 PHY configuration mode register.

Offset Address	Register Name	Total Reset Value
0x0810	CHN0_PHYCFG_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							chn0_phycfg_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved

[2:0]	RW	chn0_phycfg_mode	CHN0 PHY configuration mode 000: The PHY configuration is controlled by PHYCFG_EN and FSM. 001: The PHY configuration is controlled by PHYCFG_EN. 010: The PHY configuration is directly controlled by the value of MIPI_PHYCFG_MODE. 011: The PHY configuration is controlled by the value of MIPI_PHYCFG_MODE and FSM. 100: The PHY configuration is controlled by PHYCFG_EN and FSM, and the clock channel enable is controlled by PHYCFG_EN. Other values: reserved

CHN0_PHYCFG_EN

CHN0_PHYCFG_EN is a CHN0 PHY configuration enable register.

Offset Address	Register Name	Total Reset Value
0x0814	CHN0_PHYCFG_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															chn0_phycfg_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	chn0_phycfg_en	CHN0 PHY configuration enable 0: disabled 1: enabled

CHN0_CLR_EN

CHN0_CLR_EN is CHN0 forced setting enable register.

Offset Address	Register Name	Total Reset Value
0x0818	CHN0_CLR_EN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								clr_en_align0	clr_en_lvds0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	clr_en_align0	Forced setting control of the LVDS0 PRE SYNC module 0: disable the setting to 1 request of ALIGN0 1: enable the setting to 1 request of ALIGN0
[0]	RW	clr_en_lvds0	Forced setting control of the LVDS0 PRE SYNC module 0: disable the setting to 1 request of LVDS0 CTRL 1: enable the setting to 1 request of LVDS0 CTRL

CHN0_CIL_CTRL

MIPI_CHN0_INT_RAW is CHN0 CIL control register.

Offset Address	Register Name	Total Reset Value
0x081C	CHN0_CIL_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved									phycil0_cken
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	phycil0_cken	PHYCIL0 clock gating 0: disabled 1: enabled

MIPI_CHN0_INT_RAW

MIPI_CHN0_INT_RAW is an MIPI channel 0 raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0EF0	MIPI_CHN0_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											int_data_align_raw	int_mipi_ctrl_raw	int_mipi_csi_raw	int_lvds_ctrl_raw	int_phycil0_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	WC	int_data_align_raw	MIPI ALIGN raw interrupt status 0: There is no raw interrupt. 1: There is a raw interrupt.
[3]	WC	int_mipi_ctrl_raw	MIPI CTRL raw interrupt status 0: There is no raw interrupt. 1: There is a raw interrupt.
[2]	WC	int_mipi_csi_raw	MIPI CSI2 raw interrupt status 0: There is no raw interrupt. 1: There is a raw interrupt.
[1]	WC	int_lvds_ctrl_raw	LVDS CTRL raw interrupt status 0: There is no raw interrupt. 1: There is a raw interrupt.
[0]	WC	int_phycil0_raw	PHYCIL0 raw interrupt status 0: There is no raw interrupt. 1: There is a raw interrupt.

MIPI_CHN0_INT

MIPI_CHN0_INT is an MIPI channel 0 interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0EF4	MIPI_CHN0_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											int_data_align_st	int_mipi_ctrl_st	int_mipi_csi_st	int_lvds_ctrl_st	int_phycil0_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RO	int_data_align_st	MIPI ALIGN interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	int_mipi_ctrl_st	MIPI CTRL interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	int_mipi_csi_st	MIPI CSI2 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	int_lvds_ctrl_st	LVDS CTRL interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_phycil0_st	PHYCIL0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

MIPI_CHN0_INT_MSK

MIPI_CHN0_INT_MSK is an MIPI channel 0 interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0EF8	MIPI_CHN0_INT_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											int_data_align_msk	int_mipi_ctrl_msk	int_mipi_csi_msk	int_lvds_ctrl_msk	int_phycil0_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	int_data_align_msk	MIPI ALIGN interrupt enable 0: masked 1: enabled
[3]	RW	int_mipi_ctrl_msk	MIPI CTRL interrupt enable 0: masked 1: enabled
[2]	RW	int_mipi_csi_msk	MIPI CSI2 interrupt enable 0: masked 1: enabled
[1]	RW	int_lvds_ctrl_msk	LVDS CTRL interrupt enable 0: masked 1: enabled
[0]	RW	int_phycil0_msk	PHYCIL0 interrupt enable 0: masked 1: enabled

MIPI0_LANES_NUM

MIPI0_LANES_NUM is an MIPI 0 enabled data channel quantity register.

Offset Address	Register Name	Total Reset Value
0x1004	MIPI0_LANES_NUM	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													lane_num		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	lane_num	Number of enabled data channels 000: 1 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8

MIPI0_MAIN_INT_ST

MIPI0_MAIN_INT_ST is an MIPI 0 global interrupt status register.

Offset Address	Register Name	Total Reset Value
0x100C	MIPI0_MAIN_INT_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												status_int_line	status_int_pkt	reserved														status_int_frame_fatal	status_int_pkt_fatal	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved

[18]	RO	status_int_line	Line interrupt status. This bit is set to 1 when any of the bits in the MIPI0_LINE_INTR_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_LINE_INTR_ST must be cleared.
[17]	RO	status_int_pkt	Packet interrupt status. This bit is set to 1 when any of the bits in the MIPI0_PKT_INTR2_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_PKT_INTR2_ST must be cleared.
[16:3]	RO	reserved	Reserved
[2]	RO	status_int_frame_fatal	Frame interrupt status. This bit is set to 1 when any of the bits in the MIPI0_FRAME_INTR_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_FRAME_INTR_ST must be cleared.
[1]	RO	status_int_pkt_fatal	Packet interrupt status. This bit is set to 1 when any of the bits in the MIPI0_PKT_INTR_ST register is set to 1. This bit is cleared when it is read. To clear the reported interrupt, this bit and MIPI0_PKT_INTR_ST must be cleared.
[0]	RO	reserved	Reserved

MIPI0_DI_1

MIPI0_DI_1 is an MIPI 0 controller data ID 1 register.

Offset Address	Register Name	Total Reset Value
0x1010	MIPI0_DI_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	di3_vc		di3_dt						di2_vc		di2_dt						di1_vc		di1_dt						di0_vc		di0_dt					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	di3_vc	Virtual channel ID of data with the ID 3 Error check is performed only when the configured data ID matches the ID of received data.

[29:24]	RW	di3_dt	Type of data with the ID 3 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved
[23:22]	RW	di2_vc	Virtual channel ID of data with the ID 2 Error check is performed only when the configured data ID matches the ID of received data.
[21:16]	RW	di2_dt	Type of data with the ID 2 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved
[15:14]	RW	di1_vc	Virtual channel ID of data with the ID 1 Error check is performed only when the configured data ID matches the ID of received data.
[13:8]	RW	di1_dt	Type of data with the ID 1 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved
[7:6]	RW	di0_vc	Virtual channel ID of data with the ID 0 Error check is performed only when the configured data ID matches the ID of received data.

[5:0]	RW	di0_dt	Type of data with the ID 0 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved

MIPI0_DI_2

MIPI0_DI_2 is an MIPI 0 controller data ID 2 register.

Offset Address	Register Name	Total Reset Value
0x1014	MIPI0_DI_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	di7_vc			di7_dt					di6_vc			di6_dt					di5_vc			di5_dt				di4_vc			di4_dt				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RW	di7_vc	Virtual channel ID of data with the ID 7 Error check is performed only when the configured data ID matches the ID of received data.
[29:24]	RW	di7_dt	Type of data with the ID 7 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved
[23:22]	RW	di6_vc	Virtual channel ID of data with the ID 6 Error check is performed only when the configured data ID matches the ID of received data.

[21:16]	RW	di6_dt	Type of data with the ID 6 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved
[15:14]	RW	di5_vc	Virtual channel ID of data with the ID 5 Error check is performed only when the configured data ID matches the ID of received data.
[13:8]	RW	di5_dt	Type of data with the ID 5 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved
[7:6]	RW	di4_vc	Virtual channel ID of data with the ID 4 Error check is performed only when the configured data ID matches the ID of received data.
[5:0]	RW	di4_dt	Type of data with the ID 4 Error check is performed only when the configured data ID matches the ID of received data. 0x2A: raw8 0x2B: raw10 0x2C: raw12 0x2D: raw14 0x2E: RAW16 Other values: reserved

MIPI0_PKT_INTR_ST

MIPI0_PKT_INTR_ST is an MIPI 0 packet interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1060	MIPI0_PKT_INTR_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															err_ecc_double	reserved												vc3_err_crc	vc2_err_crc	vc1_err_crc	vc0_err_crc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RC	err_ecc_double	Whether the header has at least two uncorrectable ECC errors. This bit is cleared when it is read. 0: No ECC error occurs. 1: ECC errors occur.
[15:4]	RO	reserved	Reserved
[3]	RC	vc3_err_crc	Whether the VC 3 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes
[2]	RC	vc2_err_crc	Whether the VC 2 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes
[1]	RC	vc1_err_crc	Whether the VC 1 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes
[0]	RC	vc0_err_crc	Whether the VC 0 data has CRC errors. This bit is cleared when it is read. 0: no 1: yes

MIPI0_PKT_INTR_MSK

MIPI0_PKT_INTR_MSK is an MIPI 0 packet interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1064	MIPI0_PKT_INTR_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															mask_err_ecc_double	reserved												mask_vc3_err_crc	mask_vc2_err_crc	mask_vc1_err_crc	mask_vc0_err_crc
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	mask_err_ecc_double	err_ecc_double interrupt mask 0: masked 1: enabled
[15:4]	RO	reserved	Reserved
[3]	RW	mask_vc3_err_crc	vc3_err_crc interrupt mask 0: masked 1: enabled
[2]	RW	mask_vc2_err_crc	vc2_err_crc interrupt mask 0: masked 1: enabled
[1]	RW	mask_vc1_err_crc	vc1_err_crc interrupt mask 0: masked 1: enabled
[0]	RW	mask_vc0_err_crc	vc0_err_crc interrupt mask 0: masked 1: enabled

MIPI0_PKT_INTR2_ST

MIPI0_PKT_INTR2_ST is MIPI 0 packet interrupt status 2 register.

Offset Address	Register Name	Total Reset Value
0x1070	MIPI0_PKT_INTR2_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												vc3_err_ecc_corrected	vc2_err_ecc_corrected	vc1_err_ecc_corrected	vc0_err_ecc_corrected	reserved												err_id_vc3	err_id_vc2	err_id_vc1	err_id_vc0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RC	vc3_err_ecc_corrected	Whether the VC 3 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.
[18]	RC	vc2_err_ecc_corrected	Whether the VC 2 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.
[17]	RC	vc1_err_ecc_corrected	Whether the VC 1 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.
[16]	RC	vc0_err_ecc_corrected	Whether the VC 0 channel header has ECC errors. This bit is cleared when it is read. 0: no 1: yes. The ECC errors have been corrected.
[15:4]	RO	reserved	Reserved
[3]	RC	err_id_vc3	Whether the VC 3 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported
[2]	RC	err_id_vc2	Whether the VC 2 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported

[1]	RC	err_id_vc1	Whether the VC 1 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported
[0]	RC	err_id_vc0	Whether the VC 0 channel data type is supported. This bit is cleared when it is read. 0: supported 1: not supported

MIPI0_PKT_INTR2_MSK

MIPI0_PKT_INTR2_MSK is MIPI 0 packet interrupt mask 2 register.

Offset Address	Register Name	Total Reset Value
0x1074	MIPI0_PKT_INTR2_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mask_vc3_err_ecc_corrected	mask_vc2_err_ecc_corrected	mask_vc1_err_ecc_corrected	mask_vc0_err_ecc_corrected	reserved												mask_err_id_vc3	mask_err_id_vc2	mask_err_id_vc1	mask_err_id_vc0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RW	mask_vc3_err_ecc_corrected	vc3_err_ecc_corrected interrupt mask 0: masked 1: enabled
[18]	RW	mask_vc2_err_ecc_corrected	vc2_err_ecc_corrected interrupt mask 0: masked 1: enabled
[17]	RW	mask_vc1_err_ecc_corrected	vc1_err_ecc_corrected interrupt mask 0: masked 1: enabled

[16]	RW	mask_vc0_err_ecc_corrected	vc0_err_ecc_corrected interrupt mask 0: masked 1: enabled
[15:4]	RO	reserved	Reserved
[3]	RW	mask_err_id_vc3	err_id_vc3 interrupt mask 0: masked 1: enabled
[2]	RW	mask_err_id_vc2	err_id_vc2 interrupt mask 0: masked 1: enabled
[1]	RW	mask_err_id_vc1	err_id_vc1 interrupt mask 0: masked 1: enabled
[0]	RW	mask_err_id_vc0	err_id_vc0 interrupt mask 0: masked 1: enabled

MIPI0_FRAME_INTR_ST

MIPI0_FRAME_INTR_ST is an MIPI 0 frame interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1080	MIPI0_FRAME_INTR_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												err_frame_data_vc3	err_frame_data_vc2	err_frame_data_vc1	err_frame_data_vc0	reserved				err_f_seq_vc3	err_f_seq_vc2	err_f_seq_vc1	err_f_seq_vc0	reserved				err_f_bndry_match_vc3	err_f_bndry_match_vc2	err_f_bndry_match_vc1	err_f_bndry_match_vc0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved

[19]	RO	err_frame_data_vc3	Whether the last frame of VC 3 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.
[18]	RO	err_frame_data_vc2	Whether the last frame of VC 2 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.
[17]	RO	err_frame_data_vc1	Whether the last frame of VC 1 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.
[16]	RO	err_frame_data_vc0	Whether the last frame of VC 0 channel data has at least one CRC error. This bit is cleared when it is read. 0: No CRC error occurs. 1: CRC errors occur.
[15:12]	RO	reserved	Reserved
[11]	RO	err_f_seq_vc3	Whether the VC 3 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[10]	RO	err_f_seq_vc2	Whether the VC 2 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[9]	RO	err_f_seq_vc1	Whether the VC 1 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[8]	RO	err_f_seq_vc0	Whether the VC 0 frame sequence is correct. This bit is cleared when it is read. 0: yes 1: no
[7:4]	RO	reserved	Reserved
[3]	RO	err_f_bndry_match_vc3	Whether the SOF matches the EOF for the VC 3 channel. This bit is cleared when it is read. 0: yes 1: no

[2]	RO	err_f_bndry_match_vc2	Whether the SOF matches the EOF for the VC 2 channel. This bit is cleared when it is read. 0: yes 1: no
[1]	RO	err_f_bndry_match_vc1	Whether the SOF matches the EOF for the VC 1 channel. This bit is cleared when it is read. 0: yes 1: no
[0]	RO	err_f_bndry_match_vc0	Whether the SOF matches the EOF for the VC 0 channel. This bit is cleared when it is read. 0: yes 1: no

MIPI0_FRAME_INTR_MSK

MIPI0_FRAME_INTR_MSK is an MIPI 0 frame interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1084	MIPI0_FRAME_INTR_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												mask_err_frame_data_vc3	mask_err_frame_data_vc2	mask_err_frame_data_vc1	mask_err_frame_data_vc0	reserved				mask_err_f_seq_vc3	mask_err_f_seq_vc2	mask_err_f_seq_vc1	mask_err_f_seq_vc0	reserved				mask_err_f_bndry_match_vc3	mask_err_f_bndry_match_vc2	mask_err_f_bndry_match_vc1	mask_err_f_bndry_match_vc0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RW	mask_err_frame_data_vc3	err_frame_data_vc3 interrupt mask 0: masked 1: enabled
[18]	RW	mask_err_frame_data_vc2	err_frame_data_vc2 interrupt mask 0: masked 1: enabled

[17]	RW	mask_err_frame_data_vc1	err_frame_data_vc1 interrupt mask 0: masked 1: enabled
[16]	RW	mask_err_frame_data_vc0	err_frame_data_vc0 interrupt mask 0: masked 1: enabled
[15:12]	RO	reserved	Reserved
[11]	RW	mask_err_f_seq_vc3	err_f_seq_vc3 interrupt mask 0: masked 1: enabled
[10]	RW	mask_err_f_seq_vc2	err_f_seq_vc2 interrupt mask 0: masked 1: enabled
[9]	RW	mask_err_f_seq_vc1	err_f_seq_vc1 interrupt mask 0: masked 1: enabled
[8]	RW	mask_err_f_seq_vc0	err_f_seq_vc0 interrupt mask 0: masked 1: enabled
[7:4]	RO	reserved	Reserved
[3]	RW	mask_err_f_bndry_match_vc3	err_f_bndry_match_vc3 interrupt mask 0: masked 1: enabled
[2]	RW	mask_err_f_bndry_match_vc2	err_f_bndry_match_vc2 interrupt mask 0: masked 1: enabled
[1]	RW	mask_err_f_bndry_match_vc1	err_f_bndry_match_vc1 interrupt mask 0: masked 1: enabled
[0]	RW	mask_err_f_bndry_match_vc0	err_f_bndry_match_vc0 interrupt mask 0: masked 1: enabled

MIPI0_LINE_INTR_ST

MIPI0_LINE_INTR_ST is an MIPI 0 line interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1090	MIPI0_LINE_INTR_ST	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								err_l_seq_di7	err_l_seq_di6	err_l_seq_di5	err_l_seq_di4	err_l_seq_di3	err_l_seq_di2	err_l_seq_di1	err_l_seq_di0	reserved								err_l_bndry_match_di7	err_l_bndry_match_di6	err_l_bndry_match_di5	err_l_bndry_match_di4	err_l_bndry_match_di3	err_l_bndry_match_di2	err_l_bndry_match_di1	err_l_bndry_match_di0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23]	RC	err_l_seq_di7	Whether the line sequence of VC 7 and DT 7 is correct. This bit is cleared when it is read. 0: yes 1: no
[22]	RC	err_l_seq_di6	Whether the line sequence of VC 6 and DT 6 is correct. This bit is cleared when it is read. 0: yes 1: no
[21]	RC	err_l_seq_di5	Whether the line sequence of VC 5 and DT 5 is correct. This bit is cleared when it is read. 0: yes 1: no
[20]	RC	err_l_seq_di4	Whether the line sequence of VC 4 and DT 4 is correct. This bit is cleared when it is read. 0: yes 1: no
[19]	RC	err_l_seq_di3	Whether the line sequence of VC 3 and DT 3 is correct. This bit is cleared when it is read. 0: yes 1: no
[18]	RC	err_l_seq_di2	Whether the line sequence of VC 2 and DT 2 is correct. This bit is cleared when it is read. 0: yes 1: no

[17]	RC	err_l_seq_di1	Whether the line sequence of VC 1 and DT 1 is correct. This bit is cleared when it is read. 0: yes 1: no
[16]	RC	err_l_seq_di0	Whether the line sequence of VC 0 and DT 0 is correct. This bit is cleared when it is read. 0: yes 1: no
[15:8]	RO	reserved	Reserved
[7]	RC	err_l_bndry_match_di7	Whether the SOL matches the EOL for VC 7 and DT 7. This bit is cleared when it is read. 0: yes 1: no
[6]	RC	err_l_bndry_match_di6	Whether the SOL matches the EOL for VC 6 and DT 6. This bit is cleared when it is read. 0: yes 1: no
[5]	RC	err_l_bndry_match_di5	Whether the SOL matches the EOL for VC 5 and DT 5. This bit is cleared when it is read. 0: yes 1: no
[4]	RC	err_l_bndry_match_di4	Whether the SOL matches the EOL for VC 4 and DT 4. This bit is cleared when it is read. 0: yes 1: no
[3]	RC	err_l_bndry_match_di3	Whether the SOL matches the EOL for VC 3 and DT 3. This bit is cleared when it is read. 0: yes 1: no
[2]	RC	err_l_bndry_match_di2	Whether the SOL matches the EOL for VC 2 and DT 2. This bit is cleared when it is read. 0: yes 1: no
[1]	RC	err_l_bndry_match_di1	Whether the SOL matches the EOL for VC 1 and DT 1. This bit is cleared when it is read. 0: yes 1: no
[0]	RC	err_l_bndry_match_di0	Whether the SOL matches the EOL for VC 0 and DT 0. This bit is cleared when it is read. 0: yes 1: no

MIPI0_LINE_INTR_MSK

MIPI0_LINE_INTR_MSK is an MIPI 0 line interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x1094	MIPI0_LINE_INTR_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mask_err_1_seq_di7	mask_err_1_seq_di6	mask_err_1_seq_di5	mask_err_1_seq_di4	mask_err_1_seq_di3	mask_err_1_seq_di2	mask_err_1_seq_di1	mask_err_1_seq_di0	reserved								mask_err_1_bndry_match_di7	mask_err_1_bndry_match_di6	mask_err_1_bndry_match_di5	mask_err_1_bndry_match_di4	mask_err_1_bndry_match_di3	mask_err_1_bndry_match_di2	mask_err_1_bndry_match_di1	mask_err_1_bndry_match_di0				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23]	RW	mask_err_1_seq_di7	err_1_seq_di7 interrupt mask 0: masked 1: enabled
[22]	RW	mask_err_1_seq_di6	err_1_seq_di6 interrupt mask 0: masked 1: enabled
[21]	RW	mask_err_1_seq_di5	err_1_seq_di5 interrupt mask 0: masked 1: enabled
[20]	RW	mask_err_1_seq_di4	err_1_seq_di4 interrupt mask 0: masked 1: enabled
[19]	RW	mask_err_1_seq_di3	err_1_seq_di3 interrupt mask 0: masked 1: enabled
[18]	RW	mask_err_1_seq_di2	err_1_seq_di2 interrupt mask 0: masked 1: enabled

[17]	RW	mask_err_1_seq_di1	err_1_seq_di1 interrupt mask 0: masked 1: enabled
[16]	RW	mask_err_1_seq_di0	err_1_seq_di0 interrupt mask 0: masked 1: enabled
[15:8]	RO	reserved	Reserved
[7]	RW	mask_err_1_bndry_match_di7	err_1_bndry_match_di7 interrupt mask 0: masked 1: enabled
[6]	RW	mask_err_1_bndry_match_di6	err_1_bndry_match_di6 interrupt mask 0: masked 1: enabled
[5]	RW	mask_err_1_bndry_match_di5	err_1_bndry_match_di5 interrupt mask 0: masked 1: enabled
[4]	RW	mask_err_1_bndry_match_di4	err_1_bndry_match_di4 interrupt mask 0: masked 1: enabled
[3]	RW	mask_err_1_bndry_match_di3	err_1_bndry_match_di3 interrupt mask 0: masked 1: enabled
[2]	RW	mask_err_1_bndry_match_di2	err_1_bndry_match_di2 interrupt mask 0: masked 1: enabled
[1]	RW	mask_err_1_bndry_match_di1	err_1_bndry_match_di1 interrupt mask 0: masked 1: enabled
[0]	RW	mask_err_1_bndry_match_di0	err_1_bndry_match_di0 interrupt mask 0: masked 1: enabled

MIPI0_USERDEF_DT

MIPI0_USERDEF_DT is an MIPI 0 pixel bit width configuration register for the user-defined data type.

Offset Address	Register Name	Total Reset Value
0x1100	MIPI0_USERDEF_DT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			user_def3_dt				reserved				user_def2_dt				reserved				user_def1_dt				reserved				user_def0_dt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:12]	RW	user_def3_dt	Bit width of the transferred pixel when the data type is user_def3 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved
[11]	RO	reserved	Reserved
[10:8]	RW	user_def2_dt	Bit width of the transferred pixel when the data type is user_def2 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved
[7]	RO	reserved	Reserved
[6:4]	RW	user_def1_dt	Bit width of the transferred pixel when the data type is user_def1 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved
[3]	RO	reserved	Reserved

[2:0]	RW	user_def0_dt	Bit width of the transferred pixel when the data type is user_def0 000: 8 bits 001: 10 bits 010: 12 bits 011: 14 bits 100: 16 bits Other values: reserved

MIPI0_USER_DEF

MIPI0_USER_DEF is an MIPI 0 user-defined data type enable configuration register.

Offset Address	Register Name	Total Reset Value
0x1104	MIPI0_USER_DEF	0x1036_3534

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				user_def3				reserved				user_def2				reserved				user_def1				reserved				user_def0			
Reset	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:24]	RW	user_def3	User-defined data type 3 The value of this field is used for matching the type of the sensor output data. This field works with MIPI0_USERDEF_DT user_def3_dt.
[23:22]	RO	reserved	Reserved
[21:16]	RW	user_def2	User-defined data type 2 The value of this field is used for matching the type of the sensor output data. This field works with MIPI0_USERDEF_DT user_def2_dt.
[15:14]	RO	reserved	Reserved
[13:8]	RW	user_def1	User-defined data type 1 The value of this field is used for matching the type of the sensor output data. This field works with MIPI0_USERDEF_DT user_def1_dt.
[7:6]	RO	reserved	Reserved

[5:0]	RW	user_def0	User-defined data type 0 The value of this field is used for matching the type of the sensor output data. This field works with MIPI0_USERDEF_DT user_def0_dt.

MIPI0_CTRL_MODE_HS

MIPI0_CTRL_MODE_HS is an MIPI 0 operating mode enable register.

Offset Address	Register Name	Total Reset Value
0x1108	MIPI0_CTRL_MODE_HS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							user_def_en	reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	user_def_en	User-defined mode enable 0: disabled 1: enabled
[7:0]	RO	reserved	Reserved

MIPI0_DOL_ID_CODE0

MIPI0_DOL_ID_CODE0 is MIPI 0 DOL mode frame identification 0 register.

Offset Address	Register Name	Total Reset Value
0x1200	MIPI0_DOL_ID_CODE0	0x0242_0241

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg1																id_code_reg0															
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	id_code_reg1	ID of SEF1 frame *N* in MIPI DOL mode
[15:0]	RW	id_code_reg0	ID of LEF frame *N* in MIPI DOL mode

MIPI0_DOL_ID_CODE1

MIPI0_DOL_ID_CODE1 is MIPI 0 DOL mode frame identification 1 register.

Offset Address	Register Name	Total Reset Value
0x1204	MIPI0_DOL_ID_CODE1	0x0251_0244

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg3																id_code_reg2															
Reset	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RW	id_code_reg3	ID of LEF frame *N* + 1 in MIPI DOL mode
[15:0]	RW	id_code_reg2	ID of SEF2 frame *N* in MIPI DOL mode

MIPI0_DOL_ID_CODE2

MIPI0_DOL_ID_CODE2 is MIPI 0 DOL mode frame identification 2 register.

Offset Address	Register Name	Total Reset Value
0x1208	MIPI0_DOL_ID_CODE2	0x0254_0252

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	id_code_reg5																id_code_reg4															
Reset	0	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0

Bits	Access	Name	Description
[31:16]	RW	id_code_reg5	ID of SEF2 frame *N* + 1 in MIPI DOL mode
[15:0]	RW	id_code_reg4	ID of SEF1 frame *N* + 1 in MIPI DOL mode

MIPI0_CTRL_MODE_PIXEL

MIPI0_CTRL_MODE_PIXEL is an MIPI 0 output operating mode enable register.

Offset Address	Register Name	Total Reset Value
0x1230	MIPI0_CTRL_MODE_PIXEL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				stagger_frm_num	stagger_hdr_mode	reserved	mipi_dol_mode	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:13]	RW	stagger_frm_num	Number of frames in staggered HDR mode 01: 2-frame HDR 10: 3-frame HDR 11: 4-frame HDR Other values: reserved
[12]	RW	stagger_hdr_mode	OmniVision staggered HDR mode enable 0: disabled 1: enabled
[11:5]	RW	reserved	Reserved
[4]	RW	mipi_dol_mode	MIPI DOL mode enable 0: disabled 1: enabled
[3:0]	RO	reserved	Reserved

MIPI0_DUMMY_PIX_REG

MIPI0_DUMMY_PIX_REG is an MIPI 0 dummy line pixel value register.

Offset Address	Register Name	Total Reset Value
0x1240	MIPI0_DUMMY_PIX_REG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				dummy_pix_reg			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dummy_pix_reg	Dummy line pixel value in staggered HDR mode

MIPI0_IMGSIZE0_STATIS

MIPI0_IMGSIZE0_STATIS is an MIPI 0 VC 0 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x1250	MIPI0_IMGSIZE0_STATIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	imgheight_statis_vc0				imgwidth_statis_vc0			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc0	Height of the previous frame of image transferred by virtual channel 0 in MIPI mode
[15:0]	RO	imgwidth_statis_vc0	Width of the previous frame of image transferred by virtual channel 0 in MIPI mode

MIPI0_IMGSIZE1_STATIS

MIPI0_IMGSIZE1_STATIS is an MIPI 0 VC 1 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x1254	MIPI0_IMGSIZE1_STATIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	imgheight_statis_vc1				imgwidth_statis_vc1			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc1	Height of the previous frame of image transferred by virtual channel 1 in MIPI mode

[15:0]	RO	imgwidth_statis_vc1	Width of the previous frame of image transferred by virtual channel 1 in MIPI mode

MIPI0_IMGSIZE2_STATIS

MIPI0_IMGSIZE2_STATIS is an MIPI 0 VC 2 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x1258	MIPI0_IMGSIZE2_STATIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	imgheight_statis_vc2				imgwidth_statis_vc2			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc2	Height of the previous frame of image transferred by virtual channel 2 in MIPI mode
[15:0]	RO	imgwidth_statis_vc2	Width of the previous frame of image transferred by virtual channel 2 in MIPI mode

MIPI0_IMGSIZE3_STATIS

MIPI0_IMGSIZE3_STATIS is an MIPI 0 VC 3 transferred image size register.

Offset Address	Register Name	Total Reset Value
0x125C	MIPI0_IMGSIZE3_STATIS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	imgheight_statis_vc3				imgwidth_statis_vc3			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	imgheight_statis_vc3	Height of the previous frame of image transferred by virtual channel 3 in MIPI mode
[15:0]	RO	imgwidth_statis_vc3	Width of the previous frame of image transferred by virtual channel 3 in MIPI mode

MIPI0_CTRL_INT_RAW

MIPI0_CTRL_INT_RAW is an MIPI 0 read data error raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x12F0	MIPI0_CTRL_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_dfifo_rderr_raw	int_cfifo_rderr_raw	reserved														int_dfifo_wrerr_raw	int_cfifo_wrerr_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	WC	int_dfifo_rderr_raw	MIPI CTRL read data FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[16]	WC	int_cfifo_rderr_raw	MIPI CTRL read command FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:2]	RO	reserved	Reserved
[1]	WC	int_dfifo_wrerr_raw	MIPI CTRL write data FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	int_cfifo_wrerr_raw	MIPI CTRL write command FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

MIPI0_CTRL_INT

MIPI0_CTRL_INT is an MIPI 0 read data error interrupt status register.

Offset Address	Register Name	Total Reset Value
0x12F4	MIPI0_CTRL_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_dfifo_rderr_st	int_cfifo_rderr_st	reserved														int_dfifo_wrerr_st	int_cfifo_wrerr_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	int_dfifo_rderr_st	MIPI CTRL read data FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	int_cfifo_rderr_st	MIPI CTRL read command FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[15:2]	RO	reserved	Reserved
[1]	RO	int_dfifo_wrerr_st	MIPI CTRL write data FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	int_cfifo_wrerr_st	MIPI CTRL write command FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

MIPI0_CTRL_INT_MSK

MIPI0_CTRL_INT_MSK is an MIPI 0 read data error interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x12F8	MIPI0_CTRL_INT_MSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														int_dfifo_rderr_msk	int_cfifo_rderr_msk	reserved														int_dfifo_wrerr_msk	int_cfifo_wrerr_msk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	int_dfifo_rderr_msk	MIPI CTRL read data FIFO interrupt enable 0: masked 1: enabled
[16]	RW	int_cfifo_rderr_msk	MIPI CTRL read command FIFO interrupt enable 0: masked 1: enabled
[15:2]	RO	reserved	Reserved
[1]	RW	int_dfifo_wrerr_msk	MIPI CTRL write data FIFO interrupt enable 0: masked 1: enabled
[0]	RW	int_cfifo_wrerr_msk	MIPI CTRL write command FIFO interrupt enable 0: masked 1: enabled

LVDS0_WDR

LVDS0_WDR is an LVDS WDR control register.

Offset Address	Register Name	Total Reset Value
0x1300	LVDS0_WDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																lvds_wdr_id_shift				lvds_wdr_mode				reserved				lvds_wdr_num		reserved				lvds_wdr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	lvds_wdr_id_shift	IMX136 frame ID shift register, indicating the number of bits to be shifted rightwards to make the frame ID be in bit 0
[11:8]	RW	lvds_wdr_mode	LVDS WDR mode select 0x0: WDR mode with the SOF-EOF flag. In this mode, the long exposure frame and short exposure frame have independent synchronization codes. 0x2: HiSPI WDR mode. In this mode, the long and short exposure frames share one SOF-EOF flag, and the first several lines of the short exposure frame are stuffed with 0x04. 0x4: SONY DOL WDR mode. In this mode, the synchronization code consists of four fields, the SAV-EAV flag is used, and the long exposure frame and short exposure frame have independent synchronization codes. 0x5: SONY DOL mode. In this mode, the synchronization code consists of four fields. The SAV-EAV flag mode is used. The long and short exposure frames share a group of sync code, and the region between the long and short exposure frames is the blanking region. 0x6: SONY DOL WDR mode. In this mode, the synchronization code consists of five fields, and the fifth field indicates the long or short frame. 0x8: SONY IMX136 mode, frame WDR mode. Do not enable WDR_EN. 0x9: SHARP long and short exposure frame interleaving mode. The long exposure frame is before the short exposure frame. 0xA: SHARP long and short exposure frame interleaving mode. The short exposure frame is before the long exposure frame.
[7:6]	RO	reserved	Reserved

[5:4]	RW	lvds_wdr_num	WDR mode configuration 00: reserved 01: 2-frame WDR 10: 3-frame WDR 11: 4-frame WDR
[3:1]	RO	reserved	Reserved
[0]	RW	lvds_wdr_en	WDR enable 0: linear mode 1: WDR mode

LVDS0_CTRL

LVDS0_CTRL is an LVDS control register.

Offset Address	Register Name	Total Reset Value
0x1304	LVDS0_CTRL	0x0000_0310

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9	8	7 6 5 4	3 2 1 0
Name	reserved			lvds_split_mode	reserved		lvds_code_big_endian	lvds_pix_big_endian	reserved / lvds_raw_type	reserved / lvds_sync_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	1	1	0 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	lvds_split_mode	LVDS/HiSPI sync code transfer type 000: Per lane mode 011: Split 2 lane mode 111: Split 4 lane mode Other values: reserved
[15:10]	RO	reserved	Reserved

[9]	RW	lvds_code_big_endian	Transfer sequence of serial bits of transferred RAW data sync code (sync_code) in LVDS/HiSPI mode 0: LSB. Lower bits are transferred first. The sequence of the received sync code (sync_code) serial data is bit 0, bit 1, ..., and bit 11. 1: MSB. Upper bits are transferred first. The sequence of the received sync code (sync_code) serial data is bit 11, bit 10, ..., and bit 0.
[8]	RW	lvds_pix_big_endian	Transfer sequence of serial bits of transferred RAW data valid pixels in LVDS/HiSPI mode 0: LSB. Lower bits are transferred first. The sequence of the received valid pixel serial data is bit 0, bit 1, ..., and bit 11. 1: MSB. Upper bits are transferred first. The sequence of the received valid pixel serial data is bit 11, bit 10, ..., and bit 0.
[7]	RO	reserved	Reserved
[6:4]	RW	lvds_raw_type	Type of transferred RAW data in LVDS/HiSPI mode 001: Raw 8-bit 010: Raw 10-bit 011: Raw 12-bit 100: Raw 14-bit 101: Raw 16-bit
[3:1]	RO	reserved	Reserved
[0]	RW	lvds_sync_mode	Frame/Line sync mode in LVDS mode 0: The sync mode is SOF/EOF/SOL/EOL mode. SOF indicates the start of the first line of the valid region, EOF indicates the end of the last line of the valid region, and SOL and EOL indicate the start and end of other valid regions respectively. 1: The sync mode is SAV/EAV mode. SAV(Invalid) and EAV(Invalid) indicate the invalid data of the blanking region, and SAV(Valid) and EAV(Valid) indicate pixel data of the valid region.

LVDS0_DOLSCD_HBLK

LVDS0_DOLSCD_HBLK is an LVDS SCD control register.

Offset Address	Register Name	Total Reset Value
0x1308	LVDS0_DOLSCD_HBLK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dol_hblank2																dol_hblank1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	dol_hblank2	Value of HBLANK2 in DOL mode
[15:0]	RW	dol_hblank1	Value of HBLANK1 in DOL mode

LVDS0_IMGSIZE

LVDS0_IMGSIZE is an LVDS image size register.

Offset Address	Register Name	Total Reset Value
0x130C	LVDS0_IMGSIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight																lvds_imgwidth_lane															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lvds_imgheight	Image height minus 1
[15:0]	RW	lvds_imgwidth_lane	Width of the image transferred by each channel minus 1

LVDS0_LANE0_SOF_01

LVDS0_LANE0_SOF_01 is a lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1320	LVDS0_LANE0_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sof_1																lane0_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_1	Lane 0 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sof_0	Lane 0 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE0_SOF_23

LVDS0_LANE0_SOF_23 is a lane 0 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1324	LVDS0_LANE0_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sof_3																lane0_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sof_3	Lane 0 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sof_2	Lane 0 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_EOF_01

LVDS0_LANE0_EOF_01 is a lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1328	LVDS0_LANE0_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eof_1																lane0_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_1	Lane 0 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eof_0	Lane 0 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE0_EOF_23

LVDS0_LANE0_EOF_23 is a lane 0 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x132C	LVDS0_LANE0_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eof_3																lane0_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eof_3	Lane 0 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eof_2	Lane 0 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_SOL_01

LVDS0_LANE0_SOL_01 is a lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1330	LVDS0_LANE0_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sol_1																lane0_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sol_1	Lane 0 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sol_0	Lane 0 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE0_SOL_23

LVDS0_LANE0_SOL_23 is a lane 0 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1334	LVDS0_LANE0_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_sol_3																lane0_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_sol_3	Lane 0 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_sol_2	Lane 0 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_EOL_01

LVDS0_LANE0_EOL_01 is a lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1338	LVDS0_LANE0_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eol_1																lane0_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eol_1	Lane 0 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eol_0	Lane 0 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE0_EOL_23

LVDS0_LANE0_EOL_23 is a lane 0 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x133C	LVDS0_LANE0_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_eol_3																lane0_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_eol_3	Lane 0 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_eol_2	Lane 0 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_SOF_01

LVDS0_LANE1_SOF_01 is a lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1340	LVDS0_LANE1_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sof_1																lane1_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sof_1	Lane 1 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sof_0	Lane 1 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE1_SOF_23

LVDS0_LANE1_SOF_23 is a lane 1 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1344	LVDS0_LANE1_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sof_3																lane1_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sof_3	Lane 1 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sof_2	Lane 1 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_EOF_01

LVDS0_LANE1_EOF_01 is a lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1348	LVDS0_LANE1_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eof_1																lane1_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eof_1	Lane 1 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eof_0	Lane 1 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE1_EOF_23

LVDS0_LANE1_EOF_23 is a lane 1 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x134C	LVDS0_LANE1_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eof_3																lane1_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eof_3	Lane 1 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eof_2	Lane 1 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_SOL_01

LVDS0_LANE1_SOL_01 is a lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1350	LVDS0_LANE1_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sol_1																lane1_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sol_1	Lane 1 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sol_0	Lane 1 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE1_SOL_23

LVDS0_LANE1_SOL_23 is a lane 1 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1354	LVDS0_LANE1_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_sol_3																lane1_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_sol_3	Lane 1 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_sol_2	Lane 1 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_EOL_01

LVDS0_LANE1_EOL_01 is a lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1358	LVDS0_LANE1_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eol_1																lane1_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eol_1	Lane 1 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eol_0	Lane 1 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE1_EOL_23

LVDS0_LANE1_EOL_23 is a lane 1 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x135C	LVDS0_LANE1_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_eol_3																lane1_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_eol_3	Lane 1 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_eol_2	Lane 1 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_SOF_01

LVDS0_LANE2_SOF_01 is a lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1360	LVDS0_LANE2_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sof_1																lane2_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sof_1	Lane 2 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sof_0	Lane 2 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE2_SOF_23

LVDS0_LANE2_SOF_23 is a lane 2 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1364	LVDS0_LANE2_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sof_3																lane2_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sof_3	Lane 2 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sof_2	Lane 2 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_EOF_01

LVDS0_LANE2_EOF_01 is a lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1368	LVDS0_LANE2_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eof_1																lane2_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_1	Lane 2 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eof_0	Lane 2 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE2_EOF_23

LVDS0_LANE2_EOF_23 is a lane 2 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x136C	LVDS0_LANE2_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eof_3																lane2_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eof_3	Lane 2 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eof_2	Lane 2 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_SOL_01

LVDS0_LANE2_SOL_01 is a lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1370	LVDS0_LANE2_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sol_1																lane2_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_1	Lane 2 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sol_0	Lane 2 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE2_SOL_23

LVDS0_LANE2_SOL_23 is a lane 2 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1374	LVDS0_LANE2_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_sol_3																lane2_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_sol_3	Lane 2 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_sol_2	Lane 2 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_EOL_01

LVDS0_LANE2_EOL_01 is a lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1378	LVDS0_LANE2_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eol_1																lane2_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_1	Lane 2 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eol_0	Lane 2 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE2_EOL_23

LVDS0_LANE2_EOL_23 is a lane 2 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x137C	LVDS0_LANE2_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_eol_3																lane2_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_eol_3	Lane 2 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_eol_2	Lane 2 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_SOF_01

LVDS0_LANE3_SOF_01 is a lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1380	LVDS0_LANE3_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sof_1																lane3_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_1	Lane 3 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sof_0	Lane 3 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE3_SOF_23

LVDS0_LANE3_SOF_23 is a lane 3 SOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1384	LVDS0_LANE3_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sof_3																lane3_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sof_3	Lane 3 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sof_2	Lane 3 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_EOF_01

LVDS0_LANE3_EOF_01 is a lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1388	LVDS0_LANE3_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eof_1																lane3_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_1	Lane 3 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eof_0	Lane 3 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE3_EOF_23

LVDS0_LANE3_EOF_23 is a lane 3 EOF synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x138C	LVDS0_LANE3_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eof_3																lane3_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eof_3	Lane 3 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eof_2	Lane 3 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_SOL_01

LVDS0_LANE3_SOL_01 is a lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1390	LVDS0_LANE3_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sol_1																lane3_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sol_1	Lane 3 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sol_0	Lane 3 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE3_SOL_23

LVDS0_LANE3_SOL_23 is a lane 3 SOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1394	LVDS0_LANE3_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_sol_3																lane3_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_sol_3	Lane 3 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_sol_2	Lane 3 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_EOL_01

LVDS0_LANE3_EOL_01 is a lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1398	LVDS0_LANE3_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eol_1																lane3_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eol_1	Lane 3 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eol_0	Lane 3 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE3_EOL_23

LVDS0_LANE3_EOL_23 is a lane 3 EOL synchronization code configuration register in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x139C	LVDS0_LANE3_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_eol_3																lane3_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_eol_3	Lane 3 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_eol_2	Lane 3 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_SOF_01

LVDS0_LANE0_NXT_SOF_01 is a lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13A0	LVDS0_LANE0_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sof_1																lane0_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sof_1	Lane 0 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sof_0	Lane 0 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE0_NXT_SOF_23

LVDS0_LANE0_NXT_SOF_23 is a lane 0 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13A4	LVDS0_LANE0_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sof_3																lane0_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sof_3	Lane 0 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sof_2	Lane 0 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_EOF_01

LVDS0_LANE0_NXT_EOF_01 is a lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13A8	LVDS0_LANE0_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eof_1																lane0_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eof_1	Lane 0 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eof_0	Lane 0 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE0_NXT_EOF_23

LVDS0_LANE0_NXT_EOF_23 is a lane 0 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13AC	LVDS0_LANE0_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eof_3																lane0_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eof_3	Lane 0 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eof_2	Lane 0 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_SOL_01

LVDS0_LANE0_NXT_SOL_01 is a lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13B0	LVDS0_LANE0_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sol_1																lane0_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sol_1	Lane 0 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sol_0	Lane 0 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE0_NXT_SOL_23

LVDS0_LANE0_NXT_SOL_23 is a lane 0 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13B4	LVDS0_LANE0_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_sol_3																lane0_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_sol_3	Lane 0 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_sol_2	Lane 0 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE0_NXT_EOL_01

LVDS0_LANE0_NXT_EOL_01 is a lane 0 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13B8	LVDS0_LANE0_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eol_1																lane0_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eol_1	Lane 0 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eol_0	Lane 0 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE0_NXT_EOL_23

LVDS0_LANE0_NXT_EOL_23 is a lane 0 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13BC	LVDS0_LANE0_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane0_nxt_eol_3																lane0_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane0_nxt_eol_3	Lane 0 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane0_nxt_eol_2	Lane 0 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_SOF_01

LVDS0_LANE1_NXT_SOF_01 is a lane 1 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13C0	LVDS0_LANE1_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sof_1																lane1_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sof_1	Lane 1 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sof_0	Lane 1 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE1_NXT_SOF_23

LVDS0_LANE1_NXT_SOF_23 is a lane 1 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13C4	LVDS0_LANE1_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sof_3																lane1_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sof_3	Lane 1 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sof_2	Lane 1 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_EOF_01

LVDS0_LANE1_NXT_EOF_01 is a lane 1 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13C8	LVDS0_LANE1_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eof_1																lane1_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eof_1	Lane 1 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eof_0	Lane 1 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE1_NXT_EOF_23

LVDS0_LANE1_NXT_EOF_23 is a lane 1 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13CC	LVDS0_LANE1_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eof_3																lane1_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eof_3	Lane 1 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eof_2	Lane 1 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_SOL_01

LVDS0_LANE1_NXT_SOL_01 is a lane 1 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13D0	LVDS0_LANE1_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sol_1																lane1_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sol_1	Lane 1 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sol_0	Lane 1 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE1_NXT_SOL_23

LVDS0_LANE1_NXT_SOL_23 is a lane 1 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13D4	LVDS0_LANE1_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_sol_3																lane1_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_sol_3	Lane 1 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_sol_2	Lane 1 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE1_NXT_EOL_01

LVDS0_LANE1_NXT_EOL_01 is a lane 1 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13D8	LVDS0_LANE1_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eol_1																lane1_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eol_1	Lane 1 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eol_0	Lane 1 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE1_NXT_EOL_23

LVDS0_LANE1_NXT_EOL_23 is a lane 1 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13DC	LVDS0_LANE1_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane1_nxt_eol_3																lane1_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane1_nxt_eol_3	Lane 1 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane1_nxt_eol_2	Lane 1 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_SOF_01

LVDS0_LANE2_NXT_SOF_01 is a lane 2 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13E0	LVDS0_LANE2_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sof_1																lane2_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sof_1	Lane 2 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sof_0	Lane 2 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE2_NXT_SOF_23

LVDS0_LANE2_NXT_SOF_23 is a lane 2 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13E4	LVDS0_LANE2_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sof_3																lane2_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sof_3	Lane 2 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sof_2	Lane 2 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_EOF_01

LVDS0_LANE2_NXT_EOF_01 is a lane 2 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13E8	LVDS0_LANE2_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eof_1																lane2_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eof_1	Lane 2 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eof_0	Lane 2 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE2_NXT_EOF_23

LVDS0_LANE2_NXT_EOF_23 is a lane 2 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13EC	LVDS0_LANE2_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eof_3																lane2_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eof_3	Lane 2 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eof_2	Lane 2 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_SOL_01

LVDS0_LANE2_NXT_SOL_01 is a lane 2 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13F0	LVDS0_LANE2_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sol_1																lane2_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sol_1	Lane 2 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sol_0	Lane 2 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE2_NXT_SOL_23

LVDS0_LANE2_NXT_SOL_23 is a lane 2 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13F4	LVDS0_LANE2_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_sol_3																lane2_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_sol_3	Lane 2 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_sol_2	Lane 2 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE2_NXT_EOL_01

LVDS0_LANE2_NXT_EOL_01 is a lane 2 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13F8	LVDS0_LANE2_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eol_1																lane2_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eol_1	Lane 2 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eol_0	Lane 2 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE2_NXT_EOL_23

LVDS0_LANE2_NXT_EOL_23 is a lane 2 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x13FC	LVDS0_LANE2_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane2_nxt_eol_3																lane2_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane2_nxt_eol_3	Lane 2 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane2_nxt_eol_2	Lane 2 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_SOF_01

LVDS0_LANE3_NXT_SOF_01 is a lane 3 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1400	LVDS0_LANE3_NXT_SOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sof_1																lane3_nxt_sof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sof_1	Lane 3 SOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sof_0	Lane 3 SOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOF of frame 0. In linear mode, the value is the SOF.

LVDS0_LANE3_NXT_SOF_23

LVDS0_LANE3_NXT_SOF_23 is a lane 3 SOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1404	LVDS0_LANE3_NXT_SOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sof_3																lane3_nxt_sof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sof_3	Lane 3 SOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sof_2	Lane 3 SOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_EOF_01

LVDS0_LANE3_NXT_EOF_01 is a lane 3 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1408	LVDS0_LANE3_NXT_EOF_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eof_1																lane3_nxt_eof_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eof_1	Lane 3 EOF synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eof_0	Lane 3 EOF synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOF of frame 0. In linear mode, the value is the EOF.

LVDS0_LANE3_NXT_EOF_23

LVDS0_LANE3_NXT_EOF_23 is a lane 3 EOF synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x140C	LVDS0_LANE3_NXT_EOF_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eof_3																lane3_nxt_eof_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eof_3	Lane 3 EOF synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eof_2	Lane 3 EOF synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_SOL_01

LVDS0_LANE3_NXT_SOL_01 is a lane 3 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1410	LVDS0_LANE3_NXT_SOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sol_1																lane3_nxt_sol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sol_1	Lane 3 SOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sol_0	Lane 3 SOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the SOL of frame 0. In linear mode, the value is the SOL.

LVDS0_LANE3_NXT_SOL_23

LVDS0_LANE3_NXT_SOL_23 is a lane 3 SOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1414	LVDS0_LANE3_NXT_SOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_sol_3																lane3_nxt_sol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_sol_3	Lane 3 SOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_sol_2	Lane 3 SOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LANE3_NXT_EOL_01

LVDS0_LANE3_NXT_EOL_01 is a lane 3 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x1418	LVDS0_LANE3_NXT_EOL_01	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eol_1																lane3_nxt_eol_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eol_1	Lane 3 EOL synchronization code of frame 1 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eol_0	Lane 3 EOL synchronization code of frame 0 in LVDS or HiSPI mode In WDR mode, the value is the EOL of frame 0. In linear mode, the value is the EOL.

LVDS0_LANE3_NXT_EOL_23

LVDS0_LANE3_NXT_EOL_23 is a lane 3 EOL synchronization code configuration register for frame (N + 1) in LVDS or HiSPI mode.

Offset Address	Register Name	Total Reset Value
0x141C	LVDS0_LANE3_NXT_EOL_23	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lane3_nxt_eol_3																lane3_nxt_eol_2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	lane3_nxt_eol_3	Lane 3 EOL synchronization code of frame 3 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.
[15:0]	RW	lane3_nxt_eol_2	Lane 3 EOL synchronization code of frame 2 in LVDS or HiSPI mode This field is configurable only in WDR mode, and the configuration is invalid in linear mode.

LVDS0_LI_WORD0

LVDS0_LI_WORD0 is an LVDS DOL mode frame 0 LI register.

Offset Address	Register Name	Total Reset Value
0x1420	LVDS0_LI_WORD0	0x0211_0201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word0_1																li_word0_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	li_word0_1	LEF line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word0_0	LEF line information in DOL mode (for frame *N*)

LVDS0_LI_WORD1

LVDS0_LI_WORD1 is an LVDS DOL mode frame 1 LI register.

Offset Address	Register Name	Total Reset Value
0x1424	LVDS0_LI_WORD1	0x0212_0202

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word1_1																li_word1_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:16]	RW	li_word1_1	SEF1 line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word1_0	SEF1 line information in DOL mode (for frame *N*)

LVDS0_LI_WORD2

LVDS0_LI_WORD2 is an LVDS DOL mode frame 2 LI register.

Offset Address	Register Name	Total Reset Value
0x1428	LVDS0_LI_WORD2	0x0214_0204

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word2_1																li_word2_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:16]	RW	li_word2_1	SEF2 line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word2_0	SEF2 line information in DOL mode (for frame *N*)

LVDS0_LI_WORD3

LVDS0_LI_WORD3 is an LVDS DOL mode frame 3 LI register.

Offset Address	Register Name	Total Reset Value
0x142C	LVDS0_LI_WORD3	0x0218_0208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	li_word3_1																li_word3_0															
Reset	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RW	li_word3_1	SEF3 line information in DOL mode (for frame *N* + 1)
[15:0]	RW	li_word3_0	SEF3 line information in DOL mode (for frame *N*)

LVDS0_IMGSIZE0_STATIS

LVDS0_IMGSIZE0_STATIS is an LVDS LEF image size statistics register.

Offset Address	Register Name	Total Reset Value
0x1500	LVDS0_IMGSIZE0_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight0																lvds_imgwidth0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight0	Height of the image transferred by virtual channel 0 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth0	Width of the image transferred by virtual channel 0 in LVDS or HiSPI mode

LVDS0_IMGSIZE1_STATIS

LVDS0_IMGSIZE1_STATIS is an LVDS SEF1 image size statistics register.

Offset Address	Register Name	Total Reset Value
0x1504	LVDS0_IMGSIZE1_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight1																lvds_imgwidth1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight1	Height of the image transferred by virtual channel 1 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth1	Width of the image transferred by virtual channel 1 in LVDS or HiSPI mode

LVDS0_IMGSIZE2_STATIS

LVDS0_IMGSIZE2_STATIS is an LVDS SEF2 image size statistics register.

Offset Address	Register Name	Total Reset Value
0x1508	LVDS0_IMGSIZE2_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight2																lvds_imgwidth2															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight2	Height of the image transferred by virtual channel 2 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth2	Width of the image transferred by virtual channel 2 in LVDS or HiSPI mode

LVDS0_IMGSIZE3_STATIS

LVDS0_IMGSIZE3_STATIS is an LVDS SEF3 image size statistics register.

Offset Address	Register Name	Total Reset Value
0x150C	LVDS0_IMGSIZE3_STATIS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lvds_imgheight3																lvds_imgwidth3															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	lvds_imgheight3	Height of the image transferred by virtual channel 3 in LVDS or HiSPI mode
[15:0]	RO	lvds_imgwidth3	Width of the image transferred by virtual channel 3 in LVDS or HiSPI mode

LVDS0_CTRL_INT_RAW

LVDS0_CTRL_INT_RAW is an LVDS read data raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15F0	LVDS0_CTRL_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							link0_rderr_raw	link0_wrerr_raw	link0_hsync_err_raw	link0_vsync_err_raw	lvds_stat_err_raw	lane3_sync_err_raw	lane2_sync_err_raw	lane1_sync_err_raw	lane0_sync_err_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	WC	link0_rderr_raw	Status of the link 0 data read error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.
[7]	WC	link0_wrerr_raw	Status of the link 0 data write error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.
[6]	WC	link0_hsync_err_raw	Status of the link 0 hsync error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.

[5]	WC	link0_vsync_err_raw	Status of the link 0 vsync error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.
[4]	WC	lvds_stat_err_raw	Status of the LVDS status error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.
[3]	WC	lane3_sync_err_raw	Status of the lane 3 sync error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.
[2]	WC	lane2_sync_err_raw	Status of the lane 2 sync error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.
[1]	WC	lane1_sync_err_raw	Status of the lane 1 sync error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.
[0]	WC	lane0_sync_err_raw	Status of the lane 0 sync error raw interrupt 0: There is no raw interrupt. 1: There is a raw interrupt.

LVDS0_CTRL_INT

LVDS0_CTRL_INT is an LVDS read data interrupt status register.

Offset Address	Register Name	Total Reset Value
0x15F4	LVDS0_CTRL_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							link0_rderr_st	link0_wrerr_st	link0_hsync_err_st	link0_vsync_err_st	lvds_stat_err_st	lane3_sync_err_st	lane2_sync_err_st	lane1_sync_err_st	lane0_sync_err_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	link0_rderr_st	Status of the link 0 data read error interrupt 0: There is no interrupt. 1: There is an interrupt.

[7]	RO	link0_wrerr_st	Status of the link 0 data write error interrupt 0: There is no interrupt. 1: There is an interrupt.
[6]	RO	link0_hsync_err_st	Status of the link 0 hsync error interrupt 0: There is no interrupt. 1: There is an interrupt.
[5]	RO	link0_vsync_err_st	Status of the link 0 vsync error interrupt 0: There is no interrupt. 1: There is an interrupt.
[4]	RO	lvds_stat_err_st	Status of the LVDS status error interrupt 0: There is no interrupt. 1: There is an interrupt.
[3]	RO	lane3_sync_err_st	Status of the lane 3 sync error interrupt 0: There is no interrupt. 1: There is an interrupt.
[2]	RO	lane2_sync_err_st	Status of the lane 2 sync error interrupt 0: There is no interrupt. 1: There is an interrupt.
[1]	RO	lane1_sync_err_st	Status of the lane 1 sync error interrupt 0: There is no interrupt. 1: There is an interrupt.
[0]	RO	lane0_sync_err_st	Status of the lane 0 sync error interrupt 0: There is no interrupt. 1: There is an interrupt.

LVDS0_CTRL_INT_MSK

LVDS0_CTRL_INT_MSK is an LVDS read data interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x15F8	LVDS0_CTRL_INT_MSK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7	6	5	4	3	2	1	0
Name	reserved						link0_rderr_msk	link0_wrerr_msk	link0_hsync_err_msk	link0_vsync_err_msk	lvds_stat_err_st_msk	lane3_sync_err_msk	lane2_sync_err_msk	lane1_sync_err_msk	lane0_sync_err_msk

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	link0_rderr_msk	Link 0 data read error interrupt enable 0: masked 1: enabled
[7]	RW	link0_wrerr_msk	Link 0 data write error interrupt enable 0: masked 1: enabled
[6]	RW	link0_hsync_err_msk	Link 0 hsync error interrupt enable 0: masked 1: enabled
[5]	RW	link0_vsync_err_msk	Link 0 vsync error interrupt enable 0: masked 1: enabled
[4]	RW	lvds_stat_err_st_msk	LVDS status error interrupt enable 0: masked 1: enabled
[3]	RW	lane3_sync_err_msk	Lane 3 sync error interrupt enable 0: masked 1: enabled
[2]	RW	lane2_sync_err_msk	Lane 2 sync error interrupt enable 0: masked 1: enabled
[1]	RW	lane1_sync_err_msk	Lane 1 sync error interrupt enable 0: masked 1: enabled
[0]	RW	lane0_sync_err_msk	Lane 0 sync error interrupt enable 0: masked 1: enabled

ALIGN0_LANE_ID

ALIGN0_LANE_ID is a link 0 lane priority configuration register.

Offset Address	Register Name	Total Reset Value
0x1600	ALIGN0_LANE_ID	0x0000_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																lane3_id				lane2_id				lane1_id				lane0_id			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:12]	RW	lane3_id	Lane 3 channel ID Value range: 0−3 The field value indicates the ID of image sensor channel connected to lane 3.
[11:8]	RW	lane2_id	Lane 2 channel ID Value range: 0−3 The field value indicates the ID of image sensor channel connected to lane 2.
[7:4]	RW	lane1_id	Lane 1 channel ID Value range: 0−3 The field value indicates the ID of image sensor channel connected to lane 1.
[3:0]	RW	lane0_id	Lane 0 channel ID Value range: 0−3 The field value indicates the ID of image sensor channel connected to lane 0.

ALIGN0_INT_RAW

ALIGN0_INT_RAW is an MIPI_ALIGN raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16F0	ALIGN0_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												err_full_raw	err_lane3_raw	err_lane2_raw	err_lane1_raw	err_lane0_raw

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	WC	err_full_raw	MIPI_ALIGN FIFO raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	WC	err_lane3_raw	MIPI_ALIGN lane 3 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	WC	err_lane2_raw	MIPI_ALIGN lane 2 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	WC	err_lane1_raw	MIPI_ALIGN lane 1 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	WC	err_lane0_raw	MIPI_ALIGN lane 0 raw interrupt status 0: No raw interrupt is generated. 1: A raw interrupt is generated.

ALIGN0_INT

ALIGN0_INT is an MIPI_ALIGN interrupt status register.

Offset Address	Register Name	Total Reset Value
0x16F4	ALIGN0_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											err_full_st	err_lane3_st	err_lane2_st	err_lane1_st	err_lane0_st
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved

[4]	RO	err_full_st	MIPI_ALIGN FIFO interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	err_lane3_st	MIPI_ALIGN lane 3 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	err_lane2_st	MIPI_ALIGN lane 2 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	err_lane1_st	MIPI_ALIGN lane 1 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	err_lane0_st	MIPI_ALIGN lane 0 interrupt status 0: No interrupt is generated. 1: An interrupt is generated.

ALIGN0_INT_MSK

ALIGN0_INT_MSK is an MIPI_ALIGN interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x16F8	ALIGN0_INT_MSK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							err_full_mask	err_lane3_mask	err_lane2_mask	err_lane1_mask	err_lane0_mask
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	err_full_mask	MIPI_ALIGN FIFO interrupt enable 0: masked 1: enabled
[3]	RW	err_lane3_mask	MIPI_ALIGN lane 3 interrupt enable 0: masked 1: enabled

[2]	RW	err_lane2_mask	MIPI_ALIGN lane 2 interrupt enable 0: masked 1: enabled
[1]	RW	err_lane1_mask	MIPI_ALIGN lane 1 interrupt enable 0: masked 1: enabled
[0]	RW	err_lane0_mask	MIPI_ALIGN lane 0 interrupt enable 0: masked 1: enabled

Contents

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10 ISP

10.1 Introduction

The image signal processor (ISP) module of Hi3516C V300 supports standard sensor picture data processing. The ISP module provides basic functions such as automatic white balance (AWB), automatic exposure (AE), demosaic, defect pixel correction (DPC), and lens shading correction (LSC) as well as advanced functions such as wide dynamic range (WDR), dynamic range compression (DRC), and denoising. The picture processing functions supported by the ISP module of Hi3516C V300 are as follows:

- Black level correction (BLC)
- Static and dynamic DPC and defect pixel cluster correction
- Bayer denoising
- Fixed pattern noise (FPN) removal
- Advanced demosaic
- Chromatic abberation correction (CAC)
- Gamma correction
- DRC
- Sensor built-in WDR
- Two-in-one WDR
- AWB
- AE
- Automatic focus (AF)
- 3A (AE, AF, AWB) statistics output
- Lens shading correction
- Lens distortion correction
- Picture sharpening
- Digital image stabilization (DIS)

- Automatic anti-fog
- Color management and enhancement

The processing capability of the ISP module is as follows:

- Maximum 14-bit Bayer data input
- Maximum picture resolution of 2048 x 2048
- Minimum picture resolution of 120 x 120
- Minimum horizontal blanking region of 64 pixels
- Minimum vertical blanking region of 24 lines

10.2 Overview

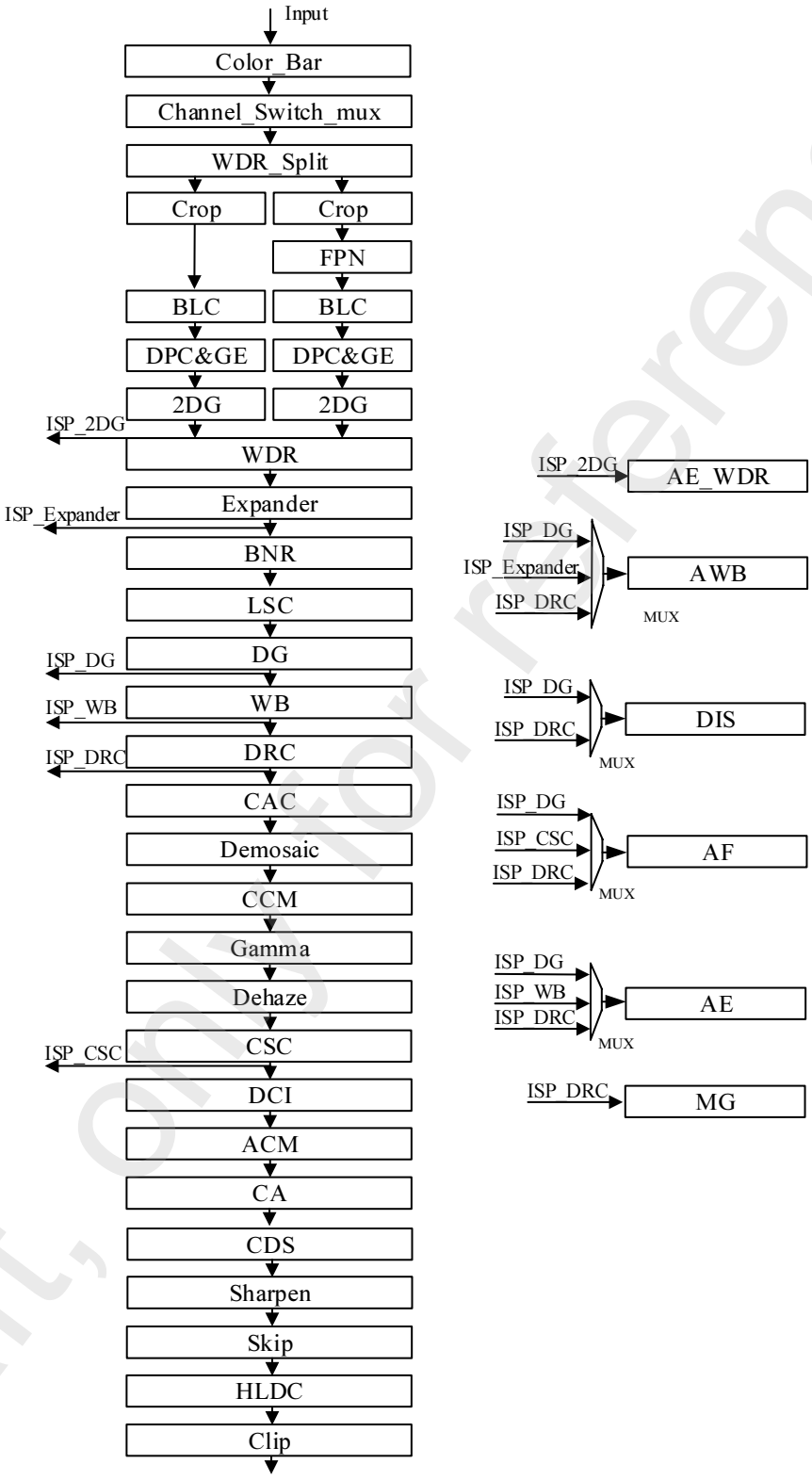
Functional Block Diagram

Figure 10-1 shows the functional block diagram of the ISP module. ISP_FE mentioned in this document refers to the part before demosaic (excluding demosaic) in the ISP pipeline, and ISP_BE refers to the part after demosaic (including demosaic) in the ISP pipeline.

NOTE

In this document, *U**.* and *S**.* represent the unsigned number and the signed number respectively. For example, U8.8 indicates that the data is an unsigned number consisting of an 8-bit integral part and an 8-bit decimal part. S8.8 indicates that the data is a signed number consisting of an 8-bit integral part (including a sign bit) and an 8-bit decimal part.

Figure 10-1 Functional block diagram of the ISP module



Operating Mode

The ISP module supports the following operating modes:

- Maximum 14-bit raw RGB Bayer data input

  When the input data width is less than 14 bits, the upper bits need to be aligned and the lower bits need to be stuffed with 0s. In this mode, any sequence of the R, Gr, Gb, and B components is supported. The registers ISP_FE_CTRL_F and ISP_BE_CTRL_F need to be matched.

- Sensor built-in WDR

  This mode supports maximum 16 bits RGB Bayer compressed raw data input.

- Two-in-one WDR

- Luminance single-component mode

  In this mode, ISP_SKIP_C_CFG in the skip module needs to be set to **0x00000000** so that the C (U and V) component is discarded and the ISP module outputs only the Y component picture data.

- External ISP mode

Table 10-1 describes the key parameters in external ISP mode.

Table 10-1 Key parameters in external ISP mode

Parameter	Description
BUF_MODE (0x0070)	Register in the video capture (VICAP) module, indicating the line_buf input data mode 0: raw data 1: YUV422
ISP_SEL[6:4] (0x0050)	Register in the VICAP module, indicating the ISP_BE input data selection 000: ISP_BE connects to ISP_FE (RAW input) 001: ISP_BE connects to LINE_BUF (YUV input) 011: ISP_BE connects to SRC0 (for debugging) 100: ISP_BE connects to SRC1 (for debugging) 101: ISP_BE connects to SRC2 (for debugging) 110: ISP_BE connects to SRC3 (for debugging) Other values: reserved

In external ISP mode, the video interface VICAP register ISP_SEL bit[6:4] needs to be set to **0x1** to mask the raw field module, and BUF_MODE in the VICAP module needs to be set to **0x1** so that the VICAP line_buf input data is in YUV422 format.

- Adjustable module position statistics

  The positions of the AE, AWB, AF, and DIS modules are adjustable.

Table 10-2 describes key module position adjustment parameters.

Table 10-2 Key statistics module position adjustment parameters

Parameter	Description
ISP_SEL bit[16] (Offset address: 0x00050)	AF position adjustment register 0: The AF module is within the ISP FE module. 1: The AF module is within the ISP BE module and in the Y field after the CSC module.
ISP_FE_MODULE_POS bit[6] (Offset address: 0x20090)	DIS position adjustment register 0: The DIS module is after the digital gain (DG) module. 1: The DIS module is after the DRC Dither module.
ISP_FE_MODULE_POS bit[4] (Offset address: 0x20090)	AF position adjustment register 0: The AF module is after the digital gain (DG) module. 1: The AF module is after the DRC Dither module.
ISP_FE_MODULE_POS bit[3:2] (Offset address: 0x20090)	AWB position adjustment register 00: The AWB module is after the DG module. 01: The AWB module is after the Expander module. 10: The AWB module is after the DRC Dither module.
ISP_FE_MODULE_POS bit[1:0] (Offset address: 0x20090)	AE position adjustment register 00: The AE module is after the DG module. 01: The AE module is after the white balance (WB) module. 10: The AE module is after the DRC Dither module.

Memory Read and Write Solutions

Table 10-3 describes the memory address mapping of each module.

Table 10-3 Memory address mapping of each module

Range of the Memory Offset Address	Module to Which the Memory Belongs
0x12288–0x1228C	AF
0x22080–0x220AC	AE
0x22180–0x2218C	AWB
0x22488–0x2249C	DIS
0x22590–0x2259C	MG
0x23080–0x2309C	LSC
0x23988–0x2399C	GE
0x23A80–0x23A8C	FPN

Range of the Memory Offset Address	Module to Which the Memory Belongs
0x23C80–0x23C8C	DPC
0x25480–0x254AC 0x25580–0x255AC	BNR
0x26080–0x2608C	WDR
0x26280–0x262AC	DRC
0x26880–0x2688C	Expander
0x26E80–0x26E8C	WDR_Split
0x29080–0x290AC	AEWDR0
0x29180–0x2918C	AEWDR1
0x45680–0x4569C	Demosaic
0x46780–0x467AC	Dehaze
0x46280–0x462BC	Dehaze
0x46A80–0x46A8C	Gamma
0x47080–0x4708C	CA

As described in Table 10-3, the ISP memory is indirectly read or written. Within the range of the memory address segments, the read data register (RDATA), read address register (RADDR), write data register (WDATA), and write address register (WADDR) are provided.

To read the memory, perform the following steps:

Step 1 Write the start address of the data to be read in the memory to the read address register (RADDR).

Step 2 Read the read data register (RDATA) continuously. The address automatically increases by 1 in the logic each time the register is read.

----End

To write to the memory, perform the following steps:

Step 1 Write the start address of data in the memory to the write address register (WADDR).

Step 2 Write data to the write data register (WADDR) continuously. The address automatically increases by 1 in the logic each time the register is written.

----End

10.3 Interrupt System

Function Description

The ISP module has 13 hardware interrupt events. For details, see Table 10-4.

Table 10-4 Interrupt indicator register

Offset Address	Event	Bit	Description
0x200F0	aewdr_int	8	AEWDR statistics completion interrupt
	dis_int	7	DIS statistics completion interrupt
	awb_int	5	AWB statistics completion interrupt
	ae_int	4	AE statistics completion interrupt
	fstart_delay	3	Configurable ISP FE trigger position interrupt. The trigger position is specified by ISP_FE_FSTART_DELAY (0x20094). Any trigger position in the unit of line in the input picture valid region is supported.
	cfg_loss	2	ISP FE register configuration loss interrupt
	update_cfg	1	ISP FE register update interrupt
	fstart	0	ISP FE frame start interrupt
0x400F0	acm_para_finish	16	ACM lookup table load completion interrupt
	fstart_delay	3	Configurable trigger position interrupt. The trigger position is specified by ISP_BE_FSTART_DELAY (0x40094). Any trigger position in the unit of line in the input picture valid region is supported.
	cfg_loss	2	ISP FE register configuration loss interrupt
	update_cfg	1	ISP FE register update interrupt
	fstart	0	ISP BE frame start interrupt

Interrupt Timing

The positions of many interrupts are determined by the ISP module switch and register configuration. Figure 10-2 shows the position of each interrupt. Note that the interrupt position is arranged based on the time sequence in a frame. Table 10-5 describes the mapping between the interrupt ID and the interrupt event shown in Figure 10-2.

Figure 10-2 Interrupt timing

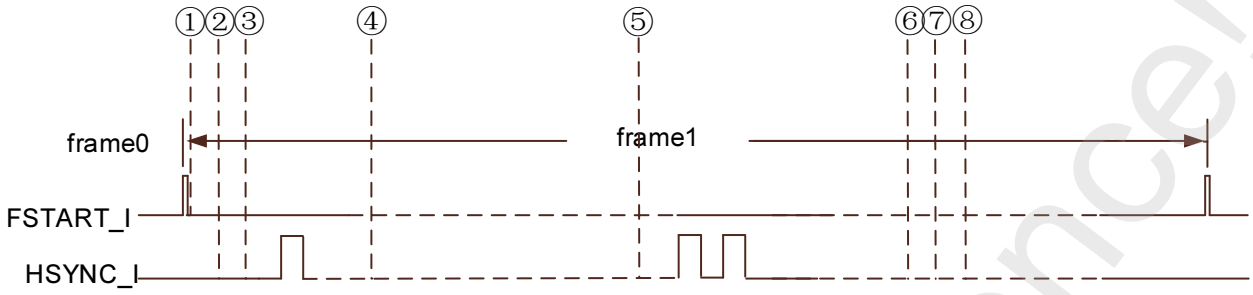


Table 10-5 Mapping between the interrupt ID and the interrupt event

No.	Interrupt Event
①	fstart(ISP_FE)/fstart(ISP_BE)
②	cfg_loss(ISP_FE)/cfg_loss(ISP_BE) update_cfg(ISP_FE) /update_cfg(ISP_BE)
③	acm_para_finish
④	fstart_delay(ISP_FE)/ fstart_delay (ISP_BE)
⑤	dis_int
⑥	awb_int
⑦	ae_int
⑧	aewdr_int

10.4 Module Functions

Color_bar

The color_bar module supports the following five picture types:

- Pure color picture configured by ISP_COLORBAR_RBACKGND[rbackgnd], ISP_COLORBAR_GBACKGND[gbackgnd], and ISP_COLORBAR_BBACKGND[bbackgnd]

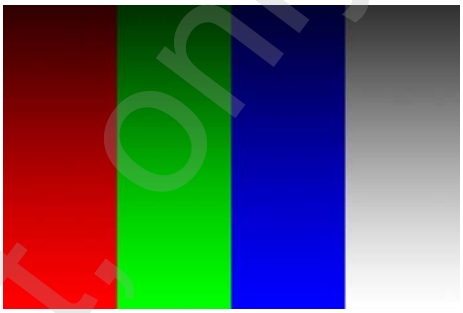
Figure 10-3 Pure color picture

- Picture consisting of four horizontal color stripes. The luminance from left to right is variable and the start value and increment are configurable.

Figure 10-4 Picture consisting of four horizontal color stripes

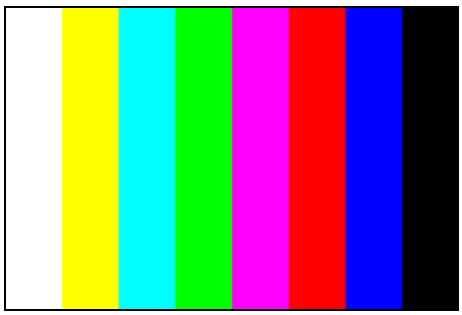
- Picture consisting of four vertical color stripes. The luminance from top to bottom is variable and the start value and increment are configurable.

Figure 10-5 Picture consisting of four vertical color stripes



- Picture consisting of eight vertical color stripes. The luminance is configured by ISP_COLORBAR_RBACKGND[rbackgnd], ISP_COLORBAR_GBACKGND[gbackgnd], and ISP_COLORBAR_BBACKGND[bbackgnd].

Figure 10-6 Picture consisting of eight vertical color stripes



- Picture with a rectangular pure color target area on the pure color background. The background color is configured by ISP_COLORBAR_RBACKGND[rbackgnd], ISP_COLORBAR_GBACKGND[gbackgnd], and ISP_COLORBAR_BBACKGND[bbackgnd]. The color of the target area is configured by ISP_COLORBAR_RFOREGND[rforegnd], ISP_COLORBAR_GFOREGND[gforegnd], and ISP_COLORBAR_BFOREGND[bforegnd].

Figure 10-7 Picture with a rectangular pure color target area on the pure color background

WDR_Split

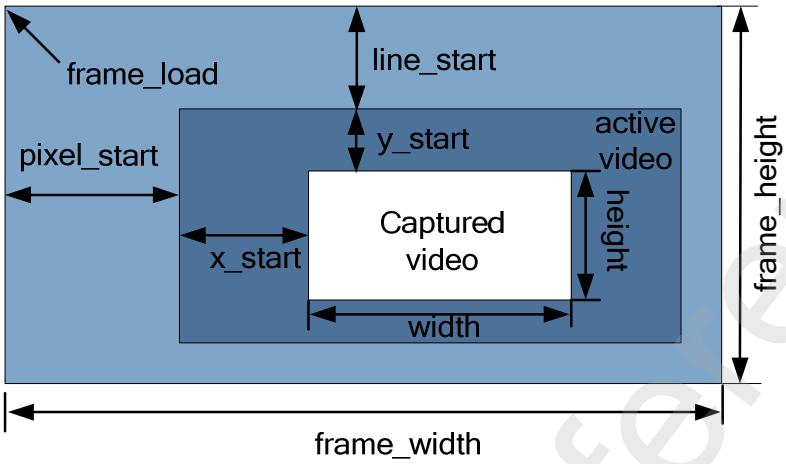
This module splits the data that is output by different sensors and has a higher bit width into data with lower bit width so that the split data can be processed by the ISP.

Crop

The crop module crops the input picture. The actual displayed view area always falls within the valid video range. That is, compared with the valid video area, the actual displayed view area shrinks.

As shown in Figure 10-8, the crop module crops the valid picture area by configuring ISP_CROP0_START[y_start], ISP_CROP0_START[x_start], ISP_CROP0_SIZE[height], and ISP_CROP0_SIZE[width].

Figure 10-8 Relationship between the valid picture area and the horizontal/vertical blanking region



FPN

The FPN module corrects the sensor input picture based on the calibrated black frame or black line to remove the FPNs of the sensor.

The FPN module supports calibration and correction in frame mode and line mode. This module needs to be enabled if the FPNs of the connected sensor are obvious, and does not need to be enabled if the the FPNs of the connected sensor are not obvious.

The two-in-one WDR mode does not support FPN calibration.

BLC

The BLC module provides the sensor-related BLC function, and configures the offsets of the R, Gr, Gb, and B components.

DPC

The DPC module detects and corrects static and dynamic defect pixels.

You can detect the static defect pixels of the sensor by using software and hardware, and store the coordinates of all the defect pixels in the external memory. Then the ISP corrects the defect pixels based on the coordinates. This module supports the detection and correction of at most 2048 static defect pixels, and supports defect pixel cluster correction within 2 x 2 pixels in a single channel.

This module automatically detects and corrects dynamic defect pixels in real time based on the configured threshold, and supports defect pixel cluster correction within 2 x 2 pixels in a single channel.

The static defect pixel correction can be replaced with the dynamic defect pixel correction. However, to avoid definition degradation caused by misjudgment during dynamic detection, you are advised to first use the static defect pixel correction function and then set harsh dynamic defect pixel detection and correction conditions to implement defect pixel correction by combining static and dynamic defect pixel correction.

GE

The GE module equalizes the Gb and Gr channels when imbalance occurs and improves the picture quality in some scenarios. The GE statistics are zoned Gr/Gb average value statistics.

This module supports a maximum of 17 x 15 blocks and a minimum of 1 x 1 block. Each block can output the average values of the Gr and Gb components (average R/Gr/Gb/B). Table 10-6 describes the mapping between the address and read data of bloc statistics. *m* indicates the number of horizontal blocks and *n* indicates the number of vertical blocks.

Table 10-6 GE zone statistics

Memory Address	Zone	Memory Read Data		
		[31:28]	[27:14]	[13:0]
0	0	0	Average Gr	Average Gb
1	1	0	Average Gr	Average Gb
2	2	0	Average Gr	Average Gb
3	3	0	Average Gr	Average Gb
…				
m x n − 3	m x n − 3	0	Average Gr	Average Gb
m x n − 2	m x n − 2	0	Average Gr	Average Gb
m x n − 1	m x n − 1	0	Average Gr	Average Gb

WDR

The WDR module provides the frame merging WDR function. Details in bright and dark regions can still be observed in WDR scenarios.

Expander

The expander module is enabled only in sensor built-in WDR mode. This module decompresses the sensor built-in compressed non-linear data into linear data. The used lookup table (LUT) contains 129 points with 15-bit precision. The points between two nodes can be obtained through interpolation. The generated LUT depends on the corresponding sensor model.

BNR

The BNR module implements picture denoising in the Bayer domain. It aims to retain details while implementing denoising. This module can eliminate noises of the sensor based on the noise model provided by the user.

LSC

The LSC module implements lens shading correction. Because of the optical characteristics of the lens, the luminous intensity of the edge area is lower than that of the central area in a sensor picture. Therefore, gain compensation based on pixel position is required.

This module provides the gains of four components (R, Gr, Gb, and B), and each gain is represented by a 13-bit unsigned number (3-bit integral part and 10-bit decimal part). The picture is divided into 16 x 16 blocks that are symmetric in the layout but differ in the block size. The closer the block is to the picture center, the larger the block size; the closer the block is to the four edges, the smaller the block size. The gains of the window vertex are provided. Other values are obtained through interpolation. The gain obtained after interpolation is multiplied by the corresponding pixel point value, and the compensated picture data is output.

DG

The DG module provides the digital gain, and configures the offsets of the R, Gr, Gb, and B components (U8.8 precision).

AE

The AE module collects AE statistics. Software adjusts the sensor based on statistics to implement AE. The AE statistics includes the block R/Gr/Gb/B average value statistics, global weighted R/Gr/Gb/B average value, and 1024-segment histogram statistics.

- AE zoned statistics

  The AE module supports a maximum of 17 x 15 blocks and a minimum of 1 x 1 block. Each block can output the average values of the R, Gr, Gb, and B components (average R/Gr/Gb/B). Table 10-7 describes the mapping between the address and read data of block statistics. *m* indicates the number of horizontal blocks and *n* indicates the number of vertical blocks.

Table 10-7 AE zone statistics

Memory Address	Zone	Memory Read Data			
		MEM_AVER_R_GR [31:16]	MEM_AVER_R_GR [15:0]	_MEM_AVER_GB_B [31:16]	_MEM_AVER_GB_B [15:0]
0	0	Average R	Average Gr	Average Gb	Average B
1	1	Average R	Average Gr	Average Gb	Average B
2	2	Average R	Average Gr	Average Gb	Average B
3	3	Average R	Average Gr	Average Gb	Average B
…					
m x n − 3	m x n − 3	Average R	Average Gr	Average Gb	Average B
m x n − 2	m x n − 2	Average R	Average Gr	Average Gb	Average B

Memory Address	Zone	Memory Read Data			
		MEM_AVER_R_GR [31:16]	MEM_AVER_R_GR [15:0]	_MEM_AVER_GB_B [31:16]	_MEM_AVER_GB_B [15:0]
m x n − 1	m x n − 1	Average R	Average Gr	Average Gb	Average B

- Weighted AE global statistics

  The AE global statistics are basically the same as the AE zoned statistics. The AE module provides four types of global statistics. For details, see the ISP_AE_TOTAL_R_AVER, ISP_AE_TOTAL_GR_AVER, ISP_AE_TOTAL_GB_AVER, and ISP_AE_TOTAL_B_AVER registers. The physical meanings of the four types of global statistics are the same as those of the zoned statistics.

- Weighted AE histogram statistics

  The AE module provides the 1024-segment histogram statistics. Table 10-8 describes the mapping between the address and read data of the histogram statistics for zone 0−1023.

Table 10-8 AE histogram statistics

Memory Address	Zone	Memory Read Data	
		[31:29]	[28:0]
0	0	0	Number of pixels whose value is 0
1	1	0	Number of pixels whose value is 1
2	2	0	Number of pixels whose value is 2
3	3	0	Number of pixels whose value is 3
…			
1022	1022	0	Number of pixels whose value is 1022
1023	1023	0	Number of pixels whose value is 1023

AF Statistics

The AF module collects statistics on picture definition evaluation information and implements AF. The number of picture blocks is configurable. This module supports a maximum of 17 x 15 blocks. The minimum block size is 32 x 32 and the maximum block size is 511 x 511. The definition evaluation information about each zone is provided.

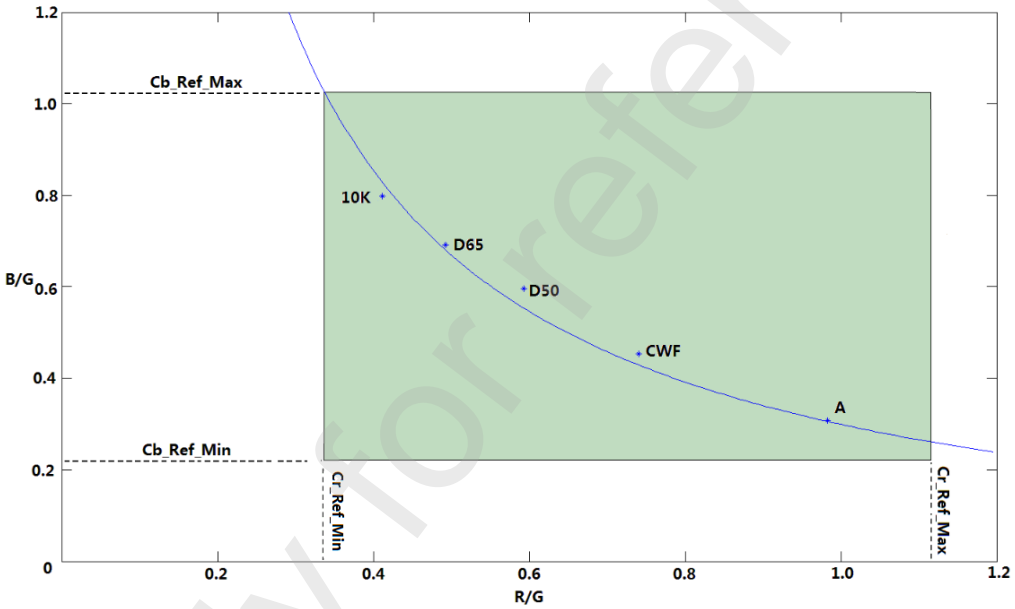
AWB

The AWB statistics includes the global statistics and zoned statistics.

- Global statistics: average values of the R, G, and B components for an entire picture, number of valid statistical points, and number of statistical points that exceed the limit
- Zoned statistics: average values of the R, G, and B components for each block (a maximum of 32 x 32 blocks are supported), number of valid statistical points, and number of statistical points that exceed the limit

  The valid AWB statistical points must meet the configured RGB upper limit and lower limit requirements described in ISP_AWB_THD_MIN and ISP_AWB_THD_MAX. In addition, the pixel point color must fall within the range of the configured color space of the valid pixel. As shown in Figure 10-9, the green area indicates the color range of the valid pixel.

Figure 10-9 Color space of valid AWB pixel



The valid pixel area of AWB statistics is a hexagon. The left, right, top, and bottom boundaries are determined by **cr_ref_min**, **cr_ref_max**, **cb_ref_min**, and **cb_ref_max**. The four parameters indicate the maximum and minimum values of R/G and B/G. The two hypotenuses of the valid area are determined by configuring the slope and intercept. ISP_AWB_TOP_K and ISP_AWB_TOP_B determine the hypotenuse on the upper right part, and ISP_AWB_BOT_K and ISP_AWB_BOT_B determine the hypotenuse on the lower left part.

- AWB zoned statistics

The AWB module supports a maximum of 32 x 32 blocks. Each block can output the average values of the R, G, and B components (average R/G/B). The width of the pixel points involved in statistics is 16 bits. If the width of the input picture data is greater than 16 bits, the pixel data needs to be truncated based on the size configured in ISP_AWB_BITMOVE. There are three types of statistics on the statistical points of a block: number of valid statistical points (Count All). The preceding statistics are normalized to 16 bits based on the picture size. Table 10-9 describes the mapping between the address and read data of block statistics.

Table 10-9 AWB zoned statistics

Memory Address	Zone	Memory Read Data	
		[31:16]	[15:0]
0	0	Average G	Average R
1	0	Count All	Average B
2	1	Average G	Average R
…			
3 x *m* x *n* − 2	*m* x *n*	Average G	Average R
3 x *m* x *n* − 1	*m* x *n*	Count All	Average B

- AWB global statistics

  The AWB global statistics are basically the same as the AWB zoned statistics. The AWB module provides four types of global statistics. For details, see the ISP_AWB_AVG_R, ISP_AWB_AVG_G, ISP_AWB_AVG_B, and ISP_AWB_CNT_ALL registers. The physical meanings of the six types of global statistics are the same as those of the zoned statistics.

DIS

The DIS module compares the two frames, finds the difference between them, and calculates the offset between frames. This module outputs the horizontal offset Offset_X and vertical offset Offset_Y. The statistics of nine windows are used for horizontal and vertical offset calculation. Each window outputs three result offsets, detail delta, and sum of absolute difference (SAD). The offset (in pixel) ranges from −64 to +64. Software calculates the Offset_X and Offset_Y of the entire picture based on the statistics of nine windows. The back-end module controls the position of the cropping window and crops the picture based on Offset_X and Offset_Y to eliminate picture jitter.

WB

The WB module provides the white balance function, and configures the gains of the R, Gr, Gb, and B components (U4.8 precision).

DRC

The DRC module adjusts the display dynamic range of the picture so that the picture display effect on the display device is consistent with the picture observed by human eyes.

CAC

The CAC module is used to correct the axial chromatic aberration (purple fringing) and lateral chromatic aberration (color fringing on opposite sides of an object with different colors) introduced by the lens.

Demosaic

The demosaic module converts the raw picture in Bayer format into the RGB picture.

This module analyzes the characteristics of the internal picture edge, uses pixel relevance interpolation, and effectively suppresses the anti-false color while ensuring high resolution and definition.

CCM

The color correction matrix (CCM) module implements linear correction of the color space by using the standard 3 x 3 matrix and vector offset.

The firmware dynamically calculates the CCM coefficients of the current picture based on the several pre-calculated groups of CCM coefficients and picture color temperature. The firmware can also use the CCM to dynamically adjust the saturation based on the luminance of the current picture.

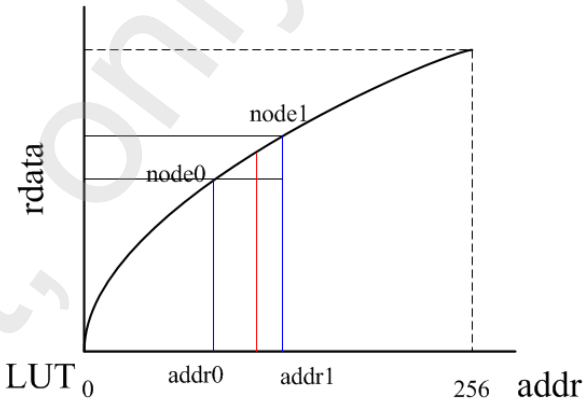
$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} coef00 & coef01 & coef02 \\ coef10 & coef11 & coef12 \\ coef20 & coef21 & coef22 \end{pmatrix} \times \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

In the preceding formula, R, G, and B indicate the input data, and coef is a 3 x 3 configurable matrix coefficient. The coefficients are 15-bit numbers in S5.10 format.

Gamma

The gamma module applies to the three color channels (R, G, and B) and outputs the gamma adjustment result. This module adjusts the luminance based on the gamma curve. The three color channels (R, G, and B) are adjusted according to the gamma curve.

Figure 10-10 Gamma curve



The gamma curve consists of 257 nodes (node 0 to node 256). The curve value corresponding to each node is a 12-bit unsigned number. The points between two nodes can be obtained through interpolation. The curve value of node 0 (gamma[0]) is 0 and the curve value of node 256 (gamma[256]) is 0xFFF.

Dehaze

The dehaze module provides the powerful zoned anti-fog function and improves video contrast and definition in the haze scenario.

This module analyzes the picture characteristics of each region, obtains the contrast specifications of each region, and implements pixel enhancement in each region. The enhancement strength of a pixel depends on the contrast specifications of the region this pixel belongs to and those of the neighboring regions.

CSC

The CSC module converts the {R, G, B} input into {Y, U, V} by using the standard 3 x 3 matrix and vector offset.

$$\begin{pmatrix} Y \\ U \\ V \end{pmatrix} = \begin{pmatrix} coef00 & coef01 & coef02 \\ coef10 & coef11 & coef12 \\ coef20 & coef21 & coef22 \end{pmatrix} \times \begin{pmatrix} R \\ G \\ B \end{pmatrix} + \begin{pmatrix} out\_dc0 \\ out\_dc0 \\ out\_dc0 \end{pmatrix}$$

The parameters can be changed based on format conversion requirements.

DCI

The DCI module dynamically improves the picture contrast, and automatically adjusts picture luminance and contrast based on the picture luminance statistics to resolve issues (for example, the picture is too dark or too bright, and the contrast is too high or too low) so that excellent display effect can be achieved on the display device.

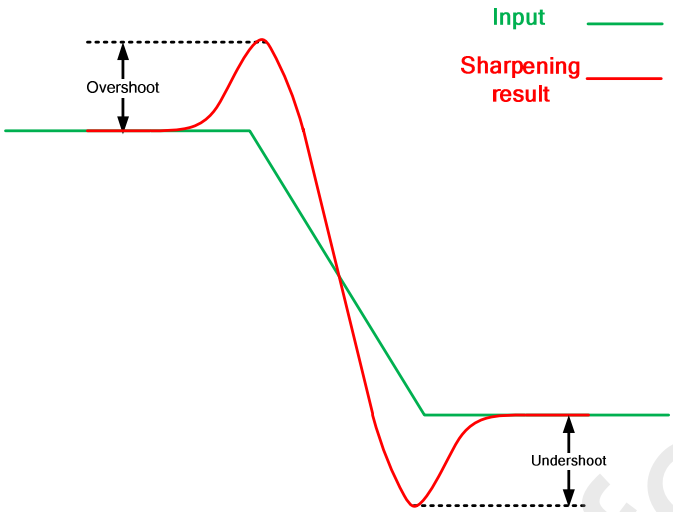
ACM

The ACM implements automatic color management, corrects hue offset, compensates for saturation loss during video transfer and the performance difference between color gamuts, and enhances specific colors such as the complexion, green, and blue based on user preference and style.

Sharpen

The sharpen module implements picture sharpening to improve picture definition. The sharpening strength can be adjusted by configuring the control parameters **edge_amt** and **sharp_amt**. Note that noises may be amplified if the sharpening strength is too high. Software adjusts parameter configurations based on the ISO value to achieve a balance between the definition and noise suppression while improving the visual effect of the picture.

Figure 10-11 Overshoot and undershoot occurrence during sharpening



In addition, white borders and black borders may appear due to the large positive and negative edge amplification caused by sharpening, as shown in Figure 10-11. The white borders and black borders can be suppressed by adjusting the overshoot and undershoot control parameters.

CDS

The CDS module converts the YUV444 into YUV422 or YUV420, and implements multi-order horizontal chrominance filtering. When the YUV420 output is required, this module implements average down sampling in the vertical direction of the chrominance. The visual loss caused by picture conversion can be minimized by setting the filtering parameters to appropriate values.

CA

This module allows you to adjust the chrominance based on the luminance information. During CSC in the YUV space, a pixel (Y, U, V) can be mapped to another pixel (Y', U', V') by using the following formula:

$$Y' = Y$$
$$U' = aU$$
$$V' = aV$$

a is the conversion factor. This formula can adjust the saturation of the pixel while retaining constant luminance to some extent. By associating the conversion factor *a* and the pixel luminance Y, you can adjust the saturation according to the variance of the luminance. In this way, partial saturation adjustment can be implemented.

HLDC

The HLDC module provides lens-induced distortion correction function and supports barrel and pincushion correction.

The maximum correct range is –20% to +20%. A negative value indicates pincushion correction, and a positive value indicates barrel correction.

10.5 Register Summary

Table 10-10 describes ISP registers.

Table 10-10 Summary of ISP registers (base address: 0x1138_0000)

Offset Address	Register	Description	Page
0x12200	ISP_AF_CFG	AF control register	10-57
0x12210	ISP_AF_ZONE	AF block configuration register	10-60
0x12214	ISP_AF_CROP_START	AF picture crop start coordinate register	10-61
0x12218	ISP_AF_CROP_SIZE	AF picture crop size register	10-61
0x1221C	ISP_AF_MEAN_THRES	AF median filtering threshold register	10-62
0x12220	ISP_AF_IIRG0	AF IIR filtering parameter register 0	10-62
0x12224	ISP_AF_IIRG1	AF IIR filtering parameter register 1	10-62
0x12228	ISP_AF_IIRG2	AF IIR filtering parameter register 2	10-63
0x1222C	ISP_AF_IIRG3	AF IIR filtering parameter register 3	10-64
0x12230	ISP_AF_IIRG4	AF IIR filtering parameter register 4	10-64
0x12234	ISP_AF_IIRG5	AF IIR filtering parameter register 5	10-65
0x12238	ISP_AF_IIRG6	AF IIR filtering parameter register 6	10-65
0x1223C	ISP_AF_IIRPL	AF IIR filtering preset register	10-66
0x12240	ISP_AF_SHIFT	AF IIR filtering shift parameter register	10-66
0x12250	ISP_AF_FIRH0	AF FIR filtering parameter register 0	10-68
0x12254	ISP_AF_FIRH1	AF FIR filtering parameter register 1	10-68
0x12258	ISP_AF_FIRH2	AF FIR filtering parameter register 2	10-69
0x1225C	ISP_AF_FIRH3	AF FIR filtering parameter register 3	10-70
0x12260	ISP_AF_FIRH4	AF FIR filtering parameter register 4	10-70
0x12278	ISP_AF_ACC_SHIFT	AF cumulative statistics shift register	10-71
0x1227C	ISP_AF_CNT_SHIFT	AF count statistics shift register	10-71

Offset Address	Register	Description	Page
0x12288	ISP_AF_STAT_IND_RADDR	Statistics indirect read address register for AF blocks	10-72
0x1228C	ISP_AF_STAT_IND_RDATA	Statistics indirect read data register for AF blocks	10-72
0x122E4	ISP_AF_CTRL_I	Immediate update control register	10-73
0x122EC	ISP_AF_UPDATE	Configuration update register	10-74
0x122F0	ISP_AF_SIZE	AF picture size register	10-74
0x12300	ISP_AF_IIRTHRE	AF IIR filtering threshold register	10-74
0x12304	ISP_AF_IIRGAIN	AF IIR filtering gain register	10-75
0x12308	ISP_AF_IIRSLOPE	AF IIR filtering slope register	10-75
0x1230C	ISP_AF_IIRDILATE	AF IIR filtering dilate register	10-76
0x12310	ISP_AF_FIRTHRE	AF FIR filtering threshold register	10-77
0x12314	ISP_AF_FIRGAIN	AF FIR filtering gain register	10-78
0x12318	ISP_AF_FIRSLOPE	AF FIR filtering slope register	10-78
0x12320	ISP_AF_IIRTHRE_CORING	AF IIR filtering coring threshold register	10-78
0x12324	ISP_AF_IIRPEAK_CORING	AF IIR filtering coring peak value register	10-79
0x12328	ISP_AF_IIRSLOPE_CORING	AF IIR filtering coring slope register	10-79
0x12330	ISP_AF_FIRTHRE_CORING	AF FIR filtering coring threshold register	10-80
0x12334	ISP_AF_FIRPEAK_CORING	AF FIR filtering coring peak value register	10-80
0x12338	ISP_AF_FIRSLOPE_CORING	AF FIR filtering coring slope register	10-81
0x12340	ISP_AF_HILIGHT	AF highlight threshold register	10-81
0x12344	ISP_AF_OFFSET	AF offset configuration register	10-82
0x123f0	ISP_AF_INT	AF interrupt indicator register	10-74
0x123f8	ISP_AF_INT_MASK	AF interrupt mask register	10-83
0x20090	ISP_FE_MODULE_POS	ISP internal module position select register	10-83
0x20094	ISP_FE_FSTART_DELAY	ISP adjustable interrupt trigger time configuration register	10-85

Offset Address	Register	Description	Page
0x200A0	ISP_FE_USER_DEFINE0	User-defined register 0	10-85
0x200A4	ISP_FE_USER_DEFINE1	User-defined register 1	10-85
0x200B0	ISP_FE_STARTUP	ISP FE startup indicator register	10-86
0x200F0	ISP_FE_INT	ISP interrupt indicator register	10-86
0x200F8	ISP_FE_INT_MASK	ISP interrupt mask register	10-87
0x201E0	ISP_FE_CTRL_F	ISP common update control register	10-88
0x201E4	ISP_FE_CTRL_I	ISP immediate update control register	10-89
0x201E8	ISP_FE_TIMING_CFG	Output timing configuration register	10-89
0x201EC	ISP_FE_REG_UPDATE	Register update register	10-90
0x20800	ISP_CROP0_CFG	Crop enable register	10-90
0x20808	ISP_CROP0_START	Region 0 crop start position register	10-91
0x2080C	ISP_CROP0_SIZE	Region 0 crop size register	10-91
0x20820	ISP_DRC_DITHER	ISP DRC dither register	10-92
0x20830	ISP_INPUT_MUX	ISP internal module position select register	10-93
0x20A00	ISP_COLORBAR_CFG	Color bar control register	10-83
0x20A10	ISP_COLORBAR_PATTERN	Color bar type register	10-95
0x20A14	ISP_COLORBAR_RBACKGND	Color bar background color register	10-95
0x20A18	ISP_COLORBAR_GBACKGND	Color bar background color register	10-96
0x20A1C	ISP_COLORBAR_BBACKGND	Color bar background color register	10-96
0x20A20	ISP_COLORBAR_RFOREGND	Color bar foreground color register	10-97
0x20A24	ISP_COLORBAR_GFOREGND	Color bar foreground color register	10-97
0x20A28	ISP_COLORBAR_BFOREGND	Color bar foreground color register	10-97
0x20A2C	ISP_COLORBAR_INIT	Color bar initial value register	10-98
0x20A30	ISP_COLORBAR_GRAD	Color bar increasing value register	10-98

Offset Address	Register	Description	Page
0x20A34	ISP_COLORBAR_POS1	Color bar rectangle coordinate register	10-99
0x20A38	ISP_COLORBAR_POS2	Color bar rectangle coordinate register	10-99
0x20A3C	ISP_COLORBAR_RGGB	RGGB sequence register	10-100
0x20AF0	ISP_COLORBAR_SIZE	Color bar picture size register	10-100
0x21000	ISP_BLC_CFG	BLC control register	10-95
0x21010	ISP_BLC_OFFSET1	BLC offset register 1	10-101
0x21014	ISP_BLC_OFFSET2	BLC offset register 2	10-101
0x21100	ISP_BLC_CFG	BLC control register	10-95
0x21110	ISP_BLC0_OFFSET1	BLC0 offset register 1	10-101
0x21114	ISP_BLC0_OFFSET2	BLC0 offset register 2	10-101
0x21118	ISP_BLC1_OFFSET1	BLC1 offset register 1	10-102
0x2111c	ISP_BLC1_OFFSET2	BLC1 offset register 2	10-102
0x21200	ISP_WB_CFG	WB control register	10-103
0x21204	ISP_WB_BLC_CFG	WB black level offset enable register	10-103
0x21210	ISP_WB_GAIN1	WB gain (R & Gr) register	10-104
0x21214	ISP_WB_GAIN2	WB gain (B & Gb) register	10-104
0x21218	ISP_WB_BLC_OFFSET1	WB black level offset register 1	10-105
0x2121C	ISP_WB_BLC_OFFSET2	WB black level offset register 2	10-105
0x21300	ISP_DG_CFG	DG control register	10-106
0x21304	ISP_DG_BLC_CFG	DG black level enable control register	10-106
0x21310	ISP_DG_GAIN1	DG gain (R & Gr) register	10-107
0x21314	ISP_DG_GAIN2	DG gain (B & Gb) register	10-107
0x21318	ISP_DG_BLC_OFFSET1	DG black level offset register 1	10-108
0x2131C	ISP_DG_BLC_OFFSET2	DG black level offset register 2	10-108
0x21C00	ISP_2DG_CFG	2DG control register	10-109
0x21C04	ISP_2DG_BLC_CFG	2DG black level control register	10-109
0x21C10	ISP_2DG_0_GAIN1	Channel 0 DG gain (R, Gr) register	10-110
0x21C14	ISP_2DG_0_GAIN2	Channel 0 DG gain (B, Gb) register	10-110

Offset Address	Register	Description	Page
0x21C18	ISP_2DG_0_BLC_OFFSET1	Channel 0 black level offset register 1	10-111
0x21C1C	ISP_2DG_0_BLC_OFFSET2	Channel 0 black level offset register 2	10-111
0x21C20	ISP_2DG_1_GAIN1	Channel 1 DG gain (R, Gr) register	10-112
0x21C24	ISP_2DG_1_GAIN2	Channel 1 DG gain (B, Gb) register	10-112
0x21C28	ISP_2DG_1_BLC_OFFSET1	Channel 1 black level offset register 1	10-113
0x21C2C	ISP_2DG_1_BLC_OFFSET2	Channel 1 black level offset register 2	10-113
0x22000	ISP_AE_CFG	AE enable register	10-114
0x22010	ISP_AE_ZONE	AE block configuration register	10-114
0x22014	ISP_AE_SKIP_CRG	AE point select configuration register	10-115
0x22018	ISP_AE_TOTAL_STAT	Selected point total number register in a picture frame during 1024-segment histogram statistics	10-116
0x2201C	ISP_AE_COUNT_STAT	Selected point total weight register in a picture frame during 1024-segment histogram statistics	10-117
0x22020	ISP_AE_TOTAL_R_AVER	R component average value register in a picture frame during average value statistics	10-117
0x22024	ISP_AE_TOTAL_GR_AVER	Gr component average value register in a picture frame during average value statistics	10-117
0x22028	ISP_AE_TOTAL_GB_AVER	Gb component average value register in a picture frame during average value statistics	10-118
0x2202C	ISP_AE_TOTAL_B_AVER	B component average value register in a picture frame during average value statistics	10-118
0x22030	ISP_AE_HIST_HIGH	Histogram statistics high register	10-119
0x22040	ISP_AE_BITMOVE	AE pixel shift value register	10-119
0x22044	ISP_AE_OFFSET_R	R component black level offset register	10-119
0x22048	ISP_AE_OFFSET_GR	Gr component black level offset register	10-120

Offset Address	Register	Description	Page
0x2204C	ISP_AE_OFFSET_GB	Gb component black level offset register	10-120
0x22050	ISP_AE_OFFSET_B	B component black level offset register	10-121
0x22060	ISP_AE_GAMMA_LIMIT	AE_gamma module shift control register	10-121
0x22070	ISP_AE_FOURPLANEMODE	AE statistics mode select register	10-121
0x22088	ISP_AE_MEM_HIST_RADDR	AE histogram statistics read address register	10-122
0x2208C	ISP_AE_MEM_HIST_RDATA	AE histogram statistics read data register	10-122
0x22098	ISP_AE_MEM_AVER_R_GR_RADDR	AE module R and Gr value statistics read address register	10-123
0x2209C	ISP_AE_MEM_AVER_R_GR_RDATA	AE module R and Gr value statistics read data register	10-123
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0x46734	ISP_DEHAZE_THLD	Dehaze T threshold coefficient configuration register	10-385
0x46738	ISP_DEHAZE_GSTRTH	Dehaze global strength coefficient register	10-386
0x4673C	ISP_DEHAZE_BLTHLD	Dehaze minimum value filtering threshold coefficient configuration register	10-386
0x46740	ISP_DEHAZE_STR_LUT_UPDATE	Dehaze strength table update register	10-387
0x46780	ISP_DEHAZE_MINSTAT_WADDR	Dehaze minimum value statistics write address register	10-387
0x46784	ISP_DEHAZE_MINSTAT_WDATA	Dehaze minimum value statistics write data register	10-387

Offset Address	Register	Description	Page
0x46788	ISP_DEHAZE_MINSTAT_RADDR	Dehaze minimum value statistics read address register	10-388
0x4678C	ISP_DEHAZE_MINSTAT_RDATA	Dehaze minimum value statistics read data register	10-388
0x46790	ISP_DEHAZE_MAXSTAT_WADDR	Dehaze maximum value statistics write address register	10-389
0x46794	ISP_DEHAZE_MAXSTAT_WDATA	Dehaze maximum value statistics write data register	10-389
0x46798	ISP_DEHAZE_MAXSTAT_RADDR	Dehaze maximum value statistics read address register	10-390
0x4679C	ISP_DEHAZE_MAXSTAT_RDATA	Dehaze maximum value statistics read data register	10-390
0x467A0	ISP_DEHAZE_PRESTAT_WADDR	Dehaze previous frame minimum value statistics write address register	10-391
0x467A4	ISP_DEHAZE_PRESTAT_WDATA	Dehaze previous frame minimum value statistics write data register	10-391
0x467A8	ISP_DEHAZE_PRESTAT_RADDR	Dehaze previous frame minimum value statistics read address register	10-392
0x467AC	ISP_DEHAZE_PRESTAT_RDATA	Dehaze previous frame minimum value statistics read data register	10-392
0x467B0	ISP_DEHAZE_LUT_WADDR	Dehaze strength LUT information write address register	10-393
0x467B4	ISP_DEHAZE_LUT_WDATA	Dehaze strength LUT information write data register	10-393
0x467B8	ISP_DEHAZE_LUT_RADDR	Dehaze strength LUT information read address register	10-394
0x467BC	ISP_DEHAZE_LUT_RDATA	Dehaze strength LUT information read data register	10-394
0x467F0	ISP_DEHAZE_SIZE	Dehaze picture size register	10-395
0x46A00	ISP_GAMMA_CFG	Gamma control register	10-395
0x46A10	ISP_GAMMA_LUT_UPDATE	Gamma LUT update register	10-395
0x46A80	ISP_GAMMA_WADDR	Gamma LUT write address register	10-396
0x46A84	ISP_GAMMA_WDATA	Gamma LUT write data register	10-396
0x46A88	ISP_GAMMA_RADDR	Gamma LUT read address register	10-397
0x46A8C	ISP_GAMMA_RDATA	Gamma LUT read data register	10-397

Offset Address	Register	Description	Page
0x47000	ISP_CA_CFG	CA enable register	10-397
0x47010	ISP_CA_CTRL	CA control register	10-398
0x47014	ISP_CA_LUMATH	Luminance threshold register	10-399
0x47018	ISP_CA_DARKCHROMA_TH	Dark region chrominance threshold register	10-399
0x4701C	ISP_CA_SDARKCHROMA_TH	Bright and dark transition region chrominance threshold register	10-399
0x47020	ISP_CA_LLHC_RATIO	Low luminance high saturation region gain register	10-400
0x47024	ISP_CA_ISORATIO	ISO gain register	10-400
0x47028	ISP_CA_LUT_UPDATE	LUT update register	10-401
0x4702C	ISP_CA_YUV2RGB_COEF0	YUV-to-RGB conversion coefficient register 0	10-401
0x47030	ISP_CA_YUV2RGB_COEF1	YUV-to-RGB conversion coefficient register 1	10-402
0x47034	ISP_CA_YUV2RGB_COEF2	YUV-to-RGB conversion coefficient register 2	10-402
0x47038	ISP_CA_YUV2RGB_COEF3	YUV-to-RGB conversion coefficient register 3	10-403
0x4703C	ISP_CA_YUV2RGB_COEF4	YUV-to-RGB conversion coefficient register 4	10-403
0x47040	ISP_CA_YUV2RGB_INDC0	YUV-to-RGB conversion input offset register 0	10-404
0x47044	ISP_CA_YUV2RGB_INDC1	YUV-to-RGB conversion input offset register 1	10-404
0x47048	ISP_CA_YUV2RGB_OUTDC0	YUV-to-RGB conversion output offset register 0	10-405
0x4704C	ISP_CA_YUV2RGB_OUTDC1	YUV-to-RGB conversion output offset register 1	10-405
0x47050	ISP_CA_RGB2YUV_COEF0	RGB-to-YUV conversion coefficient register 0	10-405
0x47054	ISP_CA_RGB2YUV_COEF1	RGB-to-YUV conversion coefficient register 1	10-406
0x47058	ISP_CA_RGB2YUV_COEF2	RGB-to-YUV conversion coefficient register 2	10-406
0x4705C	ISP_CA_RGB2YUV_COEF3	RGB-to-YUV conversion coefficient register 3	10-407

Offset Address	Register	Description	Page
0x47060	ISP_CA_RGB2YUV_COEF4	RGB-to-YUV conversion coefficient register 4	10-407
0x47064	ISP_CA_RGB2YUV_INDC0	RGB-to-YUV conversion input offset register 0	10-408
0x47068	ISP_CA_RGB2YUV_INDC1	RGB-to-YUV conversion input offset register 1	10-408
0x4706C	ISP_CA_RGB2YUV_OUTDC0	RGB-to-YUV conversion output offset register 0	10-409
0x47070	ISP_CA_RGB2YUV_OUTDC1	RGB-to-YUV conversion output offset register 1	10-409
0x47074	ISP_CA_SKINLLUMA_UTH	Complexion judgment dark region U component threshold register	10-409
0x47078	ISP_CA_SKINLLUMA_UYTH	Complexion judgment dark region U corresponding Y component threshold register	10-410
0x4707C	ISP_CA_SKINHLUMA_UTH	Complexion judgment bright region U component threshold register	10-410
0x47080	ISP_CA_GAINLUT_WADDR	Gain LUT write address register	10-411
0x47084	ISP_CA_GAINLUT_WDATA	Gain LUT write data register	10-411
0x47088	ISP_CA_GAINLUT_RADDR	Gain LUT read address register	10-412
0x4708C	ISP_CA_GAINLUT_RDATA	Gain LUT read data register	10-412
0x47110	ISP_CA_SKINHLUMA_UYTH	Complexion judgment bright region U corresponding Y component threshold register	10-413
0x47114	ISP_CA_SKINLLUMA_VTH	Complexion judgment dark region V component threshold register	10-413
0x47118	ISP_CA_SKINLLUMA_VYTH	Complexion judgment dark region V corresponding Y component threshold register	10-414
0x4711C	ISP_CA_SKINHLUMA_VTH	Complexion judgment bright region V component threshold register	10-414
0x47120	ISP_CA_SKINHLUMA_VYTH	Complexion judgment bright region V corresponding Y component threshold register	10-415

Offset Address	Register	Description	Page
0x47124	ISP_CA_SKIN_UVDIFF	Complexion judgment UV component difference register	10-415
0x47128	ISP_CA_SKIN_RATIOTH0	Complexion protection gain threshold register 0	10-415
0x4712C	ISP_CA_SKIN_RATIOTH1	Complexion protection gain threshold register 1	10-416
0x47130	ISP_CA_COLORLLUMA_UTH	Color judgment dark region U component threshold register	10-416
0x47134	ISP_CA_COLORLLUMA_UYTH	Color judgment dark region U corresponding Y component threshold register	10-417
0x47138	ISP_CA_COLORHLUMA_UTH	Color judgment bright region U component threshold register	10-417
0x4713C	ISP_CA_COLORHLUMA_UYTH	Color judgment bright region U corresponding Y component threshold register	10-418
0x47140	ISP_CA_COLORLLUMA_VTH	Color judgment dark region V component threshold register	10-418
0x47144	ISP_CA_COLORLLUMA_VYTH	Color judgment dark region V corresponding Y component threshold register	10-419
0x47148	ISP_CA_COLORHLUMA_VTH	Color judgment bright region V component threshold register	10-419
0x4714C	ISP_CA_COLORHLUMA_VYTH	Color judgment bright region V corresponding Y component threshold register	10-420
0x47150	ISP_CA_COLOR_UVDIFF	Color judgment UV component difference register	10-420
0x47154	ISP_CA_COLOR_RATIOTH0	Color protection gain threshold register 0	10-421
0x47158	ISP_CA_COLOR_RATIOTH1	Color protection gain threshold register 1	10-421
0x471F0	ISP_CA_SIZE	CA picture size register	10-422
0x51300	ISP_HLDC_CFG	HLDC enable register	10-387
0x51310	ISP_HLDC_SIZE	HLDC luminance size configuration register	10-423
0x51320	ISP_HLDC_CENTER	HLDC center coordinate parameter register	10-424

Offset Address	Register	Description	Page
0x51324	ISP_HLDC_PARA	HLDC configuration parameter register	10-424
0x51400	ISP_ACM_CTRL	ACM control register	10-425
0x51404	ISP_ACM_ADJ	ACM processed pixel change register	10-426
0x51408	ISP_ACM_PARA_REN	ACM coefficient read enable register	10-427
0x5140C	ISP_ACM_PARA_DATA	ACM coefficient read data register	10-427
0x51410	ISP_ACM_SIZE	ACM processing picture size register	10-427
0x51420	ISP_ACM_PARA_UP	ACM coefficient configuration update register	10-428
0x51C00	ISP_VPDCICTRL	DCI control register	10-428
0x51C04	ISP_VPDCIHPOS	DCI algorithm horizontal adjustment region register	10-430
0x51C08	ISP_VPDCIVPOS	DCI algorithm vertical adjustment region register	10-431
0x51C0C	ISP_VPDCIHISBLD	DCI histogram statistics weighted coefficient register	10-431
0x51C10	ISP_VPDCIHISOFT	DCI histogram statistics offset register	10-431
0x51C14	ISP_VPDCIHISCOR	DCI histogram coring register	10-432
0x51C18	ISP_VPDCIMERBLD	DCI adjustment unit blend value register	10-432
0x51C1C	ISP_VPDCIADJWGT	DCI manually configured curve weight register	10-433
0x51C20	ISP_VPDCICLIP0	DCI curve 0 weight range register	10-433
0x51C24	ISP_VPDCICLIP1	DCI curve 1 weight range register	10-434
0x51C28	ISP_VPDCICLIP2	DCI curve 2 weight range register	10-434
0x51C2C	ISP_VPDCIGLBGAIN	DCI luminance adjustment unit global gain register	10-435
0x51C30	ISP_VPDCIPOSTHR0	DCI adjustment unit threshold register 0 during positive adjustment	10-435
0x51C34	ISP_VPDCIPOSTHR1	DCI adjustment unit threshold register 1 during positive adjustment	10-436
0x51C38	ISP_VPDCIPOSGAIN0	DCI adjustment unit gain register 0 during positive adjustment	10-436

Offset Address	Register	Description	Page
0x51C3C	ISP_VPDCIPOSGAIN1	DCI adjustment unit gain register 1 during positive adjustment	10-437
0x51C40	ISP_VPDCIPOSSLP0	DCI adjustment unit slope register 0 during positive adjustment	10-437
0x51C44	ISP_VPDCIPOSSLP1	DCI adjustment unit slope register 1 during positive adjustment	10-438
0x51C48	ISP_VPDCIPOSSLP2	DCI adjustment unit slope register 2 during positive adjustment	10-438
0x51C4C	ISP_VPDCINEGTHR0	DCI adjustment unit threshold register 0 during negative adjustment	10-439
0x51C50	ISP_VPDCINEGTHR1	DCI adjustment unit threshold register 1 during negative adjustment	10-439
0x51C54	ISP_VPDCINEGGAIN0	DCI adjustment unit gain register 0 during negative adjustment	10-440
0x51C58	ISP_VPDCINEGGAIN1	DCI adjustment unit gain register 1 during negative adjustment	10-440
0x51C5C	ISP_VPDCINEGSLP0	DCI adjustment unit slope register 0 during negative adjustment	10-441
0x51C60	ISP_VPDCINEGSLP1	DCI adjustment unit slope register 1 during negative adjustment	10-441
0x51C64	ISP_VPDCINEGSLP2	DCI adjustment unit slope register 2 during negative adjustment	10-442

10.6 Register Description

ISP_AF_CFG

ISP_AF_CFG is an AF control register.

Offset Address	Register Name	Total Reset Value
0x12200	ISP_AF_CFG	0x0000_01DA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ck_gt_en	reserved						fir1_ldg_en	fir0_ldg_en	iir1_ldg_en	iir0_ldg_en	fir1_lpf_en	fir0_lpf_en	iir1_ds_en	iir0_ds_en	bayer_mode	raw_mode	sqrt_en	mean_en	lpf_en	crop_en	offset_en	squ_mode	peak_mode	iir1_en2	iir1_en1	iir1_en0	iir0_en2	iir0_en1	iir0_en0	en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31]	RW	ck_gt_en	AF clock gating enable
[30:25]	RO	reserved	Reserved
[24]	RW	fir1_ldg_en	Vertical FIR filter luma dependent gain (LDG) enable 1 0: disabled 1: enabled
[23]	RW	fir0_ldg_en	Vertical FIR filter LDG enable 0 0: disabled 1: enabled
[22]	RW	iir1_ldg_en	Horizontal IIR filter LDG enable 1 0: disabled 1: enabled
[21]	RW	iir0_ldg_en	Horizontal IIR filter LDG enable 0 0: disabled 1: enabled
[20]	RW	fir1_lpf_en	Vertical FIR filter low pass filter (LPF) enable 1 0: disabled 1: enabled
[19]	RW	fir0_lpf_en	Vertical FIR filter LPF enable 0 0: disabled 1: enabled
[18]	RW	iir1_ds_en	Horizontal IIR filter down sampling (DS) enable 1 0: disabled 1: enabled
[17]	RW	iir0_ds_en	Horizontal IIR filter DS enable 0 0: disabled 1: enabled

[16:15]	RW	bayer_mode	AF raw format 00: RGGB 01: GRBG 10: GBRG 11: BGGR
[14]	RW	raw_mode	AF data format 0: YUV data 1: raw data
[13]	RW	sqrt_en	AF gamma enable 0: disabled 1: enabled
[12]	RW	mean_en	AF median filtering enable 0: disabled 1: enabled
[11]	RW	lpf_en	AF low-pass filter enable 0: disabled 1: enabled
[10]	RW	crop_en	AF crop enable 0: disabled 1: enabled
[9]	RW	offset_en	offset enable 0: disabled 1: enabled
[8]	RW	squ_mode	Square mode of AF statistics 0: Statistics are directly accumulated. 1: Statistics are accumulated after the square operation.
[7]	RW	peak_mode	Peak value mode of AF statistics 0: All values of a block are selected for statistics. 1: The maximum value in each line of a block is selected for statistics.
[6]	RW	iir1_en2	Enable for IIR2 among the three cascaded IIRs in group 2 0: disabled 1: enabled
[5]	RW	iir1_en1	Enable for IIR1 among the three cascaded IIRs in group 2 0: disabled 1: enabled

[4]	RW	iir1_en0	Enable for IIR0 among the three cascaded IIRs in group 2 0: disabled 1: enabled
[3]	RW	iir0_en2	Enable for IIR2 among the three cascaded IIRs in group 1 0: disabled 1: enabled
[2]	RW	iir0_en1	Enable for IIR1 among the three cascaded IIRs in group 1 0: disabled 1: enabled
[1]	RW	iir0_en0	Enable for IIR0 among the three cascaded IIRs in group 1 0: disabled 1: enabled
[0]	RW	en	AF enable 0: disabled 1: enabled

ISP_AF_ZONE

ISP_AF_ZONE is an AF block configuration register.

Offset Address	Register Name	Total Reset Value
0x12210	ISP_AF_ZONE	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	vnum	Number of vertical AF blocks (15 blocks at most) Blocks are in the CH_AF_CROP_SIZE region when crop_en is 1. Blocks are in the CH_AF_SIZE region when crop_en is 0.
[7:5]	RO	reserved	Reserved
[4:0]	RW	hnum	Number of horizontal AF blocks (17 blocks at most) Blocks are in the CH_AF_CROP_SIZE region when crop_en is 1. Blocks are in the CH_AF_SIZE region when crop_en is 0.

ISP_AF_CROP_START

ISP_AF_CROP_START is an AF picture crop start coordinate register.

Offset Address	Register Name	Total Reset Value
0x12214	ISP_AF_CROP_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				pos_y												reserved				pos_x											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	pos_y	Vertical coordinate of the crop start point
[15:13]	RO	reserved	Reserved
[12:0]	RW	pos_x	Horizontal coordinate of the crop start point

ISP_AF_CROP_SIZE

ISP_AF_CROP_SIZE is an AF picture crop size register.

Offset Address	Register Name	Total Reset Value
0x12218	ISP_AF_CROP_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	vsize	Picture height after AF cropping NOTE The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	hsize	Picture width after AF cropping NOTE The configured value is the actual value minus 1.

ISP_AF_MEAN_THRES

ISP_AF_MEAN_THRES is an AF median filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x1221C	ISP_AF_MEAN_THRES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																mean_thres															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	mean_thres	Threshold for AF median filtering

ISP_AF_IIRG0

ISP_AF_IIRG0 is AF IIR filtering parameter register 0.

Offset Address	Register Name	Total Reset Value
0x12220	ISP_AF_IIRG0	0x00A1_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg0_1								reserved								iirg0_0							
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	iirg0_1	g0 gain of AF IIR filtering group 1 NOTE This field affects the configured value of ISP_AF_SHIFT.
[15:8]	RO	reserved	Reserved
[7:0]	RW	iirg0_0	g0 gain of AF IIR filtering group 0 NOTE This field affects the configured value of ISP_AF_SHIFT.

ISP_AF_IIRG1

ISP_AF_IIRG1 is AF IIR filtering parameter register 1.

Offset Address	Register Name	Total Reset Value
0x12224	ISP_AF_IIRG1	0x0244_01BC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg1_1								reserved								iirg1_0							
Reset	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg1_1	g1 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg1_0	g1 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG2

ISP_AF_IIRG2 is AF IIR filtering parameter register 2.

Offset Address	Register Name	Total Reset Value
0x12228	ISP_AF_IIRG2	0x0328_0328

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg2_1								reserved								iirg2_0							
Reset	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg2_1	g2 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg2_0	g2 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG3

ISP_AF_IIRG3 is AF IIR filtering parameter register 3.

Offset Address	Register Name	Total Reset Value
0x1222C	ISP_AF_IIRG3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg3_1								reserved								iirg3_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg3_1	g3 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg3_0	g3 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG4

ISP_AF_IIRG4 is AF IIR filtering parameter register 4.

Offset Address	Register Name	Total Reset Value
0x12230	ISP_AF_IIRG4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg4_1								reserved								iirg4_0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg4_1	g4 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved

[9:0]	RW	iirg4_0	g4 gain of AF IIR filtering group 0 **NOTE** The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG5

ISP_AF_IIRG5 is AF IIR filtering parameter register 5.

Offset Address	Register Name	Total Reset Value
0x12234	ISP_AF_IIRG5	0x0284_017C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg5_1								reserved								iirg5_0							
Reset	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	iirg5_1	g5 gain of AF IIR filtering group 1 **NOTE** The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg5_0	g5 gain of AF IIR filtering group 0 **NOTE** The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRG6

ISP_AF_IIRG6 is AF IIR filtering parameter register 6.

Offset Address	Register Name	Total Reset Value
0x12238	ISP_AF_IIRG6	0x033C_033C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iirg6_1								reserved								iirg6_0							
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved

[25:16]	RW	iirg6_1	g6 gain of AF IIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −512.
[15:10]	RO	reserved	Reserved
[9:0]	RW	iirg6_0	g6 gain of AF IIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −512.

ISP_AF_IIRPL

ISP_AF_IIRPL is an AF IIR filter preset register.

Offset Address	Register Name	Total Reset Value
0x1223C	ISP_AF_IIRPL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	iirpls_1	iirplg_1		reserved	iirpls_0	iirplg_0	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:24]	RW	iirpls_1	Preset shift for AF IIR filter group 1
[23:16]	RW	iirplg_1	Preset gain for AF IIR filter group 1
[15:11]	-	reserved	Reserved
[10:8]	RW	iirpls_0	Preset shift for AF IIR filter group 0
[7:0]	RW	iirplg_0	Preset gain for AF IIR filter group 0

ISP_AF_SHIFT

ISP_AF_SHIFT is an AF IIR filtering shift parameter register.

Offset Address	Register Name	Total Reset Value
0x12240	ISP_AF_SHIFT	0x0027_1027

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	iirshift1_3			reserved	iirshift1_2			reserved	iirshift1_1			reserved	iirshift1_0			reserved	iirshift0_3			reserved	iirshift0_2			reserved	iirshift0_1			reserved	iirshift0_0		
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	1	1	1

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:28]	RW	iirshift1_3	Shift adjustment for IIR2 in AF IIR filtering group 1
[27]	-	reserved	Reserved
[26:24]	RW	iirshift1_2	Shift adjustment for IIR1 in AF IIR filtering group 1
[23]	-	reserved	Reserved
[22:20]	RW	iirshift1_1	Shift adjustment for IIR0 in AF IIR filtering group 1
[19]	-	reserved	Reserved
[18:16]	RW	iirshift1_0	Input shift adjustment for AF IIR filtering group 1 Note the following: iirg0_1 ≥ 128, iirshift0_0 ≥ 4 iirg0_1 ≥ 64, iirshift0_0 ≥ 3 iirg0_1 ≥ 32, iirshift0_0 ≥ 2 iirg0_1 ≥ 16, iirshift0_0 ≥ 1
[15]	-	reserved	Reserved
[14:12]	RW	iirshift0_3	Shift adjustment for IIR2 in AF IIR filtering group 0
[11]	-	reserved	Reserved
[10:8]	RW	iirshift0_2	Shift adjustment for IIR1 in AF IIR filtering group 0
[7]	-	reserved	Reserved
[6:4]	RW	iirshift0_1	Shift adjustment for IIR0 in AF IIR filtering group 0
[3]	-	reserved	Reserved

[2:0]	RW	iirshift0_0	Input shift adjustment for AF IIR filtering group 0 Note the following: iirg0_0 ≥ 128, iirshift0_0 ≥ 4 iirg0_0 ≥ 64, iirshift0_0 ≥ 3 iirg0_0 ≥ 32, iirshift0_0 ≥ 2 iirg0_0 ≥ 16, iirshift0_0 ≥ 1

ISP_AF_FIRH0

ISP_AF_FIRH0 is AF FIR filtering parameter register 0.

Offset Address	Register Name	Total Reset Value
0x12250	ISP_AF_FIRH0	0x0030_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh0_1				reserved												firh0_0			
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh0_1	h0 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh0_0	h0 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH1

ISP_AF_FIRH1 is AF FIR filtering parameter register 1.

Offset Address	Register Name	Total Reset Value
0x12254	ISP_AF_FIRH1	0x0015_002B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh1_1				reserved												firh1_0			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh1_1	h1 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh1_0	h1 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH2

ISP_AF_FIRH2 is AF FIR filtering parameter register 2.

Offset Address	Register Name	Total Reset Value
0x12258	ISP_AF_FIRH2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh2_1				reserved												firh2_0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh2_1	h2 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh2_0	h2 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH3

ISP_AF_FIRH3 is AF FIR filtering parameter register 3.

Offset Address	Register Name	Total Reset Value
0x1225C	ISP_AF_FIRH3	0x002B_0015

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh3_1				reserved												firh3_0			
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh3_1	h3 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved
[5:0]	RW	firh3_0	h3 gain of AF FIR filtering group 0 NOTE The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_FIRH4

ISP_AF_FIRH4 is AF FIR filtering parameter register 4.

Offset Address	Register Name	Total Reset Value
0x12260	ISP_AF_FIRH4	0x0010_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												firh4_1				reserved												firh4_0			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:16]	RW	firh4_1	h4 gain of AF FIR filtering group 1 NOTE The value is a signed number and cannot be the negative boundary value −32.
[15:6]	RO	reserved	Reserved

[5:0]	RW	firh4_0	h4 gain of AF FIR filtering group 0 **NOTE** The value is a signed number and cannot be the negative boundary value −32.

ISP_AF_ACC_SHIFT

ISP_AF_ACC_SHIFT is an AF cumulative statistics shift register.

Offset Address	Register Name	Total Reset Value
0x12278	ISP_AF_ACC_SHIFT	0x0002_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												acc_shift_y				acc_shift1_v				acc_shift0_v				acc_shift1_h				acc_shift0_h			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:16]	RW	acc_shift_y	Luminance Y statistics shift (0−15). Y in CH_AF_STAT_RDATA is shifted.
[15:12]	RW	acc_shift1_v	Shift of vertical FIR filtering statistics in group 1 (0−15). V2 in CH_AF_STAT_RDATA is shifted.
[11:8]	RW	acc_shift0_v	Shift of vertical FIR filtering statistics in group 0 (0−15). V1 in CH_AF_STAT_RDATA is shifted.
[7:4]	RW	acc_shift1_h	Shift of horizontal IIR filtering statistics in group 1 (0−15). H2 in CH_AF_STAT_RDATA is shifted.
[3:0]	RW	acc_shift0_h	Shift of horizontal IIR filtering statistics in group 0 (0−15). H1 in CH_AF_STAT_RDATA is shifted.

ISP_AF_CNT_SHIFT

ISP_AF_CNT_SHIFT is an AF count statistics shift register.

Offset Address	Register Name	Total Reset Value
0x1227C	ISP_AF_CNT_SHIFT	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												cnt_shift_y				cnt_shift1_v				cnt_shift0_v				cnt_shift1_h				cnt_shift0_h			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[19:16]	RW	cnt_shift_y	Luminance Y count statistics shift register.
[15:12]	RW	cnt_shift1_v	Shift of vertical FIR filtering statistics in group 1 (0−15). vcnt2 in CH_AF_STAT_RDATA is shifted.
[11:8]	RW	cnt_shift0_v	Shift of vertical FIR filtering statistics in group 0 (0−15). vcnt1 in CH_AF_STAT_RDATA is shifted.
[7:4]	RW	cnt_shift1_h	Shift of horizontal IIR filtering statistics in group 1 (0−15). hcnt2 in CH_AF_STAT_RDATA is shifted.
[3:0]	RW	cnt_shift0_h	Shift of horizontal IIR filtering statistics in group 0 (0−15). hcnt1 in CH_AF_STAT_RDATA is shifted.

ISP_AF_STAT_IND_RADDR

ISP_AF_STAT_IND_RADDR is a statistics indirect read address register for AF blocks.

Offset Address	Register Name	Total Reset Value
0x12288	ISP_AF_STAT_IND_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	af_stat_ind_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	af_stat_ind_raddr	Statistics indirect read address register for AF blocks

ISP_AF_STAT_IND_RDATA

ISP_AF_STAT_IND_RDATA is a statistics indirect read data register for AF blocks.

Offset Address	Register Name	Total Reset Value
0x1228C	ISP_AF_STAT_IND_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	af_stat_ind_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	af_stat_ind_rdata	Statistics indirect read data register for AF blocks V1[16], H1[16], V2[16], H2[16], Y[16], hcnt1, hcnt2, vcnt1, vcnt2, and ycnt information about each block is collected for statistics. The following is the information for each address: 1: {V1 (16 bits), H1 (16 bits)} of block 1

			2: {V2 (16 bits), H2 (16 bits)} of block 1 3: {ycnt (16 bits), Y (16 bits)} of block 1 4: {vcnt2 (8 bits), vcnt1 (8bits), hcnt2 (8bits), cnt1 (8bits)} of block 1 5: {V1 (16bits), H1(16bits)} of block 2 … The same rule applies to other values. Note the following: V1 indicates the vertical FIR filtering statistics of group 1. V2 indicates the vertical FIR filtering statistics of group 2. H1 indicates the horizontal IIR filtering statistics of group 1. H2 indicates the horizontal IIR filtering statistics of group 2. Y indicates luminance statistics. vcnt1 indicates the number of times that the FIR filtering value is above the threshold. vcnt2 indicates the number of times that the FIR filtering value is above the threshold. hcnt1 indicates the number of times that the IIR filtering value is above the threshold. hcnt2 indicates the number of times that the IIR filtering value is above the threshold. ycnt indicates the number of times that the luminance value is above the threshold.

ISP_AF_CTRL_I

ISP_AF_CTRL_I is an immediate update control register.

Offset Address	Register Name	Total Reset Value
0x122E4	ISP_AF_CTRL_I	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								update_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update_mode	ISP update mode 0 update by using ISP_AF_UPDATE 1: frame update

ISP_AF_UPDATE

ISP_AF_UPDATE is a configuration update register.

Offset Address	Register Name	Total Reset Value
0x122EC	ISP_AF_UPDATE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							update
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update	ISP update register. This bit is cleared automatically for each frame.

ISP_AF_SIZE

ISP_AF_SIZE is an AF picture size register.

Offset Address	Register Name	Total Reset Value
0x122F0	ISP_AF_SIZE	0x0437_077F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	vsize			reserved	hsize		
Reset	0 0 0 0	0 1 0 0	0 0 1 1	0 1 1 1	0 0 0 0	0 1 1 1	0 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	vsize	AF input picture height The configured value is the actual value minus 1.
[15:13]	-	reserved	Reserved
[12:0]	RW	hsize	AF input picture width The configured value is the actual value minus 1.

ISP_AF_IIRTHRE

ISP_AF_IIRTHRE is an AF IIR filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x12300	ISP_AF_IIRTHRE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	iir_thre1_h		iir_thre1_l		iir_thre0_h		iir_thre0_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	iir_thre1_h	Luma dependent high threshold of AF IIR filter group 1
[23:16]	RW	iir_thre1_l	Luma dependent low threshold of AF IIR filter group 1
[15:8]	RW	iir_thre0_h	Luma dependent high threshold of AF IIR filter group 0
[7:0]	RW	iir_thre0_l	Luma dependent low threshold of AF IIR filter group 0

ISP_AF_IIRGAIN

ISP_AF_IIRGAIN is an AF IIR filtering gain register.

Offset Address	Register Name	Total Reset Value
0x12304	ISP_AF_IIRGAIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	iir_gain1_h		iir_gain1_l		iir_gain0_h		iir_gain0_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	iir_gain1_h	Luma dependent high gain of AF IIR filter group 1
[23:16]	RW	iir_gain1_l	Luma dependent low gain of AF IIR filter group 1
[15:8]	RW	iir_gain0_h	Luma dependent high gain of AF IIR filter group 0
[7:0]	RW	iir_gain0_l	Luma dependent low gain of AF IIR filter group 0

ISP_AF_IIRSLOPE

ISP_AF_IIRSLOPE is an AF IIR filtering slope register.

Offset Address	Register Name	Total Reset Value
0x12308	ISP_AF_IIRSLOPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								iir_slope1_h				iir_slope1_l				reserved								iir_slope0_h				iir_slope0_l			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:20]	RW	iir_slope1_h	Luma dependent high slope of AF IIR filter group 1
[19:16]	RW	iir_slope1_l	Luma dependent low slope of AF IIR filter group 1
[15:8]	-	reserved	Reserved
[7:4]	RW	iir_slope0_h	Luma dependent high slope of AF IIR filter group 0
[3:0]	RW	iir_slope0_l	Luma dependent low slope of AF IIR filter group 0

ISP_AF_IIRDILATE

ISP_AF_IIRDILATE is an AF IIR filtering dilate register.

Offset Address	Register Name	Total Reset Value
0x1230C	ISP_AF_IIRDILATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					iir_dilate1			reserved				iir_dilate0			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved

[10:8]	RW	iir_dilate1	Obtain partial maximum value for calculating the IIR1 luma dependent gain. Dilate: 000: Use the maximum value among the adjacent 8 pixels. 001: Use the maximum value among the adjacent 16 pixels. 010: Use the maximum value among the adjacent 24 pixels. 011: Use the maximum value among the adjacent 32 pixels. 100: Use the maximum value among the adjacent 40 pixels. 101: Use the maximum value among the adjacent 48 pixels. 110: Use the maximum value among the adjacent 56 pixels. 111: Use the maximum value among the adjacent 64 pixels.
[7:3]	-	reserved	Reserved
[2:0]	RW	iir_dilate0	Obtain partial maximum value for calculating the IIR0 luma dependent gain. Dilate: 000: Use the maximum value among the adjacent 8 pixels. 001: Use the maximum value among the adjacent 16 pixels. 010: Use the maximum value among the adjacent 24 pixels. 011: Use the maximum value among the adjacent 32 pixels. 100: Use the maximum value among the adjacent 40 pixels. 101: Use the maximum value among the adjacent 48 pixels. 110: Use the maximum value among the adjacent 56 pixels. 111: Use the maximum value among the adjacent 64 pixels.

ISP_AF_FIRTHRE

ISP_AF_FIRTHRE is an AF FIR filtering threshold register.

Offset Address	Register Name	Total Reset Value
0x12310	ISP_AF_FIRTHRE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fir_thre1_h		fir_thre1_l		fir_thre0_h		fir_thre0_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	fir_thre1_h	Luma dependent high threshold of AF FIR filter group 1
[23:16]	RW	fir_thre1_l	Luma dependent low threshold of AF FIR filter group 1
[15:8]	RW	fir_thre0_h	Luma dependent high threshold of AF FIR filter group 0
[7:0]	RW	fir_thre0_l	Luma dependent low threshold of AF FIR filter group 0

ISP_AF_FIRGAIN

ISP_AF_FIRGAIN is an AF FIR filtering gain register.

Offset Address	Register Name	Total Reset Value
0x12314	ISP_AF_FIRGAIN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fir_gain1_h		fir_gain1_l		fir_gain0_h		fir_gain0_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	fir_gain1_h	Luma dependent high gain of AF FIR filter group 1
[23:16]	RW	fir_gain1_l	Luma dependent low gain of AF FIR filter group 1
[15:8]	RW	fir_gain0_h	Luma dependent high gain of AF FIR filter group 0
[7:0]	RW	fir_gain0_l	Luma dependent low gain of AF FIR filter group 0

ISP_AF_FIRSLOPE

ISP_AF_FIRSLOPE is an AF FIR filtering slope register.

Offset Address	Register Name	Total Reset Value
0x12318	ISP_AF_FIRSLOPE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		fir_slope1_h	fir_slope1_l	reserved		fir_slope0_h	fir_slope0_l
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:20]	RW	fir_slope1_h	Luma dependent high slope of AF FIR filter group 1
[19:16]	RW	fir_slope1_l	Luma dependent low slope of AF FIR filter group 1
[15:8]	-	reserved	Reserved
[7:4]	RW	fir_slope0_h	Luma dependent high slope of AF FIR filter group 0
[3:0]	RW	fir_slope0_l	Luma dependent low slope of AF FIR filter group 0

ISP_AF_IIRTHRE_CORING

ISP_AF_IIRTHRE_CORING is an AF IIR filtering coring threshold register.

Offset Address	Register Name	Total Reset Value
0x12320	ISP_AF_IIRTHRE_CORING	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	iir_thre1_c			reserved	iir_thre0_c		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	iir_thre1_c	Coring threshold of AF IIR filter group 1
[15:11]	-	reserved	Reserved
[10:0]	RW	iir_thre0_c	Coring threshold of AF IIR filter group 0

ISP_AF_IIRPEAK_CORING

ISP_AF_IIRPEAK_CORING is an AF IIR filtering coring peak value register.

Offset Address	Register Name	Total Reset Value
0x12324	ISP_AF_IIRPEAK_CORING	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	iir_peak1_c			reserved	iir_peak0_c		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	iir_peak1_c	Coring peak value of AF IIR filter group 1
[15:11]	-	reserved	Reserved
[10:0]	RW	iir_peak0_c	Coring peak value of AF IIR filter group 0

ISP_AF_IIRSLOPE_CORING

ISP_AF_IIRSLOPE_CORING is an AF IIR filtering coring slope register.

Offset Address	Register Name	Total Reset Value
0x12328	ISP_AF_IIRSLOPE_CORING	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					iir_slope1_c	reserved	iir_slope0_c
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:8]	RW	iir_slope1_c	Coring slope of AF IIR filter group 1
[7:4]	-	reserved	Reserved
[3:0]	RW	iir_slope0_c	Coring slope of AF IIR filter group 0

ISP_AF_FIRTHRE_CORING

ISP_AF_FIRTHRE_CORING is an AF FIR filtering coring threshold register.

Offset Address	Register Name	Total Reset Value
0x12330	ISP_AF_FIRTHRE_CORING	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	fir_thre1_c			reserved	fir_thre0_c		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	fir_thre1_c	Coring threshold of AF FIR filter group 1
[15:11]	-	reserved	Reserved
[10:0]	RW	fir_thre0_c	Coring threshold of AF FIR filter group 0

ISP_AF_FIRPEAK_CORING

ISP_AF_FIRPEAK_CORING is an AF FIR filtering coring peak value register.

Offset Address	Register Name	Total Reset Value
0x12334	ISP_AF_FIRPEAK_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fir_peak1_c												reserved				fir_peak0_c											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	fir_peak1_c	Coring peak value of AF FIR filter group 1
[15:11]	-	reserved	Reserved
[10:0]	RW	fir_peak0_c	Coring peak value of AF FIR filter group 0

ISP_AF_FIRSLOPE_CORING

ISP_AF_FIRSLOPE_CORING is an AF FIR filtering coring slope register.

Offset Address	Register Name	Total Reset Value
0x12338	ISP_AF_FIRSLOPE_CORING	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				fir_slope1_c				reserved				fir_slope0_c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:8]	RW	fir_slope1_c	Coring slope of AF FIR filter group 1
[7:4]	-	reserved	Reserved
[3:0]	RW	fir_slope0_c	Coring slope of AF FIR filter group 0

ISP_AF_HILIGHT

ISP_AF_HILIGHT is an AF highlight threshold register.

Offset Address	Register Name	Total Reset Value
0x12340	ISP_AF_HILIGHT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hilight							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	hilight	AF luminance count threshold

ISP_AF_OFFSET

ISP_AF_OFFSET is an AF offset configuration register.

Offset Address	Register Name	Total Reset Value
0x12344	ISP_AF_OFFSET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				offset_gb												reserved				offset_gr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:16]	RW	offset_gb	Gb component offset
[15:14]	-	reserved	Reserved
[13:0]	RW	offset_gr	Gr component offset

ISP_AF_INT

ISP_AF_INT is an AF interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x123f0	ISP_AF_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_af
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	WC	int_af	AF interrupt indicator 0: No interrupt is generated. 1: An interrupt is generated.

ISP_AF_INT_MASK

ISP_AF_INT_MASK is an AF interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x123f8	ISP_AF_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_af
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	int_af	AF interrupt enable 0: masked 1: enabled

ISP_FE_MODULE_POS

ISP_FE_MODULE_POS is an ISP internal module position select register.

Offset Address	Register Name	Total Reset Value
0x20090	ISP_FE_MODULE_POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved	nr_sel	reserved	dcg_sel	reserved								reserved	dis_sel	reserved	af_sel	awb_sel		ae_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19]	-	reserved	Reserved
[18]	RW	nr_sel	BNR position adjustment register 0: The BNR module is behind the BCOM module. 1: The BNR module is behind the FPN module.
[17]	-	reserved	Reserved
[16]	RW	dcg_sel	DCG position adjustment register 0: The DCG module is behind the BLC module. 1: The DCG module is behind the DRC Dither module.
[15:8]	-	reserved	Reserved
[7]	-	reserved	Reserved
[6]	RW	dis_sel	DIS position adjustment register 0: The DIS module is behind the DG module. 1: The DIS module is behind the DRC Dither module.
[5]	-	reserved	Reserved
[4]	RW	af_sel	AF position adjustment register 0: The AF module is behind the DG module. 1: The AF module is behind the DRC Dither module.
[3:2]	RW	awb_sel	AWB position adjustment register 00: The AWB module is behind the DG module. 01: The AWB module is behind the Expander module. 10: The AWB module is behind the DRC Dither module.
[1:0]	RW	ae_sel	AE position adjustment register 00: The AE module is behind the DG module. 01: The AE module is behind the WB module. 10: The AE module is behind the DRC Dither module.

ISP_FE_FSTART_DELAY

ISP_FE_FSTART_DELAY is an ISP adjustable interrupt trigger time configuration register.

Offset Address	Register Name	Total Reset Value
0x20094	ISP_FE_FSTART_DELAY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delay																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	delay	Adjustable interrupt trigger time, in the unit of hsync

ISP_FE_USER_DEFINE0

ISP_FE_USER_DEFINE0 is user-defined register 0.

Offset Address	Register Name	Total Reset Value
0x200A0	ISP_FE_USER_DEFINE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	user_define0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	user_define0	User-defined register 0

ISP_FE_USER_DEFINE1

ISP_FE_USER_DEFINE1 is user-defined register 1.

Offset Address	Register Name	Total Reset Value
0x200A4	ISP_FE_USER_DEFINE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	user_define1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	user_define1	User-defined register 1

ISP_FE_STARTUP

ISP_FE_STARTUP is an ISP FE startup indicator register.

Offset Address	Register Name	Total Reset Value
0x200B0	ISP_FE_STARTUP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fcnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	fcnt	Frame count after startup

ISP_FE_INT

ISP_FE_INT is an ISP interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x200F0	ISP_FE_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							aewdr_int	dis_int	mg_int	awb_int	ae_int	fstart_delay	cfg_loss	update_cfg	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8]	WC	aewdr_int	Status of the AEWDR statistics completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	WC	dis_int	Status of the DIS statistics completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	WC	mg_int	Status of the MG statistics completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[5]	WC	awb_int	Status of the AWB statistics completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	WC	ae_int	Status of the AE statistics completion interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3]	WC	fstart_delay	Status of the configurable trigger delay interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	cfg_loss	Status of the register configuration loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the ISP frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

ISP_FE_INT_MASK

ISP_FE_INT_MASK is an ISP interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x200F8	ISP_FE_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							aewdr_int	dis_int	mg_int	awb_int	ae_int	int_delay	cfg_loss	update_cfg	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved

[8]	RW	aewdr_int	AEWDR statistics completion interrupt enable 0: disabled 1: enabled
[7]	RW	dis_int	DIS statistics completion interrupt enable 0: disabled 1: enabled
[6]	RW	mg_int	MG statistics completion interrupt enable 0: disabled 1: enabled
[5]	RW	awb_int	AWB statistics completion interrupt enable 0: disabled 1: enabled
[4]	RW	ae_int	AE statistics completion interrupt enable 0: disabled 1: enabled
[3]	RW	int_delay	Configurable trigger delay interrupt enable 0: disabled 1: enabled
[2]	RW	cfg_loss	Register configuration loss interrupt enable 0: disabled 1: enabled
[1]	RW	update_cfg	Register update interrupt enable 0: disabled 1: enabled
[0]	RW	fstart	ISP frame start interrupt enable 0: disabled 1: enabled

ISP_FE_CTRL_F

ISP_FE_CTRL_F is an ISP common update control register.

Offset Address	Register Name	Total Reset Value
0x201E0	ISP_FE_CTRL_F	0x0000_0003

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							rggb_cfg
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1:0]	RW	rggb_cfg	RGGB start 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

ISP_FE_CTRL_I

ISP_FE_CTRL_I is an ISP immediate update control register.

Offset Address	Register Name	Total Reset Value
0x201E4	ISP_FE_CTRL_I	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							update_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update_mode	ISP register update mode 0: updating by using ISP_FE_REG_UPDATE 1: frame update

ISP_FE_TIMING_CFG

ISP_FE_TIMING_CFG is an output timing configuration register.

Offset Address	Register Name	Total Reset Value
0x201E8	ISP_FE_TIMING_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				fix_timing											reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13:1]	RW	fix_timing	Manual timing parameter configuration, for setting the length of the generated horizontal blanking region
[0]	-	reserved	Reserved

ISP_FE_REG_UPDATE

ISP_FE_REG_UPDATE is a register update register.

Offset Address	Register Name	Total Reset Value
0x201EC	ISP_FE_REG_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update	ISP update register. This bit is automatically cleared for each frame.

ISP_CROP0_CFG

ISP_CROP0_CFG is a crop enable register.

Offset Address	Register Name	Total Reset Value
0x20800	ISP_CROP0_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								n0_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	n0_en	Region 0 enable 0: disabled 1: enabled

ISP_CROP0_START

ISP_CROP0_START is a region 0 crop start position register.

Offset Address	Register Name	Total Reset Value
0x20808	ISP_CROP0_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved	y_start			reserved	x_start			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	y_start	Row for starting obtaining the picture
[15:13]	-	reserved	Reserved
[12:0]	RW	x_start	Pixel for starting obtaining the picture

ISP_CROP0_SIZE

ISP_CROP0_SIZE is a region 0 crop size register.

Offset Address	Register Name	Total Reset Value
0x2080C	ISP_CROP0_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Obtained picture height (in the unit of row) The configured value is the actual value minus 1.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Obtained picture width (in the unit of pixel) The configured value is the actual value minus 1.

ISP_DRC_DITHER

ISP_DRC_DITHER is an ISP DRC dither register.

Offset Address	Register Name	Total Reset Value
0x20820	ISP_DRC_DITHER	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								out_bits				spatial_mode	isp_dither_round	isp_dither_en	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved

[7:4]	RW	out_bits	Output bit width 0x8: 8 bits 0xA: 10 bits 0xC: 12 bits 0xE: 14 bits Other values: forbidden
[3]	RW	spatial_mode	Spatial mode enable 0: disabled 1: enabled
[2:1]	RW	isp_dither_round	Dither mode select 00: truncation 01: round off 10: random
[0]	RW	isp_dither_en	Dither enable 0: disabled 1: enabled

ISP_INPUT_MUX

ISP_INPUT_MUX is an ISP internal module position select register.

Offset Address	Register Name	Total Reset Value
0x20830	ISP_INPUT_MUX	0x0004_3210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												input4_sel				reserved		input3_sel		reserved		input2_sel		reserved		input1_sel		reserved		input0_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved
[18:16]	RW	input4_sel	ISP FPN data input select 000: channel 0 001: channel 1 010: channel 2 011: channel 3 100: FPN black frame input Other: reserved

[15]	-	reserved	Reserved
[14:12]	RW	input3_sel	ISP channel 3 data input select 000: channel 0 001: channel 1 010: channel 2 011: channel 3 100: FPN black frame input Other: reserved
[11]	-	reserved	Reserved
[10:8]	RW	input2_sel	ISP channel 2 data input select 000: channel 0 001: channel 1 010: channel 2 011: channel 3 100: FPN black frame input Other: reserved
[7]	-	reserved	Reserved
[6:4]	RW	input1_sel	ISP channel 1 data input select 000: channel 0 001: channel 1 010: channel 2 011: channel 3 100: FPN black frame input Other: reserved
[3]	-	reserved	Reserved
[2:0]	RW	input0_sel	ISP channel 0 data input select 000: channel 0 001: channel 1 010: channel 2 011: channel 3 100: FPN black frame input Other: reserved

ISP_COLORBAR_CFG

ISP_COLORBAR_CFG is a color bar control register.

Offset Address	Register Name	Total Reset Value
0x20A00	ISP_COLORBAR_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	Color bar enable 0: disabled 1: enabled

ISP_COLORBAR_PATTERN

ISP_COLORBAR_PATTERN is a color bar type register.

Offset Address	Register Name	Total Reset Value
0x20A10	ISP_COLORBAR_PATTERN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														pattern	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	pattern	Color bar type 000: pure color picture 001: picture consisting of four horizontal color stripes (gradient color) 010: picture consisting of four vertical color stripes (gradient color) 011: picture consisting of eight vertical color stripes (fixed color) 100: PIP. A rectangular pure color target area is generated on the pure color background (configurable color and coordinates). Other values: reserved

ISP_COLORBAR_RBACKGND

ISP_COLORBAR_RBACKGND is a color bar background color register.

Offset Address	Register Name	Total Reset Value
0x20A14	ISP_COLORBAR_RBACKGND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rbackgnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rbackgnd	Background color of the R component in pure color pictures, pictures consisting of eight vertical color stripes, and PIPs

ISP_COLORBAR_GBACKGND

ISP_COLORBAR_GBACKGND is a color bar background color register.

Offset Address	Register Name	Total Reset Value
0x20A18	ISP_COLORBAR_GBACKGND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gbackgnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	gbackgnd	Background color of the G component in pure color pictures, pictures consisting of eight vertical color stripes, and PIPs

ISP_COLORBAR_BBACKGND

ISP_COLORBAR_BBACKGND is a color bar background color register.

Offset Address	Register Name	Total Reset Value
0x20A1C	ISP_COLORBAR_BBACKGND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bbackgnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	bbackgnd	Background color of the B component in pure color pictures, pictures consisting of eight vertical color stripes, and PIPs

ISP_COLORBAR_RFOREGND

ISP_COLORBAR_RFOREGND is a color bar foreground color register.

Offset Address	Register Name	Total Reset Value
0x20A20	ISP_COLORBAR_RFOREGND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rforegnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rforegnd	Foreground color of the R component in PIPs

ISP_COLORBAR_GFOREGND

ISP_COLORBAR_GFOREGND is a color bar foreground color register.

Offset Address	Register Name	Total Reset Value
0x20A24	ISP_COLORBAR_GFOREGND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																gforegnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	gforegnd	Foreground color of the G component in PIPs

ISP_COLORBAR_BFOREGND

ISP_COLORBAR_BFOREGND is a color bar foreground color register.

Offset Address	Register Name	Total Reset Value
0x20A28	ISP_COLORBAR_BFOREGND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																bforegnd															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	bforegnd	Foreground color of the B component in PIPs

ISP_COLORBAR_INIT

ISP_COLORBAR_INIT is a color bar initial value register.

Offset Address	Register Name	Total Reset Value
0x20A2C	ISP_COLORBAR_INIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rgbinit															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rgbinit	Initial value of the R/G/B component, for calculating the gradient color bar

ISP_COLORBAR_GRAD

ISP_COLORBAR_GRAD is a color bar increasing value register.

Offset Address	Register Name	Total Reset Value
0x20A30	ISP_COLORBAR_GRAD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rgbgrad															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	rgbgrad	Increasing value of the R/G/B component, for calculating the gradient color bar

ISP_COLORBAR_POS1

ISP_COLORBAR_POS1 is a color bar rectangle coordinate register.

Offset Address	Register Name	Total Reset Value
0x20A34	ISP_COLORBAR_POS1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	pos_y1			reserved	pos_x1		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	pos_y1	Vertical start coordinate (y1) of the rectangle inside the PIP
[15:13]	RO	reserved	Reserved
[12:0]	RW	pos_x1	Horizontal start coordinate (x1) of the rectangle inside the PIP

ISP_COLORBAR_POS2

ISP_COLORBAR_POS2 is a color bar rectangle coordinate register.

Offset Address	Register Name	Total Reset Value
0x20A38	ISP_COLORBAR_POS2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	pos_y2			reserved	pos_x2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	pos_y2	Vertical end coordinate (y2) of the rectangle inside the PIP
[15:13]	RO	reserved	Reserved
[12:0]	RW	pos_x2	Horizontal end coordinate (x2) of the rectangle inside the PIP

ISP_COLORBAR_RGGB

ISP_COLORBAR_RGGB is an RGGB sequence register.

Offset Address	Register Name	Total Reset Value
0x20A3C	ISP_COLORBAR_RGGB	0x0000_0003

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved								rggb
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	1 1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	rggb	RGGB sequence for generating RAW data for the color bar 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

ISP_COLORBAR_SIZE

ISP_COLORBAR_SIZE is a color bar picture size register.

Offset Address	Register Name	Total Reset Value
0x20AF0	ISP_COLORBAR_SIZE	0x0437_077F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1 0
Name	reserved	height			reserved	width			
Reset	0 0 0 0	0 1 0 0	0 0 1 1	0 1 1 1	0 0 0 0	0 1 1 1	0 1 1 1	1 1	1 1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, if the actual picture height is 1080, set this field to 1079.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, if the actual picture width is 1920, set this field to 1919.

ISP_BLC_CFG

ISP_BLC_CFG is a BLC control register.

Offset Address	Register Name	Total Reset Value
0x21100	ISP_BLC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	BLC enable 0: disabled 1: enabled

ISP_BLC0_OFFSET1

ISP_BLC0_OFFSET1 is BLC0 offset register 1.

Offset Address	Register Name	Total Reset Value
0x21110	ISP_BLC0_OFFSET1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ofsr															reserved	ofsgr														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	ofsr	BLC offset of the R component, S15
[15]	RO	reserved	Reserved
[14:0]	RW	ofsgr	BLC offset of the Gr component, S15

ISP_BLC0_OFFSET2

ISP_BLC0_OFFSET2 is BLC0 offset register 2.

Offset Address	Register Name	Total Reset Value
0x21114	ISP_BLC0_OFFSET2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ofsb												reserved				ofsgb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	ofsb	BLC offset of the B component, S15
[15]	RO	reserved	Reserved
[14:0]	RW	ofsgb	BLC offset of the Gb component, S15

ISP_BLC1_OFFSET1

ISP_BLC1_OFFSET1 is BLC1 offset register 1.

Offset Address	Register Name	Total Reset Value
0x21118	ISP_BLC1_OFFSET1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ofsr												reserved				ofsgr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsr	BLC offset of the R component, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgr	BLC offset of the Gr component, S15

ISP_BLC1_OFFSET2

ISP_BLC1_OFFSET2 is BLC1 offset register 2.

Offset Address	Register Name	Total Reset Value
0x2111c	ISP_BLC1_OFFSET2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ofsb												reserved				ofsgb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsb	BLC offset of the B component, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgb	BLC offset of the Gb component, S15

ISP_WB_CFG

ISP_WB_CFG is a WB control register.

Offset Address	Register Name	Total Reset Value
0x21200	ISP_WB_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	WB enable 0: disabled 1: enabled

ISP_WB_BLC_CFG

ISP_WB_BLC_CFG is a WB black level offset enable register.

Offset Address	Register Name	Total Reset Value
0x21204	ISP_WB_BLC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														en_out	en_in
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1]	RW	en_out	Output black level offset enable 0: disabled 1: enabled
[0]	RW	en_in	Input black level offset enable 0: disabled 1: enabled

ISP_WB_GAIN1

ISP_WB_GAIN1 is a WB gain (R & Gr) register.

Offset Address	Register Name	Total Reset Value
0x21210	ISP_WB_GAIN1	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rgain												reserved				grgain											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	rgain	WB R gain (U4.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	grgain	WB Gr gain (U4.8)

ISP_WB_GAIN2

ISP_WB_GAIN2 is a WB gain (B & Gb) register.

Offset Address	Register Name	Total Reset Value
0x21214	ISP_WB_GAIN2	0x0100_0100

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	bgain			reserved	gbgain		
Reset	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	bgain	WB B gain (U4.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	gbgain	WB Gb gain (U4.8)

ISP_WB_BLC_OFFSET1

ISP_WB_BLC_OFFSET1 is WB black level offset register 1.

Offset Address	Register Name	Total Reset Value
0x21218	ISP_WB_BLC_OFFSET1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ofsr			reserved	ofsgr		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsr	Black level R offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgr	Black level Gr offset, S15

ISP_WB_BLC_OFFSET2

ISP_WB_BLC_OFFSET2 is WB black level offset register 2.

Offset Address	Register Name	Total Reset Value
0x2121C	ISP_WB_BLC_OFFSET2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ofsb												reserved				ofsgb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsb	Black level B offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgb	Black level Gb offset, S15

ISP_DG_CFG

ISP_DG_CFG is a DG control register.

Offset Address	Register Name	Total Reset Value
0x21300	ISP_DG_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	DG enable 0: disabled 1: enabled

ISP_DG_BLC_CFG

ISP_DG_BLC_CFG is a DG black level enable control register.

Offset Address	Register Name	Total Reset Value
0x21304	ISP_DG_BLC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														en_out	en_in
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1]	RW	en_out	Output black level offset enable 0: disabled 1: enabled
[0]	RW	en_in	Input black level offset enable 0: disabled 1: enabled

ISP_DG_GAIN1

ISP_DG_GAIN1 is a DG gain (R & Gr) register.

Offset Address	Register Name	Total Reset Value
0x21310	ISP_DG_GAIN1	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgain																grgain															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rgain	DG R gain (U8.8)
[15:0]	RW	grgain	DG Gr gain (U8.8)

ISP_DG_GAIN2

ISP_DG_GAIN2 is a DG gain (B & Gb) register.

Offset Address	Register Name	Total Reset Value
0x21314	ISP_DG_GAIN2	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bgain																gbgain															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	bgain	DG B gain (U8.8)
[15:0]	RW	gbgain	DG Gb gain (U8.8)

ISP_DG_BLC_OFFSET1

ISP_DG_BLC_OFFSET1 is DG black level offset register 1.

Offset Address	Register Name	Total Reset Value
0x21318	ISP_DG_BLC_OFFSET1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ofsr															reserved	ofsgr														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsr	Black level R offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgr	Black level Gr offset, S15

ISP_DG_BLC_OFFSET2

ISP_DG_BLC_OFFSET2 is DG black level offset register 2.

Offset Address	Register Name	Total Reset Value
0x2131C	ISP_DG_BLC_OFFSET2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ofsb												reserved				ofsgb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsb	Black level B offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgb	Black level Gb offset, S15

ISP_2DG_CFG

ISP_2DG_CFG is a 2DG control register.

Offset Address	Register Name	Total Reset Value
0x21C00	ISP_2DG_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	DG enable 0: disabled 1: enabled

ISP_2DG_BLC_CFG

ISP_2DG_BLC_CFG is a 2DG black level control register.

Offset Address	Register Name	Total Reset Value
0x21C04	ISP_2DG_BLC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														en_out	en_in
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1]	RW	en_out	Output black level enable 0: disabled 1: enabled
[0]	RW	en_in	Input black level enable 0: disabled 1: enabled

ISP_2DG_0_GAIN1

ISP_2DG_0_GAIN1 is a channel 0 DG gain (R, Gr) register.

Offset Address	Register Name	Total Reset Value
0x21C10	ISP_2DG_0_GAIN1	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgain																grgain															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rgain	DG R gain (U8.8)
[15:0]	RW	grgain	DG Gr gain (U8.8)

ISP_2DG_0_GAIN2

ISP_2DG_0_GAIN2 is a channel 0 DG gain (B, Gb) register.

Offset Address	Register Name	Total Reset Value
0x21C14	ISP_2DG_0_GAIN2	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bgain																gbgain															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	bgain	DG B gain (U8.8)
[15:0]	RW	gbgain	DG Gb gain (U8.8)

ISP_2DG_0_BLC_OFFSET1

ISP_2DG_0_BLC_OFFSET1 is channel 0 black level offset register 1.

Offset Address	Register Name	Total Reset Value
0x21C18	ISP_2DG_0_BLC_OFFSET1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ofsr															reserved	ofsgr														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsr	Black level R offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgr	Black level Gr offset, S15

ISP_2DG_0_BLC_OFFSET2

ISP_2DG_0_BLC_OFFSET2 is channel 0 black level offset register 2.

Offset Address	Register Name	Total Reset Value
0x21C1C	ISP_2DG_0_BLC_OFFSET2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ofsb												reserved				ofsgb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsb	Black level B offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgb	Black level Gb offset, S15

ISP_2DG_1_GAIN1

ISP_2DG_1_GAIN1 is a channel 1 DG gain (R, Gr) register.

Offset Address	Register Name	Total Reset Value
0x21C20	ISP_2DG_1_GAIN1	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rgain																grgain															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	rgain	DG R gain (U8.8)
[15:0]	RW	grgain	DG Gr gain (U8.8)

ISP_2DG_1_GAIN2

ISP_2DG_1_GAIN2 is a channel 1 DG gain (B, Gb) register.

Offset Address	Register Name	Total Reset Value
0x21C24	ISP_2DG_1_GAIN2	0x0100_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bgain																gbgain															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	bgain	DG B gain (U8.8)
[15:0]	RW	gbgain	DG Gb gain (U8.8)

ISP_2DG_1_BLC_OFFSET1

ISP_2DG_1_BLC_OFFSET1 is channel 1 black level offset register 1.

Offset Address	Register Name	Total Reset Value
0x21C28	ISP_2DG_1_BLC_OFFSET1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ofsr															reserved	ofsgr														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsr	Black level R offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgr	Black level Gr offset, S15

ISP_2DG_1_BLC_OFFSET2

ISP_2DG_1_BLC_OFFSET2 is channel 1 black level offset register 2.

Offset Address	Register Name	Total Reset Value
0x21C2C	ISP_2DG_1_BLC_OFFSET2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ofsb												reserved				ofsgb											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	ofsb	Black level B offset, S15
[15]	-	reserved	Reserved
[14:0]	RW	ofsgb	Black level Gb offset, S15

ISP_AE_CFG

ISP_AE_CFG is an AE enable register.

Offset Address	Register Name	Total Reset Value
0x22000	ISP_AE_CFG	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	AE enable 0: disabled 1: enabled

ISP_AE_ZONE

ISP_AE_ZONE is an AE block configuration register.

Offset Address	Register Name	Total Reset Value
0x22010	ISP_AE_ZONE	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	vnum	Number of vertical blocks
[7:5]	RO	reserved	Reserved
[4:0]	RW	hnum	Number of horizontal blocks

ISP_AE_SKIP_CRG

ISP_AE_SKIP_CRG is an AE point select configuration register.

Offset Address	Register Name	Total Reset Value
0x22014	ISP_AE_SKIP_CRG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								offset_y			skip_y			offset_x	skip_x	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	offset_y	Count start row 0: count from row 0 1: count from row 1

[6:4]	RW	skip_y	Vertical jump point configuration for statistical points 000: Each pixel point is collected for statistics. 001: Statistics are collected on every two pixels. 010: Statistics are collected on every three pixels. 011: Statistics are collected on every four pixels. 100: Statistics are collected on every five pixels. 101: Statistics are collected on every eight pixels. 110 or larger values: Statistics are collected on every nine pixels.
[3]	RW	offset_x	Count start column 0: count from column 0 1: count from column 1
[2:0]	RW	skip_x	Horizontal jump point configuration for statistical points 000: Statistics are collected on every pixel (only for the four-channel mode). 001: Statistics are collected on every two pixels. 010: Statistics are collected on every three pixels. 011: Statistics are collected on every four pixels. 100: Statistics are collected on every five pixels. 101: Statistics are collected on every eight pixels. 110 or larger values: Statistics are collected on every nine pixels.

ISP_AE_TOTAL_STAT

ISP_AE_TOTAL_STAT is a selected point total number register in a picture frame during 1024-segment histogram statistics.

Offset Address	Register Name	Total Reset Value
0x22018	ISP_AE_TOTAL_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								total_pixels																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:0]	RO	total_pixels	Number of selected points in a picture frame during 1024-segment histogram statistics

ISP_AE_COUNT_STAT

ISP_AE_COUNT_STAT is a selected point total weight register in a picture frame during 1024-segment histogram statistics.

Offset Address	Register Name	Total Reset Value
0x2201C	ISP_AE_COUNT_STAT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	count_pixels						
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:0]	RO	count_pixels	Total weight of selected points in a picture frame during 1024-segment histogram statistics

ISP_AE_TOTAL_R_AVER

ISP_AE_TOTAL_R_AVER is an R component average value register in a picture frame during average value statistics.

Offset Address	Register Name	Total Reset Value
0x22020	ISP_AE_TOTAL_R_AVER	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	total_r_aver							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	total_r_aver	Global average value of the R component

ISP_AE_TOTAL_GR_AVER

ISP_AE_TOTAL_GR_AVER is a Gr component average value register in a picture frame during average value statistics.

Offset Address	Register Name	Total Reset Value
0x22024	ISP_AE_TOTAL_GR_AVER	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	total_gr_aver							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	total_gr_aver	Global average value of the Gr component

ISP_AE_TOTAL_GB_AVER

ISP_AE_TOTAL_GB_AVER is a Gb component average value register in a picture frame during average value statistics.

Offset Address	Register Name	Total Reset Value
0x22028	ISP_AE_TOTAL_GB_AVER	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	total_gb_aver							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	total_gb_aver	Global average value of the Gb component

ISP_AE_TOTAL_B_AVER

ISP_AE_TOTAL_B_AVER is a B component average value register in a picture frame during average value statistics.

Offset Address	Register Name	Total Reset Value
0x2202C	ISP_AE_TOTAL_B_AVER	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	total_b_aver							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	total_b_aver	Global average value of the B component

ISP_AE_HIST_HIGH

ISP_AE_HIST_HIGH is a histogram statistics high register.

Offset Address	Register Name	Total Reset Value
0x22030	ISP_AE_HIST_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hist_high	Upper bits in histogram statistics

ISP_AE_BITMOVE

ISP_AE_BITMOVE is an AE pixel shift value register.

Offset Address	Register Name	Total Reset Value
0x22040	ISP_AE_BITMOVE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						BLC_en	gamma_en	bitmove							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	BLC_en	AE BLC enable 0: disabled 1: enabled
[8]	RW	gamma_en	AE gamma enable 0: disabled 1: enabled
[7:0]	RW	bitmove	AE pixel shift value

ISP_AE_OFFSET_R

ISP_AE_OFFSET_R is an R component black level offset register.

Offset Address	Register Name	Total Reset Value
0x22044	ISP_AE_OFFSET_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_r	Black level offset

ISP_AE_OFFSET_GR

ISP_AE_OFFSET_GR is a Gr component black level offset register.

Offset Address	Register Name	Total Reset Value
0x22048	ISP_AE_OFFSET_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_gr	Black level offset

ISP_AE_OFFSET_GB

ISP_AE_OFFSET_GB is a Gb component black level offset register.

Offset Address	Register Name	Total Reset Value
0x2204C	ISP_AE_OFFSET_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_gb	Black level offset

ISP_AE_OFFSET_B

ISP_AE_OFFSET_B is a B component black level offset register.

Offset Address	Register Name	Total Reset Value
0x22050	ISP_AE_OFFSET_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_b	Black level offset

ISP_AE_GAMMA_LIMIT

ISP_AE_GAMMA_LIMIT is an AE_gamma module shift control register.

Offset Address	Register Name	Total Reset Value
0x22060	ISP_AE_GAMMA_LIMIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												gamma_limit			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved
[3:0]	RW	gamma_limit	Gamma module shift value control The value can be 1000, 1001, 1010, 1011, or 1100.

ISP_AE_FOURPLANEMODE

ISP_AE_FOURPLANEMODE is an AE statistics mode select register.

Offset Address	Register Name	Total Reset Value
0x22070	ISP_AE_FOURPLANEMODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															fourplanemode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	fourplanemode	Four-channel statistics mode select 0: 1024 histogram statistics 1: four-channel 256 histogram statistics

ISP_AE_MEM_HIST_RADDR

ISP_AE_MEM_HIST_RADDR is an AE histogram statistics read address register.

Offset Address	Register Name	Total Reset Value
0x22088	ISP_AE_MEM_HIST_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hist_raddr	Histogram statistics read address

ISP_AE_MEM_HIST_RDATA

ISP_AE_MEM_HIST_RDATA is an AE histogram statistics read data register.

Offset Address	Register Name	Total Reset Value
0x2208C	ISP_AE_MEM_HIST_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hist_rdata	Histogram statistics read data

ISP_AE_MEM_AVER_R_GR_RADDR

ISP_AE_MEM_AVER_R_GR_RADDR is an AE module R and Gr average value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x22098	ISP_AE_MEM_AVER_R_GR_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver_r_gr_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	aver_r_gr_raddr	Read address of the R and Gr average value statistics

ISP_AE_MEM_AVER_R_GR_RDATA

ISP_AE_MEM_AVER_R_GR_RDATA is an AE module R and Gr average value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x2209C	ISP_AE_MEM_AVER_R_GR_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver_r_gr_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	aver_r_gr_rdata	Read data of the R and Gr average value statistics

ISP_AE_MEM_AVER_GB_B_RADDR

ISP_AE_MEM_AVER_GB_B_RADDR is an AE module Gb and B average value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x220A8	ISP_AE_MEM_AVER_GB_B_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver_gb_b_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	aver_gb_b_raddr	Read address of the Gb and B average value statistics

ISP_AE_MEM_AVER_GB_B_RDATA

ISP_AE_MEM_AVER_GB_B_RDATA is an AE module Gb and B average value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x220AC	ISP_AE_MEM_AVER_GB_B_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver_gb_b_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	aver_gb_b_rdata	Read data of the Gb and B average value statistics

ISP_AE_MEM_WEIGHT_WADDR

ISP_AE_MEM_WEIGHT_WADDR is a zone weight register write address register.

Offset Address	Register Name	Total Reset Value
0x220B0	ISP_AE_MEM_WEIGHT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wei_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wei_waddr	Weight table write address

ISP_AE_MEM_WEIGHT_WDATA

ISP_AE_MEM_WEIGHT_WDATA is a zone weight register write data register.

Offset Address	Register Name	Total Reset Value
0x220B4	ISP_AE_MEM_WEIGHT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wei_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wei_wdata	Weight table write data

ISP_AE_SIZE

ISP_AE_SIZE is an AE picture size register.

Offset Address	Register Name	Total Reset Value
0x220F0	ISP_AE_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	vsize	Picture height
[15:13]	-	reserved	Reserved
[12:0]	RW	hsize	Picture width

ISP_AWB_CFG

ISP_AWB_CFG is an AWB enable register.

Offset Address	Register Name	Total Reset Value
0x22100	ISP_AWB_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								work_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	work_en	AWB enable 0: disabled 1: enabled

ISP_AWB_ZONE

ISP_AWB_ZONE is an AWB block configuration register.

Offset Address	Register Name	Total Reset Value
0x22110	ISP_AWB_ZONE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				vnum		reserved	hnum
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	vnum	Number of vertical blocks. The maximum value is 32.
[7:6]	RO	reserved	Reserved
[5:0]	RW	hnum	Number of horizontal blocks. The maximum value is 32.

ISP_AWB_BITMOVE

ISP_AWB_BITMOVE is an AWB statistics bit configuration register.

Offset Address	Register Name	Total Reset Value
0x22114	ISP_AWB_BITMOVE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														bitmove	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2:0]	RW	bitmove	If this bit is set to 0, the uppermost 16 bits of the 20 bits RAW data are used as the AWB input data. If this bit is set to 4, the lowermost 16 bits are used as the AWB input data. The rule applies to other values.

ISP_AWB_THD_MIN

ISP_AWB_THD_MIN is an AWB minimum RGB field value register.

Offset Address	Register Name	Total Reset Value
0x22118	ISP_AWB_THD_MIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																threshold_min															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	threshold_min	Minimum RGB field value during AWB statistics

ISP_AWB_THD_MAX

ISP_AWB_THD_MAX is an AWB maximum RGB field value register.

Offset Address	Register Name	Total Reset Value
0x2211C	ISP_AWB_THD_MAX	0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																threshold_max															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	threshold_max	Maximum RGB field value during AWB statistics

ISP_AWB_CR_MM

ISP_AWB_CR_MM is an AWB reference maximum/minimum R/G value register.

Offset Address	Register Name	Total Reset Value
0x22120	ISP_AWB_CR_MM	0x0040_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cr_ref_min												reserved				cr_ref_max											
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	cr_ref_min	AWB reference minimum R/G value (U4.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	cr_ref_max	AWB reference maximum R/G value (U4.8)

ISP_AWB_CB_MM

ISP_AWB_CB_MM is an AWB reference maximum/minimum B/G value register.

Offset Address	Register Name	Total Reset Value
0x22124	ISP_AWB_CB_MM	0x0040_01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cb_ref_min												reserved				cb_ref_max											
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27:16]	RW	cb_ref_min	AWB reference minimum B/G value (U4.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	cb_ref_max	AWB reference maximum R/G value (U4.8)

ISP_AWB_OFFSET_COMP

ISP_AWB_OFFSET_COMP is an AWB statistics offset compensation register.

Offset Address	Register Name	Total Reset Value
0x22128	ISP_AWB_OFFSET_COMP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_comp															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	offset_comp	Offset compensation of AWB statistics (U16.0)

ISP_AWB_TOP_K

ISP_AWB_TOP_K is an AWB gray area reference range top hypotenuse slope register.

Offset Address	Register Name	Total Reset Value
0x22130	ISP_AWB_TOP_K	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								awb_top_k																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:0]	RW	awb_top_k	Hypotenuse slope of the AWB gray area reference range, two's complement, S13.12

ISP_AWB_TOP_B

ISP_AWB_TOP_B is an AWB gray area reference range top hypotenuse intercept register.

Offset Address	Register Name	Total Reset Value
0x22134	ISP_AWB_TOP_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								awb_top_b																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	awb_top_b	Hypotenuse intercept of the AWB gray area reference range (U16.8)

ISP_AWB_BOT_K

ISP_AWB_BOT_K is an AWB gray area reference range bottom hypotenuse slope register.

Offset Address	Register Name	Total Reset Value
0x22138	ISP_AWB_BOT_K	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								awb_bot_k																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:0]	RW	awb_bot_k	Hypotenuse slope of the AWB gray area reference range, two's complement, S13.12

ISP_AWB_BOT_B

ISP_AWB_BOT_B is an AWB gray area reference range bottom hypotenuse intercept register.

Offset Address	Register Name	Total Reset Value
0x2213C	ISP_AWB_BOT_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								awb_bot_b																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23:0]	RW	awb_bot_b	Hypotenuse intercept of the AWB gray area reference range (U16.8)

ISP_AWB_AVG_R

ISP_AWB_AVG_R is an R component average value register of an entire picture.

Offset Address	Register Name	Total Reset Value
0x22140	ISP_AWB_AVG_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																avg_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	avg_r	Average value of the R component for an entire picture (U16.0)

ISP_AWB_AVG_G

ISP_AWB_AVG_G is a G component average value register of an entire picture.

Offset Address	Register Name	Total Reset Value
0x22144	ISP_AWB_AVG_G	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																avg_g															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	avg_g	Average value of the G component for an entire picture (U16.0)

ISP_AWB_AVG_B

ISP_AWB_AVG_B is a B component average value register of an entire picture.

Offset Address	Register Name	Total Reset Value
0x22148	ISP_AWB_AVG_B	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				avg_b			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	avg_b	Average value of the B component for an entire picture (U16.0)

ISP_AWB_CNT_ALL

ISP_AWB_CNT_ALL is a statistical point number register of an entire picture.

Offset Address	Register Name	Total Reset Value
0x2214C	ISP_AWB_CNT_ALL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				count_all			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	count_all	Number of statistical points in an entire picture

ISP_AWB_STAT_RADDR

ISP_AWB_STAT_RADDR is an AWB statistics read address register.

Offset Address	Register Name	Total Reset Value
0x22188	ISP_AWB_STAT_RADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					stat_raddr		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved

[10:0]	RW	stat_raddr	AWB statistics address The sequence is as follows: 0x0: AVG G+AVG R for block 0 0x1: Count All+AVG B for block 0 0x2: …for block 1 The same rule applies to other values. There are 1024 blocks, and the address value range is 0−2047.

ISP_AWB_STAT_RDATA

ISP_AWB_STAT_RDATA is an AWB statistics read return data register.

Offset Address	Register Name	Total Reset Value
0x2218C	ISP_AWB_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	stat_rdata	Read return value of AWB statistics. Each statistical value occupies 16 bits. AVG R/G/B are 16-bit integers, and Count ALL is normalized to 16 bits.

ISP_AWB_SIZE

ISP_AWB_SIZE is an AWB picture size register.

Offset Address	Register Name	Total Reset Value
0x221F0	ISP_AWB_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	vsize	Picture height. The configured value is the actual value minus 1. For example, if the actual picture height is 1080, set this field to 1079.

[15:13]	-	reserved	Reserved
[12:0]	RW	hsize	Picture width (minus 1). For example, if the actual picture width is 1920, set this field to 1919.

ISP_DIS_CFG

ISP_DIS_CFG is a DIS enable register.

Offset Address	Register Name	Total Reset Value
0x22400	ISP_DIS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															work_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	work_en	DIS enable 0: disabled 1: enabled

ISP_DIS_BLK

ISP_DIS_BLK is a block configuration register.

Offset Address	Register Name	Total Reset Value
0x22404	ISP_DIS_BLK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												srch_range				srch_range_0	reserved							blk_size							blk_size_0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RO	reserved	Reserved
[22:17]	RW	srch_range	Upper six bits of the search range. The value range is 4−32.

[16]	RO	srch_range_0	Least significant bit (LSB) of the search range. This bit is fixed at 0.
[15:8]	RO	reserved	Reserved
[7:1]	RW	blk_size	Upper seven bits of the side length of the square block. The value range is 8−64.
[0]	RO	blk_size_0	LSB of the side length of the square block. This bit is fixed at 0.

ISP_DIS_V0POS

ISP_DIS_V0POS is a vertical PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x22410	ISP_DIS_V0POS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the vertical PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_V4POS

ISP_DIS_V4POS is a vertical PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x22414	ISP_DIS_V4POS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_V8POS

ISP_DIS_V8POS is a vertical PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x22418	ISP_DIS_V8POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_V0POSE

ISP_DIS_V0POSE is a vertical PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x22420	ISP_DIS_V0POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved

[10:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_V4POSE

ISP_DIS_V4POSE is a vertical PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x22424	ISP_DIS_V4POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_V8POSE

ISP_DIS_V8POSE is a vertical PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x22428	ISP_DIS_V8POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved

[10:0]	RW	hor	Horizontal coordinate of the end point of the vertical PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_H0POS

ISP_DIS_H0POS is a horizontal PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x22430	ISP_DIS_H0POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_H4POS

ISP_DIS_H4POS is a horizontal PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x22434	ISP_DIS_H4POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_H8POS

ISP_DIS_H8POS is a horizontal PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x22438	ISP_DIS_H8POS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_H0POSE

ISP_DIS_H0POSE is a horizontal PRJ0 block address register.

Offset Address	Register Name	Total Reset Value
0x22440	ISP_DIS_H0POSE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				ver												reserved				hor											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ0 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_H4POSE

ISP_DIS_H4POSE is a horizontal PRJ4 block address register.

Offset Address	Register Name	Total Reset Value
0x22444	ISP_DIS_H4POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ4 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_H8POSE

ISP_DIS_H8POSE is a horizontal PRJ8 block address register.

Offset Address	Register Name	Total Reset Value
0x22448	ISP_DIS_H8POSE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	ver			reserved	hor		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:16]	RW	ver	Vertical coordinate of the end point of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.
[15:11]	RO	reserved	Reserved
[10:0]	RW	hor	Horizontal coordinate of the end point of the horizontal PRJ8 block. The LSB of the coordinate value is excluded, and one bit is subtracted.

ISP_DIS_GAMMA_EN

ISP_DIS_GAMMA_EN is a gamma enable register.

Offset Address	Register Name	Total Reset Value
0x22454	ISP_DIS_GAMMA_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															gamma_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	gamma_en	Gamma enable 0: disabled 1: enabled

ISP_DIS_H_STAT_RADDR

ISP_DIS_H_STAT_RADDR is a horizontal statistics read address register.

Offset Address	Register Name	Total Reset Value
0x22488	ISP_DIS_H_STAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	h_stat_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	h_stat_raddr	h_delta, h_sad, and h_mv information about each block. Each address contains only one piece of information. For example: 0x0: h_delta[14:0] of block 0 0x1: h_sad[21:0] of block 0 0x2: h_mv[7:0] of block 0 … The same rule applies to other values.

ISP_DIS_H_STAT_RDATA

ISP_DIS_H_STAT_RDATA is a horizontal statistics read data register.

Offset Address	Register Name	Total Reset Value
0x2248C	ISP_DIS_H_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	h_stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	h_stat_rdata	Horizontal statistics

ISP_DIS_V_STAT_RADDR

ISP_DIS_V_STAT_RADDR is a vertical statistics read address register.

Offset Address	Register Name	Total Reset Value
0x22498	ISP_DIS_V_STAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_stat_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	v_stat_raddr	v_delta, v_sad, and v_mv information about each block. Each address contains only one piece of information. For example: 0x0: v_delta[14:0] of block 0 0x1: v_sad[21:0] of block 0 0x2: v_mv[7:0] of block 0 … The same rule applies to other values.

ISP_DIS_V_STAT_RDATA

ISP_DIS_V_STAT_RDATA is a vertical statistics read data register.

Offset Address	Register Name	Total Reset Value
0x2249C	ISP_DIS_V_STAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	v_stat_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	v_stat_rdata	Vertical statistics

ISP_MG_CFG

ISP_MG_CFG is an MG enable register.

Offset Address	Register Name	Total Reset Value
0x22500	ISP_MG_CFG	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	MG enable 0: disabled 1: enabled

ISP_MG_ZONE

ISP_MG_ZONE is an MG zone configuration register.

Offset Address	Register Name	Total Reset Value
0x22510	ISP_MG_ZONE	0x0000_0F11

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12:8]	RW	vnum	Number of zones in the vertical direction
[7:5]	-	reserved	Reserved
[4:0]	RW	hnum	Number of zones in the horizontal direction

ISP_MG_BITMOVE

ISP_MG_BITMOVE is an MG pixel shift register.

Offset Address	Register Name	Total Reset Value
0x22540	ISP_MG_BITMOVE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						BLC_en	gamma_en	bitmove							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9]	RW	BLC_en	MG BLC enable
[8]	RW	gamma_en	MG gamma enable
[7:0]	RW	bitmove	MG pixel shift value

ISP_MG_OFFSET_R

ISP_MG_OFFSET_R is an R component black level offset register.

Offset Address	Register Name	Total Reset Value
0x22544	ISP_MG_OFFSET_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_r	Black level offset

ISP_MG_OFFSET_GR

ISP_MG_OFFSET_GR is a Gr component black level offset register.

Offset Address	Register Name	Total Reset Value
0x22548	ISP_MG_OFFSET_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_gr	Black level offset

ISP_MG_OFFSET_GB

ISP_MG_OFFSET_GB is a Gb component black level offset register.

Offset Address	Register Name	Total Reset Value
0x2254C	ISP_MG_OFFSET_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_gb	Black level offset

ISP_MG_OFFSET_B

ISP_MG_OFFSET_B is a B component black level offset register.

Offset Address	Register Name	Total Reset Value
0x22550	ISP_MG_OFFSET_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								offset_b							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	offset_b	Black level offset

ISP_MG_GAMMA_LIMIT

ISP_MG_GAMMA_LIMIT is an MG_gamma module shift control register.

Offset Address	Register Name	Total Reset Value
0x22560	ISP_MG_GAMMA_LIMIT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												gamma_limit			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved
[3:0]	RW	gamma_limit	Gamma module shift control The value can be 1000, 1001, 1010, 1011, or 1100.

ISP_MG_MEM_AVER_RADDR

ISP_MG_MEM_AVER_RADDR is an MG module R/Gr/Gb/B average value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x22598	ISP_MG_MEM_AVER_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	aver_raddr	Read address of the R/Gr/Gb/B average value statistics

ISP_MG_MEM_AVER_RDATA

ISP_MG_MEM_AVER_RDATA is an MG module R/Gr/Gb/B average value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x2259C	ISP_MG_MEM_AVER_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	aver_rdata	Read data of the R/Gr/Gb/B average value statistics

ISP_MG_SIZE

ISP_MG_SIZE is an MG picture size register.

Offset Address	Register Name	Total Reset Value
0x225F0	ISP_MG_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	vsize	Picture height

[15:13]	-	reserved	Reserved
[12:0]	RW	hsize	Picture width

ISP_LSC_CFG

ISP_LSC_CFG is an LSC enable register.

Offset Address	Register Name	Total Reset Value
0x23000	ISP_LSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	LSC enable 0: disabled 1: enabled

ISP_LSC_WINNUM

ISP_LSC_WINNUM is an LSC picture segmentation window quantity configuration register.

Offset Address	Register Name	Total Reset Value
0x23010	ISP_LSC_WINNUM	0x000F_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												numv				reserved								numh							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RW	numv	Number of windows in the vertical direction after the LSC picture is segmented. The configured value is the actual value minus 1.
[15:5]	RO	reserved	Reserved
[4:0]	RW	numh	Number of windows in the horizontal direction after the LSC picture is segmented. The configured value is the actual value minus 1.

ISP_LSC_WINX1

ISP_LSC_WINX1 is an LSC interpolation horizontal first window width information register.

Offset Address	Register Name	Total Reset Value
0x23014	ISP_LSC_WINX1	0x0125_001B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx1												reserved								deltax1							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx1	Reciprocal value of the width of the LSC interpolation horizontal first window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax1	Width of the LSC interpolation horizontal first window. The configured value is the actual value minus 1.

ISP_LSC_WINX2

ISP_LSC_WINX2 is an LSC interpolation horizontal second window width information register.

Offset Address	Register Name	Total Reset Value
0x23018	ISP_LSC_WINX2	0x00CD_0027

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx2												reserved								deltax2							
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx2	Reciprocal value of the width of the LSC interpolation horizontal second window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax2	Width of the LSC interpolation horizontal second window

ISP_LSC_WINX3

ISP_LSC_WINX3 is an LSC interpolation horizontal third window width information register.

Offset Address	Register Name	Total Reset Value
0x2301C	ISP_LSC_WINX3	0x0098_0035

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx3												reserved								deltax3							
Reset	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx3	Reciprocal value of the width of the LSC interpolation horizontal third window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax3	Width of the LSC interpolation horizontal third window

ISP_LSC_WINX4

ISP_LSC_WINX4 is an LSC interpolation horizontal fourth window width information register.

Offset Address	Register Name	Total Reset Value
0x23020	ISP_LSC_WINX4	0x006C_004B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx4												reserved								deltax4							
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx4	Reciprocal value of the width of the LSC interpolation horizontal fourth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax4	Width of the LSC interpolation horizontal fourth window

ISP_LSC_WINX5

ISP_LSC_WINX5 is an LSC interpolation horizontal fifth window width information register.

Offset Address	Register Name	Total Reset Value
0x23024	ISP_LSC_WINX5	0x004C_006B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx5												reserved								deltax5							
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx5	Reciprocal value of the width of the LSC interpolation horizontal fifth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax5	Width of the LSC interpolation horizontal fifth window

ISP_LSC_WINX6

ISP_LSC_WINX6 is an LSC interpolation horizontal sixth window width information register.

Offset Address	Register Name	Total Reset Value
0x23028	ISP_LSC_WINX6	0x0037_0095

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx6												reserved								deltax6							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx6	Reciprocal value of the width of the LSC interpolation horizontal sixth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax6	Width of the LSC interpolation horizontal sixth window

ISP_LSC_WINX7

ISP_LSC_WINX7 is an LSC interpolation horizontal seventh window width information register.

Offset Address	Register Name	Total Reset Value
0x2302C	ISP_LSC_WINX7	0x0027_00D1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx7												reserved								deltax7							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx7	Reciprocal value of the width of the LSC interpolation horizontal seventh window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax7	Width of the LSC interpolation horizontal seventh window

ISP_LSC_WINX8

ISP_LSC_WINX8 is an LSC interpolation horizontal eighth window width information register.

Offset Address	Register Name	Total Reset Value
0x23030	ISP_LSC_WINX8	0x001C_0125

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invx8												reserved								deltax8							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invx8	Reciprocal value of the width of the LSC interpolation horizontal eighth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltax8	Width of the LSC interpolation horizontal eighth window

ISP_LSC_WINY1

ISP_LSC_WINY1 is an LSC interpolation vertical first window width information register.

Offset Address	Register Name	Total Reset Value
0x23034	ISP_LSC_WINY1	0x0200_000F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	invy1			reserved		deltay1	
Reset	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy1	Reciprocal value of the width of the LSC interpolation vertical first window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay1	Width of the LSC interpolation vertical first window

ISP_LSC_WINY2

ISP_LSC_WINY2 is an LSC interpolation vertical second window width information register.

Offset Address	Register Name	Total Reset Value
0x23038	ISP_LSC_WINY2	0x0174_0015

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	invy2			reserved		deltay2	
Reset	0 0 0 0	0 0 0 1	0 1 1 1	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 1 0 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy2	Reciprocal value of the width of the LSC interpolation vertical second window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay2	Width of the LSC interpolation vertical second window

ISP_LSC_WINY3

ISP_LSC_WINY3 is an LSC interpolation vertical third window width information register.

Offset Address	Register Name	Total Reset Value
0x2303C	ISP_LSC_WINY3	0x0111_001D

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	invy3			reserved		deltay3	
Reset	0 0 0 0	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 1	1 1 0 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy3	Reciprocal value of the width of the LSC interpolation vertical third window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay3	Width of the LSC interpolation vertical third window

ISP_LSC_WINY4

ISP_LSC_WINY4 is an LSC interpolation vertical fourth window width information register.

Offset Address	Register Name	Total Reset Value
0x23040	ISP_LSC_WINY4	0x00BA_002B

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	invy4			reserved		deltay4	
Reset	0 0 0 0	0 0 0 0	1 0 1 1	1 0 1 0	0 0 0 0	0 0 0 0	0 0 1 0	1 0 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy4	Reciprocal value of the width of the LSC interpolation vertical fourth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay4	Width of the LSC interpolation vertical fourth window

ISP_LSC_WINY5

ISP_LSC_WINY5 is an LSC interpolation vertical fifth window width information register.

Offset Address	Register Name	Total Reset Value
0x23044	ISP_LSC_WINY5	0x0089_003B

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	invy5			reserved		deltay5	
Reset	0 0 0 0	0 0 0 0	1 0 0 0	1 0 0 1	0 0 0 0	0 0 0 0	0 0 1 1	1 0 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy5	Reciprocal value of the width of the LSC interpolation vertical fifth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay5	Width of the LSC interpolation vertical fifth window

ISP_LSC_WINY6

ISP_LSC_WINY6 is an LSC interpolation vertical sixth window width information register.

Offset Address	Register Name	Total Reset Value
0x23048	ISP_LSC_WINY6	0x0062_0053

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	invy6			reserved		deltay6	
Reset	0 0 0 0	0 0 0 0	0 1 1 0	0 0 1 0	0 0 0 0	0 0 0 0	0 1 0 1	0 0 1 1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy6	Reciprocal value of the width of the LSC interpolation vertical sixth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay6	Width of the LSC interpolation vertical sixth window

ISP_LSC_WINY7

ISP_LSC_WINY7 is an LSC interpolation vertical seventh window width information register.

Offset Address	Register Name	Total Reset Value
0x2304C	ISP_LSC_WINY7	0x0045_0075

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invy7												reserved								deltay7							
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy7	Reciprocal value of the width of the LSC interpolation vertical seventh window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay7	Width of the LSC interpolation vertical seventh window

ISP_LSC_WINY8

ISP_LSC_WINY8 is an LSC interpolation vertical eighth window width information register.

Offset Address	Register Name	Total Reset Value
0x23050	ISP_LSC_WINY8	0x0031_00A5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				invy8												reserved								deltay8							
Reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	invy8	Reciprocal value of the width of the LSC interpolation vertical eighth window
[15:10]	RO	reserved	Reserved
[9:0]	RW	deltay8	Width of the LSC interpolation vertical eighth window

ISP_LSC_BLCEN

ISP_LSC_BLCEN is an LSC input and output black level offset enable register.

Offset Address	Register Name	Total Reset Value
0x23054	ISP_LSC_BLCEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							BLC_out_en	reserved							BLC_in_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8]	RW	BLC_out_en	Output black level enable 0: disabled 1: enabled
[7:1]	-	reserved	Reserved
[0]	RW	BLC_in_en	Input black level enable 0: disabled 1: enabled

ISP_LSC_RBLC

ISP_LSC_RBLC is an LSC R channel black level offset register.

Offset Address	Register Name	Total Reset Value
0x23058	ISP_LSC_RBLC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																BLC_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	BLC_r	Black level data in the R channel

ISP_LSC_GRBLC

ISP_LSC_GRBLC is an LSC Gr channel black level offset register.

Offset Address	Register Name	Total Reset Value
0x2305C	ISP_LSC_GRBLC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																BLC_gr																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	BLC_gr	Black level data in the Gr channel

ISP_LSC_GBBLC

ISP_LSC_GBBLC is an LSC Gb channel black level offset register.

Offset Address	Register Name	Total Reset Value
0x23060	ISP_LSC_GBBLC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																BLC_gb																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	BLC_gb	Black level data in the Gb channel

ISP_LSC_BBLC

ISP_LSC_BBLC is an LSC B channel black level offset register.

Offset Address	Register Name	Total Reset Value
0x23064	ISP_LSC_BBLC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																BLC_b																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	BLC_b	Black level data in the B channel

ISP_LSC_LUT_UPDATE

ISP_LSC_LUT_UPDATE is an LSC gain LUT switch enable register.

Offset Address	Register Name	Total Reset Value
0x23068	ISP_LSC_LUT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															lut_update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	lut_update	LSC LUT switch enable. This bit is automatically cleared for each frame. 0: disabled 1: enabled

ISP_LSC_GRRGAIN_WADDR

ISP_LSC_GRRGAIN_WADDR is an LSC interpolation R/Gr channel gain write address register.

Offset Address	Register Name	Total Reset Value
0x23080	ISP_LSC_GRRGAIN_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	grrgain_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	grrgain_waddr	Write address of the LSC interpolation R/Gr channel gain

ISP_LSC_GRRGAIN_WDATA

ISP_LSC_GRRGAIN_WDATA is an LSC interpolation R/Gr channel gain write data register.

Offset Address	Register Name	Total Reset Value
0x23084	ISP_LSC_GRRGAIN_WDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			grrgain_wdata				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:0]	RW	grrgain_wdata	Write data of the LSC interpolation R/Gr channel gain

ISP_LSC_GRRGAIN_RADDR

ISP_LSC_GRRGAIN_RADDR is an LSC interpolation R/Gr channel gain read address register.

Offset Address	Register Name	Total Reset Value
0x23088	ISP_LSC_GRRGAIN_RADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	grrgain_raddr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	grrgain_raddr	Read address of the LSC interpolation R/Gr channel gain

ISP_LSC_GRRGAIN_RDATA

ISP_LSC_GRRGAIN_RDATA is an LSC interpolation R/Gr channel gain read data register.

Offset Address	Register Name	Total Reset Value
0x2308C	ISP_LSC_GRRGAIN_RDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			grrgain_rdata				
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:0]	RO	grgain_rdata	Read data of the LSC interpolation R/Gr channel gain

ISP_LSC_GBBGAIN_WADDR

ISP_LSC_GBBGAIN_WADDR is an LSC interpolation B/Gb channel gain write address register.

Offset Address	Register Name	Total Reset Value
0x23090	ISP_LSC_GBBGAIN_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gbbgain_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	gbbgain_waddr	Write address of the LSC interpolation B/Gb channel gain

ISP_LSC_GBBGAIN_WDATA

ISP_LSC_GBBGAIN_WDATA is an LSC interpolation B/Gb channel gain write data register.

Offset Address	Register Name	Total Reset Value
0x23094	ISP_LSC_GBBGAIN_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								gbbgain_wdata																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:0]	RW	gbbgain_wdata	Write data of the LSC interpolation B/Gb channel gain

ISP_LSC_GBBGAIN_RADDR

ISP_LSC_GBBGAIN_RADDR is an LSC interpolation B/Gb channel gain read address register.

Offset Address	Register Name	Total Reset Value
0x23098	ISP_LSC_GBBGAIN_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gbbgain_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	gbbgain_raddr	Read address of the LSC interpolation B/Gb channel gain

ISP_LSC_GBBGAIN_RDATA

ISP_LSC_GBBGAIN_RDATA is an LSC interpolation B/Gb channel gain read data register.

Offset Address	Register Name	Total Reset Value
0x2309C	ISP_LSC_GBBGAIN_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								gbbgain_rdata																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:0]	RO	gbbgain_rdata	Read data of the LSC interpolation B/Gb channel gain

ISP_GE_CFG

ISP_GE_CFG is a GE control register.

Offset Address	Register Name	Total Reset Value
0x23900	ISP_GE_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																							ge_cor_en	reserved			ge_aver_en	reserved	reserved	ge1_en	ge0_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RW	ge_cor_en	GE correction enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	ge_aver_en	GE_AVER enable 0: disabled 1: enabled
[3]	RO	reserved	Reserved
[2]	RO	reserved	Reserved

[1]	RW	ge1_en	GE1 enable 0: disabled 1: enabled
[0]	RW	ge0_en	GE0 enable 0: disabled 1: enabled

ISP_GE0_CT_TH1

ISP_GE0_CT_TH1 is a GE0 configuration register.

Offset Address	Register Name	Total Reset Value
0x23910	ISP_GE0_CT_TH1	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge0_ct_th1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	ge0_ct_th1	Threshold

ISP_GE0_CT_TH2

ISP_GE0_CT_TH2 is a GE0 configuration register.

Offset Address	Register Name	Total Reset Value
0x23914	ISP_GE0_CT_TH2	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge0_ct_th2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	ge0_ct_th2	Threshold

ISP_GE0_CT_TH3

ISP_GE0_CT_TH3 is a GE0 configuration register.

Offset Address	Register Name	Total Reset Value
0x23918	ISP_GE0_CT_TH3	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge0_ct_th3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	ge0_ct_th3	Threshold

ISP_GE0_CT_SLOPE

ISP_GE0_CT_SLOPE is a GE0 configuration register.

Offset Address	Register Name	Total Reset Value
0x2391C	ISP_GE0_CT_SLOPE	0x0000_0099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ge0_ct_slope2				ge0_ct_slope1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	ge0_ct_slope2	General correction slope 0x0: 1 0x1: 2 0x2: 4 0x3: 8 … This field can be set to **0xE** at most, and the value 14 indicates 2^{14}.
[3:0]	RW	ge0_ct_slope1	Edge correction slope 0x0: 1 0x1: 2 0x2: 4 0x3: 8 … This field can be set to **0xE** at most, and the value 14 indicates 2^{14}.

ISP_GE1_CT_TH1

ISP_GE1_CT_TH1 is a GE1 configuration register.

Offset Address	Register Name	Total Reset Value
0x23920	ISP_GE1_CT_TH1	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge1_ct_th1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	ge1_ct_th1	Threshold

ISP_GE1_CT_TH2

ISP_GE1_CT_TH2 is a GE1 configuration register.

Offset Address	Register Name	Total Reset Value
0x23924	ISP_GE1_CT_TH2	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge1_ct_th2											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	ge1_ct_th2	Threshold

ISP_GE1_CT_TH3

ISP_GE1_CT_TH3 is a GE1 configuration register.

Offset Address	Register Name	Total Reset Value
0x23928	ISP_GE1_CT_TH3	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ge1_ct_th3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved

[13:0]	RW	ge1_ct_th3	Threshold

ISP_GE1_CT_SLOPE

ISP_GE1_CT_SLOPE is a GE1 configuration register.

Offset Address	Register Name	Total Reset Value
0x2392C	ISP_GE1_CT_SLOPE	0x0000_0099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ge1_ct_slope2				ge1_ct_slope1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:4]	RW	ge1_ct_slope2	General correction slope 0x0: 1 0x1: 2 0x2: 4 0x3: 8 … This field can be set to **0xE** at most, and the value 14 indicates 2^{14}.
[3:0]	RW	ge1_ct_slope1	Edge correction slope 0x0: 1 0x1: 2 0x2: 4 0x3: 8 … This field can be set to **0xE** at most, and the value 14 indicates 2^{14}.

ISP_GE_ZONE

ISP_GE_ZONE is a GE zone configuration register.

Offset Address	Register Name	Total Reset Value
0x23950	ISP_GE_ZONE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12:8]	RW	vnum	Number of zones in the vertical direction
[7:5]	-	reserved	Reserved
[4:0]	RW	hnum	Number of zones in the horizontal direction

ISP_GE_MODE

ISP_GE_MODE is a GE correction mode select register.

Offset Address	Register Name	Total Reset Value
0x23954	ISP_GE_MODE	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																													gr_gb_en	gb_en	gr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2]	RW	gr_gb_en	Gr and Gb correction enable 0: disabled 1: enabled
[1]	RW	gb_en	Gb correction enable 0: disabled 1: enabled
[0]	RW	gr_en	Gr correction enable 0: disabled 1: enabled

ISP_GE_STRENGTH

ISP_GE_STRENGTH is a GE correction strength configuration register.

Offset Address	Register Name	Total Reset Value
0x23958	ISP_GE_STRENGTH	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								strength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8:0]	RW	strength	GE correction strength, U9.0

ISP_GE_MEM_AVER_RADDR0

ISP_GE_MEM_AVER_RADDR0 is GE average value statistics read address register 0.

Offset Address	Register Name	Total Reset Value
0x23988	ISP_GE_MEM_AVER_RADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver0_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	aver0_raddr	Read address of the GE average value statistics

ISP_GE_MEM_AVER_RDATA0

ISP_GE_MEM_AVER_RDATA0 is GE average value statistics read data register 0.

Offset Address	Register Name	Total Reset Value
0x2398C	ISP_GE_MEM_AVER_RDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	aver0_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	aver0_rdata	Read data of the GE average value statistics

ISP_GE_MEM_AVER_RADDR1

ISP_GE_MEM_AVER_RADDR1 is GE average value statistics read address register 1.

Offset Address	Register Name	Total Reset Value
0x23998	ISP_GE_MEM_AVER_RADDR1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	aver1_raddr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	aver1_raddr	Read address of the GE average value statistics

ISP_GE_MEM_AVER_RDATA1

ISP_GE_MEM_AVER_RDATA1 is GE average value statistics read data register 1.

Offset Address	Register Name	Total Reset Value
0x2399C	ISP_GE_MEM_AVER_RDATA1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	aver1_rdata							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	aver1_rdata	Read data of the GE average value statistics

ISP_GE_SIZE

ISP_GE_SIZE is a GE picture size register.

Offset Address	Register Name	Total Reset Value
0x239F0	ISP_GE_SIZE	0x0437_077F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	height			reserved	width		
Reset	0 0 0 0	0 1 0 0	0 0 1 1	0 1 1 1	0 0 0 0	0 1 1 1	0 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved

[28:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, if the actual picture height is 1080, set this field to 1079.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, if the actual picture width is 1920, set this field to 1919.

ISP_FPN_CFG

ISP_FPN_CFG is an FPN configuration register.

Offset Address	Register Name	Total Reset Value
0x23A00	ISP_FPN_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10	9	8	7 6 5 4	3 2 1	0
Name	reserved						line_frame	calib_corr	reserved		enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	line_frame	FPN frame/line mode 0: frame mode 1: line mode
[8]	RW	calib_corr	FPN correction/calibration mode 0: correction mode 1: calibration mode
[7:1]	RO	reserved	Reserved
[0]	RW	enable	FPN enable 0: disabled 1: enabled

ISP_FPN_CALIB_START

ISP_FPN_CALIB_START is an FPN calibration start signal register.

Offset Address	Register Name	Total Reset Value
0x23A04	ISP_FPN_CALIB_START	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								calib_start
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	calib_start	FPN calibration start. This bit is automatically cleared.

ISP_FPN_CORR_CFG

ISP_FPN_CORR_CFG is an FPN correction enable register.

Offset Address	Register Name	Total Reset Value
0x23A08	ISP_FPN_CORR_CFG	0x0000_000F

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								correct0_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	correct0_en	FPN correction enable for channel 0 0: disabled 1: enabled

ISP_FPN_STAT

ISP_FPN_STAT is an FPN calibration status register.

Offset Address	Register Name	Total Reset Value
0x23A0C	ISP_FPN_STAT	0xFFFF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hcnt																reserved				vcnt				reserved							busy
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	hcnt	Number of lines
[15:14]	RO	reserved	Reserved
[13:8]	RO	vcnt	Number of calibrated frames
[7:1]	RO	reserved	Reserved
[0]	RO	busy	FPN calibration status 0: idle 1: being calibrated

ISP_FPN_WHITE_LEVEL

ISP_FPN_WHITE_LEVEL is an FPN calibration white point configuration register.

Offset Address	Register Name	Total Reset Value
0x23A10	ISP_FPN_WHITE_LEVEL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				white_level											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	white_level	FPN calibration white point configuration

ISP_FPN_DIVCOEF

ISP_FPN_DIVCOEF is an FPN calibration division coefficient register.

Offset Address	Register Name	Total Reset Value
0x23A18	ISP_FPN_DIVCOEF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				divcoef											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	divcoef	FPN calibration division coefficient

ISP_FPN_FRAMELOG2

ISP_FPN_FRAMELOG2 is an FPN calibrated frame number register.

Offset Address	Register Name	Total Reset Value
0x23A1C	ISP_FPN_FRAMELOG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cpi_fpn_framelog2	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	cpi_fpn_framelog2	Number of FPN calibrated frames. The configured value is obtained by taking the logarithm of the number of frames to 2.

ISP_FPN_SUM0

ISP_FPN_SUM0 is an FPN calibration accumulated sum lower bits register.

Offset Address	Register Name	Total Reset Value
0x23A20	ISP_FPN_SUM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Lower bits of the FPN calibration accumulated sum

ISP_FPN_SUM1

ISP_FPN_SUM1 is an FPN calibration accumulated sum upper bits register.

Offset Address	Register Name	Total Reset Value
0x23A24	ISP_FPN_SUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Upper bits of the FPN calibration accumulated sum

ISP_FPN_CORR0

ISP_FPN_CORR0 is FPN correction configuration register 0.

Offset Address	Register Name	Total Reset Value
0x23A30	ISP_FPN_CORR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength (U8.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction bias

ISP_FPN_CORR1

ISP_FPN_CORR1 is FPN correction configuration register 1.

Offset Address	Register Name	Total Reset Value
0x23A34	ISP_FPN_CORR1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	strength				reserved	offset		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength (U8.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction bias

ISP_FPN_CORR2

ISP_FPN_CORR2 is FPN correction configuration register 2.

Offset Address	Register Name	Total Reset Value
0x23A38	ISP_FPN_CORR2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	strength				reserved	offset		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength (U8.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction bias

ISP_FPN_CORR3

ISP_FPN_CORR3 is FPN correction configuration register 3.

Offset Address	Register Name	Total Reset Value
0x23A3C	ISP_FPN_CORR3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	strength																reserved				offset											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	strength	FPN correction strength (U8.8)
[15:12]	RO	reserved	Reserved
[11:0]	RW	offset	FPN correction bias

ISP_FPN_SHIFT

ISP_FPN_SHIFT is an FPN shift configuration register.

Offset Address	Register Name	Total Reset Value
0x23A40	ISP_FPN_SHIFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				frame_calib_shift				reserved				out_shift				reserved				in_shift				reserved				fpn_shift			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:24]	RW	frame_calib_shift	Number of left shift bits for the last output frame during frame calibration
[23:20]	RO	reserved	Reserved
[19:16]	RW	out_shift	Number of left shift bits for the output
[15:12]	RO	reserved	Reserved
[11:8]	RW	in_shift	Number of right shift bits for the input
[7:4]	RO	reserved	Reserved
[3:0]	RW	fpn_shift	Number of right shift bits for the input FPN

ISP_FPN_MAX_O

ISP_FPN_MAX_O is an FPN maximum output value register.

Offset Address	Register Name	Total Reset Value
0x23A50	ISP_FPN_MAX_O	0x0000_3FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																max_o															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	max_o	Maximum value of the FPN output

ISP_FPN_OVERFLOWTHR

ISP_FPN_OVERFLOWTHR is an FPN correction threshold register.

Offset Address	Register Name	Total Reset Value
0x23A54	ISP_FPN_OVERFLOWTHR	0x0000_3FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				overflowthr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:0]	RW	overflowthr	FPN correction threshold

ISP_FPN_LINE_WADDR

ISP_FPN_LINE_WADDR is an FPN line mode black line write address register.

Offset Address	Register Name	Total Reset Value
0x23A80	ISP_FPN_LINE_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	fpn_line_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_waddr	Write address of the black line in FPN line mode

ISP_FPN_LINE_WDATA

ISP_FPN_LINE_WDATA is an FPN line mode black line write data register.

Offset Address	Register Name	Total Reset Value
0x23A84	ISP_FPN_LINE_WDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fpn_line_wdata							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_wdata	Write data of the black line in FPN line mode

ISP_FPN_LINE_RADDR

ISP_FPN_LINE_RADDR is an FPN line mode black line read address register.

Offset Address	Register Name	Total Reset Value
0x23A88	ISP_FPN_LINE_RADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fpn_line_raddr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_raddr	Read address of the black line in FPN line mode

ISP_FPN_LINE_RDATA

ISP_FPN_LINE_RDATA is an FPN line mode black line read data register.

Offset Address	Register Name	Total Reset Value
0x23A8C	ISP_FPN_LINE_RDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fpn_line_rdata							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	fpn_line_rdata	Read data of the black line in FPN line mode

ISP_FPN_SIZE

ISP_FPN_SIZE is an FPN picture size register.

Offset Address	Register Name	Total Reset Value
0x23AF0	ISP_FPN_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	height																width															
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, if the actual picture height is 1080, set this field to 1079.
[15:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, if the actual picture width is 1920, set this field to 1919.

ISP_DPC_CFG

ISP_DPC_CFG is a DPC control register.

Offset Address	Register Name	Total Reset Value
0x23C00	ISP_DPC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														en1	en0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	en1	DPC1 enable 0: disabled 1: enabled
[0]	RW	en0	DPC0 enable 0: disabled 1: enabled

ISP_DCG_MODE

ISP_DCG_MODE is a DCG working mode select register.

Offset Address	Register Name	Total Reset Value
0x23C04	ISP_DCG_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1:0]	RW	mode	DCG working mode select 00: Only ge0, dpc0, and cac0 can be enabled. 01: ge0 and ge1 are enabled and disabled together, dpc0 and dpc1 are enabled and disabled together, and cac0 and cac1 are enabled and disabled together. 10 and 11: invalid

ISP_DPC_ALPHA

ISP_DPC_ALPHA is a DPC blending ratio register.

Offset Address	Register Name	Total Reset Value
0x23C08	ISP_DPC_ALPHA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	alpha0_rb		alpha0_g		alpha1_rb		alpha1_g	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	alpha0_rb	Blending ratio of the R/B component 5-point median filtering result to the 9-point median filtering result
[23:16]	RW	alpha0_g	Blending ratio of the G component 5-point median filtering result to the 9-point median filtering result
[15:8]	RW	alpha1_rb	Blending ratio of the R/B component input to the median filtering result
[7:0]	RW	alpha1_g	Blending ratio of the G component input to the median filtering result

ISP_DPC_MODE

ISP_DPC_MODE is a DPC mode register.

Offset Address	Register Name	Total Reset Value
0x23C10	ISP_DPC_MODE	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						ir_channel	ir_position	dp_hightlight_en	dpt_det_sel	bpt_cor_en	grayscale_mode	bpt_update	six_det_en	cor_en	det_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	ir_channel	IR channel enable 0: disabled. The Bayer format is used. 1: enabled. The RGBIR format is used.
[8]	RW	ir_position	IR channel select 0: The IR uses the Gb channel. 1: The IR uses the Gr channel.
[7]	RW	dp_hightlight_en	Defect pixel highlight enable 0: disabled 1: enabled
[6]	RW	dpt_det_sel	Defect pixel table detection select 0: The bright dots are detected. 1: The dark dots are detected.
[5]	RW	bpt_cor_en	Defect pixel table correction enable 0: disabled 1: enabled
[4]	RW	grayscale_mode	Mode of the gray scale image 0: raw data 1: gray scale image
[3]	RW	bpt_update	Defect pixel table calibration enable 0: disabled 1: enabled
[2]	RW	six_det_en	Maximum/Minimum value detection, used only during defect pixel table calibration 0: disabled 1: enabled

[1]	RW	cor_en	Dynamic correction enable 0: disabled 1: enabled
[0]	RW	det_en	Dynamic detection enable 0: disabled 1: enabled

ISP_DPC_OUTPUT_MODE

ISP_DPC_OUTPUT_MODE is a dynamic correction mode register.

Offset Address	Register Name	Total Reset Value
0x23C14	ISP_DPC_OUTPUT_MODE	0x0000_0003

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved							stage1_incl_rb_3x3	stage1_incl_g_3x3	stage1_incl_rb_center	stage1_incl_gr_center
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	stage1_incl_rb_3x3	Whether the R/B point correction uses the 9-point median 0: no 1: yes
[2]	RW	stage1_incl_g_3x3	Whether the G point correction uses the 9-point median 0: no 1: yes
[1]	RW	stage1_incl_rb_center	Whether the R/B point correction contains the central point 0: no 1: yes
[0]	RW	stage1_incl_gr_center	Whether the G point correction contains the central point 0: no 1: yes

ISP_DPC_SET_USE

ISP_DPC_SET_USE is a dynamic detection level register.

Offset Address	Register Name	Total Reset Value
0x23C18	ISP_DPC_SET_USE	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												stage1_use_fix_set	stage1_use_set3	stage1_use_set2	stage1_use_set1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3]	RW	stage1_use_fix_set	Whether other detection levels are valid 0: no 1: yes
[2]	RW	stage1_use_set3	Whether detection level 3 is valid 0: no 1: yes
[1]	RW	stage1_use_set2	Whether detection level 2 is valid 0: no 1: yes
[0]	RW	stage1_use_set1	Whether detection level 1 is valid 0: no 1: yes

ISP_DPC_METHODS_SET_1

ISP_DPC_METHODS_SET_1 is detection switch register 1.

Offset Address	Register Name	Total Reset Value
0x23C1C	ISP_DPC_METHODS_SET_1	0x0000_1F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			rg_red_blue1_enable	rnd_red_blue1_enable	ro_red_blue1_enable	lc_red_blue1_enable	pg_red_blue1_enable	reserved				rg_green1_enable	rnd_green1_enable	ro_green1_enable	lc_green1_enable	pg_green1_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	rg_red_blue1_enable	R/B point level 1 gradient sorting detection enable 0: disabled 1: enabled
[11]	RW	rnd_red_blue1_enable	R/B point level 1 adjacent difference sorting detection enable 0: disabled 1: enabled
[10]	RW	ro_red_blue1_enable	R/B point level 1 sorting detection enable 0: disabled 1: enabled
[9]	RW	lc_red_blue1_enable	R/B point level 1 linear detection enable 0: disabled 1: enabled
[8]	RW	pg_red_blue1_enable	R/B point level 1 peak value gradient detection enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	rg_green1_enable	G point level 1 gradient sorting detection enable 0: disabled 1: enabled
[3]	RW	rnd_green1_enable	G point level 1 adjacent difference sorting detection enable 0: disabled 1: enabled

[2]	RW	ro_green1_enable	G point level 1 sorting detection enable 0: disabled 1: enabled
[1]	RW	lc_green1_enable	G point level 1 linear detection enable 0: disabled 1: enabled
[0]	RW	pg_green1_enable	G point level 1 peak value gradient detection enable 0: disabled 1: enabled

ISP_DPC_METHODS_SET_2

ISP_DPC_METHODS_SET_2 is detection switch register 2.

Offset Address	Register Name	Total Reset Value
0x23C20	ISP_DPC_METHODS_SET_2	0x0000_0707

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rg_red_blue2_enable	rnd_red_blue2_enable	ro_red_blue2_enable	lc_red_blue2_enable	pg_red_blue2_enable	reserved				rg_green2_enable	rnd_green2_enable	ro_green2_enable	lc_green2_enable	pg_green2_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	rg_red_blue2_enable	R/B point level 2 gradient sorting detection enable 0: disabled 1: enabled
[11]	RW	rnd_red_blue2_enable	R/B point level 2 adjacent difference sorting detection enable 0: disabled 1: enabled
[10]	RW	ro_red_blue2_enable	R/B point level 2 sorting detection enable 0: disabled 1: enabled

[9]	RW	lc_red_blue2_enable	R/B point level 2 linear detection enable 0: disabled 1: enabled
[8]	RW	pg_red_blue2_enable	R/B point level 2 peak value gradient detection enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	rg_green2_enable	G point level 2 gradient sorting detection enable 0: disabled 1: enabled
[3]	RW	rnd_green2_enable	G point level 2 adjacent difference sorting detection enable 0: disabled 1: enabled
[2]	RW	ro_green2_enable	G point level 2 sorting detection enable 0: disabled 1: enabled
[1]	RW	lc_green2_enable	G point level 2 linear detection enable 0: disabled 1: enabled
[0]	RW	pg_green2_enable	G point level 2 peak value gradient detection enable 0: disabled 1: enabled

ISP_DPC_METHODS_SET_3

ISP_DPC_METHODS_SET_3 is detection switch register 3.

Offset Address	Register Name	Total Reset Value
0x23C24	ISP_DPC_METHODS_SET_3	0x0000_1F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			rg_red_blue3_enable	rnd_red_blue3_enable	ro_red_blue3_enable	lc_red_blue3_enable	pg_red_blue3_enable	reserved			rg_green3_enable	rnd_green3_enable	ro_green3_enable	lc_green3_enable	pg_green3_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	rg_red_blue3_enable	R/B point level 3 gradient sorting detection enable 0: disabled 1: enabled
[11]	RW	rnd_red_blue3_enable	R/B point level 3 adjacent difference sorting detection enable 0: disabled 1: enabled
[10]	RW	ro_red_blue3_enable	R/B point level 3 sorting detection enable 0: disabled 1: enabled
[9]	RW	lc_red_blue3_enable	R/B point level 3 linear detection enable 0: disabled 1: enabled
[8]	RW	pg_red_blue3_enable	R/B point level 3 peak value gradient detection enable 0: disabled 1: enabled
[7:5]	RO	reserved	Reserved
[4]	RW	rg_green3_enable	G point level 3 gradient sorting detection enable 0: disabled 1: enabled
[3]	RW	rnd_green3_enable	G point level 3 adjacent difference sorting detection enable 0: disabled 1: enabled

[2]	RW	ro_green3_enable	G point level 3 sorting detection enable 0: disabled 1: enabled
[1]	RW	lc_green3_enable	G point level 3 linear detection enable 0: disabled 1: enabled
[0]	RW	pg_green3_enable	G point level 3 peak value gradient detection enable 0: disabled 1: enabled

ISP_DPC_LINE_THRESH_1

ISP_DPC_LINE_THRESH_1 is a linear detection parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x23C28	ISP_DPC_LINE_THRESH_1	0x0000_0808

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																line_thr1_rb								line_thr1_g							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	line_thr1_rb	R/B point detection parameter
[7:0]	RW	line_thr1_g	G point detection parameter

ISP_DPC_LINE_MAD_FAC_1

ISP_DPC_LINE_MAD_FAC_1 is a linear detection parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x23C2C	ISP_DPC_LINE_MAD_FAC_1	0x0000_1B1B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				line_mad_fac_1_rb				reserved				line_mad_fac_1_g			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	line_mad_fac_1_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	line_mad_fac_1_g	G point detection parameter

ISP_DPC_PG_FAC_1

ISP_DPC_PG_FAC_1 is a peak gradient parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x23C30	ISP_DPC_PG_FAC_1	0x0000_0808

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pg_fac_1_rb				reserved				pg_fac_1_g			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	pg_fac_1_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	pg_fac_1_g	G point detection parameter

ISP_DPC_RND_THRESH_1

ISP_DPC_RND_THRESH_1 is an adjacent difference value sorting parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x23C34	ISP_DPC_RND_THRESH_1	0x0000_0A0A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rnd_thr1_rb								rnd_thr1_g							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	rnd_thr1_rb	R/B point detection parameter
[7:0]	RW	rnd_thr1_g	G point detection parameter

ISP_DPC_RG_FAC_1

ISP_DPC_RG_FAC_1 is a gradient sorting parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x23C38	ISP_DPC_RG_FAC_1	0x0000_2626

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		rg_fac_1_rb						reserved		rg_fac_1_g					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	rg_fac_1_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	rg_fac_1_g	G point detection parameter

ISP_DPC_LINE_THRESH_2

ISP_DPC_LINE_THRESH_2 is a linear detection parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x23C3C	ISP_DPC_LINE_THRESH_2	0x0000_2121

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																line_thr2_rb								line_thr2_g							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	line_thr2_rb	R/B point detection parameter
[7:0]	RW	line_thr2_g	G point detection parameter

ISP_DPC_LINE_MAD_FAC_2

ISP_DPC_LINE_MAD_FAC_2 is a linear detection parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x23C40	ISP_DPC_LINE_MAD_FAC_2	0x0000_1810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				line_mad_fac_2_rb				reserved				line_mad_fac_2_g			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	line_mad_fac_2_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	line_mad_fac_2_g	G point detection parameter

ISP_DPC_PG_FAC_2

ISP_DPC_PG_FAC_2 is a peak gradient parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x23C44	ISP_DPC_PG_FAC_2	0x0000_0B0B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pg_fac_2_rb				reserved				pg_fac_2_g			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	pg_fac_2_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	pg_fac_2_g	G point detection parameter

ISP_DPC_RND_THRESH_2

ISP_DPC_RND_THRESH_2 is an adjacent difference value sorting parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x23C48	ISP_DPC_RND_THRESH_2	0x0000_0808

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rnd_thr2_rb								rnd_thr2_g							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	rnd_thr2_rb	R/B point detection parameter
[7:0]	RW	rnd_thr2_g	G point detection parameter

ISP_DPC_RG_FAC_2

ISP_DPC_RG_FAC_2 is a gradient sorting parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x23C4C	ISP_DPC_RG_FAC_2	0x0000_0808

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rg_fac_2_rb				reserved				rg_fac_2_g			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	rg_fac_2_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	rg_fac_2_g	G point detection parameter

ISP_DPC_LINE_THRESH_3

ISP_DPC_LINE_THRESH_3 is a linear detection parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x23C50	ISP_DPC_LINE_THRESH_3	0x0000_2020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																line_thr3_rb								line_thr3_g							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	line_thr3_rb	R/B point detection parameter
[7:0]	RW	line_thr3_g	G point detection parameter

ISP_DPC_LINE_MAD_FAC_3

ISP_DPC_LINE_MAD_FAC_3 is a linear detection parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x23C54	ISP_DPC_LINE_MAD_FAC_3	0x0000_0404

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					line_mad_fac_3_rb	reserved	line_mad_fac_3_g
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	line_mad_fac_3_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	line_mad_fac_3_g	G point detection parameter

ISP_DPC_PG_FAC_3

ISP_DPC_PG_FAC_3 is a peak gradient parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x23C58	ISP_DPC_PG_FAC_3	0x0000_0A0A

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					pg_fac_3_rb	reserved	pg_fac_3_g
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 1 0	0 0 0 0	1 0 1 0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	pg_fac_3_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	pg_fac_3_g	G point detection parameter

ISP_DPC_RND_THRESH_3

ISP_DPC_RND_THRESH_3 is an adjacent difference value sorting parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x23C5C	ISP_DPC_RND_THRESH_3	0x0000_0806

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rnd_thr3_rb								rnd_thr3_g							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RW	rnd_thr3_rb	R/B point detection parameter
[7:0]	RW	rnd_thr3_g	G point detection parameter

ISP_DPC_RG_FAC_3

ISP_DPC_RG_FAC_3 is a gradient sorting parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x23C60	ISP_DPC_RG_FAC_3	0x0000_0404

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			rg_fac_3_rb					reserved				rg_fac_3_g			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:14]	RO	reserved	Reserved
[13:8]	RW	rg_fac_3_rb	R/B point detection parameter
[7:6]	RO	reserved	Reserved
[5:0]	RW	rg_fac_3_g	G point detection parameter

ISP_DPC_RO_LIMITS

ISP_DPC_RO_LIMITS is a sorting parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x23C64	ISP_DPC_RO_LIMITS	0x0000_09A5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				ro_3_rb		ro_3_g		ro_2_rb		ro_2_g		ro_1_rb		ro_1_g	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	1	0	1

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:10]	RW	ro_3_rb	R/B point detection parameter
[9:8]	RW	ro_3_g	G point detection parameter
[7:6]	RW	ro_2_rb	R/B point detection parameter
[5:4]	RW	ro_2_g	G point detection parameter
[3:2]	RW	ro_1_rb	R/B point detection parameter
[1:0]	RW	ro_1_g	G point detection parameter

ISP_DPC_RND_OFFS

ISP_DPC_RND_OFFS is an adjacent difference value sorting parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x23C68	ISP_DPC_RND_OFFS	0x0000_0AAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rnd_offs_3_rb		rnd_offs_3_g		rnd_offs_2_rb		rnd_offs_2_g		rnd_offs_1_rb		rnd_offs_1_g	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:10]	RW	rnd_offs_3_rb	R/B point detection parameter
[9:8]	RW	rnd_offs_3_g	G point detection parameter
[7:6]	RW	rnd_offs_2_rb	R/B point detection parameter

[5:4]	RW	rnd_offs_2_g	G point detection parameter
[3:2]	RW	rnd_offs_1_rb	R/B point detection parameter
[1:0]	RW	rnd_offs_1_g	G point detection parameter

ISP_DPC_BPT_CTRL

ISP_DPC_BPT_CTRL is a defect pixel table control register.

Offset Address	Register Name	Total Reset Value
0x23C6C	ISP_DPC_BPT_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11	10	9	8	7	6	5	4	3 2 1 0
Name	bp_data				reserved	rb_3x3	g_3x3	bpt_incl_rb_center	bpt_incl_green_center	bpt_use_fix_set	bpt_use_set_3	bpt_use_set_2	bpt_use_set_1	reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0	0	0	0	0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	bp_data	Defect pixel highlight value
[15:12]	RO	reserved	Reserved
[11]	RW	rb_3x3	Whether the R/B point correction uses the 9-point median 0: no 1: yes
[10]	RW	g_3x3	Whether the G point correction uses the 9-point median 0: no 1: yes
[9]	RW	bpt_incl_rb_center	Whether the R/B point correction contains the central point 0: no 1: yes
[8]	RW	bpt_incl_green_center	Whether the G point correction contains the central point 0: no 1: yes
[7]	RW	bpt_use_fix_set	Whether other detection levels are valid 0: no 1: yes

[6]	RW	bpt_use_set_3	Whether detection level 3 is valid 0: no 1: yes
[5]	RW	bpt_use_set_2	Whether detection level 2 is valid 0: no 1: yes
[4]	RW	bpt_use_set_1	Whether detection level 1 is valid 0: no 1: yes
[3:0]	RO	reserved	Reserved

ISP_DPC_BPT_NUMBER

ISP_DPC_BPT_NUMBER is a defect pixel number register.

Offset Address	Register Name	Total Reset Value
0x23C70	ISP_DPC_BPT_NUMBER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				bpt_number											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	bpt_number	Number of defect pixels. The value range is 0–2048.

ISP_DPC_BPT_CALIB_NUMBER

ISP_DPC_BPT_CALIB_NUMBER is a calibrated defect pixel number register.

Offset Address	Register Name	Total Reset Value
0x23C74	ISP_DPC_BPT_CALIB_NUMBER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				bpt_calib_number											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	bpt_calib_number	Number of calibrated defect pixels. The value range is 0–2048.

ISP_DPC_BPT_THRD

ISP_DPC_BPT_THRD is a calibrated defect pixel parameter register.

Offset Address	Register Name	Total Reset Value
0x23C7C	ISP_DPC_BPT_THRD	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	abs_hot_thresh		dev_hot_thresh		abs_dead_thresh		dev_dead_thresh	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	abs_hot_thresh	Absolute threshold for the bright defect pixel (U8.0). The current pixel is not detected if its value is less than this threshold.
[23:16]	RW	dev_hot_thresh	Offset threshold percentage for the bright defect pixel (U8.0). If the ratio of the absolute value of the difference between the value of the current pixel and the average value of its neighboring pixels to the value of the current pixel is less than or equal to this threshold, the current pixel is considered a non-defect pixel. The field value indicates a percentage number, and the value 128 indicates 100%.
[15:8]	RW	abs_dead_thresh	Absolute threshold for the dark defect pixel (U8.0). The current pixel is considered a non-defect pixel if its value is greater than this threshold.
[7:0]	RW	dev_dead_thresh	Offset threshold percentage for the dark defect pixel (U8.0). If the ratio of the absolute value of the difference between the value of the current pixel and the average value of its neighboring pixels to the average value of its neighboring pixels is less than or equal to this threshold, the current pixel is considered a non-defect pixel. The field value indicates a percentage number, and the value 128 indicates 100%.

ISP_DPC_BPT_WADDR

ISP_DPC_BPT_WADDR is a defect pixel table write address register.

Offset Address	Register Name	Total Reset Value
0x23C80	ISP_DPC_BPT_WADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	bpt_waddr							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	bpt_waddr	Write address of the defect pixel table (bit [10:0])

ISP_DPC_BPT_WDATA

ISP_DPC_BPT_WDATA is a defect pixel table write data register.

Offset Address	Register Name	Total Reset Value
0x23C84	ISP_DPC_BPT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bpt_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	bpt_wdata	Write data of the defect pixel table. Bit [24:0] indicate the defect pixel coordinate.

ISP_DPC_BPT_RADDR

ISP_DPC_BPT_RADDR is a defect pixel table read address register.

Offset Address	Register Name	Total Reset Value
0x23C88	ISP_DPC_BPT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bpt_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	bpt_raddr	Read address of the defect pixel table (bit [10:0])

ISP_DPC_BPT_RDATA

ISP_DPC_BPT_RDATA is a defect pixel table read data register.

Offset Address	Register Name	Total Reset Value
0x23C8C	ISP_DPC_BPT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bpt_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	bpt_rdata	Read data of the defect pixel table. Bit [24:0] indicate the defect pixel coordinate.

ISP_DPC_SIZE

ISP_DPC_SIZE is a DPC picture size register.

Offset Address	Register Name	Total Reset Value
0x23CF0	ISP_DPC_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, for the 1080P picture, set the height to 1079.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, for the 1080P picture, set the width to 1919.

ISP_DPC_SOFT_THR

ISP_DPC_SOFT_THR is a DPC soft correction threshold register.

Offset Address	Register Name	Total Reset Value
0x23D10	ISP_DPC_SOFT_THR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																soft_thr_max								soft_thr_min							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	reserved	Reserved
[15:8]	RW	soft_thr_max	Maximum DPC soft threshold, signed 8.0-bit, two's complement
[7:0]	RW	soft_thr_min	Minimum DPC soft threshold, signed 8.0-bit, two's complement

ISP_DPC_BHARDTHR_EN

ISP_DPC_BHARDTHR_EN is a DPC hard correction enable register.

Offset Address	Register Name	Total Reset Value
0x23D14	ISP_DPC_BHARDTHR_EN	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															hard_thr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	hard_thr_en	DPC hard correction enable 0: disabled 1: enabled

ISP_DPC_RAKERATIO

ISP_DPC_RAKERATIO is a DPC soft correction curve slope register.

Offset Address	Register Name	Total Reset Value
0x23D18	ISP_DPC_RAKERATIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						rake_ratio									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved
[9:0]	RW	rake_ratio	Slope of the DPC soft correction curve, unsigned 8.2

ISP_BNR_CFG

ISP_BNR_CFG is a BAYERNR control register.

Offset Address	Register Name	Total Reset Value
0x25400	ISP_BNR_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															bnr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	bnr_en	BAYERNR enable 0: disabled 1: enabled

ISP_BNR_VERSION

ISP_BNR_VERSION is a BAYERNRR version register.

Offset Address	Register Name	Total Reset Value
0x2540C	ISP_BNR_VERSION	0x0010_0208

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	version																															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:0]	RO	version	BAYERNR logic version

ISP_BNR_CRATIO

ISP_BNR_CRATIO is a BAYERNR blending coefficient register.

Offset Address	Register Name	Total Reset Value
0x25410	ISP_BNR_CRATIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bg_bnr_cratio				reserved				gb_bnr_cratio				reserved				gr_bnr_cratio				reserved				rg_bnr_cratio			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:24]	RW	bg_bnr_cratio	Blending coefficient of the BAYERNR BG component.0 is the origin and 32 is the average point. The format is U6.0 and the value range is [0, 32].
[23:22]	-	reserved	Reserved
[21:16]	RW	gb_bnr_cratio	Blending coefficient of the BAYERNR GB component.0 is the origin and 32 is the average point. The format is U6.0 and the value range is [0, 32].
[15:14]	-	reserved	Reserved
[13:8]	RW	gr_bnr_cratio	Blending coefficient of the BAYERNR GR component.0 is the origin and 32 is the average point. The format is U6.0 and the value range is [0, 32].
[7:6]	-	reserved	Reserved
[5:0]	RW	rg_bnr_cratio	Blending coefficient of the BAYERNR RG component.0 is the origin and 32 is the average point. The format is U6.0 and the value range is [0, 32].

ISP_BNR_LEV

ISP_BNR_LEV is a BAYERNR chrominance median filtering level register.

Offset Address	Register Name	Total Reset Value
0x25414	ISP_BNR_LEV	0x0100_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bg_amed_mode	gb_amed_mode	gr_amed_mode	rg_amed_mode	reserved		bg_amed_lev		reserved				gb_amed_lev				reserved				gr_amed_lev				reserved				rg_amed_lev			
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	bg_amed_mode	Chrominance median filtering mode of the BAYERNR BG component 0: 5x5 window data filtering 1: 9x9 window data filtering
[30]	RW	gb_amed_mode	Chrominance median filtering mode of the BAYERNR GB component 0: 5x5 window data filtering 1: 9x9 window data filtering
[29]	RW	gr_amed_mode	Chrominance median filtering mode of the BAYERNR GR component 0: 5x5 window data filtering 1: 9x9 window data filtering
[28]	RW	rg_amed_mode	Chrominance median filtering mode of the BAYERNR RG component 0: 5x5 window data filtering 1: 9x9 window data filtering
[27:26]	-	reserved	Reserved
[25:24]	RW	bg_amed_lev	BAYERNR chrominance median filtering strength of the B component 00: median filtering disabled 01: standard median filtering 10: high-offset median filtering 11: low-offset median filtering
[23:18]	-	reserved	Reserved

[17:16]	RW	gb_amed_lev	BAYERNR chrominance median filtering strength 00: median filtering disabled 01: standard median filtering 10: high-offset median filtering 11: low-offset median filtering
[15:10]	-	reserved	Reserved
[9:8]	RW	gr_amed_lev	BAYERNR chrominance median filtering strength 00: median filtering disabled 01: standard median filtering 10: high-offset median filtering 11: low-offset median filtering
[7:2]	-	reserved	Reserved
[1:0]	RW	rg_amed_lev	BAYERNR chrominance median filtering strength 00: median filtering disabled 01: standard median filtering 10: high-offset median filtering 11: low-offset median filtering

ISP_BNR_GAIN

ISP_BNR_GAIN is a BAYERNR luminance accumulation coefficient register.

Offset Address	Register Name	Total Reset Value
0x2541C	ISP_BNR_GAIN	0x0000_0052

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bnr_jnlm_gain							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	bnr_jnlm_gain	BAYERNR luminance accumulation coefficient. The format is U8.0 and the value range is [0, 128].

ISP_BNR_SYMCOEF

ISP_BNR_SYMCOEF is a BAYERNR symmetric filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x25420	ISP_BNR_SYMCOEF	0x0000_002D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bnr_jnlm_symcoef							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	bnr_jnlm_symcoef	BAYERNR symmetric filtering coefficient. The format is U8.0 and the value range is [0, 255].

ISP_BNR_CORING

ISP_BNR_CORING is a BAYERNR truncation coefficient register.

Offset Address	Register Name	Total Reset Value
0x25424	ISP_BNR_CORING	0x0300_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				bnr_coring_hig												reserved															
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:16]	RW	bnr_coring_hig	BAYERNR truncation upper limit. The format is U14.0 and the value range is [0, 16383].
[15:0]	-	reserved	Reserved

ISP_BNR_FRMNUM

ISP_BNR_FRMNUM is a BAYERNR blending frame number register.

Offset Address	Register Name	Total Reset Value
0x25428	ISP_BNR_FRMNUM	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							frm_num
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2:0]	RW	frm_num	Number of BAYERNR blending frames 000: 0 001: 1 010: 2 011: 3 100: 4 Other values: invalid

ISP_BNR_LUT_UPDATE

ISP_BNR_LUT_UPDATE is a BAYERNR LUT switch enable register.

Offset Address	Register Name	Total Reset Value
0x2542C	ISP_BNR_LUT_UPDATE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							lut_update
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	lut_update	BAYERNR LUT switch enable. This bit is automatically cleared for each frame. 0: disabled 1: enabled

ISP_BNR_SATU0

ISP_BNR_SATU0 is a BAYERNR saturation denoising coefficient register.

Offset Address	Register Name	Total Reset Value
0x25434	ISP_BNR_SATU0	0x0000_008C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								bnr_satu_ratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8:0]	RW	bnr_satu_ratio	BAYERNR saturation denoising coefficient. The format is U9.0 and the value range is [0, 511].

ISP_BNR_SATU1

ISP_BNR_SATU1 is a BAYERNR saturation threshold 1 register.

Offset Address	Register Name	Total Reset Value
0x25438	ISP_BNR_SATU1	0x006E_0055

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bnr_satu_thhig1								reserved								bnr_satu_thlow1							
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	bnr_satu_thhig1	BAYERNR saturation high threshold 1. The format is U9.0 and the value range is [bnr_satu_thlow1 + 1, 256].
[15:9]	-	reserved	Reserved
[8:0]	RW	bnr_satu_thlow1	BAYERNR saturation low threshold 1. The format is U9.0 and the value range is [0, bnr_satu_thhig1 – 1].

ISP_BNR_SATU2

ISP_BNR_SATU2 is a BAYERNR saturation threshold 2 register.

Offset Address	Register Name	Total Reset Value
0x2543C	ISP_BNR_SATU2	0x00B4_008C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bnr_satu_thhig2								reserved								bnr_satu_thlow2							
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	bnr_satu_thhig2	BAYERNR saturation high threshold 2. The format is U9.0 and the value range is [bnr_satu_thlow2 + 1, 256].
[15:9]	-	reserved	Reserved
[8:0]	RW	bnr_satu_thlow2	BAYERNR saturation low threshold 2. The format is U9.0 and the value range is [0, bnr_satu_thhig2 – 1].

ISP_BNR_RGGB_ODD_WADDR

ISP_BNR_RGGB_ODD_WADDR is a Pattern_RGGB weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x25480	ISP_BNR_RGGB_ODD_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_RGGB weight coefficient LUT

ISP_BNR_RGGB_ODD_WDATA

ISP_BNR_RGGB_ODD_WDATA is a Pattern_RGGB weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x25484	ISP_BNR_RGGB_ODD_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_RGGB weight coefficient LUT

ISP_BNR_RGGB_ODD_RADDR

ISP_BNR_RGGB_ODD_RADDR is a Pattern_RGGB weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x25488	ISP_BNR_RGGB_ODD_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_RGGB weight coefficient LUT

ISP_BNR_RGGB_ODD_RDATA

ISP_BNR_RGGB_ODD_RDATA is a Pattern_RGGB weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x2548C	ISP_BNR_RGGB_ODD_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_RGGB weight coefficient LUT

ISP_BNR_GRBG_ODD_WADDR

ISP_BNR_GRBG_ODD_WADDR is a Pattern_GRBG weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x25490	ISP_BNR_GRBG_ODD_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GRBG_ODD_WDATA

ISP_BNR_GRBG_ODD_WDATA is a Pattern_GRBG weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x25494	ISP_BNR_GRBG_ODD_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GRBG_ODD_RADDR

ISP_BNR_GRBG_ODD_RADDR is a Pattern_GRBG weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x25498	ISP_BNR_GRBG_ODD_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GRBG_ODD_RDATA

ISP_BNR_GRBG_ODD_RDATA is a Pattern_GRBG weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x2549C	ISP_BNR_GRBG_ODD_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GBRG_ODD_WADDR

ISP_BNR_GBRG_ODD_WADDR is a Pattern_GBRG weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x254A0	ISP_BNR_GBRG_ODD_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_GBRG weight coefficient LUT

ISP_BNR_GBRG_ODD_WDATA

ISP_BNR_GBRG_ODD_WDATA is a Pattern_GBRG weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x254A4	ISP_BNR_GBRG_ODD_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_GBRG weight coefficient LUT

ISP_BNR_GBRG_ODD_RADDR

ISP_BNR_GBRG_ODD_RADDR is a Pattern_GBRG weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x254A8	ISP_BNR_GBRG_ODD_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_GBRG weight coefficient LUT

ISP_BNR_GBRG_ODD_RDATA

ISP_BNR_GBRG_ODD_RDATA is a Pattern_GBRG weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x254AC	ISP_BNR_GBRG_ODD_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_GBRG weight coefficient LUT

ISP_BNR_BGGR_ODD_WADDR

ISP_BNR_BGGR_ODD_WADDR is a Pattern_BGGR weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x254B0	ISP_BNR_BGGR_ODD_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_BGGR weight coefficient LUT

ISP_BNR_BGGR_ODD_WDATA

ISP_BNR_BGGR_ODD_WDATA is a Pattern_BGGR weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x254B4	ISP_BNR_BGGR_ODD_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_BGGR weight coefficient LUT

ISP_BNR_BGGR_ODD_RADDR

ISP_BNR_BGGR_ODD_RADDR is a Pattern_BGGR weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x254B8	ISP_BNR_BGGR_ODD_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_BGGR weight coefficient LUT

ISP_BNR_BGGR_ODD_RDATA

ISP_BNR_BGGR_ODD_RDATA is a Pattern_BGGR weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x254BC	ISP_BNR_BGGR_ODD_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_BGGR weight coefficient LUT

ISP_BNR_RLMT_ODD_WADDR

ISP_BNR_RLMT_ODD_WADDR is a Pattern_RLMT weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x254C0	ISP_BNR_RLMT_ODD_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_RLMT weight coefficient LUT

ISP_BNR_RLMT_ODD_WDATA

ISP_BNR_RLMT_ODD_WDATA is a Pattern_RLMT weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x254C4	ISP_BNR_RLMT_ODD_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_RLMT weight coefficient LUT

ISP_BNR_RLMT_ODD_RADDR

ISP_BNR_RLMT_ODD_RADDR is a Pattern_RLMT weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x254C8	ISP_BNR_RLMT_ODD_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_RLMT weight coefficient LUT

ISP_BNR_RLMT_ODD_RDATA

ISP_BNR_RLMT_ODD_RDATA is a Pattern_RLMT weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x254CC	ISP_BNR_RLMT_ODD_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_RLMT weight coefficient LUT

ISP_BNR_SIZE

ISP_BNR_SIZE is a BNR input picture size register.

Offset Address	Register Name	Total Reset Value
0x254F0	ISP_BNR_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Input picture height. The configured value is the actual value minus 1. For example, for the 1080P picture, set the height to 1079.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Input picture width. The configured value is the actual value minus 1. For example, for the 1080P picture, set the width to 1919.

ISP_BNR_RGGB_EVEN_WADDR

ISP_BNR_RGGB_EVEN_WADDR is a Pattern_RGGB weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x25580	ISP_BNR_RGGB_EVEN_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_RGGB weight coefficient LUT

ISP_BNR_RGGB_EVEN_WDATA

ISP_BNR_RGGB_EVEN_WDATA is a Pattern_RGGB weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x25584	ISP_BNR_RGGB_EVEN_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_RGGB weight coefficient LUT

ISP_BNR_RGGB_EVEN_RADDR

ISP_BNR_RGGB_EVEN_RADDR is a Pattern_RGGB weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x25588	ISP_BNR_RGGB_EVEN_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_RGGB weight coefficient LUT

ISP_BNR_RGGB_EVEN_RDATA

ISP_BNR_RGGB_EVEN_RDATA is a Pattern_RGGB weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x2558C	ISP_BNR_RGGB_EVEN_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_RGGB weight coefficient LUT

ISP_BNR_GRBG_EVEN_WADDR

ISP_BNR_GRBG_EVEN_WADDR is a Pattern_GRBG weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x25590	ISP_BNR_GRBG_EVEN_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GRBG_EVEN_WDATA

ISP_BNR_GRBG_EVEN_WDATA is a Pattern_GRBG weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x25594	ISP_BNR_GRBG_EVEN_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GRBG_EVEN_RADDR

ISP_BNR_GRBG_EVEN_RADDR is a Pattern_GRBG weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x25598	ISP_BNR_GRBG_EVEN_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GRBG_EVEN_RDATA

ISP_BNR_GRBG_EVEN_RDATA is a Pattern_GRBG weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x2559C	ISP_BNR_GRBG_EVEN_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_GRBG weight coefficient LUT

ISP_BNR_GBRG_EVEN_WADDR

ISP_BNR_GBRG_EVEN_WADDR is a Pattern_GBRG weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x255A0	ISP_BNR_GBRG_EVEN_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_GBRG weight coefficient LUT

ISP_BNR_GBRG_EVEN_WDATA

ISP_BNR_GBRG_EVEN_WDATA is a Pattern_GBRG weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x255A4	ISP_BNR_GBRG_EVEN_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_GBRG weight coefficient LUT

ISP_BNR_GBRG_EVEN_RADDR

ISP_BNR_GBRG_EVEN_RADDR is a Pattern_GBRG weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x255A8	ISP_BNR_GBRG_EVEN_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_GBRG weight coefficient LUT

ISP_BNR_GBRG_EVEN_RDATA

ISP_BNR_GBRG_EVEN_RDATA is a Pattern_GBRG weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x255AC	ISP_BNR_GBRG_EVEN_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_GBRG weight coefficient LUT

ISP_BNR_BGGR_EVEN_WADDR

ISP_BNR_BGGR_EVEN_WADDR is a Pattern_BGGR weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x255B0	ISP_BNR_BGGR_EVEN_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_BGGR weight coefficient LUT

ISP_BNR_BGGR_EVEN_WDATA

ISP_BNR_BGGR_EVEN_WDATA is a Pattern_BGGR weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x255B4	ISP_BNR_BGGR_EVEN_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_BGGR weight coefficient LUT

ISP_BNR_BGGR_EVEN_RADDR

ISP_BNR_BGGR_EVEN_RADDR is a Pattern_BGGR weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x255B8	ISP_BNR_BGGR_EVEN_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_BGGR weight coefficient LUT

ISP_BNR_BGGR_EVEN_RDATA

ISP_BNR_BGGR_EVEN_RDATA is a Pattern_BGGR weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x255BC	ISP_BNR_BGGR_EVEN_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_BGGR weight coefficient LUT

ISP_BNR_RLMT_EVEN_WADDR

ISP_BNR_RLMT_EVEN_WADDR is a Pattern_RLMT weight coefficient LUT write address register.

Offset Address	Register Name	Total Reset Value
0x255C0	ISP_BNR_RLMT_EVEN_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hwaddr	Write address of the Pattern_RLMT weight coefficient LUT

ISP_BNR_RLMT_EVEN_WDATA

ISP_BNR_RLMT_EVEN_WDATA is a Pattern_RLMT weight coefficient LUT write data register.

Offset Address	Register Name	Total Reset Value
0x255C4	ISP_BNR_RLMT_EVEN_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hwdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	lut_hwdata	Write data of the Pattern_RLMT weight coefficient LUT

ISP_BNR_RLMT_EVEN_RADDR

ISP_BNR_RLMT_EVEN_RADDR is a Pattern_RLMT weight coefficient LUT read address register.

Offset Address	Register Name	Total Reset Value
0x255C8	ISP_BNR_RLMT_EVEN_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hraddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	lut_hraddr	Read address of the Pattern_RLMT weight coefficient LUT

ISP_BNR_RLMT_EVEN_RDATA

ISP_BNR_RLMT_EVEN_RDATA is a Pattern_RLMT weight coefficient LUT read data register.

Offset Address	Register Name	Total Reset Value
0x255CC	ISP_BNR_RLMT_EVEN_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lut_hrdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	lut_hrdata	Read data of the Pattern_RLMT weight coefficient LUT

ISP_WDR_CFG

ISP_WDR_CFG is a WDR control register.

Offset Address	Register Name	Total Reset Value
0x26000	ISP_WDR_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	WDR enable (U1) 0: disabled 1: enabled

ISP_WDR_INBLC

ISP_WDR_INBLC is an input black level offset register.

Offset Address	Register Name	Total Reset Value
0x26010	ISP_WDR_INBLC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	f0_inBLC															reserved	f1_inBLC														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	f0_inBLC	Offset of the input black level of the short frame (f0). The data format is S15.
[15]	-	reserved	Reserved
[14:0]	RW	f1_inBLC	Offset of the input black level of the long frame (f1). The data format is S15.

ISP_WDR_OUTBLC

ISP_WDR_OUTBLC is an output black level offset register.

Offset Address	Register Name	Total Reset Value
0x26014	ISP_WDR_OUTBLC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												outBLC																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19:0]	RW	outBLC	Offset of the output black level. The data format is U20.

ISP_WDR_EXPOSRATIOS

ISP_WDR_EXPOSRATIOS is an exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x26018	ISP_WDR_EXPOSRATIOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		exporatio_r		reserved	exporatio		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	exporatio_r	Reciprocal of the exposure ratio of the long frame (f1) relative to the short frame (f0) (U10)
[15:12]	-	reserved	Reserved
[11:0]	RW	exporatio	Exposure ratio of the long frame (f1) relative to the short frame (f0) (U6.6)

ISP_WDR_BLCSAVE

ISP_WDR_BLCSAVE is a black level save control register.

Offset Address	Register Name	Total Reset Value
0x2601C	ISP_WDR_BLCSAVE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			esaveBLC	reserved			bsaveBLC
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved
[16]	RW	esaveBLC	Frame of which the black level is to be saved during output (U1) 0: The black level of the short frame (f0) is saved. 1: The black level of the long frame (f1) is saved.
[15:1]	-	reserved	Reserved
[0]	RW	bsaveBLC	Black level save enable (U1) 0: The unsaved black level is output. 1: The saved black level is output.

ISP_WDR_ZOOMBLC

ISP_WDR_ZOOMBLC is a black level zoom coefficient register.

Offset Address	Register Name	Total Reset Value
0x26020	ISP_WDR_ZOOMBLC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							zoomBLC
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved
[6:0]	RW	zoomBLC	Zoom coefficient of the black level. The maximum value is 64 and the data format is U7. This register takes effect for pixel values below the BLC threshold. That is, the difference between the pixel value and the black level is zoomed in (zoom in the negative signal).

ISP_WDR_BLENDRATIO

ISP_WDR_BLENDRATIO is a weight index blending coefficient register.

Offset Address	Register Name	Total Reset Value
0x26024	ISP_WDR_BLENDRATIO	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			bldrlhfidx	reserved			bldrclridx
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved
[20:16]	RW	bldrlhfidx	Blending coefficient of the high- and low-frequency weight index. The maximum value is 16 and the data format is U5.
[15:5]	-	reserved	Reserved
[4:0]	RW	bldrclridx	Blending coefficient of the point index and maximum value index. The maximum value is 16 and the data format is U5.

ISP_WDR_FLRGTTH

ISP_WDR_FLRGTTH is a long frame index threshold register.

Offset Address	Register Name	Total Reset Value
0x26028	ISP_WDR_FLRGTTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				flrgtth_high												reserved				flrgtth_low											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:16]	RW	flrgtth_high	Upper threshold of the long frame index (U14)
[15:14]	-	reserved	Reserved
[13:0]	RW	flrgtth_low	Lower threshold of the long frame index (U14)

ISP_WDR_FLDFTWGT

ISP_WDR_FLDFTWGT is a long frame default weight register.

Offset Address	Register Name	Total Reset Value
0x2602C	ISP_WDR_FLDFTWGT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fl_dftwgt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8:0]	RW	fl_dftwgt	Default weight of the long frame. The data format is U9 and the maximum value is 256.

ISP_WDR_MDT_CTRL

ISP_WDR_MDT_CTRL is a motion detection control register.

Offset Address	Register Name	Total Reset Value
0x26030	ISP_WDR_MDT_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved			bmdthf	reserved			fl_bmdtmnu	reserved							bmdtstrong	reserved															balgprocmdt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28]	RW	bmdthf	Horizontal filtering control of motion intensity (U1) 0: no filtering on motion intensity 1: horizontal low-pass filtering on motion intensity
[27:25]	-	reserved	Reserved
[24]	RW	fl_bmdtmnu	Long frame weight adjustment in motion regions (U1) 0: The long frame weight in motion regions decreases. 1: The long frame weight in motion regions increases.
[23:17]	-	reserved	Reserved
[16]	RW	bmdtstrong	Motion detection strength control (U1) 0: Weak motion detection and the small window are used. 1: Strong motion detection and the large window are used.
[15:1]	-	reserved	Reserved
[0]	RW	balgprocmdt	Motion detection enable (U1) 0: disabled 1: enabled

ISP_WDR_BLDRMDTMAX

ISP_WDR_BLDRMDTMAX is an inter-frame difference blending coefficient register.

Offset Address	Register Name	Total Reset Value
0x26034	ISP_WDR_BLDRMDTMAX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											bldrmdtmax			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved
[4:0]	RW	bldrmdtmax	Blending coefficient of inter-frame difference average value filtering and maximum value filtering. The maximum value is 16 and the data format is U5.

ISP_WDR_NOSCLIPTH

ISP_WDR_NOSCLIPTH is an inter-frame difference threshold register.

Offset Address	Register Name	Total Reset Value
0x26038	ISP_WDR_NOSCLIPTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				nosclipth											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13:0]	RW	nosclipth	Threshold when the inter-frame difference is clipped (U14) If the inter-frame difference of a certain point is lower than the threshold, it is clipped to 0.

ISP_WDR_NOSFACTOR

ISP_WDR_NOSFACTOR is a motion judgment factor register.

Offset Address	Register Name	Total Reset Value
0x2603C	ISP_WDR_NOSFACTOR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												nosfactor_low				reserved								nosfactor_high							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	-	reserved	Reserved
[21:16]	RW	nosfactor_low	Amplification factor corresponding to the lower threshold for motion judgment (U4.2)
[15:6]	-	reserved	Reserved
[5:0]	RW	nosfactor_high	Amplification factor corresponding to the upper threshold for motion judgment (U4.2)

ISP_WDR_LUT_UPDATE

ISP_WDR_LUT_UPDATE is an LUT update register.

Offset Address	Register Name	Total Reset Value
0x26040	ISP_WDR_LUT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															noslut_update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	noslut_update	WDR noise LUT update control (U1). This bit is automatically cleared for each frame.

ISP_WDR_FSNRJUDGE

ISP_WDR_FSNRJUDGE is a motion region short frame denoising judgment threshold register.

Offset Address	Register Name	Total Reset Value
0x26044	ISP_WDR_FSNRJUDGE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fsnr_judge							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8:0]	RW	fsnr_judge	Short frame denoising judgment threshold. The data format is U9 and the maximum value is 256. When the motion intensity is greater than this threshold, denoising is performed on short frames; otherwise, denoising is not performed.

ISP_WDR_FSNRTH

ISP_WDR_FSNRTH is a short frame denoising threshold register.

Offset Address	Register Name	Total Reset Value
0x26048	ISP_WDR_FSNRTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								fsnrth_low								reserved								fsnrth_high							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	fsnrth_low	Lower threshold of short frame denoising. The data format is U9 and the maximum value is 256.
[15:9]	-	reserved	Reserved
[8:0]	RW	fsnrth_high	Upper threshold of short frame denoising. The data format is U9 and the maximum value is 256.

ISP_WDR_FSNRGN

ISP_WDR_FSNRGN is a short frame denoising gain register.

Offset Address	Register Name	Total Reset Value
0x2604C	ISP_WDR_FSNRGN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			fsnrgn_low	reserved			fsnrgn_high
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	-	reserved	Reserved
[21:16]	RW	fsnrgn_low	Lower gain of short frame denoising (U4.2)
[15:6]	-	reserved	Reserved
[5:0]	RW	fsnrgn_high	Upper gain of short frame denoising (U4.2)

ISP_WDR_MDT_REFNOS

ISP_WDR_MDT_REFNOS is a motion judgment control register.

Offset Address	Register Name	Total Reset Value
0x26050	ISP_WDR_MDT_REFNOS	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							bmdtrefnos
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	bmdtrefnos	Whether the noise level is referenced during motion judgment (U1) 0: no 1: yes

ISP_WDR_NOSLUT_WADDR

ISP_WDR_NOSLUT_WADDR is a noise LUT write address register.

Offset Address	Register Name	Total Reset Value
0x26080	ISP_WDR_NOSLUT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										noslut_waddr					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved
[5:0]	RW	noslut_waddr	Write address of the noise LUT. The maximum value is 32 and the data format is U6.

ISP_WDR_NOSLUT_WDATA

ISP_WDR_NOSLUT_WDATA is a noise LUT write data register.

Offset Address	Register Name	Total Reset Value
0x26084	ISP_WDR_NOSLUT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				noslut_wdata											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13:0]	RW	noslut_wdata	Write data of the noise LUT (U14)

ISP_WDR_NOSLUT_RADDR

ISP_WDR_NOSLUT_RADDR is a noise LUT read address register.

Offset Address	Register Name	Total Reset Value
0x26088	ISP_WDR_NOSLUT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										noslut_raddr					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved
[5:0]	RW	noslut_raddr	Read address of the noise LUT. The maximum value is 32 and the data format is U6.

ISP_WDR_NOSLUT_RDATA

ISP_WDR_NOSLUT_RDATA is a noise LUT read data register.

Offset Address	Register Name	Total Reset Value
0x2608C	ISP_WDR_NOSLUT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				noslut_rdata											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13:0]	RO	noslut_rdata	Read data of the noise LUT (U14)

ISP_WDR_SIZE

ISP_WDR_SIZE is a WDR picture size register.

Offset Address	Register Name	Total Reset Value
0x260F0	ISP_WDR_SIZE	0x02CF_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height The configured value is the actual value minus 1. For example, if the actual picture height is 720, set this field to 719.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width The configured value is the actual value minus 1. For example, if the actual picture width is 1280, set this field to 1279.

ISP_DRC_CFG

ISP_DRC_CFG is a DRC configuration register.

Offset Address	Register Name	Total Reset Value
0x26200	ISP_DRC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															drc_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	drc_en	DRC module enable 0: disabled 1: enabled

ISP_DRC_ZONE

ISP_DRC_ZONE is a DRC zone configuration register.

Offset Address	Register Name	Total Reset Value
0x26210	ISP_DRC_ZONE	0x0000_1519

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	0	0	1

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12:8]	RW	vnum	DRC vertical zone configuration NOTE 5 ≤ vnum ≤ 21; vnum x hnum ≤ 525
[7:5]	RO	reserved	Reserved
[4:0]	RW	hnum	DRC horizontal zone configuration NOTE 5 ≤ hnum ≤ 29; vnum x hnum ≤ 525

ISP_DRC_ZONE_SIZE

ISP_DRC_ZONE_SIZE is a DRC block size register.

Offset Address	Register Name	Total Reset Value
0x26214	ISP_DRC_ZONE_SIZE	0x1232_284B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		chk_y						vsize								reserved		chk_x						hsize							
Reset	0	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:25]	RW	chk_y	The block sizes are unequal. chk_y = vsize%vnum
[24:16]	RW	vsize	Height of each DRC block NOTE The configured value is the actual value minus 1.
[15:14]	RO	reserved	Reserved
[13:9]	RW	chk_x	The block sizes are unequal. chk_x = hsize%hnum
[8:0]	RW	hsize	Width of each DRC block NOTE The configured value is the actual value minus 1.

ISP_DRC_ZONE_DIV0

ISP_DRC_ZONE_DIV0 is a DRC block division coefficient register.

Offset Address	Register Name	Total Reset Value
0x26218	ISP_DRC_ZONE_DIV0	0x0283_01AF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				div_y												reserved				div_x											
Reset	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	1

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	div_y	Reciprocal value of the height of each DRC block div_y = 32768/vsize
[15]	RO	reserved	Reserved
[14:0]	RW	div_x	Reciprocal value of the width of each DRC block div_x = 32768/hsize

ISP_DRC_ZONE_DIV1

ISP_DRC_ZONE_DIV1 is a DRC block division coefficient register.

Offset Address	Register Name	Total Reset Value
0x2621C	ISP_DRC_ZONE_DIV1	0x0276_01AA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				div_y												reserved				div_x											
Reset	0	0	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:16]	RW	div_y	Reciprocal value of the height of each DRC block div_y = 32768/vsize
[15]	RO	reserved	Reserved
[14:0]	RW	div_x	Reciprocal value of the width of each DRC block div_x = 32768/hsize

ISP_DRC_BIN

ISP_DRC_BIN is a DRC block histogram segment number register.

Offset Address	Register Name	Total Reset Value
0x26220	ISP_DRC_BIN	0x0000_000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											bin				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	bin	Number of required histogram segments for each DRC block NOTE 12 ≥ bin ≥ 6

ISP_DRC_BIN_DIV

ISP_DRC_BIN_DIV is a DRC histogram division coefficient register.

Offset Address	Register Name	Total Reset Value
0x26224	ISP_DRC_BIN_DIV	0x0000_0AAB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																div_z															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14:0]	RW	div_z	Reciprocal value of the number of layers of each DRC block div_z = 32768/bin

ISP_DRC_BIN_SCALE

ISP_DRC_BIN_SCALE is a DRC histogram scaling ratio register.

Offset Address	Register Name	Total Reset Value
0x26228	ISP_DRC_BIN_SCALE	0x0000_0005

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														bin_scale	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2:0]	RW	bin_scale	DRC histogram statistics weight NOTE The fewer the pixels in a block, the greater the weight.

ISP_DRC_RANGE_FLT_COEF

ISP_DRC_RANGE_FLT_COEF is a DRC value domain filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x2622C	ISP_DRC_RANGE_FLT_COEF	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												range_flt_coef			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	RO	reserved	Reserved
[3:0]	RW	range_flt_coef	The value range is 0−8.

ISP_DRC_EXPOSURE

ISP_DRC_EXPOSURE is a DRC current frame exposure ratio register.

Offset Address	Register Name	Total Reset Value
0x26230	ISP_DRC_EXPOSURE	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																exposure															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	exposure	Exposure ratio of the current DRC frame, for compensating bright-to-dark switching

ISP_DRC_LOCAL_EDGE_LMT

ISP_DRC_LOCAL_EDGE_LMT is a DRC local limit register.

Offset Address	Register Name	Total Reset Value
0x26234	ISP_DRC_LOCAL_EDGE_LMT	0x0000_009B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								local_edge_lmt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	local_edge_lmt	Limit on the input/output luminance difference of the dual-edge filter

ISP_DRC_STRENGTH

ISP_DRC_STRENGTH is a DRC strength adjustment register.

Offset Address	Register Name	Total Reset Value
0x26238	ISP_DRC_STRENGTH	0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								strength							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	strength	DRC strength

ISP_DRC_DETAIL_GAIN

ISP_DRC_DETAIL_GAIN is a DRC detail gain adjustment register.

Offset Address	Register Name	Total Reset Value
0x2623C	ISP_DRC_DETAIL_GAIN	0x0060_8010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								detail_mixing_thres								detail_mixing_dark								detail_mixing_bright							
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	detail_mixing_thres	Detail enhancement threshold
[15:8]	RW	detail_mixing_dark	Enhancement strength of the detail in dark regions
[7:0]	RW	detail_mixing_bright	Enhancement strength of the detail in bright regions

ISP_DRC_DARK_GAIN_LMT_Y

ISP_DRC_DARK_GAIN_LMT_Y is a DRC dark region luminance limit register.

Offset Address	Register Name	Total Reset Value
0x26240	ISP_DRC_DARK_GAIN_LMT_Y	0x0000_007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sft2				val2				sft1				val1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:14]	RW	sft2	Limit on the luminance gain of the dark region
[13:10]	RW	val2	Limit on the luminance gain of the dark region
[9:7]	RW	sft1	Limit on the luminance gain of the dark region
[6:0]	RW	val1	Limit on the luminance gain of the dark region

ISP_DRC_DARK_GAIN_LMT_C

ISP_DRC_DARK_GAIN_LMT_C is a DRC dark region chrominance limit register.

Offset Address	Register Name	Total Reset Value
0x26244	ISP_DRC_DARK_GAIN_LMT_C	0x0000_007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sft2				val2				sft1				val1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:14]	RW	sft2	Limit on the chrominance gain of the dark region
[13:10]	RW	val2	Limit on the chrominance gain of the dark region
[9:7]	RW	sft1	Limit on the chrominance gain of the dark region
[6:0]	RW	val1	Limit on the chrominance gain of the dark region

ISP_DRC_BRIGHT_GAIN_LMT

ISP_DRC_BRIGHT_GAIN_LMT is a DRC bright region limit register.

Offset Address	Register Name	Total Reset Value
0x26248	ISP_DRC_BRIGHT_GAIN_LMT	0x0000_007F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						sft		val							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:7]	RW	sft	Limit on the bright region gain
[6:0]	RW	val	Limit on the bright region gain

ISP_DRC_RGB_WGT

ISP_DRC_RGB_WGT is a DRC RGB weight configuration register.

Offset Address	Register Name	Total Reset Value
0x2624C	ISP_DRC_RGB_WGT	0x000E_1F03

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												b_wgt				reserved				g_wgt				reserved				r_wgt			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19:16]	RW	b_wgt	Weight of the B component
[15:13]	-	reserved	Reserved
[12:8]	RW	g_wgt	Weight of the G component
[7:4]	-	reserved	Reserved
[3:0]	RW	r_wgt	Weight of the R component

ISP_DRC_LUT_MIX_CRTL

ISP_DRC_LUT_MIX_CRTL is a DRC TMLUT mix register.

Offset Address	Register Name	Total Reset Value
0x26254	ISP_DRC_LUT_MIX_CRTL	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lut_mix_ctrl							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	lut_mix_ctrl	Mix ratio of LUT0 to LUT1

ISP_DRC_GAIN_CLIP

ISP_DRC_GAIN_CLIP is a DRC gain limit register.

Offset Address	Register Name	Total Reset Value
0x26258	ISP_DRC_GAIN_CLIP	0x0000_00A6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gain_clip_knee				gain_clip_step			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:4]	RW	gain_clip_knee	Limit start point of the bright region gain
[3:0]	RW	gain_clip_step	Limit range of the bright region gain

ISP_DRC_COLOR_CTRL

ISP_DRC_COLOR_CTRL is a DRC color correction control register.

Offset Address	Register Name	Total Reset Value
0x2625C	ISP_DRC_COLOR_CTRL	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														cc_lin_pow	cc_lut_ctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1]	RW	cc_lin_pow	DRC color correction mode select 0: linear mode 1: power-law mode
[0]	RW	cc_lut_ctrl	DRC color correction LUT mode select 0: login LUT 1: logout LUT

ISP_DRC_GLOBAL_CORR

ISP_DRC_GLOBAL_CORR is a DRC global color correction register.

Offset Address	Register Name	Total Reset Value
0x26260	ISP_DRC_GLOBAL_CORR	0x0000_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cc_global_corr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	cc_global_corr	Global color correction

ISP_DRC_MIXING_CORING

ISP_DRC_MIXING_CORING is a DRC detail threshold register.

Offset Address	Register Name	Total Reset Value
0x26264	ISP_DRC_MIXING_CORING	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								mixing_coring							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	mixing_coring	Detail threshold

ISP_DRC_MIXING_DARK

ISP_DRC_MIXING_DARK is a DRC dark detail control register.

Offset Address	Register Name	Total Reset Value
0x26268	ISP_DRC_MIXING_DARK	0x0380_402D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					dark_slo			dark_thr								dark_max								dark_min							
Reset	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0	1

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved

[26:24]	RW	dark_slo	Slope of the dark detail
[23:16]	RW	dark_thr	Threshold of the dark detail
[15:8]	RW	dark_max	Maximum value of the dark detail
[7:0]	RW	dark_min	Minimum value of the dark detail

ISP_DRC_MIXING_BRIGHT

ISP_DRC_MIXING_BRIGHT is a DRC bright detail control register.

Offset Address	Register Name	Total Reset Value
0x2626C	ISP_DRC_MIXING_BRIGHT	0x0740_402D

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	bright_slo	bright_thr		bright_max		bright_min	
Reset	0 0 0 0	0 1 1 1	0 1 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 1 0	1 1 0 1

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:24]	RW	bright_slo	Slope of the bright detail
[23:16]	RW	bright_thr	Threshold of the bright detail
[15:8]	RW	bright_max	Maximum value of the bright detail
[7:0]	RW	bright_min	Minimum value of the bright detail

ISP_DRC_RG_CTRL

ISP_DRC_RG_CTRL is a DRC purple fringing detection condition R/G control register.

Offset Address	Register Name	Total Reset Value
0x26270	ISP_DRC_RG_CTRL	0x0004_274A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rg_slo				reserved	rg_wid							rg_ctr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	1	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved
[18:16]	RW	rg_slo	R/G slope of purple fringing detection
[15]	-	reserved	Reserved
[14:8]	RW	rg_wid	R/G width of purple fringing detection
[7:0]	RW	rg_ctr	R/G center point of purple fringing detection

ISP_DRC_BG_CTRL

ISP_DRC_BG_CTRL is a DRC purple fringing detection condition B/G control register.

Offset Address	Register Name	Total Reset Value
0x26274	ISP_DRC_BG_CTRL	0x0000_0259

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						bg_slo		bg_thr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:8]	RW	bg_slo	B/G slope of purple fringing detection
[7:0]	RW	bg_thr	B/G threshold of purple fringing detection

ISP_DRC_PDW

ISP_DRC_PDW is a DRC purple fringing detection weight control register.

Offset Address	Register Name	Total Reset Value
0x26278	ISP_DRC_PDW	0x0840_0C28

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				high_slo				high_thr								reserved				low_slo				low_thr							
Reset	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:24]	RW	high_slo	High slope of the purple fringing detection weight
[23:16]	RW	high_thr	High threshold of the purple fringing detection weight
[15:12]	-	reserved	Reserved
[11:8]	RW	low_slo	Low slope of the purple fringing detection weight
[7:0]	RW	low_thr	Low threshold of the purple fringing detection weight

ISP_DRC_PPDTC_SUM

ISP_DRC_PPDTC_SUM is a DRC purple fringing detection weight statistics register.

Offset Address	Register Name	Total Reset Value
0x2627C	ISP_DRC_PPDTC_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ppdtc_sum															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	ppdtc_sum	Purple fringing detection statistics

ISP_DRC_STAT_IND_WADDR0

ISP_DRC_STAT_IND_WADDR0 is a DRC tone mapping table indirect write address 0 register.

Offset Address	Register Name	Total Reset Value
0x26280	ISP_DRC_STAT_IND_WADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_waddr0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	drc_stat_ind_waddr0	Tone mapping entry 0

ISP_DRC_STAT_IND_WDATA0

ISP_DRC_STAT_IND_WDATA0 is a DRC tone mapping table indirect write data 0 register.

Offset Address	Register Name	Total Reset Value
0x26284	ISP_DRC_STAT_IND_WDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_wdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	drc_stat_ind_wdata0	Tone mapping entry 0

ISP_DRC_STAT_IND_RADDR0

ISP_DRC_STAT_IND_RADDR0 is a DRC tone mapping table indirect read address 0 register.

Offset Address	Register Name	Total Reset Value
0x26288	ISP_DRC_STAT_IND_RADDR0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_raddr0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	drc_stat_ind_raddr0	Tone mapping entry 0

ISP_DRC_STAT_IND_RDATA0

ISP_DRC_STAT_IND_RDATA0 is a DRC tone mapping table indirect read data 0 register.

Offset Address	Register Name	Total Reset Value
0x2628C	ISP_DRC_STAT_IND_RDATA0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_rdata0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	drc_stat_ind_rdata0	Tone mapping entry 0

ISP_DRC_STAT_IND_WADDR1

ISP_DRC_STAT_IND_WADDR1 is a DRC tone mapping table indirect write address 1 register.

Offset Address	Register Name	Total Reset Value
0x26290	ISP_DRC_STAT_IND_WADDR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_waddr1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	drc_stat_ind_waddr1	Tone mapping entry 1

ISP_DRC_STAT_IND_WDATA1

ISP_DRC_STAT_IND_WDATA1 is a DRC tone mapping table indirect write data 1 register.

Offset Address	Register Name	Total Reset Value
0x26294	ISP_DRC_STAT_IND_WDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_wdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	drc_stat_ind_wdata1	Tone mapping entry 1

ISP_DRC_STAT_IND_RADDR1

ISP_DRC_STAT_IND_RADDR1 is a DRC tone mapping table indirect read address 1 register.

Offset Address	Register Name	Total Reset Value
0x26298	ISP_DRC_STAT_IND_RADDR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_raddr1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	drc_stat_ind_raddr1	Tone mapping entry 1

ISP_DRC_STAT_IND_RDATA1

ISP_DRC_STAT_IND_RDATA1 is a DRC tone mapping table indirect read data 1 register.

Offset Address	Register Name	Total Reset Value
0x2629C	ISP_DRC_STAT_IND_RDATA1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_rdata1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	drc_stat_ind_rdata1	Tone mapping entry 1

ISP_DRC_STAT_IND_WADDR2

ISP_DRC_STAT_IND_WADDR2 is a DRC color correct table indirect write address 2 register.

Offset Address	Register Name	Total Reset Value
0x262A0	ISP_DRC_STAT_IND_WADDR2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_waddr2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	drc_stat_ind_waddr2	Color correct entry

ISP_DRC_STAT_IND_WDATA2

ISP_DRC_STAT_IND_WDATA2 is a DRC color correct table indirect write data 2 register.

Offset Address	Register Name	Total Reset Value
0x262A4	ISP_DRC_STAT_IND_WDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_wdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	drc_stat_ind_wdata2	Color correct entry

ISP_DRC_STAT_IND_RADDR2

ISP_DRC_STAT_IND_RADDR2 is a DRC color correct table indirect read address 2 register.

Offset Address	Register Name	Total Reset Value
0x262A8	ISP_DRC_STAT_IND_RADDR2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_raddr2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	drc_stat_ind_raddr2	Color correct entry

ISP_DRC_STAT_IND_RDATA2

ISP_DRC_STAT_IND_RDATA2 is a DRC color correct table indirect read data 2 register.

Offset Address	Register Name	Total Reset Value
0x262AC	ISP_DRC_STAT_IND_RDATA2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drc_stat_ind_rdata2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	drc_stat_ind_rdata2	Color correct entry

ISP_DRC_GRAD_REV

ISP_DRC_GRAD_REV is a DRC gradient reverse adjustment register.

Offset Address	Register Name	Total Reset Value
0x26300	ISP_DRC_GRAD_REV	0x020D_0029

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				grad_rev_shift				reserved				grad_rev_slope				reserved	grad_rev_max							grad_rev_thres							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:24]	RW	grad_rev_shift	Gradient reverse adjustment
[23:20]	-	reserved	Reserved
[19:16]	RW	grad_rev_slope	Gradient reverse slope
[15]	-	reserved	Reserved
[14:8]	RW	grad_rev_max	Maximum value of the gradient reverse limit
[7:0]	RW	grad_rev_thres	Gradient reverse threshold

ISP_DRC_VBI_STRENGTH

ISP_DRC_VBI_STRENGTH is a DRC VBI filtering strength register.

Offset Address	Register Name	Total Reset Value
0x26304	ISP_DRC_VBI_STRENGTH	0x00AA_6666

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								var_sap_coarse				var_spa_medium				var_spa_fine				var_rng_coarse				var_rng_medium				var_rng_fine			
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:20]	RW	var_sap_coarse	Bilateral filtering spatial coarse strength
[19:16]	RW	var_spa_medium	Bilateral filtering spatial medium strength

[15:12]	RW	var_spa_fine	Bilateral filtering spatial fine strength
[11:8]	RW	var_rng_coarse	Bilateral filtering range coarse strength
[7:4]	RW	var_rng_medium	Bilateral filtering range medium strength
[3:0]	RW	var_rng_fine	Bilateral filtering range fine strength

ISP_DRC_VBI_MIXING

ISP_DRC_VBI_MIXING is a DRC VBI mixing strength register.

Offset Address	Register Name	Total Reset Value
0x26308	ISP_DRC_VBI_MIXING	0x0000_0D06

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				bin_mix_coarse				reserved				bin_mix_medium			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12:8]	RW	bin_mix_coarse	Mixing ratio of coarse and medium strength
[7:5]	-	reserved	Reserved
[4:0]	RW	bin_mix_medium	Mixing ratio of medium and fine strength

ISP_DRC_VBI_STATE

ISP_DRC_VBI_STATE is a DRC VBI status indicator register.

Offset Address	Register Name	Total Reset Value
0x26310	ISP_DRC_VBI_STATE	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																vbi_state															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	vbi_state	VBI status indicator

ISP_DRC_SIZE

ISP_DRC_SIZE is a DRC picture size register.

Offset Address	Register Name	Total Reset Value
0x263F0	ISP_DRC_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	vsize	DRC input picture height Note: The configured value is the actual value minus 1.
[15:13]	-	reserved	Reserved
[12:0]	RW	hsize	DRC input picture width Note: The configured value is the actual value minus 1.

ISP_EXPANDER_CFG

ISP_EXPANDER_CFG is an expander configuration register.

Offset Address	Register Name	Total Reset Value
0x26800	ISP_EXPANDER_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	Expander enable 0: disabled 1: enabled

ISP_EXPANDER_BITW

ISP_EXPANDER_BITW is a data bit width configuration register.

Offset Address	Register Name	Total Reset Value
0x26810	ISP_EXPANDER_BITW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												bitw_in				reserved												bitw_out			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RW	bitw_in	Bit width of the expander input data 0xC: 12 bits 0xE: 14 bits 0x10: 16 bits Other values: reserved
[15:5]	RO	reserved	Reserved
[4:0]	RW	bitw_out	Bit width of the expander output data 0xE: 14 bits 0x10: 16 bits 0x12: 18 bits 0x14: 20 bits Other values: reserved

ISP_EXPANDER_OFFSETR

ISP_EXPANDER_OFFSETR is an R channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26814	ISP_EXPANDER_OFFSETR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_r																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	offset_r	EXPANDER R channel data offset configuration

ISP_EXPANDER_OFFSETGR

ISP_EXPANDER_OFFSETGR is a Gr channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26818	ISP_EXPANDER_OFFSETGR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_gr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	offset_gr	Expander Gr channel data offset configuration

ISP_EXPANDER_OFFSETGB

ISP_EXPANDER_OFFSETGB is a Gb channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x2681C	ISP_EXPANDER_OFFSETGB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_gb																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	offset_gb	Expander Gb channel data offset configuration

ISP_EXPANDER_OFFSETB

ISP_EXPANDER_OFFSETB is a B channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26820	ISP_EXPANDER_OFFSETB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_b																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:0]	RW	offset_b	Expander B channel data offset configuration

ISP_EXPANDER_WADDR

ISP_EXPANDER_WADDR is an indirect write address register.

Offset Address	Register Name	Total Reset Value
0x26880	ISP_EXPANDER_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	expander_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	expander_waddr	Write address of the 129-entry expander LUT

ISP_EXPANDER_WDATA

ISP_EXPANDER_WDATA is indirect write data register.

Offset Address	Register Name	Total Reset Value
0x26884	ISP_EXPANDER_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	expander_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	expander_wdata	Write data of the 129-entry expander LUT

ISP_EXPANDER_RADDR

ISP_EXPANDER_RADDR is an indirect read address register.

Offset Address	Register Name	Total Reset Value
0x26888	ISP_EXPANDER_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	expander_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	expander_raddr	Read address of the 129-entry expander LUT

ISP_EXPANDER_RDATA

ISP_EXPANDER_RDATA is indirect read data register.

Offset Address	Register Name	Total Reset Value
0x2688C	ISP_EXPANDER_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	expander_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	expander_rdata	Read data of the 129-entry expander LUT

ISP_BCOM_CFG

ISP_BCOM_CFG is a BCOM enable register.

Offset Address	Register Name	Total Reset Value
0x26C00	ISP_BCOM_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	BCOM enable 0: disabled 1: enabled

ISP_BCOM_ALPHA

ISP_BCOM_ALPHA is an alpha coefficient register.

Offset Address	Register Name	Total Reset Value
0x26C10	ISP_BCOM_ALPHA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							alpha
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2:0]	RW	alpha	Alpha coefficient The value ranges from 0 to 6.

ISP_BDEC_CFG

ISP_BDEC_CFG is a BDEC enable register.

Offset Address	Register Name	Total Reset Value
0x26D00	ISP_BDEC_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	BDEC enable 0: disabled 1: enabled

ISP_BDEC_ALPHA

ISP_BDEC_ALPHA is an alpha coefficient register.

Offset Address	Register Name	Total Reset Value
0x26D10	ISP_BDEC_ALPHA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														alpha	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	-	reserved	Reserved
[2:0]	RW	alpha	Alpha coefficient The value ranges from 0 to 6.

ISP_WDRSPLIT_CFG

ISP_WDRSPLIT_CFG is a WDRSPLIT configuration register.

Offset Address	Register Name	Total Reset Value
0x26E00	ISP_WDRSPLIT_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	WDRSPLIT enable 0: disabled 1: enabled

ISP_WDRSPLIT_BITW

ISP_WDRSPLIT_BITW is a data bit width configuration register.

Offset Address	Register Name	Total Reset Value
0x26E10	ISP_WDRSPLIT_BITW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												bitw_in				reserved												bitw_out			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved
[20:16]	RW	bitw_in	Bit width of WDRSPLIT input data 0xC: 12-bit input 0xE: 14-bit input 0x10: 16-bit input 0x14: 20-bit input Other values: reserved Note: The value 0x14 is supported only when mode_in is linear.
[15:5]	-	reserved	Reserved
[4:0]	RW	bitw_out	Bit width of decompressed WDRSPLIT data 0xC: 12-bit output 0xD: 13-bit output 0xE: 14-bit output 0xF: 15-bit output 0x10: 16-bit output 0x11: 17-bit output 0x12: 18-bit output 0x13: 19-bit output 0x14: 20-bit output Other values: reserved

ISP_WDRSPLIT_MODE

ISP_WDRSPLIT_MODE is a mode configuration register.

Offset Address	Register Name	Total Reset Value
0x26E14	ISP_WDRSPLIT_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										mode_in		reserved		mode_out	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved
[5:4]	RW	mode_in	WDRSPLIT input data mode 00: linear mode 01: 2–3mux mode 10: LOG mode 11: sensor built-in mode
[3:2]	-	reserved	Reserved
[1:0]	RW	mode_out	WDRSPLIT output data mode 00: 1-channel output 01: 2-channel output 10: 3-channel output 11: 4-channel output

ISP_WDRSPLIT_OFFSETR

ISP_WDRSPLIT_OFFSETR is an R channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26E20	ISP_WDRSPLIT_OFFSETR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_r																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19:0]	RW	offset_r	Offset of the WDRSPLIT R channel

ISP_WDRSPLIT_OFFSETGR

ISP_WDRSPLIT_OFFSETGR is a Gr channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26E24	ISP_WDRSPLIT_OFFSETGR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_gr																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19:0]	RW	offset_gr	Offset of the WDRSPLIT Gr channel

ISP_WDRSPLIT_OFFSETGB

ISP_WDRSPLIT_OFFSETGB is a Gb channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26E28	ISP_WDRSPLIT_OFFSETGB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_gb																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19:0]	RW	offset_gb	Offset of the WDRSPLIT Gb channel

ISP_WDRSPLIT_OFFSETB

ISP_WDRSPLIT_OFFSETB is a B channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26E2C	ISP_WDRSPLIT_OFFSETB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												offset_b																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved

[19:0]	RW	offset_b	Offset of the WDRSPLIT B channel

ISP_WDRSPLIT_BLC

ISP_WDRSPLIT_BLC is a B channel data offset configuration register.

Offset Address	Register Name	Total Reset Value
0x26E30	ISP_WDRSPLIT_BLC	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												BLC																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19:0]	RW	BLC	BLC offset of the WDRSPLIT output

ISP_WDRSPLIT_WADDR

ISP_WDRSPLIT_WADDR is an indirect write address register.

Offset Address	Register Name	Total Reset Value
0x26E80	ISP_WDRSPLIT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdrsplit_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdrsplit_waddr	Write address of the 129-entry WDRSPLIT LUT

ISP_WDRSPLIT_WDATA

ISP_WDRSPLIT_WDATA is an indirect write data register.

Offset Address	Register Name	Total Reset Value
0x26E84	ISP_WDRSPLIT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdrsplit_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdrsplit_wdata	Write data of the 129-entry WDRSPLIT LUT

ISP_WDRSPLIT_RADDR

ISP_WDRSPLIT_RADDR is an indirect read address register.

Offset Address	Register Name	Total Reset Value
0x26E88	ISP_WDRSPLIT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdrsplit_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wdrsplit_raddr	Read address of the 129-entry WDRSPLIT LUT

ISP_WDRSPLIT_RDATA

ISP_WDRSPLIT_RDATA is an indirect read data register.

Offset Address	Register Name	Total Reset Value
0x26E8C	ISP_WDRSPLIT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdrsplit_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	wdrsplit_rdata	Read data of the 129-entry WDRSPLIT LUT

ISP_AEWDR0_CFG

ISP_AEWDR0_CFG is an AEWDR0 enable register.

Offset Address	Register Name	Total Reset Value
0x29000	ISP_AEWDR0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	AEWDR0 enable 0: disabled 1: enabled

ISP_AEWDR0_ZONE

ISP_AEWDR0_ZONE is an AEWDR0 zone configuration register.

Offset Address	Register Name	Total Reset Value
0x29010	ISP_AEWDR0_ZONE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12:8]	RW	vnum	Number of zones in the vertical direction
[7:5]	-	reserved	Reserved
[4:0]	RW	hnum	Number of zones in the horizontal direction

ISP_AEWDR0_SKIP_CRG

ISP_AEWDR0_SKIP_CRG is an AEWDR0 point select configuration register.

Offset Address	Register Name	Total Reset Value
0x29014	ISP_AEWDR0_SKIP_CRG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						offset_y	skip_y	offset_x	skip_x
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7]	RW	offset_y	Count start row 0: count from row 0 1: count from row 1
[6:4]	RW	skip_y	Vertical point skip for statistics 000: counted for each pixel point 001: counted for every two pixels 010: counted for every three pixels 011: counted for every four pixels 100: counted for every five pixels 101: counted for every eight pixels 110 or above: counted for every nine pixels
[3]	RW	offset_x	Count start column 0: count from column 0 1: count from column 1
[2:0]	RW	skip_x	Horizontal point skip for statistics 000: counted for every two pixels 001: counted for every three pixels 010: counted for every four pixels 011: counted for every five pixels 100: counted for every eight pixels 101 or above: counted for every nine pixels

ISP_AEWDR0_TOTAL_STAT

ISP_AEWDR0_TOTAL_STAT is a selected pixel count register in a frame during 256 histogram statistics.

Offset Address	Register Name	Total Reset Value
0x29018	ISP_AEWDR0_TOTAL_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								total_pixels																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:0]	RO	total_pixels	Number of selected pixels in a frame during 256 histogram statistics

ISP_AEWDR0_COUNT_STAT

ISP_AEWDR0_COUNT_STAT is a selected pixel weight count register in a frame during 256 histogram statistics.

Offset Address	Register Name	Total Reset Value
0x2901C	ISP_AEWDR0_COUNT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				count_pixels																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:0]	RO	count_pixels	Total weight of the selected pixels in a frame during 256 histogram statistics

ISP_AEWDR0_HIST_HIGH

ISP_AEWDR0_HIST_HIGH is a histogram statistics high register.

Offset Address	Register Name	Total Reset Value
0x29030	ISP_AEWDR0_HIST_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hist_high	Upper bits in histogram statistics

ISP_AEWDR0_BITMOVE

ISP_AEWDR0_BITMOVE is an AEWDR0 pixel shift register.

Offset Address	Register Name	Total Reset Value
0x29040	ISP_AEWDR0_BITMOVE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						BLC_en	reserved				bitmove			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9]	RW	BLC_en	AEWDR0 BLC enable 0: disabled 1: enabled
[8:5]	-	reserved	Reserved
[4:0]	RW	bitmove	AEWDR0 pixel shift value

ISP_AEWDR0_OFFSET_R

ISP_AEWDR0_OFFSET_R is an R component black level offset register.

Offset Address	Register Name	Total Reset Value
0x29044	ISP_AEWDR0_OFFSET_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_r	Black level offset

ISP_AEWDR0_OFFSET_GR

ISP_AEWDR0_OFFSET_GR is a Gr component black level offset register.

Offset Address	Register Name	Total Reset Value
0x29048	ISP_AEWDR0_OFFSET_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_gr	Black level offset

ISP_AEWDR0_OFFSET_GB

ISP_AEWDR0_OFFSET_GB is a Gb component black level offset register.

Offset Address	Register Name	Total Reset Value
0x2904C	ISP_AEWDR0_OFFSET_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_gb	Black level offset

ISP_AEWDR0_OFFSET_B

ISP_AEWDR0_OFFSET_B is a B component black level offset register.

Offset Address	Register Name	Total Reset Value
0x29050	ISP_AEWDR0_OFFSET_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_b	Black level offset

ISP_AEWDR0_MEM_HIST_RADDR

ISP_AEWDR0_MEM_HIST_RADDR is an AEWDR0 histogram statistics read address register.

Offset Address	Register Name	Total Reset Value
0x29088	ISP_AEWDR0_MEM_HIST_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hist_raddr	Read address of histogram statistics

ISP_AEWDR0_MEM_HIST_RDATA

ISP_AEWDR0_MEM_HIST_RDATA is an AEWDR0 histogram statistics read data register.

Offset Address	Register Name	Total Reset Value
0x2908C	ISP_AEWDR0_MEM_HIST_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hist_rdata	Read data of histogram statistics

ISP_AEWDR0_MEM_WEIGHT_WADDR

ISP_AEWDR0_MEM_WEIGHT_WADDR is a zone weight write address register.

Offset Address	Register Name	Total Reset Value
0x290A0	ISP_AEWDR0_MEM_WEIGHT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wei_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wei_waddr	Write address of the weight table

ISP_AEWDR0_MEM_WEIGHT_WDATA

ISP_AEWDR0_MEM_WEIGHT_WDATA is a zone weight write data register.

Offset Address	Register Name	Total Reset Value
0x290A4	ISP_AEWDR0_MEM_WEIGHT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wei_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	wei_wdata	Write data of the weight table

ISP_AEWDR0_SIZE

ISP_AEWDR0_SIZE is an AEWDR0 picture size register.

Offset Address	Register Name	Total Reset Value
0x290F0	ISP_AEWDR0_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	vsize	Picture height
[15:13]	-	reserved	Reserved
[12:0]	RW	hsize	Picture width

ISP_AEWDR1_CFG

ISP_AEWDR1_CFG is an AEWDR1 enable register.

Offset Address	Register Name	Total Reset Value
0x29100	ISP_AEWDR1_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	AEWDR1 enable 0: disabled 1: enabled

ISP_AEWDR1_ZONE

ISP_AEWDR1_ZONE is an AEWDR1 zone configuration register.

Offset Address	Register Name	Total Reset Value
0x29110	ISP_AEWDR1_ZONE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				vnum				reserved				hnum			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12:8]	RW	vnum	Number of zones in the vertical direction
[7:5]	-	reserved	Reserved
[4:0]	RW	hnum	Number of zones in the horizontal direction

ISP_AEWDR1_SKIP_CRG

ISP_AEWDR1_SKIP_CRG is an AEWDR1 point select configuration register.

Offset Address	Register Name	Total Reset Value
0x29114	ISP_AEWDR1_SKIP_CRG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						offset_y	skip_y	offset_x	skip_x
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7]	RW	offset_y	Count start row 0: count from row 0 1: count from row 1
[6:4]	RW	skip_y	Vertical point skip for statistics 000: counted for each pixel point 001: counted for every two pixels 010: counted for every three pixels 011: counted for every four pixels 100: counted for every five pixels 101: counted for every eight pixels 110 or above: counted for every nine pixels
[3]	RW	offset_x	Count start column 0: count from column 0 1: count from column 1
[2:0]	RW	skip_x	Horizontal point skip for statistics 000: counted for every two pixels 001: counted for every three pixels 010: counted for every four pixels 011: counted for every five pixels 100: counted for every eight pixels 101 or above: counted for every nine pixels

ISP_AEWDR1_TOTAL_STAT

ISP_AEWDR1_TOTAL_STAT is a selected pixel count register in a frame during 256 histogram statistics.

Offset Address	Register Name	Total Reset Value
0x29118	ISP_AEWDR1_TOTAL_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								total_pixels																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:0]	RO	total_pixels	Number of selected pixels in a frame during 256 histogram statistics

ISP_AEWDR1_COUNT_STAT

ISP_AEWDR1_COUNT_STAT is a selected pixel weight count register in a frame during 256 histogram statistics.

Offset Address	Register Name	Total Reset Value
0x2911C	ISP_AEWDR1_COUNT_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				count_pixels																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:0]	RO	count_pixels	Total weight of the selected pixels in a frame during 256 histogram statistics

ISP_AEWDR1_HIST_HIGH

ISP_AEWDR1_HIST_HIGH is a histogram statistics high register.

Offset Address	Register Name	Total Reset Value
0x29130	ISP_AEWDR1_HIST_HIGH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_high																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hist_high	Upper bits in histogram statistics

ISP_AEWDR1_BITMOVE

ISP_AEWDR1_BITMOVE is an AEWDR1 pixel shift register.

Offset Address	Register Name	Total Reset Value
0x29140	ISP_AEWDR1_BITMOVE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						BLC_en	reserved				bitmove			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9]	RW	BLC_en	AEWDR1 BLC enable
[8:5]	-	reserved	Reserved
[4:0]	RW	bitmove	AEWDR1 pixel shift value

ISP_AEWDR1_OFFSET_R

ISP_AEWDR1_OFFSET_R is an R component black level offset register.

Offset Address	Register Name	Total Reset Value
0x29144	ISP_AEWDR1_OFFSET_R	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_r															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_r	Black level offset

ISP_AEWDR1_OFFSET_GR

ISP_AEWDR1_OFFSET_GR is a Gr component black level offset register.

Offset Address	Register Name	Total Reset Value
0x29148	ISP_AEWDR1_OFFSET_GR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gr															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_gr	Black level offset

ISP_AEWDR1_OFFSET_GB

ISP_AEWDR1_OFFSET_GB is a Gb component black level offset register.

Offset Address	Register Name	Total Reset Value
0x2914C	ISP_AEWDR1_OFFSET_GB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_gb															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_gb	Black level offset

ISP_AEWDR1_OFFSET_B

ISP_AEWDR1_OFFSET_B is a B component black level offset register.

Offset Address	Register Name	Total Reset Value
0x29150	ISP_AEWDR1_OFFSET_B	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																offset_b															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	RW	reserved	Reserved
[14:0]	RW	offset_b	Black level offset

ISP_AEWDR1_MEM_HIST_RADDR

ISP_AEWDR1_MEM_HIST_RADDR is an AEWDR1 histogram statistics read address register.

Offset Address	Register Name	Total Reset Value
0x29188	ISP_AEWDR1_MEM_HIST_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	hist_raddr	Read address of histogram statistics

ISP_AEWDR1_MEM_HIST_RDATA

ISP_AEWDR1_MEM_HIST_RDATA is an AEWDR1 histogram statistics read data register.

Offset Address	Register Name	Total Reset Value
0x2918C	ISP_AEWDR1_MEM_HIST_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hist_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hist_rdata	Read data of histogram statistics

ISP_AEWDR1_SIZE

ISP_AEWDR1_SIZE is an AEWDR1 picture size register.

Offset Address	Register Name	Total Reset Value
0x291F0	ISP_AEWDR1_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				vsize												reserved				hsize											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	vsize	Picture height
[15:13]	-	reserved	Reserved
[12:0]	RW	hsize	Picture width

ISP_BE_FSTART_DELAY

ISP_BE_FSTART_DELAY is an ISP adjustable interrupt trigger time configuration register.

Offset Address	Register Name	Total Reset Value
0x40094	ISP_BE_FSTART_DELAY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	delay																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	delay	Adjustable interrupt trigger time

ISP_BE_USER_DEFINE0

ISP_BE_USER_DEFINE0 is user-defined register 0.

Offset Address	Register Name	Total Reset Value
0x400A0	ISP_BE_USER_DEFINE0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	user_define0							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	user_define0	User-defined register 0

ISP_BE_USER_DEFINE1

ISP_BE_USER_DEFINE1 is user-defined register 1.

Offset Address	Register Name	Total Reset Value
0x400A4	ISP_BE_USER_DEFINE1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	user_define1							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	user_define1	User-defined register 1

ISP_BE_STARTUP

ISP_BE_STARTUP is an ISP BE startup indicator register.

Offset Address	Register Name	Total Reset Value
0x400B0	ISP_BE_STARTUP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	fcnt							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RO	fcnt	Frame count after startup

ISP_BE_INT

ISP_BE_INT is an ISP interrupt indicator register.

Offset Address	Register Name	Total Reset Value
0x400F0	ISP_BE_INT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															acm_para_finish	reserved												fstart_delay	cfg_loss	update_cfg	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved
[16]	WC	acm_para_finish	Status of the ACM LUT load completion interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[15:4]	-	reserved	Reserved
[3]	WC	fstart_delay	Status of the configurable trigger delay interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[2]	WC	cfg_loss	Status of the register configuration loss interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[1]	WC	update_cfg	Status of the register update interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.
[0]	WC	fstart	Status of the ISP frame start interrupt. Writing 1 clears the interrupt. 0: No interrupt is generated. 1: An interrupt is generated.

ISP_BE_INT_MASK

ISP_BE_INT_MASK is an ISP interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x400F8	ISP_BE_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															acm_para_finish	reserved												int_delay	cfg_loss	update_cfg	fstart
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved
[16]	RW	acm_para_finish	ACM LUT load completion interrupt enable 0: disabled 1: enabled
[15:4]	-	reserved	Reserved
[3]	RW	int_delay	Configurable trigger delay interrupt enable 0: disabled 1: enabled
[2]	RW	cfg_loss	Register configuration loss interrupt enable 0: disabled 1: enabled
[1]	RW	update_cfg	Register update interrupt enable 0: disabled 1: enabled
[0]	RW	fstart	ISP frame start interrupt enable 0: disabled 1: enabled

ISP_BE_CTRL_F

ISP_BE_CTRL_F is an ISP common update control register.

Offset Address	Register Name	Total Reset Value
0x401E0	ISP_BE_CTRL_F	0x0000_0003

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							rggb_cfg
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 1

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1:0]	RW	rggb_cfg	RGGB start 00: R Gr Gb B 01: Gr R B Gb 10: Gb B R Gr 11: B Gb Gr R

ISP_BE_CTRL_I

ISP_BE_CTRL_I is an ISP immediate update control register.

Offset Address	Register Name	Total Reset Value
0x401E4	ISP_BE_CTRL_I	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							update_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update_mode	ISP register update mode 0: update by using ISP_BE_REG_UPDATE 1: frame update

ISP_BE_TIMING_CFG

ISP_BE_TIMING_CFG is an output timing configuration register.

Offset Address	Register Name	Total Reset Value
0x401E8	ISP_BE_TIMING_CFG	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				fix_timing											reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13:1]	RW	fix_timing	Manual timing parameter configuration, for setting the length of the generated horizontal blanking region
[0]	-	reserved	Reserved

ISP_BE_REG_UPDATE

ISP_BE_REG_UPDATE is a register update register.

Offset Address	Register Name	Total Reset Value
0x401EC	ISP_BE_REG_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update	ISP update register. This bit is automatically cleared for each frame.

ISP_CLIP_Y_CFG

ISP_CLIP_Y_CFG is a luminance clamping configuration register.

Offset Address	Register Name	Total Reset Value
0x40800	ISP_CLIP_Y_CFG	0xFFFF_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	max				min			
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum value of luminance clamping. If the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum value of luminance clamping. If the data bit width is less than 16 bits, the upper bits are valid.

ISP_CLIP_C_CFG

ISP_CLIP_C_CFG is a chrominance clamping configuration register.

Offset Address	Register Name	Total Reset Value
0x40804	ISP_CLIP_C_CFG	0xFFFF_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	max				min			
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RW	max	Maximum value of chrominance clamping. If the data bit width is less than 16 bits, the upper bits are valid.
[15:0]	RW	min	Minimum value of chrominance clamping. If the data bit width is less than 16 bits, the upper bits are valid.

ISP_SKIP_Y_CFG

ISP_SKIP_Y_CFG is a Y component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x40810	ISP_SKIP_Y_CFG	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	skip_cfg							
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration

ISP_SKIP_C_CFG

ISP_SKIP_C_CFG is a C component skip configuration register.

Offset Address	Register Name	Total Reset Value
0x40818	ISP_SKIP_C_CFG	0xFFFF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	skip_cfg																															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:0]	RW	skip_cfg	Skip configuration

ISP_CSC_SUM_CFG

ISP_CSC_SUM_CFG is a CSC statistics and configuration register.

Offset Address	Register Name	Total Reset Value
0x40820	ISP_CSC_SUM_CFG	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	Summation enable 0: disabled 1: enabled

ISP_DMNR_DITHER

ISP_DMNR_DITHER is an ISP DMNR dither register.

Offset Address	Register Name	Total Reset Value
0x40840	ISP_DMNR_DITHER	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								out_bits				spatial_mode	isp_dither_round		isp_dither_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:4]	RW	out_bits	Output bit width 0x8: 8 bits 0xA: 10 bits 0xC: 12 bits 0xE: 14 bits Other values: forbidden
[3]	RW	spatial_mode	Spatial mode enable 0: disabled 1: enabled
[2:1]	RW	isp_dither_round	Dither mode select 00: truncation 01: round off 10: random
[0]	RW	isp_dither_en	Dither enable 0: disabled 1: enabled

ISP_ACM_DITHER

ISP_ACM_DITHER is an ISP ACM dither register.

Offset Address	Register Name	Total Reset Value
0x40850	ISP_ACM_DITHER	0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								out_bits				spatial_mode	isp_dither_round		isp_dither_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:4]	RW	out_bits	Output bit width 0x8: 8 bits 0xA: 10 bits 0xC: 12 bits 0xE: 14 bits Other values: forbidden
[3]	RW	spatial_mode	Spatial mode enable 0: disabled 1: enabled
[2:1]	RW	isp_dither_round	Dither mode select 00: truncation 01: round off 10: random
[0]	RW	isp_dither_en	Dither enable 0: disabled 1: enabled

ISP_Y_SUM0

ISP_Y_SUM0 is an input picture luminance sum low register.

Offset Address	Register Name	Total Reset Value
0x40880	ISP_Y_SUM0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Lower 32 bits of luminance sum statistics

ISP_Y_SUM1

ISP_Y_SUM1 is an input picture luminance sum high register.

Offset Address	Register Name	Total Reset Value
0x40884	ISP_Y_SUM1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sum																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sum	Upper 32 bits of luminance sum statistics

ISP_SPLIT_CFG

ISP_SPLIT_CFG is a split enable register.

Offset Address	Register Name	Total Reset Value
0x40900	ISP_SPLIT_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	SPLIT enable 0: disabled 1: enabled

ISP_SPLIT_DATA_CFG

ISP_SPLIT_DATA_CFG is a split configuration register.

Offset Address	Register Name	Total Reset Value
0x40910	ISP_SPLIT_DATA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dc_data								reserved				data_sel		SPLIT_en		ex_yuv_en				ex_v_en	ex_u_en	ex_y_en	replace_v_en	replace_u_en	replace_y_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	-	reserved	Reserved
[22:16]	RW	dc_data	Data split DC component
[15:12]	-	reserved	Reserved
[11:10]	RW	data_sel	Data component to be splited 00: data 0 01: data 1 10: data 2 11: data 0
[9]	RW	SPLIT_en	Data split enable 0: disabled 1: enabled
[8:6]	RW	ex_yuv_en	YUV sequence of split data 000: YUV output 001: YVU output 010: UYV output 011: UVY output 100: VYU output 101: VUY output Other values: YUV output
[5]	RW	ex_v_en	Adjacent data exchange of split data V (Repeated exchange is not allowed. One data segment can be exchanged with the one that is two data segments away from it.) 0: disabled 1: enabled

[4]	RW	ex_u_en	Adjacent data exchange of split data U (Repeated exchange is not allowed. One data segment can be exchanged with the one that is two data segments away from it.) 0: disabled 1: enabled
[3]	RW	ex_y_en	Adjacent data exchange of split data Y (Repeated exchange is not allowed. One data segment can be exchanged with the one that is two data segments away from it.) 0: disabled 1: enabled
[2]	RW	replace_v_en	Storing split data information in channel V 0: disabled 1: enabled
[1]	RW	replace_u_en	Storing split data information in channel U 0: disabled 1: enabled
[0]	RW	replace_y_en	Storing split data information in channel Y 0: disabled 1: enabled

ISP_SPLIT_DATA_VERSION

ISP_SPLIT_DATA_VERSION is a split data version register.

Offset Address	Register Name	Total Reset Value
0x40914	ISP_SPLIT_DATA_VERSION	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																data_version															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	data_version	Split data version

ISP_SPLIT_DATA_BITWIDTH

ISP_SPLIT_DATA_BITWIDTH is a split data bit width register.

Offset Address	Register Name	Total Reset Value
0x40918	ISP_SPLIT_DATA_BITWIDTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																data_bitw															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	data_bitw	Bit width of split data

ISP_SPLIT_DATA_AGAIN

ISP_SPLIT_DATA_AGAIN is a split data analog gain information register.

Offset Address	Register Name	Total Reset Value
0x4091C	ISP_SPLIT_DATA_AGAIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_again																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data_again	Analog gain of split data

ISP_SPLIT_DATA_DGAIN

ISP_SPLIT_DATA_DGAIN is a split data digital gain information register.

Offset Address	Register Name	Total Reset Value
0x40920	ISP_SPLIT_DATA_DGAIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_dgain																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data_dgain	Digital gain of split data

ISP_SPLIT_DATA_SHUTTER

ISP_SPLIT_DATA_SHUTTER is a split data SHUTTER information register.

Offset Address	Register Name	Total Reset Value
0x40924	ISP_SPLIT_DATA_SHUTTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_shutter																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data_shutter	SHUTTER information of split data

ISP_CCM_CFG

ISP_CCM_CFG is a CCM enable register.

Offset Address	Register Name	Total Reset Value
0x41400	ISP_CCM_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												prot_ext_en	colortone_en	prot_en	en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved
[3]	RW	prot_ext_en	CCM dark region protection extended function enable 0: disabled 1: enabled
[2]	RW	colortone_en	CCM hue adjustment enable 0: disabled 1: enabled
[1]	RW	prot_en	CCM dark region protection enable 0: disabled 1: enabled
[0]	RW	en	CCM enable 0: disabled 1: enabled

ISP_CCM_COEF0

ISP_CCM_COEF0 is CCM coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x41410	ISP_CCM_COEF0	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef01															reserved	coef00															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef01	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef00	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CCM_COEF1

ISP_CCM_COEF1 is CCM coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x41414	ISP_CCM_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef10															reserved	coef02															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef10	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved

[15:1]	RW	coef02	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CCM_COEF2

ISP_CCM_COEF2 is CCM coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x41418	ISP_CCM_COEF2	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef12															reserved	coef11															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef12	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef11	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CCM_COEF3

ISP_CCM_COEF3 is CCM coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x4141C	ISP_CCM_COEF3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef21															reserved	coef20															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	coef21	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef20	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CCM_COEF4

ISP_CCM_COEF4 is CCM coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x41420	ISP_CCM_COEF4	0x0000_0800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																coef22															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:1]	RW	coef22	CCM coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CCM_BRIT_THRES

ISP_CCM_BRIT_THRES is a CCM luminance protection threshold register.

Offset Address	Register Name	Total Reset Value
0x41448	ISP_CCM_BRIT_THRES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								brit_thres1								reserved								brit_thres0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	brit_thres1	Luminance protection threshold 1 It is an unsigned integer.
[15:8]	-	reserved	Reserved
[7:0]	RW	brit_thres0	Luminance protection threshold 0 It is an unsigned integer.

ISP_CCM_COLOR_THRES

ISP_CCM_COLOR_THRES is a CCM chrominance protection threshold register.

Offset Address	Register Name	Total Reset Value
0x4144C	ISP_CCM_COLOR_THRES	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								color_thres1								reserved								color_thres0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	color_thres1	Chrominance protection threshold 1 It is an unsigned integer.
[15:8]	-	reserved	Reserved
[7:0]	RW	color_thres0	Chrominance protection threshold 0 It is an unsigned integer.

ISP_CCM_LOW_RATIO

ISP_CCM_LOW_RATIO is a CCM blending ratio threshold register.

Offset Address	Register Name	Total Reset Value
0x41450	ISP_CCM_LOW_RATIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								low_ratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	low_ratio	Blending ratio threshold It is an unsigned integer.

ISP_CCM_PRO_RATIO

ISP_CCM_PRO_RATIO is a CCM blending ratio register.

Offset Address	Register Name	Total Reset Value
0x41454	ISP_CCM_PRO_RATIO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				brit_ratio												reserved				color_ratio											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	brit_ratio	Luminance blending ratio
[15:12]	-	reserved	Reserved
[11:0]	RW	color_ratio	Chromiance blending ratio

ISP_CCM_COLORTONE_RB_GAIN

ISP_CCM_COLORTONE_RB_GAIN is a CCM hue adjustment RB channel gain register.

Offset Address	Register Name	Total Reset Value
0x41458	ISP_CCM_COLORTONE_RB_GAIN	0x0100_0100

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	r_gain			reserved	b_gain		
Reset	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	r_gain	R channel gain of CCM hue adjustment, 4.8 precision. It is an unsigned number.
[15:12]	-	reserved	Reserved
[11:0]	RW	b_gain	B channel gain of CCM hue adjustment, 4.8 precision. It is an unsigned number.

ISP_CCM_COLORTONE_G_GAIN

ISP_CCM_COLORTONE_G_GAIN is a CCM hue adjustment G channel gain register.

Offset Address	Register Name	Total Reset Value
0x4145C	ISP_CCM_COLORTONE_G_GAIN	0x0000_0100

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					g_gain		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	g_gain	G channel gain of CCM hue adjustment, 4.8 precision. It is an unsigned number.

ISP_CCM_PROT_EX_TH0

ISP_CCM_PROT_EX_TH0 is a CCM dark region protection extended function threshold 0 register.

Offset Address	Register Name	Total Reset Value
0x41460	ISP_CCM_PROT_EX_TH0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				data_bb_thd0								data_gg_thd0								data_rr_thd0											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:20]	RW	data_bb_thd0	BB threshold 0
[19:10]	RW	data_gg_thd0	GG threshold 0
[9:0]	RW	data_rr_thd0	RR threshold 0

ISP_CCM_PROT_EX_TH1

ISP_CCM_PROT_EX_TH1 is a CCM dark region protection extended function threshold 1 register.

Offset Address	Register Name	Total Reset Value
0x41464	ISP_CCM_PROT_EX_TH1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				data_bb_thd1								data_gg_thd1								data_rr_thd1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:20]	RW	data_bb_thd1	BB threshold 1
[19:10]	RW	data_gg_thd1	GG threshold 1
[9:0]	RW	data_rr_thd1	RR threshold 1

ISP_CCM_PROT_EX_RGB_SET

ISP_CCM_PROT_EX_RGB_SET is a CCM dark region protection extended function RGB configuration register.

Offset Address	Register Name	Total Reset Value
0x41468	ISP_CCM_PROT_EX_RGB_SET	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								max_rgb_thd								reserved								rgb_prot_ration							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	max_rgb_thd	Dark region threshold
[15:9]	-	reserved	Reserved
[8:0]	RW	rgb_prot_ration	Minimum gain of dark region color protection. It ranges from 0 to 256.

ISP_CSC_CFG

ISP_CSC_CFG is a CSC enable register.

Offset Address	Register Name	Total Reset Value
0x41500	ISP_CSC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	CSC enable 0: disabled 1: enabled

ISP_CSC_COEF0

ISP_CSC_COEF0 is CSC coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x41510	ISP_CSC_COEF0	0x05B8_01B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef01															reserved	coef00															reserved
Reset	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:17]	RW	coef01	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef00	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_COEF1

ISP_CSC_COEF1 is CSC coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x41514	ISP_CSC_COEF1	0xFF12_0092

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef10															reserved	coef02															reserved
Reset	1	1	1	1	1	1	1	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:17]	RW	coef10	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef02	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.

[0]	RO	reserved	Reserved

ISP_CSC_COEF2

ISP_CSC_COEF2 is CSC coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x41518	ISP_CSC_COEF2	0x0416_FCDA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef12															reserved	coef11															reserved
Reset	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	0	0	1	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:17]	RW	coef12	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef11	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_COEF3

ISP_CSC_COEF3 is CSC coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x4151C	ISP_CSC_COEF3	0xFC4A_0416

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	coef21															reserved	coef20															reserved
Reset	1	1	1	1	1	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0

Bits	Access	Name	Description
[31:17]	RW	coef21	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[16]	RO	reserved	Reserved
[15:1]	RW	coef20	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_COEF4

ISP_CSC_COEF4 is CSC coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x41520	ISP_CSC_COEF4	0x0000_FFA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															reserved	coef22															reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	reserved	Reserved
[15:1]	RW	coef22	CSC coefficient Its format is S5.10. It consists of a sign bit, a 4-bit integral part, and a 10-bit decimal part.
[0]	RO	reserved	Reserved

ISP_CSC_IN_DC0

ISP_CSC_IN_DC0 is CSC input DC component register 0.

Offset Address	Register Name	Total Reset Value
0x41530	ISP_CSC_IN_DC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	in_dc1												reserved				in_dc0												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RW	in_dc1	DC offset of the input G component, signed integer
[20:16]	RO	reserved	Reserved
[15:5]	RW	in_dc0	DC offset of the input R component, signed integer
[4:0]	RO	reserved	Reserved

ISP_CSC_IN_DC1

ISP_CSC_IN_DC1 is CSC input DC component register 1.

Offset Address	Register Name	Total Reset Value
0x41534	ISP_CSC_IN_DC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												reserved				in_dc2												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RO	reserved	Reserved
[15:5]	RW	in_dc2	DC offset of the output B component, signed integer
[4:0]	RO	reserved	Reserved

ISP_CSC_OUT_DC0

ISP_CSC_OUT_DC0 is CSC output DC component register 0.

Offset Address	Register Name	Total Reset Value
0x41540	ISP_CSC_OUT_DC0	0x4000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	out_dc1			reserved	out_dc0			reserved
Reset	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RW	out_dc1	DC offset of the output U component, signed integer
[20:16]	RO	reserved	Reserved
[15:5]	RW	out_dc0	DC offset of the output Y component, signed integer
[4:0]	RO	reserved	Reserved

ISP_CSC_OUT_DC1

ISP_CSC_OUT_DC1 is CSC output DC component register 1.

Offset Address	Register Name	Total Reset Value
0x41544	ISP_CSC_OUT_DC1	0x0000_4000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			reserved	out_dc2			reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20:16]	RO	reserved	Reserved
[15:5]	RW	out_dc2	DC offset of the output V component, signed integer
[4:0]	RO	reserved	Reserved

ISP_MCDS_CFG

ISP_UVNR_CFG is a MCDS control register.

Offset Address	Register Name	Total Reset Value
0x41800	ISP_MCDS_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											midf_en	uv2c_mode	reserved	vcds_en	hcds_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4]	RW	uvnr_sel	MCDSILTER enable 0: disabled 1: enabled
[3]	RW	uv2c_mode	UV2C bypass mode 0: Output the U component data. 1: Output the V component data.
[2]	-	reserved	Reserved
[1]	RW	vcds_en	Chrominance vertical down sampling enable 0: disabled 1: enabled
[0]	RW	hcds_en	Chrominance horizontal down sampling enable 0: disabled 1: enabled

ISP_HCDS_SIZE

ISP_HCDS_SIZE is a horizontal chrominance down sampling input size configuration register.

Offset Address	Register Name	Total Reset Value
0x41814	ISP_HCDS_SIZE	0x03BF_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				width_out												reserved				width_in											
Reset	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	width_out	U/V line width (in pixel) of the output picture during horizontal chrominance down sampling. The configured value is the actual value minus 1.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width_in	U/V line width (in pixel) of the input picture. The configured value is the actual value minus 1.

ISP_HCDS_COEF0

ISP_HCDS_COEF0 is horizontal chrominance down sampling coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x4181C	ISP_HCDS_COEF0	0x0910_03F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef2								coef1								coef0											
Reset	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	coef2	Horizontal chrominance scaling and filtering coefficient 2
[19:10]	RW	coef1	Horizontal chrominance scaling and filtering coefficient 1
[9:0]	RW	coef0	Horizontal chrominance scaling and filtering coefficient 0 Horizontal scaling contains eight taps, and the sum of the eight coefficients is 512. The format is S10.0 and the value range is [–512, 511].

ISP_HCDS_COEF1

ISP_HCDS_COEF1 is horizontal chrominance down sampling coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x41820	ISP_HCDS_COEF1	0x0002_44FE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				coef5								coef4								coef3											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	coef5	Horizontal chrominance scaling and filtering coefficient 5
[19:10]	RW	coef4	Horizontal chrominance scaling and filtering coefficient 4
[9:0]	RW	coef3	Horizontal chrominance scaling and filtering coefficient 3

ISP_HCDS_COEF2

ISP_HCDS_COEF2 is horizontal chrominance down sampling coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x41824	ISP_HCDS_COEF2	0x0000_03F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												coef7								coef6											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:10]	RW	coef7	Horizontal chrominance scaling and filtering coefficient 7
[9:0]	RW	coef6	Horizontal chrominance scaling and filtering coefficient 6

ISP_VCDS_COEF

ISP_VCDS_COEF is a vertical chrominance down sampling coefficient register.

Offset Address	Register Name	Total Reset Value
0x41828	ISP_VCDS_COEF	0x0606_0404

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	coef3	reserved	coef2	reserved	coef1	reserved	coef0
Reset	0 0 0 0	0 1 1 0	0 0 0 0	0 1 1 0	0 0 0 0	0 1 0 0	0 0 0 0	0 1 0 0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:24]	RW	coef3	Down sampling coefficient 3. The value meanings are the same as those of coefficient 0.
[23:19]	RO	reserved	Reserved
[18:16]	RW	coef2	Down sampling coefficient 2. The value meanings are the same as those of coefficient 0.
[15:11]	RO	reserved	Reserved
[10:8]	RW	coef1	Down sampling coefficient 1. The value meanings are the same as those of coefficient 0.
[7:3]	RO	reserved	Reserved
[2:0]	RW	coef0	Down sampling coefficient 0 000: multiplied by 1 001: multiplied by 2 010: multiplied by 4 011: multiplied by 8 100: multiplied by 16 101: multiplied by 32 110: multiplied by 0 111: multiplied by 0 (invalid)

ISP_MIDF_SIZE

ISP_MIDF_SIZE is a median filtering input picture chrominance width/height register.

Offset Address	Register Name	Total Reset Value
0x4182C	ISP_MIDF_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Picture height after vertical chrominance down sampling. The configured value is the actual height minus 1. For example, if the actual picture height is 720, set this field to 719.
[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Picture width after vertical chrominance down sampling (UV-to-C conversion). The configured value is the actual width minus 1. For example, if the actual picture width is 1280, set this field to 1279.

ISP_MCDS_PARA

ISP_MCDS_PARA is an NR blending ratio and shift register.

Offset Address	Register Name	Total Reset Value
0x41844	ISP_MCDS_PARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				midf_bldr				reserved	limit							reserved															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:24]	RW	midf_bldr	MIDF blending ratio. The format is U5.0 and the value range is [0, 16].
[23]	-	reserved	Reserved
[22:16]	RW	limit	Coring function limit configuration. The format is U7.0 and the value range is [0, 127].
[15:0]	-	reserved	Reserved

ISP_MCDS_SIZE

ISP_MCDS_SIZE is an MCDS input picture size register.

Offset Address	Register Name	Total Reset Value
0x418F0	ISP_MCDS_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Input picture height. The configured value is the actual value minus 1. For example, for the 1080P picture, set the height to 1079.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Input picture width. The configured value is the actual value minus 1. For example, for the 1080P picture, set the width to 1919.

ISP_GCAC_CFG

ISP_GCAC_CFG is global CAC control register.

Offset Address	Register Name	Total Reset Value
0x43200	ISP_GCAC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															gcac_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	gcac_en	Global CAC enable 0: disabled 1: enabled

ISP_GCAC_PARAMA

ISP_GCAC_PARAMA is a global CAC polynomial coefficient A register.

Offset Address	Register Name	Total Reset Value
0x43210	ISP_GCAC_PARAMA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blue_a								reserved								red_a							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	blue_a	Coefficient A of the B component. The format is S9.0 and the value range is [–256, 255].
[15:9]	-	reserved	Reserved
[8:0]	RW	red_a	Coefficient A of the R component. The format is S9.0 and the value range is [–256, 255].

ISP_GCAC_PARAMB

ISP_GCAC_PARAMB is a global CAC polynomial coefficient B register.

Offset Address	Register Name	Total Reset Value
0x43214	ISP_GCAC_PARAMB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								blue_b								reserved								red_b							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	blue_b	Coefficient B of the B component. The format is S9.0 and the value range is [–256, 255].
[15:9]	-	reserved	Reserved
[8:0]	RW	red_b	Coefficient B of the R component. The format is S9.0 and the value range is [–256, 255].

ISP_GCAC_PARAMC

ISP_GCAC_PARAMC is a global CAC polynomial coefficient C register.

Offset Address	Register Name	Total Reset Value
0x43218	ISP_GCAC_PARAMC	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			blue_c	reserved		red_c	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	blue_c	Coefficient C of the B component. The format is S9.0 and the value range is [–256, 255].
[15:9]	-	reserved	Reserved
[8:0]	RW	red_c	Coefficient C of the R component. The format is S9.0 and the value range is [–256, 255].

ISP_GCAC_YNORM

ISP_GCAC_YNORM is a global CAC vertical normalization factor register.

Offset Address	Register Name	Total Reset Value
0x4321C	ISP_GCAC_YNORM	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			ns_y	reserved		nf_y	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved
[18:16]	RW	ns_y	Vertical shift factor. The format is U4.0 and the value range is [0, 7].
[15:5]	-	reserved	Reserved
[4:0]	RW	nf_y	Vertical normalization factor. The format is U5.0 and the value range is [0, 31].

ISP_GCAC_XNORM

ISP_GCAC_XNORM is a global CAC horizontal normalization factor register.

Offset Address	Register Name	Total Reset Value
0x43220	ISP_GCAC_XNORM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												ns_x				reserved								nf_x							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	-	reserved	Reserved
[18:16]	RW	ns_x	Horizontal shift factor. The format is U4.0 and the value range is [0, 7].
[15:5]	-	reserved	Reserved
[4:0]	RW	nf_x	Horizontal normalization factor. The format is U5.0 and the value range is [0, 31].

ISP_GCAC_CNTSTART

ISP_GCAC_CNTSTART is a global CAC optical center coordinate register.

Offset Address	Register Name	Total Reset Value
0x43224	ISP_GCAC_CNTSTART	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cnt_start_v												reserved				cnt_start_h											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	cnt_start_v	Vertical coordinate of the global CAC optical center. The format is U13.0 and the value range is [0, 8191].
[15:13]	-	reserved	Reserved
[12:0]	RW	cnt_start_h	Horizontal coordinate of the global CAC optical center. The format is U13.0 and the value range is [0, 8191].

ISP_GCAC_CORSTART

ISP_GCAC_CORSTART is a global CAC original picture start coordinate register.

Offset Address	Register Name	Total Reset Value
0x43228	ISP_GCAC_CORSTART	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cor_start_v												reserved				cor_start_h											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	cor_start_v	Start vertical coordinate of the global CAC original picture. The format is U13.0 and the value range is [0, 8191].
[15:13]	-	reserved	Reserved
[12:0]	RW	cor_start_h	Start horizontal coordinate of the global CAC original picture. The format is U13.0 and the value range is [0, 8191].

ISP_GCAC_FILTEN

ISP_GCAC_FILTEN is a global CAC filtering enable register.

Offset Address	Register Name	Total Reset Value
0x4322C	ISP_GCAC_FILTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ver_filt_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	ver_filt_en	Global CAC vertical filtering enable 0: disabled 1: enabled

ISP_GCAC_CHRVMODE

ISP_GCAC_CHRVMODE is a global CAC filtering mode select register.

Offset Address	Register Name	Total Reset Value
0x43230	ISP_GCAC_CHRVMODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							chrv_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0

Bits	Access	Name	Description
[31:2]	-	reserved	Reserved
[1:0]	RW	chrv_mode	Global CAC vertical filtering mode 00: invalid 01: filtering coefficient {8,16,8} 10: filtering coefficient {10,12,10} 11: filtering coefficient {12,8,12}

ISP_GCAC_CLIPMODE

ISP_GCAC_CLIPMODE is a global CAC clipping mode select register.

Offset Address	Register Name	Total Reset Value
0x43234	ISP_GCAC_CLIPMODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				clip_mode_v	reserved		clip_mode_h
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved

[17:16]	RW	clip_mode_v	Global CAC vertical clipping mode. The value ranges from 0 to 2. 00: fixed clipping. The clipping range is [96, 160]. 01: fixed clipping. The clipping range is [80, 176]. 10: dynamic clipping. The clipping range is determined by the Bayer format of the pixel. The clipping range for the R and B pixels is [64, 192], and that for the Gr and Gb pixels is [80, 176]. 11: invalid
[15:1]	-	reserved	Reserved
[0]	RW	clip_mode_h	Global CAC horizontal clipping mode 0: fixed clipping. The clipping range is [64, 192]. 1: dynamic clipping, The clipping range is determined by the Bayer format of the pixel. The clipping range for column R (R and Gb) on plane R is [64, 192], that for column B (B and Gr) on plane R is [80,176], that for column R on plane B is [80, 176], and that for column B on plane B is [64, 192].

ISP_GCAC_SIZE

ISP_GCAC_SIZE is a global CAC input picture size register.

Offset Address	Register Name	Total Reset Value
0x432F0	ISP_GCAC_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Input picture height. The configured value is the actual value minus 1. For example, for the 1080P picture, set the height to 1079.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Input picture width. The configured value is the actual value minus 1. For example, for the 1080P picture, set the width to 1919.

ISP_DEMOSAIC_CFG

ISP_DEMOSAIC_CFG is a demosaic control register.

Offset Address	Register Name	Total Reset Value
0x44000	ISP_DEMOSAIC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	Demosaic enable 0: disabled 1: enabled

ISP_DEMOSAIC_CFG1

ISP_DEMOSAIC_CFG1 is a demosaic internal algorithm enable register.

Offset Address	Register Name	Total Reset Value
0x44004	ISP_DEMOSAIC_CFG1	0x003B_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										de_fake_en	mid_filter_en	hv_dir_en	gcac_blend_select	local_cac_en	fcr_en	reserved																	ahd_en
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21]	RW	de_fake_en	Demosaic anti-false color enable 1: enabled 0: disabled
[20]	RW	mid_filter_en	Demosaic RGB interpolation median filtering enable 1: enabled 0: disabled
[19]	RW	hv_dir_en	Demosaic HV direction correction enable 0: disabled 1: enabled

[18]	RW	gcac_blend_select	GCAC and Demosaic data blending control 0: The output data is the GCAC and demosaic blending data. 1: The RB component of the output data is GCAC data.
[17]	RW	local_cac_en	Demosaic local cac nable 0: disabled 1: enabled
[16]	RW	fcr_en	Demosaic FCR enable 0: disabled 1: enabled
[15:1]	RO	reserved	Reserved
[0]	RW	ahd_en	Demosaic AHD enable 0: disabled 1: enabled

ISP_DEMOSAIC_COEF0

ISP_DEMOSAIC_COEF0 is a demosaic parameter register 0.

Offset Address	Register Name	Total Reset Value
0x44010	ISP_DEMOSAIC_COEF0	0x0018_0028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								bld_limit1								reserved								bld_limit2							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	bld_limit1	Demosaic gradient blending threshold (U8.0)
[15:8]	RO	reserved	Reserved
[7:0]	RW	bld_limit2	Demosaic gradient blending threshold (U8.0)

ISP_DEMOSAIC_COEF1

ISP_DEMOSAIC_COEF1 is a demosaic parameter register 1.

Offset Address	Register Name	Total Reset Value
0x44014	ISP_DEMOSAIC_COEF1	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												bld_ratio1				reserved								bld_ratio2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	bld_ratio1	Demosaic gradient blending threshold (U9.0)
[15:9]	RO	reserved	Reserved
[8:0]	RW	bld_ratio2	Demosaic gradient blending threshold (U9.0)

ISP_DEMOSAIC_COEF2

ISP_DEMOSAIC_COEF2 is a demosaic parameter register 2.

Offset Address	Register Name	Total Reset Value
0x44018	ISP_DEMOSAIC_COEF2	0x0010_00A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fcr_limit1												reserved				fcr_limit2											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	fcr_limit1	Demosaic FCR threshold (U12.0)
[15:12]	RO	reserved	Reserved
[11:0]	RW	fcr_limit2	Demosaic FCR threshold (U12.0)

ISP_DEMOSAIC_COEF3

ISP_DEMOSAIC_COEF3 is a demosaic parameter register 3.

Offset Address	Register Name	Total Reset Value
0x4401C	ISP_DEMOSAIC_COEF3	0x0190_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ahd_par1								reserved								ahd_par2							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	ahd_par1	Demosaic AHD coefficient (U10.0)
[15:8]	RO	reserved	Reserved
[7:0]	RW	ahd_par2	Demosaic AHD coefficient (U8.0)

ISP_DEMOSAIC_COEF4

ISP_DEMOSAIC_COEF4 is a demosaic parameter register 4.

Offset Address	Register Name	Total Reset Value
0x44020	ISP_DEMOSAIC_COEF4	0x0001_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fcr_thr												reserved												fcr_gain			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	fcr_thr	Demosaic FCR threshold (U12.0)
[15:5]	RO	reserved	Reserved
[4:0]	RW	fcr_gain	Demosaic FCR gain (U5.0)

ISP_DEMOSAIC_COEF5

ISP_DEMOSAIC_COEF5 is a demosaic parameter register 5.

Offset Address	Register Name	Total Reset Value
0x44024	ISP_DEMOSAIC_COEF5	0x0000_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								hv_ratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	hv_ratio	Direction ratio (U8.0)

ISP_DEMOSAIC_COEF6

ISP_DEMOSAIC_COEF6 is a demosaic parameter register 6.

Offset Address	Register Name	Total Reset Value
0x44028	ISP_DEMOSAIC_COEF6	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												fcr_ratio			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:0]	RW	fcr_ratio	DEMOSAIC FCR adjustment ratio (U6.0)

ISP_DEMOSAIC_SEL

ISP_DEMOSAIC_SEL is a direction select register.

Offset Address	Register Name	Total Reset Value
0x44030	ISP_DEMOSAIC_SEL	0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														hv_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1:0]	RW	hv_sel	Direction select (U2.0)

ISP_DEMOSAIC_LCAC_CNT_THR

ISP_DEMOSAIC_LCAC_CNT_THR is a demosaic LCAC highlight count threshold register.

Offset Address	Register Name	Total Reset Value
0x44038	ISP_DEMOSAIC_LCAC_CNT_THR	0x0000_0421

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																g_counter_thr				b_counter_thr				r_counter_thr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:10]	RW	g_counter_thr	Demosaic LCAC highlight count G threshold
[9:5]	RW	b_counter_thr	Demosaic LCAC highlight count B threshold
[4:0]	RW	r_counter_thr	Demosaic LCAC highlight count R threshold

ISP_DEMOSAIC_LCAC_LUMA_RB_THR

ISP_DEMOSAIC_LCAC_LUMA_RB_THR is a demosaic LCAC_RB highlight threshold register.

Offset Address	Register Name	Total Reset Value
0x4403C	ISP_DEMOSAIC_LCAC_LUMA_RB_THR	0x01F4_01F4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				b_luma_thr												reserved				r_luma_thr											
Reset	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	b_luma_thr	Demosaic LCAC highlight B threshold
[15:12]	-	reserved	Reserved
[11:0]	RW	r_luma_thr	Demosaic LCAC highlight R threshold

ISP_DEMOSAIC_LCAC_LUMA_G_THR

ISP_DEMOSAIC_LCAC_LUMA_G_THR is a demosaic LCAC_G highlight threshold register.

Offset Address	Register Name	Total Reset Value
0x44040	ISP_DEMOSAIC_LCAC_LUMA_G_THR	0x0000_01F4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				g_luma_thr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	g_luma_thr	Demosaic LCAC highlight G threshold

ISP_DEMOSAIC_PURPLE_VAR_THR

ISP_DEMOSAIC_PURPLE_VAR_THR is a demosaic purple fringing detection variance threshold register.

Offset Address	Register Name	Total Reset Value
0x44044	ISP_DEMOSAIC_PURPLE_VAR_THR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				purple_var_thr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	purple_var_thr	Variance threshold of demosaic purple fringing detection

ISP_DEMOSAIC_FAKE_CR_VAR_THR

ISP_DEMOSAIC_FAKE_CR_VAR_THR is a demosaic false color detection threshold register.

Offset Address	Register Name	Total Reset Value
0x44048	ISP_DEMOSAIC_FAKE_CR_VAR_THR	0x012C_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fake_cr_var_thr_high												reserved				fake_cr_var_thr_low											
Reset	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved

[27:16]	RW	fake_cr_var_thr_high	Upper threshold of demosaic false color detection
[15:12]	-	reserved	Reserved
[11:0]	RW	fake_cr_var_thr_low	Lower threshold of demosaic false color detection

ISP_DEMOSAIC_DEPURPLECTR

ISP_DEMOSAIC_DEPURPLECTR is a demosaic purple fringing removal strength control register.

Offset Address	Register Name	Total Reset Value
0x4404C	ISP_DEMOSAIC_DEPURPLECTR	0x0008_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												depurplectrcr				reserved												depurplectrcb			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:20]	-	reserved	Reserved
[19:16]	RW	depurplectrcr	Demosaic de-purple fringing Cr strength
[15:4]	-	reserved	Reserved
[3:0]	RW	depurplectrcb	Demosaic de-purple fringing Cb strength

ISP_DEMOSAIC_HV_POINT_THLD

ISP_DEMOSAIC_HV_POINT_THLD is a demosaic direction detection threshold register.

Offset Address	Register Name	Total Reset Value
0x44050	ISP_DEMOSAIC_HV_POINT_THLD	0x0014_0014

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tot_point_thld								reserved				sig_point_thld											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	tot_point_thld	Demosaic block direction detection threshold
[15:10]	-	reserved	Reserved
[9:0]	RW	sig_point_thld	Demosaic single-point direction detection threshold

ISP_DEMOSAIC_BLD_ADJUST

ISP_DEMOSAIC_BLD_ADJUST is a demosaic direction correction strength control register.

Offset Address	Register Name	Total Reset Value
0x44054	ISP_DEMOSAIC_BLD_ADJUST	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												bld_adjust			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved
[3:0]	RW	bld_adjust	Demosiac direction correction strength

ISP_DEMOSAIC_CBCRAVGTHLD

ISP_DEMOSAIC_CBCRAVGTHLD is a demosaic anti-false color average chromatic aberration threshold register.

Offset Address	Register Name	Total Reset Value
0x44058	ISP_DEMOSAIC_CBCRAVGTHLD	0x0000_0096

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				cbcr_avg_thld											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	cbcr_avg_thld	Demosaic anti-false color average chromatic aberration threshold

ISP_DEMOSAIC_GAPTHLD

ISP_DEMOSAIC_GAPTHLD is a demosaic median filtering condition register.

Offset Address	Register Name	Total Reset Value
0x4405C	ISP_DEMOSAIC_GAPTHLD	0x0064_00C8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				g_gap_thld												reserved				cr_gap_thld											
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	g_gap_thld	Luminance difference threshold of the demosaic median filtering condition
[15:12]	-	reserved	Reserved
[11:0]	RW	cr_gap_thld	Chrominance difference threshold of the demosaic median filtering condition

ISP_DEMOSAIC_COLORTHLD

ISP_DEMOSAIC_COLORTHLD is a demosaic direction correction register.

Offset Address	Register Name	Total Reset Value
0x44060	ISP_DEMOSAIC_COLORTHLD	0x0000_0032

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				colorthld											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	colorthld	Average chrominance threshold of demosaic direction correction

ISP_DEMOSAIC_GVAR_BLEND_THLD

ISP_DEMOSAIC_GVAR_BLEND_THLD is a demosaic blending threshold register.

Offset Address	Register Name	Total Reset Value
0x44064	ISP_DEMOSAIC_GVAR_BLEND_THLD	0x0000_0082

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				varthrforblend											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	varthrforblend	Threshold for demosaic GCAC and DM result blending

ISP_DEMOSAIC_SATU_THR

ISP_DEMOSAIC_SATU_THR is a demosaic purple detection saturation threshold register.

Offset Address	Register Name	Total Reset Value
0x44068	ISP_DEMOSAIC_SATU_THR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				satu_thr											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	satu_thr	Saturation threshold of demosaic purple detection

ISP_DEMOSAIC_CBCR_RATIO_LIMIT

ISP_DEMOSAIC_CBCR_RATIO_LIMIT is a demosaic purple region detection threshold register.

Offset Address	Register Name	Total Reset Value
0x4406C	ISP_DEMOSAIC_CBCR_RATIO_LIMIT	0x0124_0F21

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cbcr_ratio_high_limit												reserved				cbcr_ratio_low_limit											
Reset	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved

[27:16]	RW	cbcr_ratio_high_limit	Upper threshold of purple region detection
[15:12]	-	reserved	Reserved
[11:0]	RW	cbcr_ratio_low_limit	Lower threshold of purple region detection

ISP_DEMOSAIC_FCR_GRAY_RATIO

ISP_DEMOSAIC_FCR_GRAY_RATIO is a demosaic FCR blending ratio register.

Offset Address	Register Name	Total Reset Value
0x44070	ISP_DEMOSAIC_FCR_GRAY_RATIO	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												fcr_gray_ratio			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved
[4:0]	RW	fcr_gray_ratio	Demosaic FCR blending ratio. The value ranges from 0 to 16.

ISP_DEMOSAIC_FCR_SEL

ISP_DEMOSAIC_FCR_SEL is a demosaic FCR calculated maximum value select register.

Offset Address	Register Name	Total Reset Value
0x44074	ISP_DEMOSAIC_FCR_SEL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								fcr_cmax_sel				fcr_detg_sel			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:4]	RW	fcr_cmax_sel	FCR CMAX select. The value range is [0, 8].
[3:0]	RW	fcr_detg_sel	FCR DETG select. The value range is [0, 8].

ISP_DEMOSAIC_BLEND_RATIO

ISP_DEMOSAIC_BLEND_RATIO is a demosaic same-channel blending ratio configuration register.

Offset Address	Register Name	Total Reset Value
0x44078	ISP_DEMOSAIC_BLEND_RATIO	0x0C84_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7 6 5 4	3 2 1 0
Name	reserved	var_blend_th		reserved	dif_blend_ratio1		reserved	dif_blend_ratio0	
Reset	0 0 0 0	1 1 0 0	1 0 0 0	0 1 0 0	0 0 0 0	0 0 0	0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:20]	RW	var_blend_th	Same-channel blending threshold. The value range is [0, 256].
[19]	-	reserved	Reserved
[18:10]	RW	dif_blend_ratio1	Same-channel blending ratio 1. The value range is [0, 256].
[9]	-	reserved	Reserved
[8:0]	RW	dif_blend_ratio0	Same-channel blending ratio 0. The value range is [0, 256].

ISP_DEMOSAIC_BLEND_DIF_LIMIT

ISP_DEMOSAIC_BLEND_DIF_LIMIT is a demosaic same-channel blending limit configuration register.

Offset Address	Register Name	Total Reset Value
0x4407c	ISP_DEMOSAIC_BLEND_DIF_LIMIT	0x0064_2014

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		dif2max_res_th		dif_blend_limit1		dif_blend_limit0	
Reset	0 0 0 0	0 0 0 0	0 1 1 0	0 1 0 0	0 0 1 0	0 0 0 0	0 0 0 1	0 1 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	dif2max_res_th	DIF MAX threshold
[15:8]	RW	dif_blend_limit1	Same-channel blending limit 1. The value range is [0, 255].
[7:0]	RW	dif_blend_limit0	Same-channel blending limit 0. The value range is [0, 255].

ISP_DEMOSAIC_HF_INTP_TH

ISP_DEMOSAIC_HF_INTP_TH is an HF filtering threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x44110	ISP_DEMOSAIC_HF_INTP_TH	0x0010_0030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hf_intp_th_high								reserved				hf_intp_th_low											
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	hf_intp_th_high	High threshold of high-frequency interpolation judgment
[15:10]	-	reserved	Reserved
[9:0]	RW	hf_intp_th_low	Low threshold of high-frequency interpolation judgment

ISP_DEMOSAIC_HF_INTP_BLD

ISP_DEMOSAIC_HF_INTP_BLD is an HF filtering threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x44114	ISP_DEMOSAIC_HF_INTP_BLD	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hf_intp_bld_high								reserved				hf_intp_bld_low											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	hf_intp_bld_high	Low threshold of the high-frequency interpolation ratio. The value range is [0, 256].
[15:9]	-	reserved	Reserved
[8:0]	RW	hf_intp_bld_low	High threshold of the high-frequency interpolation ratio. The value range is [0, 256].

ISP_DEMOSAIC_HF_INTP_TH1

ISP_DEMOSAIC_HF_INTP_TH1 is an HF filtering threshold configuration register 1.

Offset Address	Register Name	Total Reset Value
0x44118	ISP_DEMOSAIC_HF_INTP_TH1	0x0136_012C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								hf_intp_th_high1								reserved				hf_intp_th_low1											
Reset	0	0	0	0	0	0	0	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	hf_intp_th_high1	Low threshold 1 of high-frequency interpolation judgment
[15:10]	-	reserved	Reserved
[9:0]	RW	hf_intp_th_low1	High threshold 1 of high-frequency interpolation judgment

ISP_DEMOSAIC_HF_INTP_RATIO0

ISP_DEMOSAIC_HF_INTP_RATIO0 is an HF filtering ratio 1 register.

Offset Address	Register Name	Total Reset Value
0x4411c	ISP_DEMOSAIC_HF_INTP_RATIO0	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																interp_ratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved
[16:0]	RW	interp_ratio	HF filtering ratio 1 (S9.8)

ISP_DEMOSAIC_HF_INTP_RATIO1

ISP_DEMOSAIC_HF_INTP_RATIO1 is an HF filtering ratio 2 register.

Offset Address	Register Name	Total Reset Value
0x44120	ISP_DEMOSAIC_HF_INTP_RATIO1	0x0001_FFF3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																interp_ratio															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved

[16:0]	RW	interp_ratio	HF filtering ratio 2 (S9.8)

ISP_DEMOSAIC_SIZE

ISP_DEMOSAIC_SIZE is a demosaic picture size register.

Offset Address	Register Name	Total Reset Value
0x441F0	ISP_DEMOSAIC_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height The configured value is the actual value minus 1. For example, if the actual picture height is 1920, set this field to 1919.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width The configured value is the actual value minus 1. For example, if the actual picture width is 1080, set this field to 1079.

ISP_SHARPEN_CFG

ISP_SHARPEN_CFG is a sharpen control register.

Offset Address	Register Name	Total Reset Value
0x45200	ISP_SHARPEN_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RW	en	Sharpen enable 0: disabled 1: enabled

ISP_SHARPEN_AMT

ISP_SHARPEN_AMT is a sharpen strength register.

Offset Address	Register Name	Total Reset Value
0x45210	ISP_SHARPEN_AMT	0x01CC_012D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				edge_amt												reserved				sharp_amt											
Reset	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	1

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved
[27:16]	RW	edge_amt	Edge enhancement strength (U12.0)
[15:12]	RO	reserved	Reserved
[11:0]	RW	sharp_amt	Detail enhancement strength (U12.0)

ISP_SHARPEN_THD1

ISP_SHARPEN_THD1 is sharpen threshold register 1.

Offset Address	Register Name	Total Reset Value
0x45214	ISP_SHARPEN_THD1	0x0014_0096

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								edge_thd1								reserved								sharp_thd1							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	edge_thd1	Edge enhancement threshold (U10.0)
[15:10]	RO	reserved	Reserved
[9:0]	RW	sharp_thd1	Detail enhancement threshold (U10.0)

ISP_SHARPEN_THD2

ISP_SHARPEN_THD2 is a sharpen threshold 2 register.

Offset Address	Register Name	Total Reset Value
0x45218	ISP_SHARPEN_THD2	0x0000_0064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								edge_thd2								reserved								sharp_thd2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	edge_thd2	Edge enhancement threshold (U10.0)
[15:10]	-	reserved	Reserved
[9:0]	RW	sharp_thd2	Detail enhancement threshold (U10.0)

ISP_SHARPEN_SHOOTAMT

ISP_SHARPEN_SHOOTAMT is a sharpen shoot AMT control register.

Offset Address	Register Name	Total Reset Value
0x45220	ISP_SHARPEN_SHOOTAMT	0x00B4_00F5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								over_amt								reserved								under_amt							
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	over_amt	Overshoot control coefficient (U8.0)
[15:8]	RO	reserved	Reserved
[7:0]	RW	under_amt	Undershoot control coefficient (U8.0)

ISP_SHARPEN_JAGTHD

ISP_SHARPEN_JAGTHD is an aliasing control threshold parameter register.

Offset Address	Register Name	Total Reset Value
0x45224	ISP_SHARPEN_JAGTHD	0x01C2_0190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								varjagthd2								reserved								varjagthd1							
Reset	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	varjagthd2	Aliasing control threshold 2 (U10.0)
[15:10]	-	reserved	Reserved
[9:0]	RW	varjagthd1	Aliasing control threshold 1 (U10.0)

ISP_SHARPEN_EDGEJAG

ISP_SHARPEN_EDGEJAG is an aliasing high-frequency parameter register.

Offset Address	Register Name	Total Reset Value
0x45228	ISP_SHARPEN_EDGEJAG	0x1FF8_0032

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				edgejagamt											
Reset	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	edgejagamt	Aliasing high-frequency gain (U12.0)

ISP_SHARPEN_OSHTJAG

ISP_SHARPEN_OSHTJAG is an aliasing overshoot parameter register.

Offset Address	Register Name	Total Reset Value
0x4522C	ISP_SHARPEN_OSHTJAG	0x0000_00B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								oshtjagamt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	oshtjagamt	Aliasing overshoot gain (U8.8)

ISP_SHARPEN_USHTJAG

ISP_SHARPEN_USHTJAG is an aliasing undershoot parameter register.

Offset Address	Register Name	Total Reset Value
0x45230	ISP_SHARPEN_USHTJAG	0x0000_00F5

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								ushtjagamt							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	ushtjagamt	Aliasing undershoot gain (U8.8)

ISP_SHARPEN_MID0

ISP_SHARPEN_MID0 is a sharpen IF filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x45234	ISP_SHARPEN_MID0	0x00F0_F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mid_tmp02								mid_tmp01								mid_tmp00							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	mid_tmp02	IF filtering coefficient 02 (S8.0)

[15:8]	RW	mid_tmp01	IF filtering coefficient 01 (S8.0)
[7:0]	RW	mid_tmp00	IF filtering coefficient 00 (S8.0)

ISP_SHARPEN_MID1

ISP_SHARPEN_MID1 is a sharpen IF filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x45238	ISP_SHARPEN_MID1	0x001C_1CF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mid_tmp12								mid_tmp11								mid_tmp10							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	mid_tmp12	IF filtering coefficient 12 (S8.0)
[15:8]	RW	mid_tmp11	IF filtering coefficient 11 (S8.0)
[7:0]	RW	mid_tmp10	IF filtering coefficient 10 (S8.0)

ISP_SHARPEN_MID2

ISP_SHARPEN_MID2 is a sharpen IF filtering coefficient register.

Offset Address	Register Name	Total Reset Value
0x4523C	ISP_SHARPEN_MID2	0x0020_1CF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								mid_tmp22								mid_tmp21								mid_tmp20							
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:16]	RW	mid_tmp22	IF filtering coefficient 22 (S8.0)
[15:8]	RW	mid_tmp21	IF filtering coefficient 21 (S8.0)
[7:0]	RW	mid_tmp20	IF filtering coefficient 20 (S8.0)

ISP_SHARPEN_CTRL

ISP_SHARPEN_CTRL is a sharpen control register.

Offset Address	Register Name	Total Reset Value
0x45244	ISP_SHARPEN_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pixsel				lowbandesm_en	rgbshp_en	shadsup_en	jagctrl	lumactrlnoise	shtvarctrl	lumactrl	skinctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12:8]	RW	pixsel	Overshoot reference value. The value range is [0, 31].
[7]	RW	lowbandesm_en	Low-pass filter select enable 0: disabled 1: enabled
[6]	RW	rgbshp_en	RGB sharpening enable 0: disabled 1: enabled
[5]	RW	shadsup_en	Shadow region noise suppression enable 0: disabled 1: enabled
[4]	RW	jagctrl	Aliasing control enable 0: disabled 1: enabled
[3]	RW	lumactrlnoise	Noise threshold control based on the luminance 0: disabled 1: enabled
[2]	RW	shtvarctrl	Variance control 0: disabled 1: enabled
[1]	RW	lumactrl	Sharpening strength control based on the luminance 0: disabled 1: enabled

[0]	RW	skinctrl	Complexion detection and complexion sharpening decreasing enable 0: disabled 1: enabled

ISP_SHARPEN_SHIFT

ISP_SHARPEN_SHIFT is a shift parameter register.

Offset Address	Register Name	Total Reset Value
0x45248	ISP_SHARPEN_SHIFT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				maxshift		minshift	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:8]	RW	maxshift	Maximum offset (S8.0). The value range is [–128, 127].
[7:0]	RW	minshift	Minimum offset (S8.0). The value range is [–128, 127].

ISP_SHARPEN_ST

ISP_SHARPEN_ST is a sharpen strength control parameter register.

Offset Address	Register Name	Total Reset Value
0x4524C	ISP_SHARPEN_ST	0x0005_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					luma_nost	reserved	luma_limit
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:8]	RW	luma_nost	Noise threshold strength control based on the luminance
[7:5]	-	reserved	Reserved
[4:0]	RW	luma_limit	IF noise coring strength control based on the luminance

ISP_SHARPEN_OSHTVARTH

ISP_SHARPEN_OSHTVARTH is a variance threshold parameter 0 register.

Offset Address	Register Name	Total Reset Value
0x45250	ISP_SHARPEN_OSHTVARTH	0x012C_007D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								overvarth1								reserved								overvarth0							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	overvarth1	Overshoot variance threshold 1
[15:10]	-	reserved	Reserved
[9:0]	RW	overvarth0	Overshoot variance threshold 0

ISP_SHARPEN_OSHTVAR

ISP_SHARPEN_OSHTVAR is an overshoot variance parameter 0 register.

Offset Address	Register Name	Total Reset Value
0x45254	ISP_SHARPEN_OSHTVAR	0x0FFA_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				reserved												reserved								overvaramt							
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RO	reserved	Reserved
[15:8]	-	reserved	Reserved
[7:0]	RW	overvaramt	Overshoot variance gain

ISP_SHARPEN_USHTVARTH

ISP_SHARPEN_USHTVARTH is a variance threshold parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x45258	ISP_SHARPEN_USHTVARTH	0x012C_007D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								undervarth1								reserved								undervarth0							
Reset	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	undervarth1	Undershoot variance threshold 1
[15:10]	-	reserved	Reserved
[9:0]	RW	undervarth0	Undershoot variance threshold 0

ISP_SHARPEN_USHTVAR

ISP_SHARPEN_USHTVAR is an undershoot variance parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x4525C	ISP_SHARPEN_USHTVAR	0x0FFA_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				reserved												reserved								undervaramt							
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RO	reserved	Reserved
[15:8]	-	reserved	Reserved
[7:0]	RW	undervaramt	Undershoot variance gain

ISP_SHARPEN_LUMAWGT0

ISP_SHARPEN_LUMAWGT0 is a luminance weight parameter 0 register.

Offset Address	Register Name	Total Reset Value
0x45260	ISP_SHARPEN_LUMAWGT0	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt3		lumawgt2		lumawgt1		lumawgt0	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt3	Luminance weight 3
[23:16]	RW	lumawgt2	Luminance weight 2
[15:8]	RW	lumawgt1	Luminance weight 1
[7:0]	RW	lumawgt0	Luminance weight 0

ISP_SHARPEN_LUMAWGT1

ISP_SHARPEN_LUMAWGT1 is a luminance weight parameter 1 register.

Offset Address	Register Name	Total Reset Value
0x45264	ISP_SHARPEN_LUMAWGT1	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt7		lumawgt6		lumawgt5		lumawgt4	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt7	Luminance weight 7
[23:16]	RW	lumawgt6	Luminance weight 6
[15:8]	RW	lumawgt5	Luminance weight 5
[7:0]	RW	lumawgt4	Luminance weight 4

ISP_SHARPEN_LUMAWGT2

ISP_SHARPEN_LUMAWGT2 is a luminance weight parameter 2 register.

Offset Address	Register Name	Total Reset Value
0x45268	ISP_SHARPEN_LUMAWGT2	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt11		lumawgt10		lumawgt9		lumawgt8	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt11	Luminance weight 11
[23:16]	RW	lumawgt10	Luminance weight 10
[15:8]	RW	lumawgt9	Luminance weight 9
[7:0]	RW	lumawgt8	Luminance weight 8

ISP_SHARPEN_LUMAWGT3

ISP_SHARPEN_LUMAWGT3 is a luminance weight parameter 3 register.

Offset Address	Register Name	Total Reset Value
0x4526C	ISP_SHARPEN_LUMAWGT3	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt15		lumawgt14		lumawgt13		lumawgt12	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt15	Luminance weight 15
[23:16]	RW	lumawgt14	Luminance weight 14
[15:8]	RW	lumawgt13	Luminance weight 13
[7:0]	RW	lumawgt12	Luminance weight 12

ISP_SHARPEN_LUMAWGT4

ISP_SHARPEN_LUMAWGT4 is a luminance weight parameter 4 register.

Offset Address	Register Name	Total Reset Value
0x45270	ISP_SHARPEN_LUMAWGT4	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt19		lumawgt18		lumawgt17		lumawgt16	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt19	Luminance weight 19
[23:16]	RW	lumawgt18	Luminance weight 18
[15:8]	RW	lumawgt17	Luminance weight 17
[7:0]	RW	lumawgt16	Luminance weight 16

ISP_SHARPEN_LUMAWGT5

ISP_SHARPEN_LUMAWGT5 is a luminance weight parameter 5 register.

Offset Address	Register Name	Total Reset Value
0x45274	ISP_SHARPEN_LUMAWGT5	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt23		lumawgt22		lumawgt21		lumawgt20	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt23	Luminance weight 23
[23:16]	RW	lumawgt22	Luminance weight 22
[15:8]	RW	lumawgt21	Luminance weight 21
[7:0]	RW	lumawgt20	Luminance weight 20

ISP_SHARPEN_LUMAWGT6

ISP_SHARPEN_LUMAWGT6 is a luminance weight parameter 6 register.

Offset Address	Register Name	Total Reset Value
0x45278	ISP_SHARPEN_LUMAWGT6	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt27		lumawgt26		lumawgt25		lumawgt24	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt27	Luminance weight 27
[23:16]	RW	lumawgt26	Luminance weight 26
[15:8]	RW	lumawgt25	Luminance weight 25
[7:0]	RW	lumawgt24	Luminance weight 24

ISP_SHARPEN_LUMAWGT7

ISP_SHARPEN_LUMAWGT7 is a luminance weight parameter 7 register.

Offset Address	Register Name	Total Reset Value
0x4527C	ISP_SHARPEN_LUMAWGT7	0xFFFF_FFFF

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	lumawgt31		lumawgt30		lumawgt29		lumawgt28	
Reset	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

Bits	Access	Name	Description
[31:24]	RW	lumawgt31	Luminance weight 31
[23:16]	RW	lumawgt30	Luminance weight 30
[15:8]	RW	lumawgt29	Luminance weight 29
[7:0]	RW	lumawgt28	Luminance weight 28

ISP_SHARPEN_SIZE

ISP_SHARPEN_SIZE is a sharpen picture size register.

Offset Address	Register Name	Total Reset Value
0x452F0	ISP_SHARPEN_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height. The configured value is the actual value minus 1. For example, for the 1080P picture, set the height to 1079.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width. The configured value is the actual value minus 1. For example, for the 1080P picture, set the width to 1919.

ISP_SHARPEN_SKIN_VARTH

ISP_SHARPEN_SKIN_VARTH is a complexion variance threshold register.

Offset Address	Register Name	Total Reset Value
0x45314	ISP_SHARPEN_SKIN_VARTH	0x0096_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skin_var_th2								reserved								skin_var_th1							
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skin_var_th2	Complexion variance threshold 2
[15:10]	-	reserved	Reserved
[9:0]	RW	skin_var_th1	Complexion variance threshold 1

ISP_SHARPEN_SKIN_VARWGT

ISP_SHARPEN_SKIN_VARWGT is a complexion weight register.

Offset Address	Register Name	Total Reset Value
0x45318	ISP_SHARPEN_SKIN_VARWGT	0x0FFB_2050

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				skinvarwgtmulcoef												skin_var_wgt2								skin_var_wgt1							
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	skinvarwgtmulcoef	Complexion weight coefficient. The format is S13.0 and the value range is [–4096, 4095].
[15:8]	RW	skin_var_wgt2	Complexion weight 2
[7:0]	RW	skin_var_wgt1	Complexion weight 1

ISP_SHARPEN_SKIN_U

ISP_SHARPEN_SKIN_U is a complexion U threshold register.

Offset Address	Register Name	Total Reset Value
0x4531C	ISP_SHARPEN_SKIN_U	0x007F_0064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skin_u_max								reserved								skin_u_min							
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	skin_u_max	Maximum threshold of complexion U
[15:8]	-	reserved	Reserved
[7:0]	RW	skin_u_min	Minimum threshold of complexion U

ISP_SHARPEN_SKIN_V

ISP_SHARPEN_SKIN_V is a complexion V threshold register.

Offset Address	Register Name	Total Reset Value
0x45320	ISP_SHARPEN_SKIN_V	0x0096_0087

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skin_v_max								reserved								skin_v_min							
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	skin_v_max	Maximum threshold of complexion V
[15:8]	-	reserved	Reserved
[7:0]	RW	skin_v_min	Minimum threshold of complexion V

ISP_SHARPEN_EDGSM

ISP_SHARPEN_EDGSM is an edge filter parameter register.

Offset Address	Register Name	Total Reset Value
0x45328	ISP_SHARPEN_EDGSM	0x0000_1022

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							edgsm_en	reserved								edgsm_str				diff_thd								diff_mul			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24]	RW	edgsm_en	Edge filtering enable 0: disabled 1: enabled
[23:17]	-	reserved	Reserved
[16:12]	RW	edgsm_str	Edge filtering strength
[11:4]	RW	diff_thd	Edge noise threshold
[3:0]	RW	diff_mul	Edge strength multiple

ISP_SHARPEN_OSUP_VAR

ISP_SHARPEN_OSUP_VAR is an overshoot control variance threshold register.

Offset Address	Register Name	Total Reset Value
0x45330	ISP_SHARPEN_OSUP_VAR	0x0005_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oshtvarmax								reserved								oshtvarmin							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	oshtvarmax	Maximum overshoot control variance
[15:8]	-	reserved	Reserved
[7:0]	RW	oshtvarmin	Minimum overshoot control variance

ISP_SHARPEN_OSUP_VARCOEF

ISP_SHARPEN_OSUP_VARCOEF is an overshoot control variance coefficient register.

Offset Address	Register Name	Total Reset Value
0x45334	ISP_SHARPEN_OSUP_VARCOEF	0x0000_0330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oshtwgtmin								reserved				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	oshtwgtmin	Minimum weight of the overshoot control variance
[15:12]	-	reserved	Reserved
[11:0]	RO	reserved	Reserved

ISP_SHARPEN_USUP_VAR

ISP_SHARPEN_USUP_VAR is an undershoot control variance threshold register.

Offset Address	Register Name	Total Reset Value
0x45338	ISP_SHARPEN_USUP_VAR	0x0005_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ushtvarmax								reserved								ushtvarmin							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	ushtvarmax	Maximum undershoot control variance
[15:8]	-	reserved	Reserved
[7:0]	RW	ushtvarmin	Minimum undershoot control variance

ISP_SHARPEN_USUP_VARCOEF

ISP_SHARPEN_USUP_VARCOEF is an undershoot control variance coefficient register.

Offset Address	Register Name	Total Reset Value
0x4533C	ISP_SHARPEN_USUP_VARCOEF	0x0000_0330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ushtwgtmin								reserved				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	ushtwgtmin	Minimum weight of the undershoot control variance
[15:12]	-	reserved	Reserved
[11:0]	RO	reserved	Reserved

ISP_SHARPEN_OSUP_DIFF

ISP_SHARPEN_OSUP_DIFF is an overshoot control difference threshold register.

Offset Address	Register Name	Total Reset Value
0x45340	ISP_SHARPEN_OSUP_DIFF	0x0019_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oshtdiffmax								reserved								oshtdiffmin							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	oshtdiffmax	Maximum overshoot control difference
[15:8]	-	reserved	Reserved
[7:0]	RW	oshtdiffmin	Minimum overshoot control difference

ISP_SHARPEN_OSUP_DIFFCOEF

ISP_SHARPEN_OSUP_DIFFCOEF is an overshoot control difference coefficient register.

Offset Address	Register Name	Total Reset Value
0x45344	ISP_SHARPEN_OSUP_DIFFCOEF	0x003C_0EC8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								oshtdiffwgtmin								reserved				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	oshtdiffwgtmin	Minimum weight of the overshoot control difference
[15:13]	-	reserved	Reserved
[12:0]	RO	reserved	Reserved

ISP_SHARPEN_USUP_DIFF

ISP_SHARPEN_USUP_DIFF is an undershoot control difference threshold register.

Offset Address	Register Name	Total Reset Value
0x45348	ISP_SHARPEN_USUP_DIFF	0x0019_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ushtdiffmax								reserved								ushtdiffmin							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	ushtdiffmax	Maximum undershoot control difference
[15:8]	-	reserved	Reserved
[7:0]	RW	ushtdiffmin	Minimum undershoot control difference

ISP_SHARPEN_USUP_DIFFCOEF

ISP_SHARPEN_USUP_DIFFCOEF is an undershoot control difference coefficient register.

Offset Address	Register Name	Total Reset Value
0x4534C	ISP_SHARPEN_USUP_DIFFCOEF	0x003C_0EC8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ushtdiffwgtmin								reserved	reserved														
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	0	0	1	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	ushtdiffwgtmin	Minimum weight of the undershoot control difference
[15:13]	-	reserved	Reserved
[12:0]	RO	reserved	Reserved

ISP_SHARPEN_SUP_NOS

ISP_SHARPEN_SUP_NOS is a shoot control noise threshold register.

Offset Address	Register Name	Total Reset Value
0x45350	ISP_SHARPEN_SUP_NOS	0x0002_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								maxnosthd								reserved								minnosthd							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	maxnosthd	Maximum threshold of shoot noises
[15:8]	-	reserved	Reserved
[7:0]	RW	minnosthd	Minimum threshold of shoot noises

ISP_SHARPEN_SUP_BLDR

ISP_SHARPEN_SUP_BLDR is a shoot control blending parameter register.

Offset Address	Register Name	Total Reset Value
0x45354	ISP_SHARPEN_SUP_BLDR	0x0003_0009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														shtmax_en	shtsup_en	reserved												shtsupbldr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved
[17]	RW	shtmax_en	Maximum shoot control enable
[16]	RW	shtsup_en	Shoot control enable
[15:4]	-	reserved	Reserved
[3:0]	RW	shtsupbldr	Shoot control blending ratio

ISP_SHARPEN_UDHFGAIN

ISP_SHARPEN_UDHFGAIN is a directionless high-frequency detail control register.

Offset Address	Register Name	Total Reset Value
0x45358	ISP_SHARPEN_UDHFGAIN	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						udhfgain									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9:0]	RW	udhfgain	Directionless high-frequency detail control

ISP_SHARPEN_SHTMAX

ISP_SHARPEN_SHTMAX is a shoot maximum limit parameter register.

Offset Address	Register Name	Total Reset Value
0x4535C	ISP_SHARPEN_SHTMAX	0x0064_1212

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ushtmaxchg								oshtmaxchg								ushtmaxvargain								oshtmaxvargain							
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[31:24]	RW	ushtmaxchg	Maximum undershoot limit
[23:16]	RW	oshtmaxchg	Maximum overshoot limit
[15:8]	RW	ushtmaxvargain	Maximum limit gain of the undershoot variance
[7:0]	RW	oshtmaxvargain	Maximum limit gain of the overshoot variance

ISP_SHARPEN_SHADVAR

ISP_SHARPEN_SHADVAR is a shadow region noise variance threshold register.

Offset Address	Register Name	Total Reset Value
0x45360	ISP_SHARPEN_SHADVAR	0x003C_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								shadvar2								reserved				shadvar1											
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved

[25:16]	RW	shadvar2	Shadow region noise variance threshold 2
[15:10]	-	reserved	Reserved
[9:0]	RW	shadvar1	Shadow region noise variance threshold 1

ISP_SHARPEN_GRADTHD

ISP_SHARPEN_GRADTHD is a shadow region noise gradient threshold register.

Offset Address	Register Name	Total Reset Value
0x45364	ISP_SHARPEN_GRADTHD	0x0010_000A

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			gradthd2	reserved			gradthd1
Reset	0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 1 0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved
[20:16]	RW	gradthd2	Shadow region noise gradient threshold 2
[15:5]	-	reserved	Reserved
[4:0]	RW	gradthd1	Shadow region noise gradient threshold 1

ISP_SHARPEN_WGTCOEF

ISP_SHARPEN_WGTCOEF is a shadow region noise weight coefficient register.

Offset Address	Register Name	Total Reset Value
0x45368	ISP_SHARPEN_WGTCOEF	0x0029_1F00

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		reserved		reserved	wgtthd2	reserved	wgtthd1
Reset	0 0 0 0	0 0 0 0	0 0 1 0	1 0 0 1	0 0 0 1	1 1 1 1	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RO	reserved	Reserved
[15:13]	-	reserved	Reserved
[12:8]	RW	wgtthd2	Shadow region noise gradient weight threshold 2

[7:5]	-	reserved	Reserved
[4:0]	RW	wgtthd1	Shadow region noise gradient weight threshold 1

ISP_SHARPEN_RC

ISP_SHARPEN_RC is an red sharpening threshold coefficient register.

Offset Address	Register Name	Total Reset Value
0x4536C	ISP_SHARPEN_RC	0x6000_9090

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rcrmin								rcbmin								rcrmax								rcbmax							
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	rcrmin	Minimum threshold of red V. The value range is [0, 144].
[23:16]	RW	rcbmin	Minimum threshold of red U. The value range is [0, 144].
[15:8]	RW	rcrmax	Maximum threshold of red V. The value range is [0, 144].
[7:0]	RW	rcbmax	Maximum threshold of red U. The value range is [0, 144].

ISP_SHARPEN_BC

ISP_SHARPEN_BC is a blue sharpening threshold coefficient register.

Offset Address	Register Name	Total Reset Value
0x45370	ISP_SHARPEN_BC	0x2C52_4662

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bcrmin								bcbmin								bcrmax								bcbmax							
Reset	0	0	1	0	1	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0	0	1	1	0	0	1	1	0	0	0	1	0

Bits	Access	Name	Description
[31:24]	RW	bcrmin	Minimum threshold of blue V. The value range is [0, 144].
[23:16]	RW	bcbmin	Minimum threshold of blue U. The value range is [0, 144].
[15:8]	RW	bcrmax	Maximum threshold of blue V. The value range is [0, 144].
[7:0]	RW	bcbmax	Maximum threshold of blue U. The value range is [0, 144].

ISP_SHARPEN_GC

ISP_SHARPEN_GC is a green sharpening threshold coefficient register.

Offset Address	Register Name	Total Reset Value
0x45374	ISP_SHARPEN_GC	0x3222_4A44

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gcrmin								gcbmin								gcrmax								gcbmax							
Reset	0	0	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0	1	0	1	0	0	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:24]	RW	gcrmin	Minimum threshold of green V. The value range is [0, 144].
[23:16]	RW	gcbmin	Minimum threshold of green U. The value range is [0, 144].
[15:8]	RW	gcrmax	Maximum threshold of green V. The value range is [0, 144].
[7:0]	RW	gcbmax	Maximum threshold of green U. The value range is [0, 144].

ISP_SHARPEN_RGBWGT

ISP_SHARPEN_RGBWGT is an RGB color sharpening gain coefficient register.

Offset Address	Register Name	Total Reset Value
0x45378	ISP_SHARPEN_RGBWGT	0x001F_1F04

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												rwgt				reserved				bwgt				reserved				gwgt			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved
[20:16]	RW	rwgt	Maximum sharpening value of red. The value range is [0, 31].
[15:13]	-	reserved	Reserved
[12:8]	RW	bwgt	Maximum sharpening value of blue. The value range is [0, 31].
[7:4]	-	reserved	Reserved
[3:0]	RW	gwgt	Maximum sharpening value of green. The value range is [0, 15].

ISP_SHARPEN_RBCOEF

ISP_SHARPEN_RBCOEF is an RGB sharpening gain difference and threshold register.

Offset Address	Register Name	Total Reset Value
0x4537C	ISP_SHARPEN_RBCOEF	0x7657_1F1F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rcrthd								bcbthd								reserved				rshpgainsft				reserved				bshpgainsft			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	rcrthd	Threshold of red V. The value range is [0, 144].
[23:16]	RW	bcbthd	Threshold of blue U. The value range is [0, 144].
[15:14]	-	reserved	Reserved
[13:8]	RW	rshpgainsft	Red high- and intermediate-frequency sharpening gain difference. The format is S6.0 and the value range is [–32, 31].
[7:6]	-	reserved	Reserved
[5:0]	RW	bshpgainsft	Blue high- and intermediate-frequency sharpening gain difference. The format is S6.0 and the value range is [–32, 31].

ISP_NDDM_CFG

ISP_NDDM_CFG is an NDDM control register.

Offset Address	Register Name	Total Reset Value
0x45600	ISP_NDDM_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															cac_blend_en	reserved															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	-	reserved	Reserved

[16]	RW	cac_blend_en	CAC blending enable 0: disabled 1: enabled
[15:1]	-	reserved	Reserved
[0]	RW	en	NDDM enable 0: disabled 1: enabled

ISP_NDDM_GF_TH

ISP_NDDM_GF_TH is an NDDM filtering strength range control register.

Offset Address	Register Name	Total Reset Value
0x45604	ISP_NDDM_GF_TH	0x0100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								gf_th_high								reserved								gf_th_low							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24:16]	RW	gf_th_high	High threshold
[15:9]	-	reserved	Reserved
[8:0]	RW	gf_th_low	Low threshold

ISP_NDDM_GF_BLDR

ISP_NDDM_GF_BLDR is a filtering window 5x5 and 9x9 blending ratio control register.

Offset Address	Register Name	Total Reset Value
0x45608	ISP_NDDM_GF_BLDR	0x0008_0303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												bldr_cbcr				reserved				bldr_var_str				reserved				bldr_gf_str			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved

[20:16]	RW	bldr_cbcr	Cb & Cr window ratio control
[15:13]	-	reserved	Reserved
[12:8]	RW	bldr_var_str	9x9 and 5x5 window variance ratio control
[7:5]	-	reserved	Reserved
[4:0]	RW	bldr_gf_str	R & G & B window ratio control

ISP_NDDM_GF_CHRM

ISP_NDDM_GF_CHRM is a saturation control filtering strength register.

Offset Address	Register Name	Total Reset Value
0x4560C	ISP_NDDM_GF_CHRM	0x0042_F882

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								chrm_fix				reserved	chrm_high									reserved	chrm_low								
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:20]	RW	chrm_fix	Maximum enhancement gain
[19]	-	reserved	Reserved
[18:10]	RW	chrm_high	High threshold of saturation
[9]	-	reserved	Reserved
[8:0]	RW	chrm_low	Low threshold of saturation

ISP_NDDM_USM_CFG

ISP_NDDM_USM_CFG is a USM enhancement control register.

Offset Address	Register Name	Total Reset Value
0x45610	ISP_NDDM_USM_CFG	0x0006_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												multi_mf				reserved				clip_usm											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved
[20:16]	RW	multi_mf	USM gain (U3.2)
[15:12]	-	reserved	Reserved
[11:0]	RW	clip_usm	USM clipping threshold (U12.0)

ISP_NDDM_USM_SATU

ISP_NDDM_USM_SATU is a saturation attenuation USM strength register.

Offset Address	Register Name	Total Reset Value
0x45614	ISP_NDDM_USM_SATU	0x0A43_2082

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				satu_th_fix								reserved	satu_th_high									reserved	satu_th_low								
Reset	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:20]	RW	satu_th_fix	Maximum gain
[19]	-	reserved	Reserved
[18:10]	RW	satu_th_high	High threshold of saturation
[9]	-	reserved	Reserved
[8:0]	RW	satu_th_low	Low threshold of saturation

ISP_NDDM_USM_GRAY

ISP_NDDM_USM_GRAY is a gray attenuation USM strength register.

Offset Address	Register Name	Total Reset Value
0x45618	ISP_NDDM_USM_GRAY	0x0200_5000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				gray_th_fix								reserved				gray_th_high						reserved		gray_th_low							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:20]	RW	gray_th_fix	Minimum USM gain
[19]	-	reserved	Reserved
[18:10]	RW	gray_th_high	High threshold of gray
[9]	-	reserved	Reserved
[8:0]	RW	gray_th_low	Low threshold of gray

ISP_NDDM_APT_INTP_BLD

ISP_NDDM_APT_INTP_BLD is an adaptive filtering and interpolation Gb and Gr blending register.

Offset Address	Register Name	Total Reset Value
0x4561C	ISP_NDDM_APT_INTP_BLD	0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												bldr_gr_gb			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved
[3:0]	RW	bldr_gr_gb	Gb and Gr blending ratio

ISP_NDDM_DITHER_CFG

ISP_NDDM_DITHER_CFG is a dither control register.

Offset Address	Register Name	Total Reset Value
0x45624	ISP_NDDM_DITHER_CFG	0x0002_200F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dith_max								dith_ratio								dith_mask							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	dith_max	Maximum dither value
[15:8]	RW	dith_ratio	Dither overlapping ratio
[7:0]	RW	dith_mask	Dither mask

ISP_NDDM_FCR_LIMIT

ISP_NDDM_FCR_LIMIT is an FCR de-moire protection range register.

Offset Address	Register Name	Total Reset Value
0x45628	ISP_NDDM_FCR_LIMIT	0x0100_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fcr_limit_high												reserved				fcr_limit_low											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	fcr_limit_high	High threshold
[15:12]	-	reserved	Reserved
[11:0]	RW	fcr_limit_low	Low threshold

ISP_NDDM_FCR_GAIN

ISP_NDDM_FCR_GAIN is an FCR function control register.

Offset Address	Register Name	Total Reset Value
0x4562C	ISP_NDDM_FCR_GAIN	0x0096_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fcr_det_low												reserved												fcr_gf_gain			
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	fcr_det_low	FCR effective threshold
[15:5]	-	reserved	Reserved
[4:0]	RW	fcr_gf_gain	FCR strength control of the filter

ISP_NDDM_FCR_SCALE

ISP_NDDM_FCR_SCALE is an FCR de-moire scale register.

Offset Address	Register Name	Total Reset Value
0x45630	ISP_NDDM_FCR_SCALE	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												scale			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:4]	-	reserved	Reserved
[3:0]	RW	scale	Scale

ISP_NDDM_DM_BLDRATE

ISP_NDDM_DM_BLDRATE is a CAC VHDM ratio register.

Offset Address	Register Name	Total Reset Value
0x45634	ISP_NDDM_DM_BLDRATE	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												cac_blend_rate			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved

[8:0]	RW	cac_blend_rate	VHDM ratio

ISP_NDDM_GF_LUT_UPDATE

ISP_NDDM_GF_LUT_UPDATE is an NDDM filter fuzzy table update configuration register.

Offset Address	Register Name	Total Reset Value
0x45638	ISP_NDDM_GF_LUT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update	Update of the filter fuzzy table

ISP_NDDM_USM_LUT_UPDATE

ISP_NDDM_USM_LUT_UPDATE is an NDDM strength table update configuration register.

Offset Address	Register Name	Total Reset Value
0x45640	ISP_NDDM_USM_LUT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update	Update of the USM strength table

ISP_NDDM_USM_GRAY_TH_FIX2

ISP_NDDM_USM_GRAY_TH_FIX2 is a gray attenuation USM gain 2 register.

Offset Address	Register Name	Total Reset Value
0x45644	ISP_NDDM_USM_GRAY_TH_FIX2	0x0000_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gray_th_fix2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8:0]	RW	gray_th_fix2	Maximum USM gain. The value range is [0, 256].

ISP_NDDM_APT_INTP_CLIP2

ISP_NDDM_APT_INTP_CLIP2 is adaptive filtering the interpolation threshold register 2.

Offset Address	Register Name	Total Reset Value
0x45648	ISP_NDDM_APT_INTP_CLIP2	0x0002_0028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								clip_delta_gain								reserved								clip_adjust_max							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	clip_delta_gain	Adaptive filtering and interpolation gain
[15:8]	-	reserved	Reserved
[7:0]	RW	clip_adjust_max	Maximum value of adaptive filtering and interpolation

ISP_NDDM_APT_AVG_CFG_0

ISP_NDDM_APT_AVG_CFG_0 is adaptive filtering configuration register 0.

Offset Address	Register Name	Total Reset Value
0x4564C	ISP_NDDM_APT_AVG_CFG_0	0x1000_A00A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				filter_str_intp				clip_delta_intp_high												clip_delta_intp_low											
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:24]	RW	filter_str_intp	Strength of non-linear interpolation
[23:12]	RW	clip_delta_intp_high	High threshold of non-linear interpolation
[11:0]	RW	clip_delta_intp_low	Low threshold of non-linear interpolation

ISP_NDDM_APT_AVG_CFG_1

ISP_NDDM_APT_AVG_CFG_1 is adaptive filtering configuration register 0.

Offset Address	Register Name	Total Reset Value
0x45650	ISP_NDDM_APT_AVG_CFG_1	0x1000_A00A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				filter_str_filt				clip_delta_filt_high												clip_delta_filt_low											
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:24]	RW	filter_str_filt	Strength of non-linear filtering
[23:12]	RW	clip_delta_filt_high	High threshold of non-linear filtering
[11:0]	RW	clip_delta_filt_low	Low threshold of non-linear filtering

ISP_NDDM_VAR_OFFSET_CFG

ISP_NDDM_VAR_OFFSET_CFG is a variance offset control register.

Offset Address	Register Name	Total Reset Value
0x45654	ISP_NDDM_VAR_OFFSET_CFG	0x0001_2C20

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	var_offset_low																								var_offset_gain							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	var_offset_low	Variance threshold
[7:0]	RW	var_offset_gain	Variance offset gain

ISP_NDDM_SHT_CTRL

ISP_NDDM_SHT_CTRL is a black and white border suppression control register.

Offset Address	Register Name	Total Reset Value
0x45658	ISP_NDDM_SHT_CTRL	0x0200_0006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				sht_ctrl_th												reserved												sht_ctrl_gain			
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	sht_ctrl_th	Black and white border suppression control threshold
[15:4]	-	reserved	Reserved
[3:0]	RW	sht_ctrl_gain	Black and white border suppression control gain. The value range is [0, 8].

ISP_NDDM_SHT_CLIP_R

ISP_NDDM_SHT_CLIP_R is an R channel black and white border suppression threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x4565C	ISP_NDDM_SHT_CLIP_R	0x0100_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_r_ov_sht												reserved				clip_r_ud_sht											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	clip_r_ov_sht	Upper threshold for R channel black and white border suppression
[15:12]	-	reserved	Reserved
[11:0]	RW	clip_r_ud_sht	Lower threshold for R channel black and white border suppression

ISP_NDDM_SHT_CLIP_B

ISP_NDDM_SHT_CLIP_B is a B channel black and white border suppression threshold configuration register.

Offset Address	Register Name	Total Reset Value
0x45660	ISP_NDDM_SHT_CLIP_B	0x0100_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				clip_b_ov_sht												reserved				clip_b_ud_sht											
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	clip_b_ov_sht	Upper threshold for B channel black and white border suppression
[15:12]	-	reserved	Reserved
[11:0]	RW	clip_b_ud_sht	Lower threshold for B channel black and white border suppression

ISP_NDDM_MULTI_MF_RB

ISP_NDDM_MULTI_MF_RB is an R and B channel USM enhancement control register.

Offset Address	Register Name	Total Reset Value
0x45664	ISP_NDDM_MULTI_MF_RB	0x0000_0C0C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				multi_mf_b				reserved				multi_mf_r			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0

Bits	Access	Name	Description
[31:13]	-	reserved	Reserved
[12:8]	RW	multi_mf_b	Enhancement of channel B
[7:5]	-	reserved	Reserved
[4:0]	RW	multi_mf_r	Enhancement of channel R

ISP_NDDM_USM_SATU_R

ISP_NDDM_USM_SATU_R is an R channel saturation attenuation USM strength register.

Offset Address	Register Name	Total Reset Value
0x45668	ISP_NDDM_USM_SATU_R	0x05C3_2082

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				satu_r_th_fix								reserved	satu_r_th_high									reserved	satu_r_th_low								
Reset	0	0	0	0	0	1	0	1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:20]	RW	satu_r_th_fix	Maximum gain of the R component. The value range is [0, 256].
[19]	-	reserved	Reserved
[18:10]	RW	satu_r_th_high	High threshold of the R component saturation. The value range is [0, 256].
[9]	-	reserved	Reserved
[8:0]	RW	satu_r_th_low	Low threshold of the R component saturation. The value range is [0, 256].

ISP_NDDM_USM_SATU_B

ISP_NDDM_USM_SATU_B is a B channel saturation attenuation USM strength register.

Offset Address	Register Name	Total Reset Value
0x4566C	ISP_NDDM_USM_SATU_B	0x05C3_2082

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				satu_b_th_fix								reserved	satu_b_th_high									reserved	satu_b_th_low								
Reset	0	0	0	0	0	1	0	1	1	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:20]	RW	satu_b_th_fix	Maximum gain of the B component. The value range is [0, 256].
[19]	-	reserved	Reserved
[18:10]	RW	satu_b_th_high	High threshold of the B component saturation. The value range is [0, 256].
[9]	-	reserved	Reserved
[8:0]	RW	satu_b_th_low	Low threshold of the B component saturation. The value range is [0, 256].

ISP_NDDM_SATU_FIX_EHCY

ISP_NDDM_SATU_FIX_EHCY is a saturation control luminance gain register.

Offset Address	Register Name	Total Reset Value
0x45670	ISP_NDDM_SATU_FIX_EHCY	0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								satu_fix_ehcy							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9:0]	RW	satu_fix_ehcy	Luminance gain in regions with high saturation. The value range is [–256, 256].

ISP_NDDM_GF_LUT_WADDR

ISP_NDDM_GF_LUT_WADDR is an NDDM fuzzy table write address register.

Offset Address	Register Name	Total Reset Value
0x45680	ISP_NDDM_GF_LUT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											gf_lut_waddr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved
[4:0]	RW	gf_lut_waddr	Write address of the NDDM filter fuzzy table. The value range is [0, 16].

ISP_NDDM_GF_LUT_WDATA

ISP_NDDM_GF_LUT_WDATA is an NDDM fuzzy table write data register.

Offset Address	Register Name	Total Reset Value
0x45684	ISP_NDDM_GF_LUT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gf_lut_wdata											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	gf_lut_wdata	Write data of the NDDM filter fuzzy table

ISP_NDDM_GF_LUT_RADDR

ISP_NDDM_GF_LUT_RADDR is an NDDM fuzzy table read address register.

Offset Address	Register Name	Total Reset Value
0x45688	ISP_NDDM_GF_LUT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												gf_lut_raddr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved
[4:0]	RW	gf_lut_raddr	Read address of the NDDM filter fuzzy table. The value range is [0, 16].

ISP_NDDM_GF_LUT_RDATA

ISP_NDDM_GF_LUT_RDATA is an NDDM fuzzy table read data register.

Offset Address	Register Name	Total Reset Value
0x4568C	ISP_NDDM_GF_LUT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				gf_lut_rdata											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RO	gf_lut_rdata	Read data of the NDDM filter fuzzy table

ISP_NDDM_USM_LUT_WADDR

ISP_NDDM_USM_LUT_WADDR is an NDDM strength table write address register.

Offset Address	Register Name	Total Reset Value
0x45690	ISP_NDDM_USM_LUT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												usm_lut_waddr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved
[4:0]	RW	usm_lut_waddr	Write address of the NDDM USM strength table. The value range is [0, 16].

ISP_NDDM_USM_LUT_WDATA

ISP_NDDM_USM_LUT_WDATA is an NDDM strength table write data register.

Offset Address	Register Name	Total Reset Value
0x45694	ISP_NDDM_USM_LUT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								usm_lut_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	usm_lut_wdata	Write data of the NDDM USM strength table

ISP_NDDM_USM_LUT_RADDR

ISP_NDDM_USM_LUT_RADDR is an NDDM strength table read address register.

Offset Address	Register Name	Total Reset Value
0x45698	ISP_NDDM_USM_LUT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												usm_lut_raddr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	-	reserved	Reserved
[4:0]	RW	usm_lut_raddr	Read address of the NDDM USM strength table. The value range is [0, 16].

ISP_NDDM_USM_LUT_RDATA

ISP_NDDM_USM_LUT_RDATA is an NDDM strength table read data register.

Offset Address	Register Name	Total Reset Value
0x4569C	ISP_NDDM_USM_LUT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								usm_lut_rdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RO	usm_lut_rdata	Read data of the NDDM USM strength table

ISP_NDDM_SIZE

ISP_NDDM_SIZE is an NDDM picture size register.

Offset Address	Register Name	Total Reset Value
0x456F0	ISP_NDDM_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height The configured value is the actual value minus 1. For example, if the actual height is 1920, set this field to 1919.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width The configured value is the actual value minus 1. For example, if the actual width is 1080, set this field to 1079.

ISP_DEHAZE_CFG

ISP_DEHAZE_CFG is a dehaze enable register.

Offset Address	Register Name	Total Reset Value
0x46700	ISP_DEHAZE_CFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	en	Dehaze enable 0: disabled 1: enabled

ISP_DEHAZE_PRE_UPDATE

ISP_DEHAZE_PRE_UPDATE is a dehaze statistical result update register.

Offset Address	Register Name	Total Reset Value
0x46710	ISP_DEHAZE_PRE_UPDATE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								pre_update
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	pre_update	Dehaze statistical result update. This bit is automatically cleared for each frame.

ISP_DEHAZE_BLK_SIZE

ISP_DEHAZE_BLK_SIZE is a dehaze block size configuration register.

Offset Address	Register Name	Total Reset Value
0x46714	ISP_DEHAZE_BLK_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								block_sizeh								reserved								block_sizev							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	block_sizeh	Horizontal block size. The configured value is the actual value minus 1.
[15:9]	RO	reserved	Reserved
[8:0]	RW	block_sizev	Vertical block size. The configured value is the actual value minus 1.

ISP_DEHAZE_BLK_SUM

ISP_DEHAZE_BLK_SUM is a dehaze block number register.

Offset Address	Register Name	Total Reset Value
0x46718	ISP_DEHAZE_BLK_SUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								block_sum							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:0]	RW	block_sum	Number of dehaze blocks. block_sum = Number of horizontal zones x (Number of vertical zones – 1)

ISP_DEHAZE_DC_SIZE

ISP_DEHAZE_DC_SIZE is a dehaze bilinear interpolation point quantity configuration register.

Offset Address	Register Name	Total Reset Value
0x4671C	ISP_DEHAZE_DC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						dc_numh						dc_numv			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:5]	RW	dc_numh	Number of bilinear interpolation horizontal points. The configured value is the number of horizontal zones minus 1.
[4:0]	RW	dc_numv	Number of bilinear interpolation vertical points. The configured value is the number of vertical zones minus 1.

ISP_DEHAZE_X

ISP_DEHAZE_X is a configuration register for the horizontal phase difference between the pixels of the dehaze enlarged picture.

Offset Address	Register Name	Total Reset Value
0x46720	ISP_DEHAZE_X	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								phase_x																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	phase_x	Horizontal phase difference between the pixels of the enlarged picture (unsigned integer) phase_x = Size of the horizontal zone x (1<<22)

ISP_DEHAZE_Y

ISP_DEHAZE_Y is a configuration register for the vertical phase difference between the pixels of the dehaze enlarged picture.

Offset Address	Register Name	Total Reset Value
0x46724	ISP_DEHAZE_Y	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								phase_y																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	phase_y	Vertical phase difference between the pixels of the enlarged picture (unsigned integer) phase_y = Size of the vertical zone x (1<<22)

ISP_DEHAZE_STAT_MODE

ISP_DEHAZE_STAT_MODE is a dehaze statistics module control register.

Offset Address	Register Name	Total Reset Value
0x46728	ISP_DEHAZE_STAT_MODE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															max_mode
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	max_mode	Maximum value statistics control 0: Mean filtering is performed on RGB components, and then the RGB components corresponding to the maximum RGB sum of each window are counted. 1: The RGB components corresponding to the maximum RGB sum of each window are counted.

ISP_DEHAZE_NEG_MODE

ISP_DEHAZE_NEG_MODE is a dehaze inversion control register.

Offset Address	Register Name	Total Reset Value
0x4672C	ISP_DEHAZE_NEG_MODE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								neg_mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	neg_mode	Inversion mode control 0: normal mode 1: inversion mode

ISP_DEHAZE_AIR

ISP_DEHAZE_AIR is a dehaze airglow configuration register.

Offset Address	Register Name	Total Reset Value
0x46730	ISP_DEHAZE_AIR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	air_r		air_g		air_b		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	air_r	Airglow A corresponding to the R channel
[19:10]	RW	air_g	Airglow A corresponding to the G channel
[9:0]	RW	air_b	Airglow A corresponding to the B channel

ISP_DEHAZE_THLD

ISP_DEHAZE_THLD is a dehaze T threshold coefficient configuration register.

Offset Address	Register Name	Total Reset Value
0x46734	ISP_DEHAZE_THLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						thld									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	thld	T threshold coefficient, unsigned integer

ISP_DEHAZE_GSTRTH

ISP_DEHAZE_GSTRTH is a dehaze global strength coefficient register.

Offset Address	Register Name	Total Reset Value
0x46738	ISP_DEHAZE_GSTRTH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gstrth							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	gstrth	G calculation coefficient, unsigned integer

ISP_DEHAZE_BLTHLD

ISP_DEHAZE_BLTHLD is a dehaze minimum value filtering threshold coefficient configuration register.

Offset Address	Register Name	Total Reset Value
0x4673C	ISP_DEHAZE_BLTHLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						blthld									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	blthld	Minimum value filtering threshold coefficient, unsigned integer

ISP_DEHAZE_STR_LUT_UPDATE

ISP_DEHAZE_STR_LUT_UPDATE is a dehaze strength table update register.

Offset Address	Register Name	Total Reset Value
0x46740	ISP_DEHAZE_STR_LUT_UPDATE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								str_lut_update
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	str_lut_update	Update of the dehaze strength table configuration. This bit is automatically cleared for each frame.

ISP_DEHAZE_MINSTAT_WADDR

ISP_DEHAZE_MINSTAT_WADDR is a dehaze minimum value statistics write address register.

Offset Address	Register Name	Total Reset Value
0x46780	ISP_DEHAZE_MINSTAT_WADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								minstat_waddr
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8:0]	RW	minstat_waddr	Write address of the dehaze minimum value statistics. The value range is [0, 511].

ISP_DEHAZE_MINSTAT_WDATA

ISP_DEHAZE_MINSTAT_WDATA is a dehaze minimum value statistics write data register.

Offset Address	Register Name	Total Reset Value
0x46784	ISP_DEHAZE_MINSTAT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								minstat_wdata_h								reserved								minstat_wdata_l							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	minstat_wdata_h	Write data of dehaze minimum value statistics, high block number
[15:10]	-	reserved	Reserved
[9:0]	RW	minstat_wdata_l	Write data of dehaze minimum value statistics, low block number

ISP_DEHAZE_MINSTAT_RADDR

ISP_DEHAZE_MINSTAT_RADDR is a dehaze minimum value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x46788	ISP_DEHAZE_MINSTAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								minstat_raddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:9]	-	reserved	Reserved
[8:0]	RW	minstat_raddr	Read address of dehaze minimum value statistics. The value range is [0, 511].

ISP_DEHAZE_MINSTAT_RDATA

ISP_DEHAZE_MINSTAT_RDATA is a dehaze minimum value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x4678C	ISP_DEHAZE_MINSTAT_RDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		minstat_rdata_h		reserved		minstat_rdata_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RO	minstat_rdata_h	Read data of dehaze minimum value statistics, high block number
[15:10]	-	reserved	Reserved
[9:0]	RO	minstat_rdata_l	Read data of dehaze minimum value statistics, low block number

ISP_DEHAZE_MAXSTAT_WADDR

ISP_DEHAZE_MAXSTAT_WADDR is a dehaze maximum value statistics write address register.

Offset Address	Register Name	Total Reset Value
0x46790	ISP_DEHAZE_MAXSTAT_WADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						maxstat_waddr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9:0]	RW	maxstat_waddr	Write address of dehaze maximum value statistics. The value range is [0, 1023].

ISP_DEHAZE_MAXSTAT_WDATA

ISP_DEHAZE_MAXSTAT_WDATA is a dehaze maximum value statistics write data register.

Offset Address	Register Name	Total Reset Value
0x46794	ISP_DEHAZE_MAXSTAT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				maxstat_wdata																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:0]	RW	maxstat_wdata	Write data of dehaze maximum value statistics

ISP_DEHAZE_MAXSTAT_RADDR

ISP_DEHAZE_MAXSTAT_RADDR is a dehaze maximum value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x46798	ISP_DEHAZE_MAXSTAT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								maxstat_raddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9:0]	RW	maxstat_raddr	Read address of dehaze maximum value statistics. The value range is [0, 1023].

ISP_DEHAZE_MAXSTAT_RDATA

ISP_DEHAZE_MAXSTAT_RDATA is a dehaze maximum value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x4679C	ISP_DEHAZE_MAXSTAT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				maxstat_rdata																											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	-	reserved	Reserved
[29:0]	RO	maxstat_rdata	Read data of dehaze maximum value statistics R: bit[29:20] G: bit[19:10] B: bit[9:0]

ISP_DEHAZE_PRESTAT_WADDR

ISP_DEHAZE_PRESTAT_WADDR is a dehaze previous frame minimum value statistics write address register.

Offset Address	Register Name	Total Reset Value
0x467A0	ISP_DEHAZE_PRESTAT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								prestat_waddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9:0]	RW	prestat_waddr	Write address of dehaze previous frame minimum value statistics. The value range is [0, 511].

ISP_DEHAZE_PRESTAT_WDATA

ISP_DEHAZE_PRESTAT_WDATA is a dehaze previous frame minimum value statistics write data register.

Offset Address	Register Name	Total Reset Value
0x467A4	ISP_DEHAZE_PRESTAT_WDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		prestat_wdata_h		reserved		prestat_wdata_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	prestat_wdata_h	Write data of dehaze previous frame minimum value statistics
[15:10]	-	reserved	Reserved
[9:0]	RW	prestat_wdata_l	Write data of dehaze previous frame minimum value statistics

ISP_DEHAZE_PRESTAT_RADDR

ISP_DEHAZE_PRESTAT_RADDR is a dehaze previous frame minimum value statistics read address register.

Offset Address	Register Name	Total Reset Value
0x467A8	ISP_DEHAZE_PRESTAT_RADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						prestat_raddr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:10]	-	reserved	Reserved
[9:0]	RW	prestat_raddr	Read address of dehaze previous frame minimum value statistics. The value range is [0, 511].

ISP_DEHAZE_PRESTAT_RDATA

ISP_DEHAZE_PRESTAT_RDATA is a dehaze previous frame minimum value statistics read data register.

Offset Address	Register Name	Total Reset Value
0x467AC	ISP_DEHAZE_PRESTAT_RDATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		prestat_rdata_h		reserved		prestat_rdata_l	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RO	prestat_rdata_h	Read data of dehaze previous frame minimum value statistics, high block number
[15:10]	-	reserved	Reserved
[9:0]	RO	prestat_rdata_l	Read data of dehaze previous frame minimum value statistics, low block number

ISP_DEHAZE_LUT_WADDR

ISP_DEHAZE_LUT_WADDR is a dehaze strength LUT information write address register.

Offset Address	Register Name	Total Reset Value
0x467B0	ISP_DEHAZE_LUT_WADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved						lut_waddr	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	lut_waddr	Write address of the dehaze strength LUT information. The value range is [0, 255].

ISP_DEHAZE_LUT_WDATA

ISP_DEHAZE_LUT_WDATA is a dehaze strength LUT information write data register.

Offset Address	Register Name	Total Reset Value
0x467B4	ISP_DEHAZE_LUT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lut_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	lut_wdata	Write data of the dehaze strength LUT information

ISP_DEHAZE_LUT_RADDR

ISP_DEHAZE_LUT_RADDR is a dehaze strength LUT information read address register.

Offset Address	Register Name	Total Reset Value
0x467B8	ISP_DEHAZE_LUT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lut_raddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RW	lut_raddr	Read address of the dehaze strength LUT information. The value range is [0, 255].

ISP_DEHAZE_LUT_RDATA

ISP_DEHAZE_LUT_RDATA is a dehaze strength LUT information read data register.

Offset Address	Register Name	Total Reset Value
0x467BC	ISP_DEHAZE_LUT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								lut_rdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RO	lut_rdata	Read data of the dehaze strength LUT information

ISP_DEHAZE_SIZE

ISP_DEHAZE_SIZE is a dehaze picture size register.

Offset Address	Register Name	Total Reset Value
0x467F0	ISP_DEHAZE_SIZE	0x0437_077F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Window height (unit: row) The configured value is the actual value minus 1.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Window width (unit: pixel) The configured value is the actual value minus 1.

ISP_GAMMA_CFG

ISP_GAMMA_CFG is a gamma control register.

Offset Address	Register Name	Total Reset Value
0x46A00	ISP_GAMMA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	en	Gamma enable 0: disabled 1: enabled

ISP_GAMMA_LUT_UPDATE

ISP_GAMMA_LUT_UPDATE is a gamma LUT update register.

Offset Address	Register Name	Total Reset Value
0x46A10	ISP_GAMMA_LUT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	update	Gamma LUT update This bit is automatically cleared for each frame.

ISP_GAMMA_WADDR

ISP_GAMMA_WADDR is a gamma LUT write address register.

Offset Address	Register Name	Total Reset Value
0x46A80	ISP_GAMMA_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gamma_waddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	gamma_waddr	Write address of the gamma 257-entry LUT

ISP_GAMMA_WDATA

ISP_GAMMA_WDATA is a gamma LUT write data register.

Offset Address	Register Name	Total Reset Value
0x46A84	ISP_GAMMA_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gamma_wdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	gamma_wdata	Write data of the gamma 257-entry LUT

ISP_GAMMA_RADDR

ISP_GAMMA_RADDR is a gamma LUT read address register.

Offset Address	Register Name	Total Reset Value
0x46A88	ISP_GAMMA_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gamma_raddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	gamma_raddr	Read address of the gamma 257-entry LUT

ISP_GAMMA_RDATA

ISP_GAMMA_RDATA is a gamma LUT read data register.

Offset Address	Register Name	Total Reset Value
0x46A8C	ISP_GAMMA_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	gamma_rdata																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	gamma_rdata	Read data of the gamma 257-entry LUT

ISP_CA_CFG

ISP_CA_CFG is a CA enable register.

Offset Address	Register Name	Total Reset Value
0x47000	ISP_CA_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved

[0]	RW	en	CA enable (U1) 0: disabled 1: enabled

ISP_CA_CTRL

ISP_CA_CTRL is a CA control register.

Offset Address	Register Name	Total Reset Value
0x47010	ISP_CA_CTRL	0x0101_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved							llhcproc_en	reserved							skinproc_en	reserved							colorproc_en	reserved							satadj_en
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:25]	-	reserved	Reserved
[24]	RW	llhcproc_en	Dark high-saturation region protection enable (U1) 0: disabled 1: enabled
[23:17]	-	reserved	Reserved
[16]	RW	skinproc_en	Complexion protection enable (U1) 0: disabled 1: enabled
[15:9]	-	reserved	Reserved
[8]	RW	colorproc_en	Color protection enable (U1) 0: disabled 1: enabled
[7:1]	-	reserved	Reserved
[0]	RW	satadj_en	Saturation adjustment enable (U1) 0: disabled 1: enabled

ISP_CA_LUMATH

ISP_CA_LUMATH is a luminance threshold register.

Offset Address	Register Name	Total Reset Value
0x47014	ISP_CA_LUMATH	0x00FA_0190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								lumath_low								reserved								lumath_high							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	lumath_low	Low threshold of the luminance (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	lumath_high	High threshold of the luminance (U10)

ISP_CA_DARKCHROMA_TH

ISP_CA_DARKCHROMA_TH is a dark region chrominance threshold register.

Offset Address	Register Name	Total Reset Value
0x47018	ISP_CA_DARKCHROMA_TH	0x021C_0228

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								darkchromath_low								reserved								darkchromath_high							
Reset	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	darkchromath_low	Low threshold of the dark region chrominance (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	darkchromath_high	High threshold of the dark region chrominance (U10)

ISP_CA_SDARKCHROMA_TH

ISP_CA_SDARKCHROMA_TH is a bright and dark transition region chrominance threshold register.

Offset Address	Register Name	Total Reset Value
0x4701C	ISP_CA_SDARKCHROMA_TH	0x021C_0230

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sdarkchromath_low								reserved								sdarkchromath_high							
Reset	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	sdarkchromath_low	Low threshold of chrominance in the bright and dark transition region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	sdarkchromath_high	High threshold of chrominance in the bright and dark transition region (U10)

ISP_CA_LLHC_RATIO

ISP_CA_LLHC_RATIO is a low luminance and high saturation region gain register.

Offset Address	Register Name	Total Reset Value
0x47020	ISP_CA_LLHC_RATIO	0x0320_02C4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								lumaratio_low								reserved								lumaratio_high							
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	lumaratio_low	Gain of the dark high-chrominance region (U10)
[15:11]	-	reserved	Reserved
[10:0]	RW	lumaratio_high	Gain of the bright high-chrominance region (U10)

ISP_CA_ISORATIO

ISP_CA_ISORATIO is an ISO gain register.

Offset Address	Register Name	Total Reset Value
0x47024	ISP_CA_ISORATIO	0x0000_0578

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								isoratio							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RW	isoratio	ISO gain of the chrominance component (U10)

ISP_CA_LUT_UPDATE

ISP_CA_LUT_UPDATE is an LUT update register.

Offset Address	Register Name	Total Reset Value
0x47028	ISP_CA_LUT_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															lut_update
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	lut_update	LUT update control (U10). This bit is automatically cleared for each frame.

ISP_CA_YUV2RGB_COEF0

ISP_CA_YUV2RGB_COEF0 is a YUV-to-RGB conversion coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x4702C	ISP_CA_YUV2RGB_COEF0	0x0400_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				yuv2rgb_coef00												reserved				yuv2rgb_coef01											
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	yuv2rgb_coef00	YUV-to-RGB conversion coefficient 00 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	yuv2rgb_coef01	YUV-to-RGB conversion coefficient 01 (S5.10)

ISP_CA_YUV2RGB_COEF1

ISP_CA_YUV2RGB_COEF1 is YUV-to-RGB conversion coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x47030	ISP_CA_YUV2RGB_COEF1	0x064C_0400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				yuv2rgb_coef02												reserved				yuv2rgb_coef10											
Reset	0	0	0	0	0	1	1	0	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	yuv2rgb_coef02	YUV-to-RGB conversion coefficient 02 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	yuv2rgb_coef10	YUV-to-RGB conversion coefficient 10 (S5.10)

ISP_CA_YUV2RGB_COEF2

ISP_CA_YUV2RGB_COEF2 is YUV-to-RGB conversion coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x47034	ISP_CA_YUV2RGB_COEF2	0x7F41_7E21

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				yuv2rgb_coef11												reserved				yuv2rgb_coef12											
Reset	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	1	0	0	0	0	1

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	yuv2rgb_coef11	YUV-to-RGB conversion coefficient 11 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	yuv2rgb_coef12	YUV-to-RGB conversion coefficient 12 (S5.10)

ISP_CA_YUV2RGB_COEF3

ISP_CA_YUV2RGB_COEF3 is YUV-to-RGB conversion coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x47038	ISP_CA_YUV2RGB_COEF3	0x0400_076C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				yuv2rgb_coef20												reserved				yuv2rgb_coef21											
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	yuv2rgb_coef20	YUV-to-RGB conversion coefficient 20 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	yuv2rgb_coef21	YUV-to-RGB conversion coefficient 21 (S5.10)

ISP_CA_YUV2RGB_COEF4

ISP_CA_YUV2RGB_COEF4 is YUV-to-RGB conversion coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x4703C	ISP_CA_YUV2RGB_COEF4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				yuv2rgb_coef22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	yuv2rgb_coef22	YUV-to-RGB conversion coefficient 22 (S5.10)

ISP_CA_YUV2RGB_INDC0

ISP_CA_YUV2RGB_INDC0 is YUV-to-RGB conversion input offset register 0

Offset Address	Register Name	Total Reset Value
0x47040	ISP_CA_YUV2RGB_INDC0	0x0000_0600

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				yuv2rgb_indc0												reserved				yuv2rgb_indc1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	yuv2rgb_indc0	Input offset 0 of YUV-to-RGB conversion (S11)
[15:11]	-	reserved	Reserved
[10:0]	RW	yuv2rgb_indc1	Input offset 1 of YUV-to-RGB conversion (S11)

ISP_CA_YUV2RGB_INDC1

ISP_CA_YUV2RGB_INDC1 is YUV-to-RGB conversion input offset register 1.

Offset Address	Register Name	Total Reset Value
0x47044	ISP_CA_YUV2RGB_INDC1	0x0000_0600

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								yuv2rgb_indc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved

[10:0]	RW	yuv2rgb_indc2	Input offset 2 of YUV-to-RGB conversion (S11)

ISP_CA_YUV2RGB_OUTDC0

ISP_CA_YUV2RGB_OUTDC0 is YUV-to-RGB conversion output offset register 0.

Offset Address	Register Name	Total Reset Value
0x47048	ISP_CA_YUV2RGB_OUTDC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				yuv2rgb_outdc0												reserved				yuv2rgb_outdc1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	yuv2rgb_outdc0	Output offset 0 of YUV-to-RGB conversion (S11)
[15:11]	-	reserved	Reserved
[10:0]	RW	yuv2rgb_outdc1	Output offset 1 of YUV-to-RGB conversion (S11)

ISP_CA_YUV2RGB_OUTDC1

ISP_CA_YUV2RGB_OUTDC1 is YUV-to-RGB conversion output offset register 1.

Offset Address	Register Name	Total Reset Value
0x4704C	ISP_CA_YUV2RGB_OUTDC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								yuv2rgb_outdc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RW	yuv2rgb_outdc2	Output offset 2 of YUV-to-RGB conversion (S11)

ISP_CA_RGB2YUV_COEF0

ISP_CA_RGB2YUV_COEF0 is RGB-to-YUV conversion coefficient register 0.

Offset Address	Register Name	Total Reset Value
0x47050	ISP_CA_RGB2YUV_COEF0	0x00DA_02DC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rgb2yuv_coef00												reserved				rgb2yuv_coef01											
Reset	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	rgb2yuv_coef00	RGB-to-YUV conversion coefficient 00 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	rgb2yuv_coef01	RGB-to-YUV conversion coefficient 01 (S5.10)

ISP_CA_RGB2YUV_COEF1

ISP_CA_RGB2YUV_COEF1 is RGB-to-YUV conversion coefficient register 1.

Offset Address	Register Name	Total Reset Value
0x47054	ISP_CA_RGB2YUV_COEF1	0x0049_7F89

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rgb2yuv_coef02												reserved				rgb2yuv_coef10											
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	1

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	rgb2yuv_coef02	RGB-to-YUV conversion coefficient 02 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	rgb2yuv_coef10	RGB-to-YUV conversion coefficient 10 (S5.10)

ISP_CA_RGB2YUV_COEF2

ISP_CA_RGB2YUV_COEF2 is RGB-to-YUV conversion coefficient register 2.

Offset Address	Register Name	Total Reset Value
0x47058	ISP_CA_RGB2YUV_COEF2	0x7E6D_020B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rgb2yuv_coef11												reserved				rgb2yuv_coef12											
Reset	0	1	1	1	1	1	1	0	0	1	1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	rgb2yuv_coef11	RGB-to-YUV conversion coefficient 11 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	rgb2yuv_coef12	RGB-to-YUV conversion coefficient 12 (S5.10)

ISP_CA_RGB2YUV_COEF3

ISP_CA_RGB2YUV_COEF3 is RGB-to-YUV conversion coefficient register 3.

Offset Address	Register Name	Total Reset Value
0x4705C	ISP_CA_RGB2YUV_COEF3	0x020B_7E25

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rgb2yuv_coef20												reserved				rgb2yuv_coef21											
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	0	0	0	1	0	0	1	0	1

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:16]	RW	rgb2yuv_coef20	RGB-to-YUV conversion coefficient 20 (S5.10)
[15]	-	reserved	Reserved
[14:0]	RW	rgb2yuv_coef21	RGB-to-YUV conversion coefficient 21 (S5.10)

ISP_CA_RGB2YUV_COEF4

ISP_CA_RGB2YUV_COEF4 is RGB-to-YUV conversion coefficient register 4.

Offset Address	Register Name	Total Reset Value
0x47060	ISP_CA_RGB2YUV_COEF4	0x0000_7FD0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				rgb2yuv_coef22											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14:0]	RW	rgb2yuv_coef22	RGB-to-YUV conversion coefficient 22 (S5.10)

ISP_CA_RGB2YUV_INDC0

ISP_CA_RGB2YUV_INDC0 is RGB-to-YUV conversion input offset register 0.

Offset Address	Register Name	Total Reset Value
0x47064	ISP_CA_RGB2YUV_INDC0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rgb2yuv_indc0												reserved				rgb2yuv_indc1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	rgb2yuv_indc0	Input offset 0 of RGB-to-YUV conversion (S11)
[15:11]	-	reserved	Reserved
[10:0]	RW	rgb2yuv_indc1	Input offset 1 of RGB-to-YUV conversion (S11)

ISP_CA_RGB2YUV_INDC1

ISP_CA_RGB2YUV_INDC1 is RGB-to-YUV conversion input offset register 1.

Offset Address	Register Name	Total Reset Value
0x47068	ISP_CA_RGB2YUV_INDC1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgb2yuv_indc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved

[10:0]	RW	rgb2yuv_indc2	Input offset 2 of RGB-to-YUV conversion (S11)

ISP_CA_RGB2YUV_OUTDC0

ISP_CA_RGB2YUV_OUTDC0 is RGB-to-YUV conversion output offset register 0.

Offset Address	Register Name	Total Reset Value
0x4706C	ISP_CA_RGB2YUV_OUTDC0	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				rgb2yuv_outdc0												reserved				rgb2yuv_outdc1											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	-	reserved	Reserved
[26:16]	RW	rgb2yuv_outdc0	Output offset 0 of RGB-to-YUV conversion (S11)
[15:11]	-	reserved	Reserved
[10:0]	RW	rgb2yuv_outdc1	Output offset 1 of RGB-to-YUV conversion (S11)

ISP_CA_RGB2YUV_OUTDC1

ISP_CA_RGB2YUV_OUTDC1 is RGB-to-YUV conversion output offset register 1.

Offset Address	Register Name	Total Reset Value
0x47070	ISP_CA_RGB2YUV_OUTDC1	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rgb2yuv_outdc2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RW	rgb2yuv_outdc2	Input offset 2 of RGB-to-YUV conversion (S11)

ISP_CA_SKINLLUMA_UTH

ISP_CA_SKINLLUMA_UTH is a complexion judgment dark region U component threshold register.

Offset Address	Register Name	Total Reset Value
0x47074	ISP_CA_SKINLLUMA_UTH	0x01CC_0200

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		skinlluma_umin		reserved		skinlluma_umax	
Reset	0 0 0 0	0 0 0 1	1 1 0 0	1 1 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinlluma_umin	Low threshold of the U component in the complexion judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinlluma_umax	High threshold of the U component in the complexion judgment dark region (U10)

ISP_CA_SKINLLUMA_UYTH

ISP_CA_SKINLLUMA_UYTH is a complexion judgment dark region U corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x47078	ISP_CA_SKINLLUMA_UYTH	0x0040_0190

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		skinlluma_uymin		reserved		skinlluma_uymax	
Reset	0 0 0 0	0 0 0 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 1	1 0 0 1	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinlluma_uymin	Low threshold of the Y component corresponding to the U in the complexion judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinlluma_uymax	High threshold of the Y component corresponding to the U in the complexion judgment dark region (U10)

ISP_CA_SKINHLUMA_UTH

ISP_CA_SKINHLUMA_UTH is a complexion judgment bright region U component threshold register.

Offset Address	Register Name	Total Reset Value
0x4707C	ISP_CA_SKINHLUMA_UTH	0x0180_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skinhluma_umin								reserved								skinhluma_umax							
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinhluma_umin	Low threshold of the U component in the complexion judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinhluma_umax	High threshold of the U component in the complexion judgment bright region (U10)

ISP_CA_GAINLUT_WADDR

ISP_CA_GAINLUT_WADDR is a gain LUT write address register.

Offset Address	Register Name	Total Reset Value
0x47080	ISP_CA_GAINLUT_WADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									gainlut_waddr						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved
[6:0]	RW	gainlut_waddr	Write address of the gain LUT (U7)

ISP_CA_GAINLUT_WDATA

ISP_CA_GAINLUT_WDATA is a gain LUT write data register.

Offset Address	Register Name	Total Reset Value
0x47084	ISP_CA_GAINLUT_WDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gainlut_wdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RW	gainlut_wdata	Write data of the gain LUT (U11)

ISP_CA_GAINLUT_RADDR

ISP_CA_GAINLUT_RADDR is a gain LUT read address register.

Offset Address	Register Name	Total Reset Value
0x47088	ISP_CA_GAINLUT_RADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									gainlut_raddr							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	-	reserved	Reserved
[6:0]	RW	gainlut_raddr	Read address of the gain LUT (U7)

ISP_CA_GAINLUT_RDATA

ISP_CA_GAINLUT_RDATA is a gain LUT read data register.

Offset Address	Register Name	Total Reset Value
0x4708C	ISP_CA_GAINLUT_RDATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								gainlut_rdata							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RO	gainlut_rdata	Read data of the gain LUT (U11)

ISP_CA_SKINHLUMA_UYTH

ISP_CA_SKINHLUMA_UYTH is a complexion judgment bright region U corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x47110	ISP_CA_SKINHLUMA_UYTH	0x0190_03C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skinhluma_uymin								reserved								skinhluma_uymax							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinhluma_uymin	Low threshold of the Y component corresponding to the U in the complexion judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinhluma_uymax	High threshold of the Y component corresponding to the U in the complexion judgment bright region (U10)

ISP_CA_SKINLLUMA_VTH

ISP_CA_SKINLLUMA_VTH is a complexion judgment dark region V component threshold register.

Offset Address	Register Name	Total Reset Value
0x47114	ISP_CA_SKINLLUMA_VTH	0x0208_0272

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skinlluma_vmin								reserved								skinlluma_vmax							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinlluma_vmin	Low threshold of the V component in the complexion judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinlluma_vmax	High threshold of the V component in the complexion judgment dark region (U10)

ISP_CA_SKINLLUMA_VYTH

ISP_CA_SKINLLUMA_VYTH is a complexion judgment dark region V corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x47118	ISP_CA_SKINLLUMA_VYTH	0x0040_0190

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skinlluma_vymin								reserved								skinlluma_vymax							
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinlluma_vymin	Low threshold of the Y component corresponding to the V in the complexion judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinlluma_vymax	High threshold of the Y component corresponding to the V in the complexion judgment dark region (U10)

ISP_CA_SKINHLUMA_VTH

ISP_CA_SKINHLUMA_VTH is a complexion judgment bright region V component threshold register.

Offset Address	Register Name	Total Reset Value
0x4711C	ISP_CA_SKINHLUMA_VTH	0x0208_0272

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skinhluma_vmin								reserved								skinhluma_vmax							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	1	0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinhluma_vmin	Low threshold of the V component in the complexion judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinhluma_vmax	High threshold of the V component in the complexion judgment dark region (U10)

ISP_CA_SKINHLUMA_VYTH

ISP_CA_SKINHLUMA_VYTH is a complexion judgment bright region V corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x47120	ISP_CA_SKINHLUMA_VYTH	0x0190_033F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								skinhluma_vymin								reserved								skinhluma_vymax							
Reset	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	skinhluma_vymin	Low threshold of the Y component corresponding to the V in the complexion judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	skinhluma_vymax	High threshold of the Y component corresponding to the V in the complexion judgment bright region (U10)

ISP_CA_SKIN_UVDIFF

ISP_CA_SKIN_UVDIFF is a complexion judgment UV component difference register.

Offset Address	Register Name	Total Reset Value
0x47124	ISP_CA_SKIN_UVDIFF	0x0000_0028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								skin_uvdiff							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RW	skin_uvdiff	UV difference threshold for complexion judgment (S11)

ISP_CA_SKIN_RATIOTH0

ISP_CA_SKIN_RATIOTH0 is complexion protection gain threshold register 0.

Offset Address	Register Name	Total Reset Value
0x47128	ISP_CA_SKIN_RATIOTH0	0x0384_0514

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				skinratioth_low												reserved				skinratioth_mid											
Reset	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	skinratioth_low	Low threshold of the complexion protection gain (U12). The maximum value is 1024.
[15:12]	-	reserved	Reserved
[11:0]	RW	skinratioth_mid	Medium threshold of the complexion protection gain (U12)

ISP_CA_SKIN_RATIOTH1

ISP_CA_SKIN_RATIOTH1 is complexion protection gain threshold register 1.

Offset Address	Register Name	Total Reset Value
0x4712C	ISP_CA_SKIN_RATIOTH1	0x0000_05DC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				skinratioth_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	skinratioth_high	High threshold of the complexion protection gain (U12)

ISP_CA_COLORLLUMA_UTH

ISP_CA_COLORLLUMA_UTH is a color judgment dark region U component threshold register.

Offset Address	Register Name	Total Reset Value
0x47130	ISP_CA_COLORLLUMA_UTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorlluma_umin		reserved		colorlluma_umax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorlluma_umin	Low threshold of the U component in the color judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorlluma_umax	High threshold of the U component in the color judgment dark region (U10)

ISP_CA_COLORLLUMA_UYTH

ISP_CA_COLORLLUMA_UYTH is a color judgment dark region U corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x47134	ISP_CA_COLORLLUMA_UYTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorlluma_uymin		reserved		colorlluma_uymax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorlluma_uymin	Low threshold of the Y component corresponding to the U in the color judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorlluma_uymax	High threshold of the Y component corresponding to the U in the color judgment dark region (U10)

ISP_CA_COLORHLUMA_UTH

ISP_CA_COLORHLUMA_UTH is a color judgment bright region U component threshold register.

Offset Address	Register Name	Total Reset Value
0x47138	ISP_CA_COLORHLUMA_UTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorhluma_umin		reserved		colorhluma_umax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorhluma_umin	Low threshold of the U component in the color judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorhluma_umax	High threshold of the U component in the color judgment bright region (U10)

ISP_CA_COLORHLUMA_UYTH

ISP_CA_COLORHLUMA_UYTH is a color judgment bright region U corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x4713C	ISP_CA_COLORHLUMA_UYTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorhluma_uymin		reserved		colorhluma_uymax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorhluma_uymin	Low threshold of the Y component corresponding to the U in the color judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorhluma_uymax	High threshold of the Y component corresponding to the U in the color judgment bright region (U10)

ISP_CA_COLORLLUMA_VTH

ISP_CA_COLORLLUMA_VTH is a color judgment dark region V component threshold register.

Offset Address	Register Name	Total Reset Value
0x47140	ISP_CA_COLORLLUMA_VTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorlluma_vmin		reserved		colorlluma_vmax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorlluma_vmin	Low threshold of the V component in the color judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorlluma_vmax	High threshold of the V component in the color judgment dark region (U10)

ISP_CA_COLORLLUMA_VYTH

ISP_CA_COLORLLUMA_VYTH is a color judgment dark region V corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x47144	ISP_CA_COLORLLUMA_VYTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorlluma_vymin		reserved		colorlluma_vymax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorlluma_vymin	Low threshold of the Y component corresponding to the V in the color judgment dark region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorlluma_vymax	High threshold of the Y component corresponding to the V in the color judgment dark region (U10)

ISP_CA_COLORHLUMA_VTH

ISP_CA_COLORHLUMA_VTH is a color judgment bright region V component threshold register.

Offset Address	Register Name	Total Reset Value
0x47148	ISP_CA_COLORHLUMA_VTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorhluma_vmin		reserved		colorhluma_vmax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorhluma_vmin	Low threshold of the V component in the color judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorhluma_vmax	High threshold of the V component in the color judgment bright region (U10)

ISP_CA_COLORHLUMA_VYTH

ISP_CA_COLORHLUMA_VYTH is a color judgment bright region V corresponding Y component threshold register.

Offset Address	Register Name	Total Reset Value
0x4714C	ISP_CA_COLORHLUMA_VYTH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		colorhluma_vymin		reserved		colorhluma_vymax	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	-	reserved	Reserved
[25:16]	RW	colorhluma_vymin	Low threshold of the Y component corresponding to the V in the color judgment bright region (U10)
[15:10]	-	reserved	Reserved
[9:0]	RW	colorhluma_vymax	High threshold of the Y component corresponding to the V in the color judgment bright region (U10)

ISP_CA_COLOR_UVDIFF

ISP_CA_COLOR_UVDIFF is a color judgment UV component difference register.

Offset Address	Register Name	Total Reset Value
0x47150	ISP_CA_COLOR_UVDIFF	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								color_uvdiff							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10:0]	RW	color_uvdiff	UV difference threshold for color judgment (S11)

ISP_CA_COLOR_RATIOTH0

ISP_CA_COLOR_RATIOTH0 is color protection gain threshold register 0.

Offset Address	Register Name	Total Reset Value
0x47154	ISP_CA_COLOR_RATIOTH0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				colorratioth_low												reserved				colorratioth_mid											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27:16]	RW	colorratioth_low	Low threshold of the color protection gain (U12). The maximum value is 1024.
[15:12]	-	reserved	Reserved
[11:0]	RW	colorratioth_mid	Medium threshold of the color protection gain (U12)

ISP_CA_COLOR_RATIOTH1

ISP_CA_COLOR_RATIOTH1 is color protection gain threshold register 1.

Offset Address	Register Name	Total Reset Value
0x47158	ISP_CA_COLOR_RATIOTH1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				colorratioth_high											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	colorratioth_high	High threshold of the color protection gain (U12)

ISP_CA_SIZE

ISP_CA_SIZE is a CA picture size register.

Offset Address	Register Name	Total Reset Value
0x471F0	ISP_CA_SIZE	0x02CF_04FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height The configured value is the actual value minus 1. For example, if the actual height is 720, set this field to 719.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width The configured value is the actual value minus 1. For example, if the actual width is 1280, set this field to 1279.

ISP_HLDC_CFG

ISP_HLDC_CFG is an HLDC enable register.

Offset Address	Register Name	Total Reset Value
0x51300	ISP_HLDC_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hldc_l_en	hldc_c_en	reserved																													hldc_in_b422
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	hldc_l_en	HLDC luminance enable 0: disabled 1: enabled
[30]	RW	hldc_c_en	HLDC chrominance enable 0: disabled 1: enabled
[29:1]	RO	reserved	Reserved
[0]	RW	hldc_in_b422	Format of data processed by the HLDC 0: yuv420 1: yuv422

ISP_HLDC_SIZE

ISP_HLDC_SIZE is an HLDC luminance size configuration register.

Offset Address	Register Name	Total Reset Value
0x51310	ISP_HLDC_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:16]	RW	height	Height of a picture luminance column (in pixel). The configured value is the actual value minus 1.

[15:13]	RO	reserved	Reserved
[12:0]	RW	width	Width of a picture luminance row (in pixel). The configured value is the actual value minus 1.

ISP_HLDC_CENTER

ISP_HLDC_CENTER is an HLDC center coordinate parameter register.

Offset Address	Register Name	Total Reset Value
0x51320	ISP_HLDC_CENTER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ldc_norcoef								ldc_y_center												ldc_x_center											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	ldc_norcoef	Normalization parameter
[23:12]	RW	ldc_y_center	Vertical central coordinate
[11:0]	RW	ldc_x_center	Horizontal central coordinate

ISP_HLDC_PARA

ISP_HLDC_PARA is an HLDC configuration parameter register.

Offset Address	Register Name	Total Reset Value
0x51324	ISP_HLDC_PARA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								ldc_mode	ldc_barrel_mode	reserved		shift_right				ratio								scale							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved

[23]	RW	ldc_mode	LDC mode 0: barrel mode 1: pincushion mode
[22]	RW	ldc_barrel_mode	LDC barrel mode 0: forward 1: reverse
[21]	RO	reserved	Reserved
[20:16]	RW	shift_right	Number of right shift bits for the denominator
[15:7]	RW	ratio	Distortion coefficient
[6:0]	RW	scale	Scaling ratio

ISP_ACM_CTRL

ISP_ACM_CTRL is an ACM control register.

Offset Address	Register Name	Total Reset Value
0x51400	ISP_ACM_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acm_en		acm_dbg_en		acm_stretch		acm_cliprange		acm_cliporwrap		reserved						acm_dbg_pos								acm_dbg_mode		acm_cbcrthr					
Reset	0		0		0		0		0		0		0		0		0		0		0		0		0		0		0		0	

Bits	Access	Name	Description
[31]	RW	acm_en	ACM enable 0: disabled (data output bypassed) 1: enabled (implementing luminance and contrast adjustment)
[30]	RW	acm_dbg_en	ACM debugging enable. When acm_dbg_en is valid, the original picture is displayed on the left part of the screen, and the picture processed by ABC is displayed on the right part of the screen.
[29]	RW	acm_stretch	Input pixel range 0: Y 64−940, C 64−960 1: Y 0−1023, C 0−1023

[28]	RW	acm_cliprange	Output pixel range 0: Y 64−940, C 64−960 1: Y 0−1023, C 0−1023
[27]	RW	acm_cliporwrap	Hue component value limit after ACM 0: The hue component is wrapped around to fall within [0, 1023]. 1: The hue component is clipped to fall within [0, 1023].
[26:23]	RO	reserved	Reserved
[22:10]	RW	ACM_dbg_pos	ACM debugging position
[9]	RW	ACM_dbg_mode	ACM debugging mode 0: The left picture is the original picture and the right picture is the one after ACM processing. 1: The right picture is the original picture and the left picture is the one after ACM processing.
[8:0]	RW	acm_cbcrthr	ACM algorithm adjustment enable threshold. It is a 9-bit unsigned number and ranges from 0 to 255.

ISP_ACM_ADJ

ISP_ACM_ADJ is an ACM processed pixel change register.

Offset Address	Register Name	Total Reset Value
0x51404	ISP_ACM_ADJ	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	acm_gain0		acm_gain1		acm_gain2		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:20]	RW	acm_gain0	Control coefficient of the luminance adjustment range. The value range is 0−512.
[19:10]	RW	acm_gain1	Control coefficient of the hue adjustment range. The value range is 0−512.
[9:0]	RW	acm_gain2	Control coefficient of the saturation adjustment range. The value range is 0−512.

ISP_ACM_PARA_REN

ISP_ACM_PARA_REN is an ACM coefficient read enable register.

Offset Address	Register Name	Total Reset Value
0x51408	ISP_ACM_PARA_REN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								acm_para_rd_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ACM_para_rd_en	ACM coefficient read enable

ISP_ACM_PARA_DATA

ISP_ACM_PARA_DATA is an ACM coefficient read data register.

Offset Address	Register Name	Total Reset Value
0x5140C	ISP_ACM_PARA_DATA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	acm_para_data								
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:0]	RO	ACM_para_data	Read data of the ACM coefficient

ISP_ACM_SIZE

ISP_ACM_SIZE is an ACM processing picture size register.

Offset Address	Register Name	Total Reset Value
0x51410	ISP_ACM_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				height												reserved				width											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	-	reserved	Reserved
[28:16]	RW	height	Picture height (in pixel) The configured value is the actual value minus 1.
[15:13]	-	reserved	Reserved
[12:0]	RW	width	Picture width (in pixel) The configured value is the actual value minus 1.

ISP_ACM_PARA_UP

ISP_ACM_PARA_UP is an ACM coefficient configuration update register.

Offset Address	Register Name	Total Reset Value
0x51420	ISP_ACM_PARA_UP	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															para_up
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	para_up	Parameter update. This bit is automatically cleared for each frame.

ISP_VPDCICTRL

ISP_VPDCICTRL is a DCI control register.

Offset Address	Register Name	Total Reset Value
0x51C00	ISP_VPDCICTRL	0x02E0_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_en	dci_dbg_en	dci_scene_flg	dci_man_adj0	dci_man_adj1	dci_man_adj2	dci_cbcrcmp_en	dci_cbcrsta_en	dci_in_range	dci_out_range	dci_shift_ctrl		dci_histlpf_en	reserved																		
Reset	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	dci_en	DCI enable 0: disabled (data output bypassed) 1: enabled (implementing luminance and contrast adjustment)
[30]	RW	dci_dbg_en	DCI demo mode enable 0: disabled 1: The original picture is displayed on the left part of the screen, and the picture processed by the DCI is displayed on the right part of the screen.
[29]	RW	dci_scene_flg	DCI scenario switch enable 0: disabled 1: enabled
[28]	RW	dci_man_adj0	Adjustment mode of curve 0 0: automatic mode. The result calculated by hardware is used. 1: manual mode. The result configured by software is used.
[27]	RW	dci_man_adj1	Adjustment mode of curve 1 0: automatic mode. The result calculated by hardware is used. 1: manual mode. The result configured by software is used.
[26]	RW	dci_man_adj2	Adjustment mode of curve 2 0: automatic mode. The result calculated by hardware is used. 1: manual mode. The result configured by software is used.
[25]	RW	dci_cbcrcmp_en	DCI chrominance compensation enable 0: The DCI algorithm does not adjust the chrominance component. 1: The DCI algorithm adjusts the chrominance component.

[24]	RW	dci_cbcrsta_en	Histogram statistics select 0: Histogram statistics are collected only on the luminance component. 1: Histogram statistics are collected on the weighted Y, Cb, and Cr components.
[23]	RW	dci_in_range	Input range 0: limited range (Y ranges from 64 to 940 and C ranges from 64 to 960 for the input 10-bit pixel data) 1: full range (Y ranges from 0 to 1023 and C ranges from 0 to 1023 for the input 10-bit pixel data)
[22]	RW	dci_out_range	Output range 0: limited range (Y ranges from 64 to 940 and C ranges from 64 to 960 for the output 10-bit pixel data) 1: full range (Y ranges from 0 to 1023 and C ranges from 0 to 1023 for the output 10-bit pixel data)
[21:20]	RW	dci_shift_ctrl	DCI histogram statistics shift control 00: shifted rightwards by 6 bits 01: shifted rightwards by 7 bits 10: shifted rightwards by 8 bits 11: shifted rightwards by 9 bits
[19]	RW	dci_histlpf_en	Histogram low-pass filtering enable 0: disabled 1: enabled
[18:0]	RO	reserved	Reserved

ISP_VPDCIHPOS

ISP_VPDCIHPOS is a DCI algorithm horizontal adjustment region register.

Offset Address	Register Name	Total Reset Value
0x51C04	ISP_VPDCIHPOS	0x0007_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_hstart												dci_hend												reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	dci_hstart	Start value of the DCI algorithm horizontal active region
[19:8]	RW	dci_hend	End value of the DCI algorithm horizontal active region
[7:0]	RO	reserved	Reserved

ISP_VPDCIVPOS

ISP_VPDCIVPOS is a DCI algorithm vertical adjustment region register.

Offset Address	Register Name	Total Reset Value
0x51C08	ISP_VPDCIVPOS	0x0004_3800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_vstart												dci_vend												reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RW	dci_vstart	Start value of the DCI algorithm vertical active region
[19:8]	RW	dci_vend	End value of the DCI algorithm vertical active region
[7:0]	RO	reserved	Reserved

ISP_VPDCIHISBLD

ISP_VPDCIHISBLD is a DCI histogram statistics weighted coefficient register.

Offset Address	Register Name	Total Reset Value
0x51C0C	ISP_VPDCIHISBLD	0x4000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_cbcrsta_y								dci_cbcrsta_cb								dci_cbcrsta_cr								reserved							
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_cbcrsta_y	Weighted coefficient of the Y component when histogram statistics are added. It is an 8-bit signed number and the most significant bit (MSB) is the sign bit.
[23:16]	RW	dci_cbcrsta_cb	Weighted coefficient of the Cb component when histogram statistics are added. It is an 8-bit signed number and the MSB is the sign bit.
[15:8]	RW	dci_cbcrsta_cr	Weighted coefficient of the Cr component when histogram statistics are added. It is an 8-bit signed number and the MSB is the sign bit.
[7:0]	RO	reserved	Reserved

ISP_VPDCIHISOFT

ISP_VPDCIHISOFT is a DCI histogram statistics offset register.

Offset Address	Register Name	Total Reset Value
0x51C10	ISP_VPDCIHISOFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_cbcrsta_oft												reserved																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	RW	dci_cbcrsta_oft	Offset when histogram statistics are added. It is a 9-bit signed number and the MSB is the sign bit.
[22:0]	RO	reserved	Reserved

ISP_VPDCIHISCOR

ISP_VPDCIHISCOR is a DCI histogram coring register.

Offset Address	Register Name	Total Reset Value
0x51C14	ISP_VPDCIHISCOR	0x0303_0300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_histcor_thr0								dci_histcor_thr1								dci_histcor_thr2								reserved							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_histcor_thr0	Coring threshold for histogram 0
[23:16]	RW	dci_histcor_thr1	Coring threshold for histogram 1
[15:8]	RW	dci_histcor_thr2	Coring threshold for histogram 2
[7:0]	RO	reserved	Reserved

ISP_VPDCIMERBLD

ISP_VPDCIMERBLD is a DCI adjustment unit blend value register.

Offset Address	Register Name	Total Reset Value
0x51C18	ISP_VPDCIMERBLD	0x4514_5048

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_metrc_abld0	dci_metrc_abld1	dci_metrc_abld2	dci_hist_abld			dci_org_abld	reserved
Reset	0 1 0 0	0 1 0 1	0 0 0 1	0 1 0 0	0 1 0 1	0 0 0 0	0 1 0 0	1 0 0 0

Bits	Access	Name	Description
[31:26]	RW	dci_metrc_abld0	Weighted alpha blend value of the current frame for metric 0
[25:20]	RW	dci_metrc_abld1	Weighted alpha blend value of the current frame for metric 1
[19:14]	RW	dci_metrc_abld2	Weighted alpha blend value of the current frame for metric 2
[13:8]	RW	dci_hist_abld	Weighted alpha blend value of the current histogram and the previous histogram
[7:2]	RW	dci_org_abld	Alpha blend value when the luminance component is adjusted
[1:0]	RO	reserved	Reserved

ISP_VPDCIADJWGT

ISP_VPDCIADJWGT is a DCI manually configured curve weight register.

Offset Address	Register Name	Total Reset Value
0x51C1C	ISP_VPDCIADJWGT	0xC864_E600

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_man_adjwgt0		dci_man_adjwgt1		dci_man_adjwgt2		reserved	
Reset	1 1 0 0	1 0 0 0	0 1 1 0	0 1 0 0	1 1 1 0	0 1 1 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dci_man_adjwgt0	Weighted value of curve 0 in manual mode
[23:16]	RW	dci_man_adjwgt1	Weighted value of curve 1 in manual mode
[15:8]	RW	dci_man_adjwgt2	Weighted value of curve 2 in manual mode
[7:0]	RO	reserved	Reserved

ISP_VPDCICLIP0

ISP_VPDCICLIP0 is a DCI curve 0 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C20	ISP_VPDCICLIP0	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_wgt_cliplow0								dci_wgt_cliphigh0								reserved															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow0	Lower limit of the weighted value of curve 0
[23:16]	RW	dci_wgt_cliphigh0	Upper limit of the weighted value of curve 0
[15:0]	RO	reserved	Reserved

ISP_VPDCICLIP1

ISP_VPDCICLIP1 is a DCI curve 1 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C24	ISP_VPDCICLIP1	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_wgt_cliplow1								dci_wgt_cliphigh1								reserved															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow1	Lower limit of the weighted value of curve 1
[23:16]	RW	dci_wgt_cliphigh1	Upper limit of the weighted value of curve 1
[15:0]	RO	reserved	Reserved

ISP_VPDCICLIP2

ISP_VPDCICLIP2 is a DCI curve 2 weight range register.

Offset Address	Register Name	Total Reset Value
0x51C28	ISP_VPDCICLIP2	0x00FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_wgt_cliplow2								dci_wgt_cliphigh2								reserved															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_wgt_cliplow2	Lower limit of the weighted value of curve 2

[23:16]	RW	dci_wgt_cliphigh2	Upper limit of the weighted value of curve 2
[15:0]	RO	reserved	Reserved

ISP_VPDCIGLBGAIN

ISP_VPDCIGLBGAIN is a DCI luminance adjustment unit global gain register.

Offset Address	Register Name	Total Reset Value
0x51C2C	ISP_VPDCIGLBGAIN	0x8208_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_glb_gain0								dci_glb_gain1				dci_glb_gain2				reserved															
Reset	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	dci_glb_gain0	Global gain 0 when the luminance component is adjusted
[25:20]	RW	dci_glb_gain1	Global gain 1 when the luminance component is adjusted
[19:14]	RW	dci_glb_gain2	Global gain 2 when the luminance component is adjusted
[13:0]	RO	reserved	Reserved

ISP_VPDCIPOSTHR0

ISP_VPDCIPOSTHR0 is DCI adjustment unit threshold register 0 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C30	ISP_VPDCIPOSTHR0	0x141E_2832

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainpos_thr1								dci_gainpos_thr2								dci_gainpos_thr3								dci_gainpos_thr4							
Reset	0	0	0	1	0	1	0	0	0	0	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0	0	1	1	0	0	1	0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr1	Threshold 1 for luminance Y when the picture is adjusted from dark to bright
[23:16]	RW	dci_gainpos_thr2	Threshold 2 for luminance Y when the picture is adjusted from dark to bright
[15:8]	RW	dci_gainpos_thr3	Threshold 3 for luminance Y when the picture is adjusted from dark to bright
[7:0]	RW	dci_gainpos_thr4	Threshold 4 for luminance Y when the picture is adjusted from dark to bright

ISP_VPDCIPOSTHR1

ISP_VPDCIPOSTHR1 is DCI adjustment unit threshold register 1 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C34	ISP_VPDCIPOSTHR1	0x3C46_7300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainpos_thr5								dci_gainpos_thr6								dci_gainpos_thr7								reserved							
Reset	0	0	1	1	1	1	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_gainpos_thr5	Threshold 5 for luminance Y when the picture is adjusted from dark to bright
[23:16]	RW	dci_gainpos_thr6	Threshold 6 for luminance Y when the picture is adjusted from dark to bright
[15:8]	RW	dci_gainpos_thr7	Threshold 7 for luminance Y when the picture is adjusted from dark to bright
[7:0]	RO	reserved	Reserved

ISP_VPDCIPOSGAIN0

ISP_VPDCIPOSGAIN0 is DCI adjustment unit gain register 0 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C38	ISP_VPDCIPOSGAIN0	0x0234_5678

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainpos_cbcr0				dci_gainpos_cbcr1				dci_gainpos_cbcr2				dci_gainpos_cbcr3				dci_gainpos_cbcr4				dci_gainpos_cbcr5				dci_gainpos_cbcr6				dci_gainpos_cbcr7			
Reset	0	0	0	0	0	0	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1	1	0	0	0

Bits	Access	Name	Description
[31:28]	RW	dci_gainpos_cbcr0	Chrominance compensation gain of threshold 0 when the picture is adjusted from dark to bright
[27:24]	RW	dci_gainpos_cbcr1	Chrominance compensation gain of threshold 1 when the picture is adjusted from dark to bright
[23:20]	RW	dci_gainpos_cbcr2	Chrominance compensation gain of threshold 2 when the picture is adjusted from dark to bright
[19:16]	RW	dci_gainpos_cbcr3	Chrominance compensation gain of threshold 3 when the picture is adjusted from dark to bright
[15:12]	RW	dci_gainpos_cbcr4	Chrominance compensation gain of threshold 4 when the picture is adjusted from dark to bright

[11:8]	RW	dci_gainpos_cbcr5	Chrominance compensation gain of threshold 5 when the picture is adjusted from dark to bright
[7:4]	RW	dci_gainpos_cbcr6	Chrominance compensation gain of threshold 6 when the picture is adjusted from dark to bright
[3:0]	RW	dci_gainpos_cbcr7	Chrominance compensation gain of threshold 7 when the picture is adjusted from dark to bright

ISP_VPDCIPOSGAIN1

ISP_VPDCIPOSGAIN1 is DCI adjustment unit gain register 1 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C3C	ISP_VPDCIPOSGAIN1	0x9000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainpos_cbcr8				reserved																											
Reset	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	dci_gainpos_cbcr8	Chrominance compensation gain of threshold 8 when the picture is adjusted from dark to bright
[27:0]	RO	reserved	Reserved

ISP_VPDCIPOSSLP0

ISP_VPDCIPOSSLP0 is DCI adjustment unit slope register 0 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C40	ISP_VPDCIPOSSLP0	0x0641_9064

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainpos_slp0												dci_gainpos_slp1								dci_gainpos_slp2										reserved	
Reset	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	1	0	0	1	0	0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp0	Slope of region 1 when the picture is adjusted from dark to bright, 10-bit signed number
[21:12]	RW	dci_gainpos_slp1	Slope of region 2 when the picture is adjusted from dark to bright, 10-bit signed number

[11:2]	RW	dci_gainpos_slp2	Slope of region 3 when the picture is adjusted from dark to bright, 10-bit signed number
[1:0]	RO	reserved	Reserved

ISP_VPDCIPOSSLP1

ISP_VPDCIPOSSLP1 is DCI adjustment unit slope register 1 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C44	ISP_VPDCIPOSSLP1	0x0641_9064

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp3		dci_gainpos_slp4		dci_gainpos_slp5			reserved
Reset	0 0 0 0	0 1 1 0	0 1 0 0	0 0 0 1	1 0 0 1	0 0 0 0	0 1 1 0	0 1 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp3	Slope of region 4 when the picture is adjusted from dark to bright, 10-bit signed number
[21:12]	RW	dci_gainpos_slp4	Slope of region 5 when the picture is adjusted from dark to bright, 10-bit signed number
[11:2]	RW	dci_gainpos_slp5	Slope of region 6 when the picture is adjusted from dark to bright, 10-bit signed number
[1:0]	RO	reserved	Reserved

ISP_VPDCIPOSSLP2

ISP_VPDCIPOSSLP2 is DCI adjustment unit slope register 2 during positive adjustment.

Offset Address	Register Name	Total Reset Value
0x51C48	ISP_VPDCIPOSSLP2	0x0140_1000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainpos_slp6		dci_gainpos_slp7		reserved			
Reset	0 0 0 0	0 0 0 1	0 1 0 0	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainpos_slp6	Slope of region 7 when the picture is adjusted from dark to bright, 10-bit signed number

[21:12]	RW	dci_gainpos_slp7	Slope of region 8 when the picture is adjusted from dark to bright, 10-bit signed number
[11:0]	RO	reserved	Reserved

ISP_VPDCINEGTHR0

ISP_VPDCINEGTHR0 is DCI adjustment unit threshold register 0 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C4C	ISP_VPDCINEGTHR0	0x1E32_465A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainneg_thr1								dci_gainneg_thr2								dci_gainneg_thr3								dci_gainneg_thr4							
Reset	0	0	0	1	1	1	1	0	0	0	1	1	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr1	Threshold 1 for luminance Y when the picture is adjusted from bright to dark
[23:16]	RW	dci_gainneg_thr2	Threshold 2 for luminance Y when the picture is adjusted from bright to dark
[15:8]	RW	dci_gainneg_thr3	Threshold 3 for luminance Y when the picture is adjusted from bright to dark
[7:0]	RW	dci_gainneg_thr4	Threshold 4 for luminance Y when the picture is adjusted from bright to dark

ISP_VPDCINEGTHR1

ISP_VPDCINEGTHR1 is DCI adjustment unit threshold register 1 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C50	ISP_VPDCINEGTHR1	0x8296_AA00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainneg_thr5								dci_gainneg_thr6								dci_gainneg_thr7								reserved							
Reset	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	dci_gainneg_thr5	Threshold 5 for luminance Y when the picture is adjusted from bright to dark

[23:16]	RW	dci_gainneg_thr6	Threshold 6 for luminance Y when the picture is adjusted from bright to dark
[15:8]	RW	dci_gainneg_thr7	Threshold 7 for luminance Y when the picture is adjusted from bright to dark
[7:0]	RO	reserved	Reserved

ISP_VPDCINEGGAIN0

ISP_VPDCINEGGAIN0 is DCI adjustment unit gain register 0 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C54	ISP_VPDCINEGGAIN0	0x0123_3456

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_cbcr0	dci_gainneg_cbcr1	dci_gainneg_cbcr2	dci_gainneg_cbcr3	dci_gainneg_cbcr4	dci_gainneg_cbcr5	dci_gainneg_cbcr6	dci_gainneg_cbcr7
Reset	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr0	Chrominance compensation gain of threshold 0 when the picture is adjusted from bright to dark
[27:24]	RW	dci_gainneg_cbcr1	Chrominance compensation gain of threshold 1 when the picture is adjusted from bright to dark
[23:20]	RW	dci_gainneg_cbcr2	Chrominance compensation gain of threshold 2 when the picture is adjusted from bright to dark
[19:16]	RW	dci_gainneg_cbcr3	Chrominance compensation gain of threshold 3 when the picture is adjusted from bright to dark
[15:12]	RW	dci_gainneg_cbcr4	Chrominance compensation gain of threshold 4 when the picture is adjusted from bright to dark
[11:8]	RW	dci_gainneg_cbcr5	Chrominance compensation gain of threshold 5 when the picture is adjusted from bright to dark
[7:4]	RW	dci_gainneg_cbcr6	Chrominance compensation gain of threshold 6 when the picture is adjusted from bright to dark
[3:0]	RW	dci_gainneg_cbcr7	Chrominance compensation gain of threshold 7 when the picture is adjusted from bright to dark

ISP_VPDCINEGGAIN1

ISP_VPDCINEGGAIN1 is DCI adjustment unit gain register 1 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C58	ISP_VPDCINEGGAIN1	0x6000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainneg_cbcr8				reserved																											
Reset	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	dci_gainneg_cbcr8	Chrominance compensation gain of threshold 8 when the picture is adjusted from bright to dark
[27:0]	RO	reserved	Reserved

ISP_VPDCINEGSLP0

ISP_VPDCINEGSLP0 is DCI adjustment unit slope register 0 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C5C	ISP_VPDCINEGSLP0	0x0200_C030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dci_gainneg_slp0												dci_gainneg_slp1								dci_gainneg_slp2										reserved	
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp0	Slope of region 1 when the picture is adjusted from bright to dark, 10-bit signed number
[21:12]	RW	dci_gainneg_slp1	Slope of region 2 when the picture is adjusted from bright to dark, 10-bit signed number
[11:2]	RW	dci_gainneg_slp2	Slope of region 3 when the picture is adjusted from bright to dark, 10-bit signed number
[1:0]	RO	reserved	Reserved

ISP_VPDCINEGSLP1

ISP_VPDCINEGSLP1 is DCI adjustment unit slope register 1 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C60	ISP_VPDCINEGSLP1	0x0000_6030

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_slp3			dci_gainneg_slp4		dci_gainneg_slp5		reserved
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 0	0 0 0 0	0 0 1 1	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp3	Slope of region 4 when the picture is adjusted from bright to dark, 10-bit signed number
[21:12]	RW	dci_gainneg_slp4	Slope of region 5 when the picture is adjusted from bright to dark, 10-bit signed number
[11:2]	RW	dci_gainneg_slp5	Slope of region 6 when the picture is adjusted from bright to dark, 10-bit signed number
[1:0]	RO	reserved	Reserved

ISP_VPDCINEGSLP2

ISP_VPDCINEGSLP2 is DCI adjustment unit slope register 2 during negative adjustment.

Offset Address	Register Name	Total Reset Value
0x51C64	ISP_VPDCINEGSLP2	0x0300_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dci_gainneg_slp6			dci_gainneg_slp7		reserved		
Reset	0 0 0 0	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RW	dci_gainneg_slp6	Slope of region 7 when the picture is adjusted from bright to dark, 10-bit signed number
[21:12]	RW	dci_gainneg_slp7	Slope of region 8 when the picture is adjusted from bright to dark, 10-bit signed number
[11:0]	RO	reserved	Reserved

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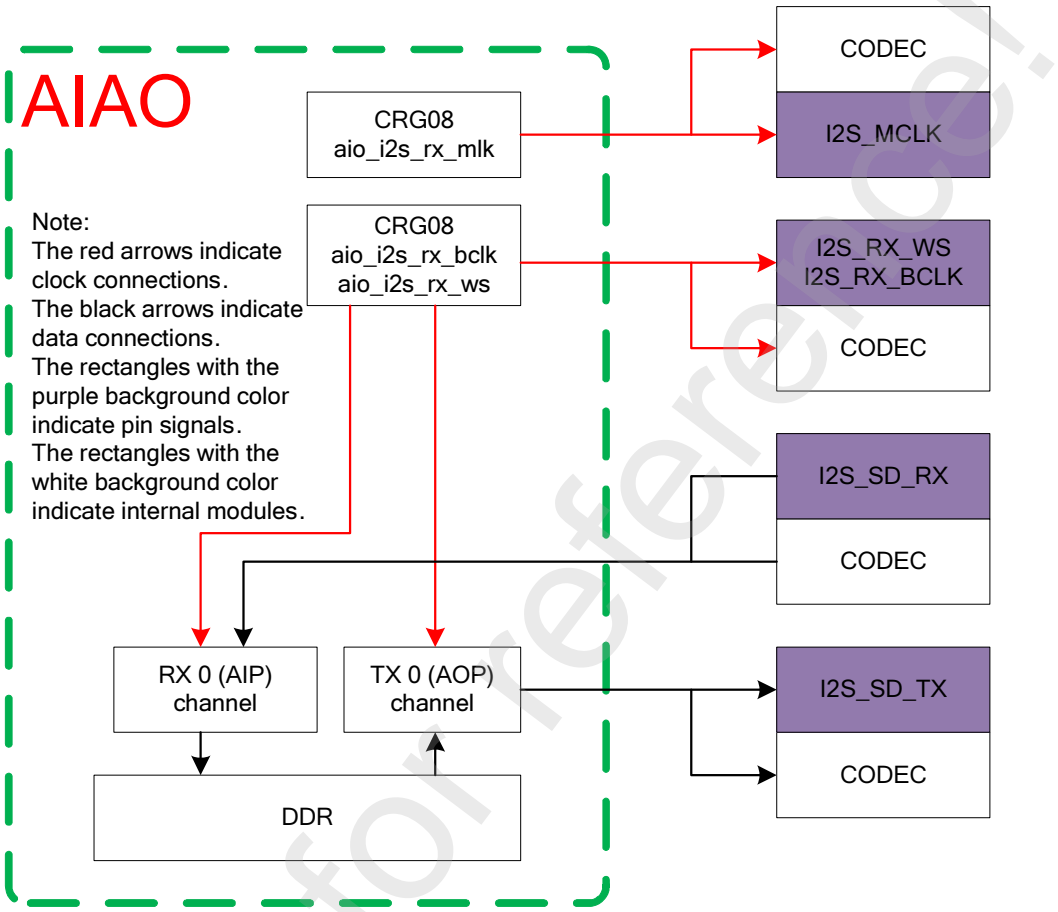
11 Audio Interfaces

11.1 AIAO

11.1.1 Overview

The audio input/output (AIAO) interface is used to connect to the off-chip audio coder/decoder (CODEC) to input and output audio data, implementing the recording, talkback, and playback functions. Hi3516C V300 has an integrated AIAO interface that includes one audio input port (AIP) and one audio output port (AOP) and supported stereo inputs and outputs. Figure 11-1 shows the block diagram of the Hi3516C V300 AIAO.

Figure 11-1 Block diagram of the Hi3516C V300 AIAO



11.1.2 Features

The AIAO interface supports the pulse code modulation (PCM) mode and inter-IC sound (I^2S) mode. The AIAO interface reads data from or writes data to the memory in DMA mode.

PCM Interfaces

The PCM interfaces have the following features:

- Transmit or receive the 16-bit linear PCM code from a channel in master mode.
- Support only short pulse sync signals in frame sync signals (the duration of those sync signals is one clock cycle). The PCM interfaces can work in both the standard mode and customized mode.
- Separately enable or disable input (AIP) and output (AOP).
- Support DMA for inputs (AIP) and outputs (AOP). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

I²S Interfaces

The I^2S interfaces have the following features:

- Transmit or receive 16- or 24-bit stereo data in master mode.
- Support the sampling rate ranging from 8 kHz to 192 kHz.
- Separately enables or disables input (AIP) and output (AOP).
- Support DMA for inputs (AIP) and outputs (AOP). The AIAO reads data from and writes data to a cyclic buffer created by using software. The cyclic buffer size and threshold are adjustable.

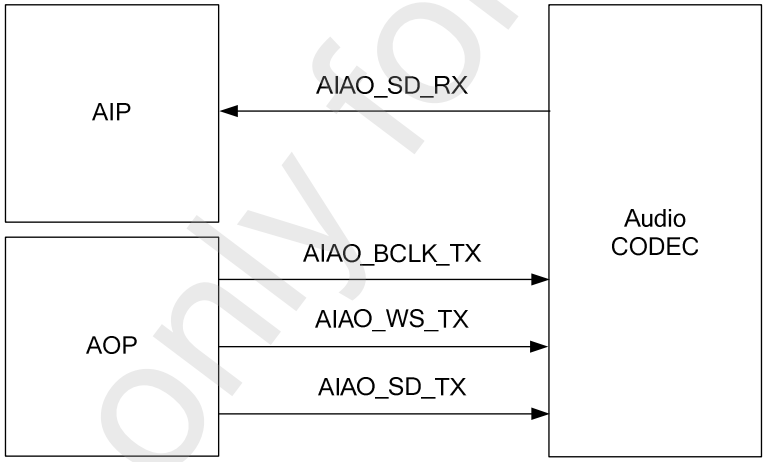
11.1.3 Function Description

Typical Application

Hi3516C V300 provides one AIP and one AOP. Their functions are as follows:

- The AIP supports data reception in PCM or I^2S mode.
- The AOP supports music playback in PCM or I^2S mode.
- The AIP supports interconnection with the internal audio CODEC in I^2S master mode or interconnection with the external analog-to-digital converter (ADC) in PCM/I^2S master mode to implement voice sampling.
- The AOP supports interconnection with the internal audio CODEC in I^2S master mode or interconnection with the external digital-to-analog converter (DAC) in PCM/I^2S master mode to implement music playback.

Figure 11-2 Connection diagram over the 4-line I^2S/PCM interface in master mode



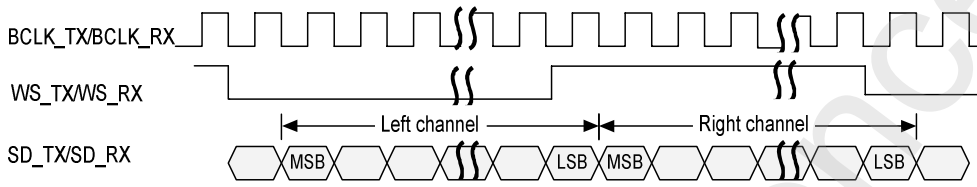
Function Principle

The AIP receives the audio data after the analog-to-digital (AD) conversion performed by the internal audio CODEC or external ADC over the I^2S or PCM interface, and stores the data into the cyclic FIFO created for the AIP. Then, the CPU fetches the data and stores it. In this way, audio recording is complete.

AOP reads audio data from the cyclic buffer and sends the audio data to the interconnected audio CODEC over the I^2S or PCM interface at a specified sampling rate. The internal audio CODEC or external ADC performs digital-to-analog (DA) conversion on the audio data and plays the audio.

Figure 11-3 shows the supported I²S interface timing when the external I²S interface is connected.

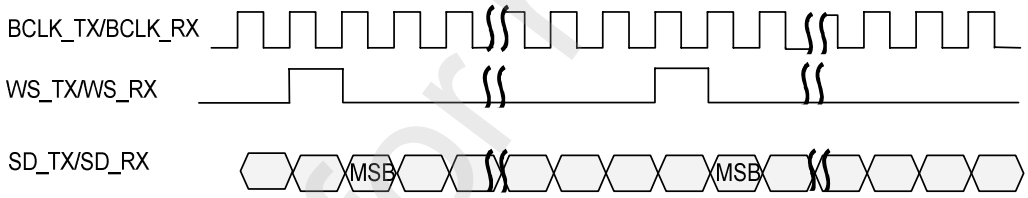
Figure 11-3 I²S interface timing



The I²S interface transmits data in most significant bit (MSB) first mode. Data and WS signals are sent at the falling edge of the BCLK and sampled at the rising edge of the BCLK. The data is delayed by one BCLK cycle compared with WS signals.

When the external PCM interface is connected, the PCM standard timing and data left-aligned timing are supported. Figure 11-4 shows the timing of the PCM interface in standard mode.

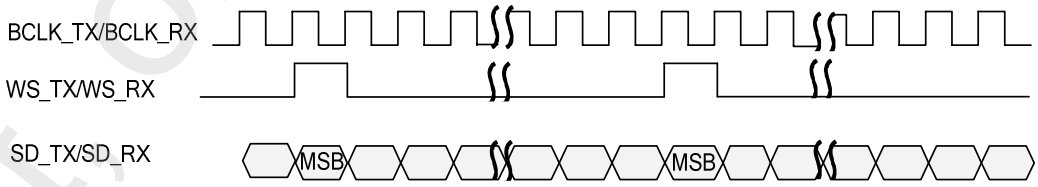
Figure 11-4 Timing of the PCM interface in standard mode



The PCM interface transmits data in MSB first mode. Data and WS signals are sent at the rising edge of the BCLK and sampled at the falling edge of the BCLK. In standard mode, the data is delayed by one BCLK cycle compared with WS signals.

Figure 11-5 shows the timing of the PCM interface in customized mode.

Figure 11-5 Timing of the PCM interface in customized mode



In customized mode, data and WS pulses start to be sent when they are in the same cycle.

11.1.4 Operating Mode

Channel Multiplexing Configuration

As there is only one AIP/AOP, the internal audio CODEC and the external ADC/DAC connected to the I²S/PCM interface cannot work simultaneously.

If the system MISC registers i2s_pad_enable and audio_enable are set to 1 and 0 respectively, the AIP/AOP connects to the external I^2S/PCM pin. If i2s_pad_enable and audio_enable are set to 0 and 1 respectively, the AIP/AOP connects to the internal audio CODEC.

Clock Gating and Configuration

Before enabling the AIAO interface for audio recording or playback, you must enable clock gating of the related channels (AIP/AOP). To enable clock gating, perform the following steps:

Step 1 Set the system CRG register PERI_CRG35 to 0x2 to deassert the reset on the AIAO and enable clock gating.

Step 2 Configure the AIAO registers I2S_CRG_CFG0_08 and I2S_CRG_CFG1_08 to select appropriate frequency division coefficients. Note that the MCLK/WS frequency division ratio in the i2s1_fs_sel register for the audio CODEC must be consistent with the configuration in this step when the internal audio CODEC is used.

----End

Soft Reset

The two internal channels (AIP and AOP) of the AIAO module support separate soft reset. When the AIAO module is reset, the two channels are reset at the same time.

Recording Process

The following example assumes that the audio channels are stereo channels in I^2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a 1188 MHz clock, and the AIAO clock of the system controller is enabled. To record data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_08 to 0x152EF0 to set the MCLK output frequency to 12.288 MHz.

Step 2 Set I2S_CRG_CFG1_08 to 0x00000133 to enable the clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set RX_IF_ATTRI to 0xE4800014 to set the operating mode of the RX channel to I^2S stereo mode and sampling precision to 16 bits.

Step 4 Set RX_BUFF_SADDR to the start address of the allocated DDR (for example, 0x00000100), set RX_BUFF_SIZE to the size of the allocated DDR buffer (for example, 0x0000f000), set RX_BUFF_WPTR and RX_BUFF_RPTR to 0x0 to initialize the write and read pointers, and set RX_TRANS_SIZE to the data transfer length (for example, 0x00000f00).

Step 5 Configure RX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set RX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 6 Set RX_DSP_CTRL to 0x10000000 to enable the RX channel. Then the RX channel starts recording.

Step 7 Read RX_BUFF_WPTR and RX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that data is fetched before the cyclic buffer is full and the updated read address for the cyclic buffer is written to RX_BUFF_RPTR. Otherwise, overflow occurs in the cyclic buffer and the audio is discontinuous.

Step 8 After recording, write 0x00000000 to RX_DSP_CTRL and query RX_DSP_CTRL until its value is 0x20000000, which indicates that the RX channel stops working.

----End

CAUTION

Configure the AIP clock before starting the AIP, ensuring that AIAO_BCLK_RX and AIAO_WS_RX are normal.

Playback Process

The following assumes that the audio channels are stereo channels in I^2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits, the AIAO PLL clock source is a 1188 MHz clock, and the AIAO clock of the system controller is enabled. To play data, perform the following steps:

Step 1 Set I2S_CRG_CFG0_08 to 0x152EF0 to set the MCLK output frequency to 12.288 MHz.

Step 2 Set I2S_CRG_CFG1_08 to 0x00000133 to enable the clock, set the BCLK to the divide-by-4 clock of the MCLK, and set the FCLK to the divide-by-64 clock of the BCLK. The FCLK is 48 kHz.

Step 3 Set TX_IF_ATTRI to 0xE4000014 to set the operating mode of the RX channel to I^2S stereo mode and sampling precision to 16 bits.

Step 4 Set TX_BUFF_SADDR to the start address for the allocated buffer (for example, 0x00000100), set TX_BUFF_SIZE to the size of the allocated buffer, set TX_BUFF_WPTR and TX_BUFF_RPTR to 0x0, and set TX_TRANS_SIZE to the data transfer length. For details, see step 5 in the "Recording Process" section.

Step 5 Configure TX_INT_ENA to enable the corresponding interrupt of the RX channel as required. For example, set TX_INT_ENA to 0x00000001 to enable the trans_int interrupt.

Step 6 Set TX_DSP_CTRL to 0x10000000 to enable the playback channel.

Step 7 Read TX_BUFF_WPTR and TX_BUFF_RPTR to check the empty/full status of the cyclic buffer and the valid data amount.

Ensure that new audio data is stuffed before the cyclic buffer is empty and the updated write address for the cyclic buffer is written to TX_BUFF_WPTR. Otherwise, an underflow occurs in the cyclic buffer and the audio is discontinuous.

Step 8 After playback, write 0x00000000 to TX_DSP_CTRL to stop the playback channel and query TX_DSP_CTRL until its value is 0x20000000, which indicates that the playback channel stops working.

----End

CAUTION

- Configure AOP clock before starting AOP, ensuring that AIAO_BCLK_RX and AIAO_WS_RX are normal.
- Ensure that the minimum available space of the AOP cyclic buffer is 32 bytes when writing data to the cyclic buffer and updating TX_BUFF_WPTR.

11.1.5 Register Summary

Table 11-1 describes AIAO registers.

Table 11-1 Summary of AIAO registers (base address: 0x1131_0000)

Offset Address	Register	Description	Page
0x0000	AIAO_INT_ENA	AIAO interrupt enable register	11-8
0x0004	AIAO_INT_STATUS	AIAO interrupt status register	11-9
0x0008	AIAO_INT_RAW	AIAO raw interrupt register	11-10
0x0104	I2S_CRG_CFG1_00	I^2S00 CRG configuration register 1	11-10
0x0140	I2S_CRG_CFG0_08	I^2S08 CRG configuration register 0	11-10
0x0144	I2S_CRG_CFG1_08	I^2S08 CRG configuration register 1	11-11
0x1000	RX_IF_ATTRI	Interface attribute configuration register for the RX channel	11-12
0x1004	RX_DSP_CTRL	RX channel control register	11-13
0x1080	RX_BUFF_SADDR	DDR buffer start address register for the RX channel	11-14
0x1084	RX_BUFF_SIZE	DDR buffer size register for the RX channel	11-15
0x1088	RX_BUFF_WPTR	DDR buffer write address register for the RX channel	11-15
0x108C	RX_BUFF_RPTR	DDR buffer read address register for the RX channel	11-15
0x1090	RX_BUFF_ALFULL_TH	DDR buffer almost full threshold register for the RX channel	11-16
0x1094	RX_TRANS_SIZE	Data transfer length register for the RX channel	11-16
0x10A0	RX_INT_ENA	Interrupt enable register for the RX channel	11-17
0x10A4	RX_INT_RAW	Raw interrupt register for the RX channel	11-18

Offset Address	Register	Description	Page
0x10A8	RX_INT_STATUS	Interrupt status register for the RX channel	11-19
0x10AC	RX_INT_CLR	Interrupt clear register for the RX channel	11-20
0x2000	TX_IF_ATTRI	Interface attribute configuration register for the TX channel	11-21
0x2004	TX_DSP_CTRL	TX channel control register	11-22
0x2080	TX_BUFF_SADDR	DDR buffer start address register for the TX channel	11-24
0x2084	TX_BUFF_SIZE	DDR buffer size register for the TX channel	11-24
0x2088	TX_BUFF_WPTR	DDR buffer write address register for the TX channel	11-25
0x208C	TX_BUFF_RPTR	DDR buffer read address register for the TX channel	11-25
0x2090	TX_BUFF_ALEMPTY_TH	DDR buffer almost empty threshold register for the TX channel	11-26
0x2094	TX_TRANS_SIZE	Data transfer length register for the TX channel	11-26
0x20A0	TX_INT_ENA	Interrupt enable register for the TX channel	11-27
0x20A4	TX_INT_RAW	Raw interrupt register for the TX channel	11-28
0x20A8	TX_INT_STATUS	Interrupt status register for the TX channel	11-29
0x20AC	TX_INT_CLR	Interrupt clear register for the TX channel	11-31

11.1.6 Register Description

AIAO_INT_ENA

AIAO_INT_ENA is an AIAO interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0000	AIAO_INT_ENA	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			tx_ch0_int_ena	reserved			rx_ch0_int_ena

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	reserved	Reserved
[16]	RW	tx_ch0_int_ena	TX channel 0 interrupt enable 0: disabled 1: enabled
[15:1]	RW	reserved	Reserved
[0]	RW	rx_ch0_int_ena	RX channel 0 interrupt enable 0: disabled 1: enabled

AIAO_INT_STATUS

AIAO_INT_STATUS is an AIAO interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0004	AIAO_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															tx_ch0_int_status	reserved															rx_ch0_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	tx_ch0_int_status	Interrupt status of TX channel 0 0: No interrupt is generated. 1: An interrupt is generated.
[15:1]	RO	reserved	Reserved
[0]	RO	rx_ch0_int_status	Interrupt status of RX channel 0 0: No interrupt is generated. 1: An interrupt is generated.

AIAO_INT_RAW

AIAO_INT_RAW is an AIAO raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x0008	AIAO_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															tx_ch0_int_raw	reserved															rx_ch0_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	tx_ch0_int_raw	Raw interrupt of TX channel 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[15:1]	RO	reserved	Reserved
[0]	RO	rx_ch0_int_raw	Raw interrupt of RX channel 0 0: No raw interrupt is generated. 1: A raw interrupt is generated.

I2S_CRG_CFG1_00

I2S_CRG_CFG1_00 is I^2S00 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0104	I2S_CRG_CFG1_00	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						aiao_srst_req	reserved								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved

[9]	RW	aiao_srst_req	Independent soft reset request of the RX 0 channel 0: deassert reset 1: reset
[8:0]	RO	reserved	Reserved

I2S_CRG_CFG0_08

I2S_CRG_CFG0_08 is I^{2}S08 CRG configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0140	I2S_CRG_CFG0_08	0x00AA_AAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								aiao_mclk_div																							
Reset	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26:0]	RW	aiao_mclk_div	Configured value of the frequency division clock of the MCLK. The configured value is calculated as follows: (Target MCLK frequency/PLL frequency of the MCLK clock source) x 2^27. For details about the PLL frequency of the MCLK clock source, see section 3.2 "Clock" in chapter 3 "System" in the *Hi3516C V300 Professional HD IP Camera SoC Data Sheet*.

I2S_CRG_CFG1_08

I2S_CRG_CFG1_08 is I^{2}S08 CRG configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0144	I2S_CRG_CFG1_08	0x0000_0131

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						aiao_srst_req	aiao_cken	reserved	aiao_fsclk_div			aiao_bclk_div			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved

[9]	RW	aiao_srst_req	Independent soft reset request of the TX 0 channel 0: deassert reset 1: reset
[8]	RW	aiao_cken	MCLK/BCLK/WS clock gating for CRG00 0: disabled 1: enabled
[7]	RO	reserved	Reserved
[6:4]	RW	aiao_fsclk_div	Frequency division relationship between the bit clock BCLK and the sampling clock FS 000: The FS is obtained by dividing the BCLK by 16. 001: The FS is obtained by dividing the BCLK by 32. 010: The FS is obtained by dividing the BCLK by 48. 011: The FS is obtained by dividing the BCLK by 64. 100: The FS is obtained by dividing the BCLK by 128. 101: The FS is obtained by dividing the BCLK by 256. Other values: The FS is obtained by dividing the BCLK by 8.
[3:0]	RW	aiao_bclk_div	Frequency division relationship between the main clock MCLK and the bit clock BCLK 0x0: The BCLK is obtained by dividing the MCLK by 1. 0x1: The BCLK is obtained by dividing the MCLK by 3. 0x2: The BCLK is obtained by dividing the MCLK by 2. 0x3: The BCLK is obtained by dividing the MCLK by 4. 0x4: The BCLK is obtained by dividing the MCLK by 6. 0x5: The BCLK is obtained by dividing the MCLK by 8. 0x6: The BCLK is obtained by dividing the MCLK by 12. 0x7: The BCLK is obtained by dividing the MCLK by 16. 0x8: The BCLK is obtained by dividing the MCLK by 24. 0x9: The BCLK is obtained by dividing the MCLK by 32. 0xA: The BCLK is obtained by dividing the MCLK by 48. 0xB: The BCLK is obtained by dividing the MCLK by 64. Other values: The BCLK is obtained by dividing the MCLK by 8.

RX_IF_ATTRI

RX_IF_ATTRI is an interface attribute configuration register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1000	RX_IF_ATTRI	0xE400_0004

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19	18 17 16	15 14 13 12	11 10 9 8	7	6 5 4	3 2	1 0
Name	reserved		rx_sd_source_sel	reserved	rx_trackmode	rx_sd_offset		reserved	rx_ch_num	rx_i2s_precision	rx_mode
Reset	1 1 1 0	0 1 0 0	0 0 0 0	0	0 0 0	0 0 0 0	0 0 0 0	0	0 0 0	0 1	0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:20]	RW	rx_sd_source_sel	This bit is set to 0x1000 in normal mode.
[19]	RO	reserved	Reserved
[18:16]	RW	rx_trackmode	Audio-left and audio-right channel mode in I^2S mode 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. **NOTE** rx_trackmode is still valid in 1-channel RX mode.
[15:8]	RW	rx_sd_offset	PCM timing mode 0x0: left-aligned mode 0x1: standard mode Other values: reserved
[7]	RW	reserved	Reserved
[6:4]	RW	rx_ch_num	Number of RX channels 00: 1 01: 2 Other values: reserved

[3:2]	RW	rx_i2s_precision	Data sampling precision I^{2}S mode: 01: 16 bits 10: 24 bits Other values: reserved PCM mode: 01: 16 bits Other values: reserved
[1:0]	RW	rx_mode	Interface mode of the RX channel 00: I^{2}S mode 01: PCM mode Other values: reserved

RX_DSP_CTRL

RX_DSP_CTRL is an RX channel control register.

Offset Address	Register Name	Total Reset Value
0x1004	RX_DSP_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		rx_disable_done	rx_enable	bypass_en	reserved																										
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RO	rx_disable_done	RX channel disable completion identifier 0: not complete 0: complete
[28]	RW	rx_enable	RX channel start/stop control bit 0: stop 1: start
[27]	RW	bypass_en	Data processing disable bit. The control function still takes effect after data processing is disabled. 0: Data processing is implemented normally. 1: Operations such as trackmode are not implemented.

[26:0]	RO	reserved	Reserved

RX_BUFF_SADDR

RX_BUFF_SADDR is a DDR buffer start address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1080	RX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	rx_buff_saddr	Start address for the DDR buffer of RX channel 0. Its unit is byte. NOTE The start address must be 128x8-bit-aligned.

RX_BUFF_SIZE

RX_BUFF_SIZE is a DDR buffer size register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1084	RX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_size	DDR buffer size of the RX channel. Its unit is byte. NOTE The buffer size must be an integral multiple of 128 bytes.

RX_BUFF_WPTR

RX_BUFF_WPTR is a DDR buffer write address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1088	RX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_wptr	Write address for the DDR buffer of the RX channel. Its unit is byte. NOTE • The write address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The write address must be 128x2-bit-aligned.

RX_BUFF_RPTR

RX_BUFF_RPTR is a DDR buffer read address register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x108C	RX_BUFF_RPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								rx_buff_rptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_rptr	Read address for the DDR buffer of the RX channel. Its unit is byte. NOTE • The read address in the RX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The software operation is performed by byte, and the hardware operation is performed based on 128 x 2-bit alignment.

RX_BUFF_ALFULL_TH

RX_BUFF_ALFULL_TH is a DDR buffer almost full threshold register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x1090	RX_BUFF_ALFULL_TH	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		rx_buff_alfull_th					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_buff_alfull_th	Almost full threshold for the DDR buffer of the RX channel. Its unit is byte. If the available space of the DDR buffer is below the almost full threshold, the almost full raw interrupt is generated. **NOTE** If the rx_alfull_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x40.

RX_TRANS_SIZE

RX_TRANS_SIZE is data transfer length register for the RX interrupt.

Offset Address	Register Name	Total Reset Value
0x1094	RX_TRANS_SIZE	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		rx_trans_size					
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	rx_trans_size	After the RX channel receives the audio data with the length of rx_trans_size (in byte), a transfer completion interrupt is generated.

RX_INT_ENA

RX_INT_ENA is an interrupt enable register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A0	RX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_if_full_lost_int_ena	reserved	rx_stop_int_ena	reserved	rx_bfifo_full_int_ena	rx_alfull_int_ena	rx_full_int_ena	rx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	rx_if_full_lost_int_ena	Interface data full loss raw interrupt enable for the RX channel 0: disabled 1: enabled
[6]	RO	reserved	Reserved
[5]	RW	rx_stop_int_ena	Stop interrupt enable for the RX channel 0: disabled 1: enabled
[4]	RO	reserved	Reserved
[3]	RW	rx_bfifo_full_int_ena	Bus fifo overflow interrupt enable for the RX channel 0: disabled 1: enabled
[2]	RW	rx_alfull_int_ena	DDR buffer almost full interrupt enable for the RX channel 0: disabled 1: enabled
[1]	RW	rx_full_int_ena	DDR buffer full interrupt for the RX channel 0: disabled 1: enabled
[0]	RW	rx_trans_int_ena	Transfer completion interrupt enable for the RX channel 0: disabled 1: enabled

RX_INT_RAW

RX_INT_RAW is a raw interrupt register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A4	RX_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_if_full_lost_int_raw	reserved	rx_stop_int_raw	reserved	rx_bfifo_full_int_raw	rx_alfull_int_raw	rx_full_int_raw	rx_trans_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	rx_if_full_lost_int_raw	Data full lost raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	reserved	Reserved
[5]	RO	rx_stop_int_raw	Stop raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RO	reserved	Reserved
[3]	RO	rx_bfifo_full_int_raw	Bus FIFO overflow raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[2]	RO	rx_alfull_int_raw	DDR buffer almost full raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	rx_full_int_raw	DDR buffer full raw interrupt of the RX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	rx_trans_int_raw	Transfer completion raw interrupt of the RX interrupt 0: No raw interrupt is generated. 1: A raw interrupt is generated.

RX_INT_STATUS

RX_INT_STATUS is an interrupt status register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10A8	RX_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_if_full_lost_int_status	reserved	rx_stop_int_status	reserved	rx_bfifo_full_int_status	rx_alfull_int_status	rx_full_int_status	rx_trans_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_if_full_lost_int_status	Status of the data full loss interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	reserved	Reserved
[5]	RO	rx_stop_int_status	Status of the stop interrupt of the RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	reserved	Reserved
[3]	RO	rx_bfifo_full_int_status	Status of the bus fifo overflow interrupt of the RC channel 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	rx_alfull_int_status	Status of the DDR buffer almost full interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	rx_full_int_status	Status of the DDR buffer full interrupt of the RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	rx_trans_int_status	Status of the transfer completion interrupt of the RX channel 0: No interrupt is generated. 1: An interrupt is generated.

RX_INT_CLR

RX_INT_CLR is an interrupt clear register for the RX channel.

Offset Address	Register Name	Total Reset Value
0x10AC	RX_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_if_full_lost_int_clear	reserved	rx_stop_int_clear	reserved	rx_bfifo_full_int_clear	rx_alfull_int_clear	rx_full_int_clear	rx_trans_int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	WC	tx_if_full_lost_int_clear	Data full loss interrupt clear for the TX channel 0: not cleared 1: cleared
[6]	RO	reserved	Reserved
[5]	WC	rx_stop_int_clear	Stop interrupt clear for the RX channel 0: not cleared 1: cleared
[4]	RO	reserved	Reserved
[3]	WC	rx_bfifo_full_int_clear	Bus fifo overflow interrupt clear for the RX channel 0: not cleared 1: cleared
[2]	WC	rx_alfull_int_clear	DDR buffer almost full interrupt clear for the RX channel 0: not cleared 1: cleared
[1]	WC	rx_full_int_clear	DDR buffer full interrupt clear for the RX channel 0: not cleared 1: cleared
[0]	WO	rx_trans_int_clear	Transfer completion interrupt clear for the RX interrupt 0: not cleared 1: cleared

TX_IF_ATTRI

TX_IF_ATTRI is an interface attribute configuration register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2000	TX_IF_ATTRI	0xE400_0004

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			tx_trackmode	tx_sd_offset		reserved	tx_ch_num	tx_i2s_precision	tx_mode
Reset	1 1 1 0	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18:16]	RW	tx_trackmode	Audio-left and audio-right channel mode in I^2S mode 000: The sound is not processed. 001: The sounds in two channels are audio-left channel sounds. 010: The sounds in two channels are audio-right channel sounds. 011: The sounds in two channels are exchanged. 100: The sounds of two channels are added and then output. 101: The audio-left channel is muted, and the sound of the audio-right channel is from the original audio-right channel. 110: The audio-right channel is muted, and the sound of the audio-left channel is from the original audio-left channel. 111: The audio-left and audio-right channels are muted. **NOTE** tx_trackmode is still valid in 1-channel TX mode.
[15:8]	RW	tx_sd_offset	PCM timing mode 0x0: left-aligned mode 0x1: standard mode Other values: reserved
[7:6]	RO	reserved	Reserved
[5:4]	RW	tx_ch_num	Select of the TX channel 00: Data is transmitted by one audio channel. 01: Data is transmitted by two audio channels as stereo. Other values: reserved

[3:2]	RW	tx_i2s_precision	Data sampling precision I^{2}S mode: 01: 16 bits 10: 24 bits Other values: reserved PCM mode: 01: 16 bits Other values: reserved
[1:0]	RW	tx_mode	Interface mode of the TX channel 00: I^{2}S mode 01: PCM mode Other values: reserved

TX_DSP_CTRL

TX_DSP_CTRL is a TX channel control register.

Offset Address	Register Name	Total Reset Value
0x2004	TX_DSP_CTRL	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		tx_disable_done	tx_enable	bypass_en	reserved			fade_out_rate				fade_in_rate				reserved	volume							reserved						mute_fade_en	mute_en
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29]	RO	tx_disable_done	TX channel disable completion identifier 0: not complete 1: complete
[28]	RW	tx_enable	TX channel start/stop control bit 0: stop 1: start

[27]	RW	bypass_en	Data processing disable bit. The control function still takes effect after data processing is disabled. 0: Data processing is implemented normally. 1: Operations such as trackmode and volume processing are not implemented.
[26:24]	RO	reserved	Reserved
[23:20]	RW	fade_out_rate	Fade-out rate 0x0: The fade-out rate changes every one sampling point. 0x1: The fade-out rate changes every two sampling points. 0x2: The fade-out rate changes every four sampling points. 0x3: The fade-out rate changes every eight sampling points. 0x4: The fade-out rate changes every 16 sampling points. 0x5: The fade-out rate changes every 32 sampling points. 0x6: The fade-out rate changes every 64 sampling points. 0x7: The fade-out rate changes every 128 sampling points. Other values: reserved
[19:16]	RW	fade_in_rate	Fade-in rate 0x0: The fade-in rate changes every one sampling point. 0x1: The fade-in rate changes every two sampling points. 0x2: The fade-in rate changes every four sampling points. 0x3: The fade-in rate changes every eight sampling points. 0x4: The fade-in rate changes every 16 sampling points. 0x5: The fade-in rate changes every 32 sampling points. 0x6: The fade-in rate changes every 64 sampling points. 0x7: The fade-in rate changes every 128 sampling points. Other values: reserved
[15]	RO	reserved	Reserved
[14:8]	RW	volume	Volume. The volume is incremented by 1 dB when the field value is incremented by 1. 0x00−0x28: mute 0x29: −80 dB 0x2A: −79 dB … 0x75: −4 dB 0x77: −2 dB 0x79: 0 dB 0x7B: +2 dB 0x7D: +4 dB 0x7F: +6 dB (maximum value)
[7:2]	RO	reserved	Reserved.

[1]	RW	mute_fade_en	Mute fade-in/fade-out control 0: disabled 1: enabled
[0]	RW	mute_en	Mute control 0: not muted 1: muted

TX_BUFF_SADDR

TX_BUFF_SADDR is a DDR buffer start address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2080	TX_BUFF_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tx_buff_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	tx_buff_saddr	Start address for the DDR buffer of the TX channel. Its unit is byte. **NOTE** The start address must be 128x8-bit-aligned.

TX_BUFF_SIZE

TX_BUFF_SIZE is a DDR buffer size register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2084	TX_BUFF_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_size	DDR buffer size of the TX channel. Its unit is byte. **NOTE** The buffer size must be an integral multiple of 128 bytes.

TX_BUFF_WPTR

TX_BUFF_WPTR is a DDR buffer write address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2088	TX_BUFF_WPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_wptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_wptr	Write address for the DDR buffer of the TX channel **NOTE** • The write address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The available space of the TX buffer must be greater than or equal to 128 bytes. • The software operation is performed by byte, and the hardware operation is performed by 128 x 2 bytes.

TX_BUFF_RPTR

TX_BUFF_RPTR is a DDR buffer read address register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x208C	TX_BUFF_RPTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_rptr																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_rptr	Read address for the DDR buffer of the TX channel **NOTE** • The read address in the TX direction is maintained by the logic and is the offset address relative to the start address for the DDR buffer. • The address must be 128x2-bit-aligned.

TX_BUFF_ALEMPTY_TH

TX_BUFF_ALEMPTY_TH is a DDR buffer almost empty threshold register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2090	TX_BUFF_ALEMPTY_TH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_buff_alempty_th																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_buff_alempty_th	Almost empty threshold for the DDR buffer of the TX channel. Its unit is byte. If the available space of the DDR buffer is below the almost empty threshold, the almost empty raw interrupt is generated. **NOTE** If the tx_alempty_int interrupt is used, the field value must be an integral multiple of 16 bytes and greater than or equal to 0x20.

TX_TRANS_SIZE

TX_TRANS_SIZE is a data transfer length register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x2094	TX_TRANS_SIZE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								tx_trans_size																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:0]	RW	tx_trans_size	After the TX channel transmits the audio data with the length of tx_trans_size (in byte), a transfer completion interrupt is generated.

TX_INT_ENA

TX_INT_ENA is an interrupt enable register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A0	TX_INT_ENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_ena	tx_mfade_int_ena	tx_stop_int_ena	tx_ififo_empty_int_ena	tx_bfifo_empty_int_ena	tx_alempty_int_ena	tx_empty_int_ena	tx_trans_int_ena
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	tx_dat_break_int_ena	Interface data break interrupt enable for the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RW	tx_mfade_int_ena	Mute fade-in/fade-output completion interrupt enable for the TX channel 0: disabled 1: enabled
[5]	RW	tx_stop_int_ena	Stop interrupt enable for the TX channel 0: disabled 1: enabled
[4]	RW	tx_ififo_empty_int_ena	Interface fifo underflow interrupt enable for the TX channel 0: disabled 1: enabled
[3]	RW	tx_bfifo_empty_int_ena	Bus fifo underflow interrupt enable for the TX channel 0: disabled 1: enabled
[2]	RW	tx_alempty_int_ena	DDR buffer almost empty interrupt enable for the TX channel 0: disabled 1: enabled
[1]	RW	tx_empty_int_ena	DDR buffer empty interrupt for the TX channel 0: disabled 1: enabled

[0]	RW	tx_trans_int_ena	Transfer completion interrupt enable for the TX channel 0: disabled 1: enabled

TX_INT_RAW

TX_INT_RAW is a raw interrupt register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A4	TX_INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_raw	tx_mfade_int_raw	tx_stop_int_raw	tx_ififo_empty_int_raw	tx_bfifo_empty_int_raw	tx_alempty_int_raw	tx_empty_int_raw	tx_trans_int_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_raw	Interface data break raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[6]	RO	tx_mfade_int_raw	Mute fade-in/fade-output completion raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[5]	RO	tx_stop_int_raw	Stop raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[4]	RO	tx_ififo_empty_int_raw	Interface fifo underflow raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[3]	RO	tx_bfifo_empty_int_raw	Bus fifo underflow raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[2]	RO	tx_alempty_int_raw	DDR buffer almost empty raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[1]	RO	tx_empty_int_raw	DDR buffer empty raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.
[0]	RO	tx_trans_int_raw	Transfer completion raw interrupt of the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

TX_INT_STATUS

TX_INT_STATUS is an interrupt status register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20A8	TX_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_status	tx_mfade_int_status	tx_stop_int_status	tx_ififo_empty_int_status	tx_bfifo_empty_int_status	tx_alempty_int_status	tx_empty_int_status	tx_trans_int_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_status	Status of the interface data break interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	tx_mfade_int_status	Status of the mute fade-in/fade-output completion interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	tx_stop_int_status	Status of the stop interrupt of the TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.

[4]	RO	tx_ififo_empty_int_status	Status of the interface FIFO underflow interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	tx_bfifo_empty_int_status	Status of the bus FIFO underflow interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	tx_alempty_int_status	DDR buffer almost empty interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	tx_empty_int_status	Status of the DDR buffer empty interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	tx_trans_int_status	Status of the transfer completion interrupt of the TX channel 0: No interrupt is generated. 1: An interrupt is generated.

TX_INT_CLR

TX_INT_CLR is an interrupt clear register for the TX channel.

Offset Address	Register Name	Total Reset Value
0x20AC	TX_INT_CLR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_dat_break_int_clear	tx_mfade_int_clear	tx_stop_int_clear	tx_ififo_empty_int_clear	tx_bfifo_empty_int_clear	tx_alempty_int_clear	tx_empty_int_clear	tx_trans_int_clear
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RO	tx_dat_break_int_clear	Interface data break interrupt clear for the TX channel 0: No raw interrupt is generated. 1: A raw interrupt is generated.

[6]	WC	tx_mfade_int_clear	Mute fade-in/fade-output completion interrupt clear for the TX channel 0: not cleared 1: cleared
[5]	WC	tx_stop_int_clear	Stop interrupt clear for the TX channel 0: not cleared 1: cleared
[4]	WC	tx_ififo_empty_int_clear	Interface fifo underflow interrupt clear for the TX channel 0: not cleared 1: cleared
[3]	WC	tx_bfifo_empty_int_clear	Bus fifo underflow interrupt clear for the TX channel 0: not cleared 1: cleared
[2]	WC	tx_alempty_int_clear	DDR buffer almost empty interrupt clear for the TX channel 0: not cleared 1: cleared
[1]	WC	tx_empty_int_clear	DDR buffer empty interrupt clear for the RX channel 0: not cleared 1: cleared
[0]	WC	tx_trans_int_clear	Transfer completion interrupt clear for the TX channel 0: not cleared 1: cleared

11.2 Audio CODEC

11.2.1 Overview

The Hi3516C V300 is integrated with high-performance audio CODECs, including high-quality stereo playback DAC (96 dB DR A-weighted), two single-ended line outputs; high-quality stereo recording ADC (93 dB DR A-weighted), two single-ended stereo inputs or one differential input; –1.5 dB to 30 dB MIC input, and for the gain ranging from –1.5 dB to 0 dB, the gain control step is 1.5 dB; for the gain ranging from 0 dB to 30 dB, the gain control step is 2 dB. The boost gain is 20 dB. The I^2S data interface supports the standard sampling rates ranging from 8 kHz to 192 kHz. Besides, it allows two sampling rates to be used simultaneously and supports digital mixing.

11.2.2 Features

The audio CODEC module has the following features:

- 96 dBA DR stereo DAC

- Single-ended stereo line output or one differential line output
- DAC digital volume control range: –121 dB to +6 dB, at 1 dB step
- 93 dBA DR stereo ADC
- Analog volume control range of ADC channel: –1.5 dB to 30 dB, at 2 dB step. The boost gain is 20 dB.
- Digital volume control range of ADC channel: –96 dB to 30 dB, at 1 dB step
- Two alternative single-ended stereo inputs or one differential input
- Provides internal MIC biasing
- Master and slave I^2S data interfaces, supporting 24 bits, 20 bits, 18 bits, and 16 bits, in binary format
- Audio sampling frequencies: 48 kHz, 44.1 kHz, and 32 kHz

  The sampling frequencies of each series are as follows:
  - The 32 kHz sampling frequencies series include 8 kHz, 16 kHz, 32 kHz, 64 kHz, and 128 kHz.
  - The 44.1 kHz sampling frequencies series include 11.025 kHz, 22.05 kHz, 44.1 kHz, 88.2 kHz, and 176.4 kHz.
  - The 48 kHz sampling frequencies series include 12 kHz, 24 kHz, 48 kHz, 96 kHz, and 192 kHz.
- The jitter tolerance of the analog clock CLKIN is 50 ps RMS.

11.2.3 Function Description

The audio CODEC module provides the recording and playing function. In the case of audio recording, analog signals are input from the MIC or line-in end, the gain is amplified at the analog part, and the signals converted into digital signals and output from the I^2S interface. Stereo recording is supported. In the case of playback, audio signals are input through the I^2S interface, converted into analog signals by the DAC, and then output. Stereo playing is supported.

Recording Mode

In recording mode, the MIC or line-in signals are input from the analog input end, processed by using the programmable gain method, converted by the ADC, filtered and volume-adjusted at the digital part, and finally output from the I^2S interface. Then, the entire recording procedure is complete.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Input analog audio signals to start recording. Signals are then output from the I^2S interface.

----End

Playing Mode

In playing mode, audio signals are transmitted from the I^2S interface to the DAC digital part for filtering and volume control, filtering is performed at the analog part, and finally output by the line-out end.

The procedure is as follows:

Step 1 Power on the audio CODEC module, and the reference voltage works normally one second later.

Step 2 Configure the registers according to register descriptions.

Step 3 Transmit signals from the I^2S interface, and then output analog audio signals from the lineout end.

----End

11.2.4 Register Summary

Table 11-2 describes audio codec registers.

Table 11-2 Summary of audio codec registers (base address: 0x1132_0000)

Offset Address	Register	Description	Page
0x00B4	AUDIO_ANA_CTRL_0	Audio CODEC ANA register 0 (this register cannot be soft reset)	11-35
0x00B8	AUDIO_ANA_CTRL_1	Audio CODEC ANA register 1 (this register cannot be soft reset)	11-37
0x00BC	AUDIO_ANA_CTRL_2	Audio CODEC ANA register 2 (this register cannot be soft reset)	11-39
0x00C0	AUDIO_ANA_CTRL_3	Audio CODEC ANA register 3 (this register cannot be soft reset)	11-40
0x00CC	AUDIO_CTRL_REG_1	Audio CODEC DIG control register 0 (this register cannot be soft reset)	11-41
0x00D0	AUDIO_DAC_REG_0	Audio CODEC DIG control register 1 (this register cannot be soft reset)	11-42
0x00D4	AUDIO_DAC_REG_1	Audio CODEC DIG control register 2 (this register cannot be soft reset)	11-44
0x00D8	AUDIO_ADC_REG_0	Audio CODEC DIG control register 3 (this register cannot be soft reset)	11-45
0x00E0	AUDIO_REG_1	I^2S channel selection control register (this register cannot be soft reset)	11-46

11.2.5 Register Description

AUDIO_ANA_CTRL_0

AUDIO_ANA_CTRL_0 is audio CODEC ANA register 0 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00B4	AUDIO_ANA_CTRL_0	0x6405_FCFD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													acodec_dacl_pop_en	reserved	acodec_dacr_pop_en	reserved	acodec_mute_dacr	acodec_mute_dacl	acodec_pd_dacr	acodec_pd_dacl	reserved	acodec_pd_dacr_dff	acodec_pd_dacl_dff	acodec_pd_micbias2	acodec_pd_micbias1	acodec_pd_linein_r	acodec_pd_linein_l	acodec_pd_adcr	acodec_pd_adcl	reserved	acodec_pd_vref
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	1

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	acodec_dacl_pop_en	Audio-left channel pop circuit enable 0: The pop tone removal function is disabled. 1: The pop tone removal function is enabled. Note: acodec_dacl_pop_en must be set to 1 only during the power-on/power-off pop suppression process and be set to 0 when the DAC channel works properly.
[17]	RO	reserved	Reserved
[16]	RW	acodec_dacr_pop_en	Audio-right channel pop circuit enable 0: The pop tone removal function is disabled. 1: The pop tone removal function is enabled. Note: acodec_dacr_pop_en must be set to 1 only during the power-on/power-off pop suppression process and be set to 0 when the DAC channel works properly.
[15]	RO	reserved	Reserved
[14]	RW	acodec_mute_dacr	Mute control for the DAC audio-right channel 0: The DAC audio-right channel works properly. 1: The DAC audio-right channel is muted.
[13]	RW	acodec_mute_dacl	Mute control for the DAC audio-left channel 0: The DAC audio-left channel works properly. 1: The DAC audio-left channel is muted.

[12]	RW	acodec_pd_dacr	Power-down control for the DAC audio-right channel (DACR) 0: The analog DACR works properly. 1: The analog DACR is powered down.
[11]	RW	acodec_pd_dacl	Power-down control for the DAC audio-left channel (DACL) 0: The analog DACL works properly. 1: The analog DACL is powered down.
[10]	RO	reserved	Reserved
[9]	RW	acodec_pd_dacr_dff	Power-down control for the DACR D trigger 0: The DACR D trigger works properly. 1: The DACR D trigger is powered down.
[8]	RW	acodec_pd_dacl_dff	Power-down control for the DACL D trigger 0: The DACL D trigger works properly. 1: The DACL D trigger is powered down.
[7]	RW	acodec_pd_micbias2	Power down control for the MICBIAS2 0: The MICBIAS2 works properly. 1: The MICBIAS2 is powered down.
[6]	RW	acodec_pd_micbias1	Power down control for the MICBIAS1 0: The MICBIAS1 works properly. 1: The MICBIAS1 is powered down.
[5]	RW	acodec_pd_linein_r	LINEIN_R power-down control 0: The LINEIN_R works properly. 1: The LINEIN_R is powered down.
[4]	RW	acodec_pd_linein_l	LINEIN_L power-down control 0: The LINEIN_L works properly. 1: The LINEIN_L is powered down.
[3]	RW	acodec_pd_adcr	Power down control for the ADC audio-right channel (ADCR) 0: The digital and analog ADCRs work properly. 1: The digital and analog ADCRs are powered down.
[2]	RW	acodec_pd_adcl	Power down control for the ADC audio-left channel (ADCL) 0: The digital and analog ADCLs work properly. 1: The digital and analog ADCLs are powered down.
[1]	RW	reserved	This bit is set to 1 in normal mode.
[0]	RW	acodec_pd_vref	Power-down control for the reference voltage 0: The reference voltage works properly. 1: The reference voltage is powered down.

AUDIO_ANA_CTRL_1

AUDIO_ANA_CTRL_1 is audio CODEC ANA register 1 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00B8	AUDIO_ANA_CTRL_1	0x0000_0034

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	acodec_linein_r_sel				acodec_linein_l_sel				reserved	acodec_adcr_gain_boost	reserved		acodec_linein_r_gain_codec				reserved	acodec_adcl_gain_boost	reserved		acodec_linein_l_gain_code				reserved		acodec_mute_lineinr	acodec_mute_lineinl	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0

Bits	Access	Name	Description
[31:28]	RW	acodec_linein_r_sel	Input signal select for the line-in right channel 0x3: IN1R single-ended input 0x4: IN1R (positive end)/IN1L (negative end) differential input Other values: reserved
[27:24]	RW	acodec_linein_l_sel	Input signal select for the line-in left channel 0x3: IN1L single-ended input 0x4: IN1L (positive end)/IN1R (negative end) differential input Other values: reserved
[23]	RO	reserved	Reserved
[22]	RW	acodec_adcr_gain_boost	ADCR gain boost control 0: 0 dB 1: 20 dB
[21]	RO	reserved	Reserved

[20:16]	RW	acodec_linein_r_gain_codec	LINEINR input gain control 0x00: 0 dB 0x01: 2 dB 0x02: 4 dB 0x03: 6 dB 0x04: 8 dB 0x05: 10 dB 0x06: 12 dB 0x07: 14 dB 0x08: 16 dB 0x09: 18 dB 0x0A: 20 dB 0x0B: 22 dB 0x0C: 24 dB 0x0D: 26 dB 0x0E: 28 dB 0x0F: 30 dB 0x10: −1.5 dB Other values: reserved
[15]	RO	reserved	Reserved
[14]	RW	acodec_adcl_gain_boost	ADCL gain boost control 0: 0 dB 1: 20 dB
[13]	RO	reserved	Reserved

[12:8]	RW	acodec_linein_l_gain_code	LINEINL input gain control 0x00: 0 dB 0x01: 2 dB 0x02: 4 dB 0x03: 6 dB 0x04: 8 dB 0x05: 10 dB 0x06: 12 dB 0x07: 14 dB 0x08: 16 dB 0x09: 18 dB 0x0A: 20 dB 0x0B: 22 dB 0x0C: 24 dB 0x0D: 26 dB 0x0E: 28 dB 0x0F: 30 dB 0x10: −1.5 dB Other values: reserved
[7:6]	RO	reserved	Reserved
[5]	RW	acodec_mute_linein_r	LINEINR mute control of the right channel 0: The right channel LINEINR works properly. 1: The right channel LINEINR is muted.
[4]	RW	acodec_mute_linein_l	LINEINL mute control of the left channel 0: The left channel LINEINL works properly. 1: The left channel LINEINL is muted.
[3:0]	RO	reserved	Reserved

AUDIO_ANA_CTRL_2

AUDIO_ANA_CTRL_2 is audio CODEC ANA register 2 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00BC	AUDIO_ANA_CTRL_2	0x4018_008D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		reserved						acodec_rst				reserved																			
Reset	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30]	RW	reserved	This bit is set to 0 in normal mode.
[29:24]	RO	reserved	Reserved
[23]	RW	acodec_rst	Analog signal reset 0: reset deasserted 1: reset
[22:0]	RO	reserved	Reserved

AUDIO_ANA_CTRL_3

AUDIO_ANA_CTRL_3 is audio CODEC ANA register 3 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00C0	AUDIO_ANA_CTRL_3	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								acodec_vref_exmode	reserved			acodec_pop_res_sel		reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7]	RW	acodec_vref_exmode	VREF PD 0: pull-down, normal PD 1: no pull-down. The external VREF is supported.

[6:5]	RO	reserved	Reserved
[4:3]	RW	acodec_pop_res_sel	Resistance of the resistor between the pop-free circuit and the main output 00: 100 Ω 01: 1 kΩ 10: 10 kΩ 11: 100 kΩ
[2:0]	RO	reserved	Reserved

AUDIO_CTRL_REG_1

AUDIO_CTRL_REG_1 is audio CODEC DIG control register 0 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00CC	AUDIO_CTRL_REG_1	0x00F3_5A4A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_rst_n	dacr_rst_n	adcl_rst_n	adcr_rst_n	dacl_en	dacr_en	adcl_en	adcr_en	reserved				i2s1_fs_sel				reserved															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0	1	0	1	0

Bits	Access	Name	Description
[31]	RW	dacl_rst_n	DACL reset 0: valid 1: invalid
[30]	RW	dacr_rst_n	DACR reset 0: valid 1: invalid
[29]	RW	adcl_rst_n	ADCL reset 0: valid 1: invalid
[28]	RW	adcr_rst_n	ADCR reset 0: valid 1: invalid

[27]	RW	dacl_en	DACL enable 0: disabled 1: enabled
[26]	RW	dacr_en	DACR enable 0: disabled 1: enabled
[25]	RW	adcl_en	ADCL enable 0: disabled 1: enabled
[24]	RW	adcr_en	ADCR enable 0: disabled 1: enabled
[23:18]	RO	reserved	Reserved
[17:13]	RW	i2s1_fs_sel	Sampling rate of the I^2S channel 11000: mclk/512/2 11001: mclk/256/2 11010: mclk/128/2 11011: mclk/64/2 111xx: mclk/32/2
[12:0]	RO	reserved	Reserved

AUDIO_DAC_REG_0

AUDIO_DAC_REG_0 is audio CODEC DIG control register 1 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D0	AUDIO_DAC_REG_0	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smutel	smuter	sunmutel	sunmuter	dacvu	mutel_rate		muter_rate	reserved																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	smutel	DACL soft mute control 0: disabled 1: enabled
[30]	RW	smuter	DACR soft mute control 0: disabled 1: enabled
[29]	RW	sunmutel	DACL soft unmute control 0: disabled 1: enabled
[28]	RW	sunmuter	DACR soft unmute control 0: disabled 1: enabled
[27]	RW	dacvu	DAC volume update control 0: not updated 1: updated
[26:25]	RW	mutel_rate	DACL soft mute rate control 00: fs/2 01: fs/8 10: fs/32 11: fs/64
[24:23]	RW	muter_rate	DACR soft mute rate control 00: fs/2 01: fs/8 10: fs/32 11: fs/64
[22:0]	RO	reserved	Reserved

AUDIO_DAC_REG_1

AUDIO_DAC_REG_1 is audio CODEC DIG control register 2 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D4	AUDIO_DAC_REG_1	0x0606_2424

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dacl_mute	dacl_vol							dacr_mute	dacr_vol							reserved															
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0

Bits	Access	Name	Description
[31]	RW	dacl_mute	DACL digital mute control 0: normal mode 1: muted
[30:24]	RW	dacl_vol	DACL digital volume control The volume is calculated as follows: (6 − dacl_vol x 1) dB 0x00: 6 dB 0x01: 5 dB 0x02: 4 dB … 0x7E: −120 dB 0x7F: muted
[23]	RW	dacr_mute	DACR digital mute control 0: normal mode 1: muted
[22:16]	RW	dacr_vol	DACR digital volume control The volume is calculated as follows: (6 − dacr_vol x 1) dB 0x00: 6 dB 0x01: 5 dB 0x02: 4 dB … 0x7E: −120 dB 0x7F: muted
[15:0]	RO	reserved	Reserved

AUDIO_ADC_REG_0

AUDIO_ADC_REG_0 is audio CODEC DIG control register 3 (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00D8	AUDIO_ADC_REG_0	0x1E1E_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	adcl_mute				adcl_vol				adcr_mute				adcr_vol				adcl_hpf_en	adcr_hpf_en	reserved													
Reset	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31]	RW	adcl_mute	ADCL digital mute control 0: unmuted 1: muted
[30:24]	RW	adcl_vol	ADCL volume control The volume is calculated as follows: (30 − adcl_vol x 1) dB 00: 30 dB 01: 29 dB 02: 28 dB … 7E: −96 dB 7F: −97 dB
[23]	RW	adcr_mute	ADCR digital mute control 0: unmuted 1: muted
[22:16]	RW	adcr_vol	ADCR volume control The volume is calculated as follows: (30 − adcr_vol x 1) dB 00: 30 dB 01: 29 dB 02: 28 dB … 7E: −96 dB 7F: −97 dB
[15]	RW	adcl_hpf_en	ADCL high-pass filter enable 0: disabled 1: enabled

[14]	RW	adcr_hpf_en	ADCR high-pass filter enable 0: disabled 1: enabled
[13:0]	RO	reserved	Reserved

AUDIO_REG_1

AUDIO_REG_1 is an I²S channel selection control register (this register cannot be soft reset).

Offset Address	Register Name	Total Reset Value
0x00E0	AUDIO_REG_1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Name	reserved								i2s_pad_enable	audio_enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RW	i2s_pad_enable	Enable for the channel between the I²S interface of the chip and AIAO 0: The channel between the I²S interface of the chip and AIAO is disabled, and the I²S interface of the chip has no output. 1: The channel between the I²S interface of the chip and AIAO is enabled, and the I²S interface of the chip connects to the I²S interface of the AIAO. Note: i2s_pad_enable and audio_enable cannot be 1 at the same time.
[0]	RW	audio_enable	Enable for the channel between the I²S interface of the internal audio CODEC and AIAO 0: The channel between the I²S interface of the internal audio CODEC and AIAO is disabled, and the I²S interface of the internal audio CODEC has no output. 1: The channel between the I²S interface of the internal audio CODEC and AIAO is enabled, and the I²S interface of internal audio CODEC connects to the I²S interface of the AIAO. Note: i2s_pad_enable and audio_enable cannot be 1 at the same time.

Contents

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Tables

12 Peripherals

12.1 I²C Controller

12.1.1 Overview

The I^2C controller provides the master I^2C interface which allows the CPU to read/write data from/to slave devices on the I^2C bus.

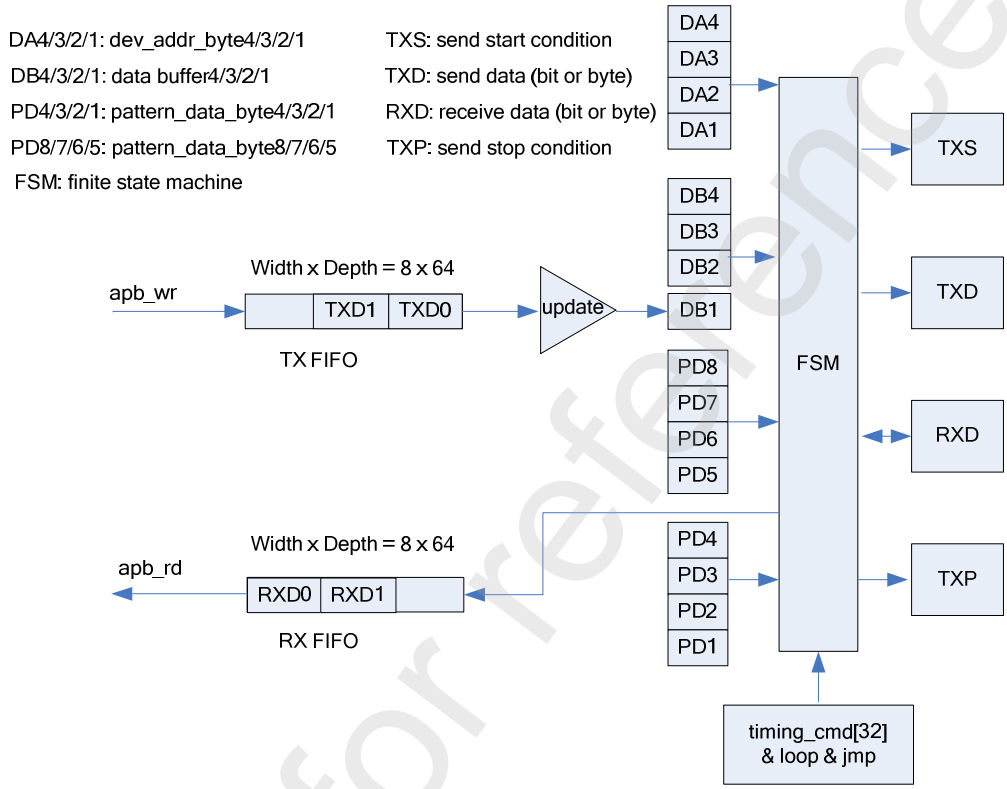
12.1.2 Function Description

The I^2C module has the following features:

- Master I^2C interface which supports standard timing and non-standard timing
- Bus arbitration in the case of multiple master devices
- Clock synchronization and bit and byte waiting
- 7-bit standard address and 10-bit extended address
- Standard mode (100 kbit/s) and high-speed mode (400 kbit/s)
- General call and start byte
- CBUS components not supported
- DMA operation.
- 64x8 bits TX FIFOs and 64x8 bits RX FIFOs

12.1.3 Functional Block Diagram

Figure 12-1 Functional block diagram of the controller



12.1.4 Timing Description Principles

Timing description includes timing format description and timing data preparation. Timing format description is implemented by configuring I2C_TIMING_CMD, I2C_LOOP1, I2C_DST1, I2C_LOOP2, I2C_DST2, I2C_LOOP3, and I2C_DST3. Both standard timings and non-standard timings can be configured.

- Timing data preparation is implemented by configuring I2C_DEV_ADDR, I2C_DATA_BUF, I2C_PATTERN_DATA1, I2C_PATTERN_DATA2, and I2C_TX_FIFO. The configured values need to be transmitted to the slave device.
- In timing format description, I2C_TIMING_CMD configures the timing command information, while I2C_LOOP1, I2C_DST1, I2C_LOOP2, I2C_DST2, I2C_LOOP3, and I2C_DST3 configure the jump control information. Table 12-1 describes the timing command information that can be configured in I2C_TIMING_CMD.

Table 12-1 Timing commands

Timing Command ID	Timing Command	Description
0x00	EXIT	Exit. This command is used for the controller to exit.

Timing Command ID	Timing Command	Description
0x01	S	Bus START
0x02	SDA4	Send dev_addr_byte4.
0x03	SDA3	Send dev_addr_byte3.
0x04	SDA2	Send dev_addr_byte2.
0x05	SDA1	Send dev_addr_byte1.
0x06	SDB4	Send data_buf_byte4.
0x07	SDB3	Send data_buf_byte3.
0x08	SDB2	Send data_buf_byte2.
0x09	SDB1	Send data_buf_byte1.
0x0A	SPD8	Send pattern_data_byte8.
0x0B	SPD7	Send pattern_data_byte7.
0x0C	SPD6	Send pattern_data_byte6.
0x0D	SPD5	Send pattern_data_byte5.
0x0E	SPD4	Send pattern_data_byte4.
0x0F	SPD3	Send pattern_data_byte3.
0x10	SPD2	Send pattern_data_byte2.
0x11	SPD1	Send pattern_data_byte1.
0x12	RD	Receive 1 byte data. Note: When the RD command is executed, if the RX FIFO is full, the controller waits until the RX FIFO has spare space. During waiting, the controller does not change the status of the I^2C bus.
0x13	RACK	Receive low-level acknowledgement.
0x14	RNACK	Receive high-level non-acknowledgement.
0x15	RNC	Receive acknowledgement, regardless of the level.
0x16	SACK	Send low-level acknowledgement.
0x17	SNACK	Send high-level non-acknowledgement.
0x18	JMPN1	Jump for limited times. The destination is specified by the DST1 register, and the number of jump times is specified by the LOOP1 register.
0x19	JMPN2	Jump for limited times. The destination is specified by the DST2 register, and the number of jump times is specified by the LOOP2 register.

Timing Command ID	Timing Command	Description
0x1A	JMPN3	Jump for limited times. The destination is specified by the DST3 register, and the number of jump times is specified by the LOOP3 register.
0x1B	UNDEF	Undefined
0x1C	UNDEF	Undefined
0x1D	UDB1	Update data to data_buf_byte1 from the TX FIFO. Note: When the UDB1 command is executed, if the TX FIFO is empty, the controller waits until the TX FIFO has data. During waiting, the controller does not change the status of the I^2C bus.
0x1E	SR	Bus repeated START
0x1F	P	Bus STOP

Standard Timing – 7-Bit Addressing, Write Operation

Figure 12-2 7-bit addressing, write timing

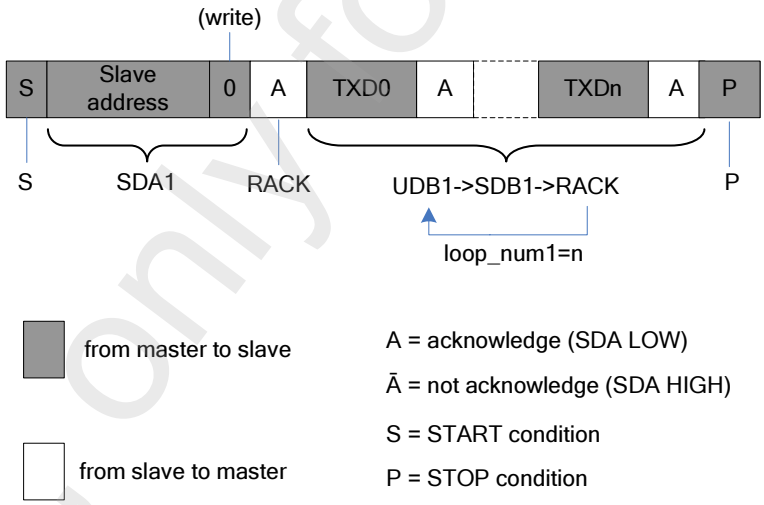


Table 12-2 describes the timing description configurations in Figure 12-2.

Table 12-2 7-bit addressing, write timing description configurations

Type	Register	Configuration
Timing format description	I2C_TIMING_CMD[0]	S
	I2C_TIMING_CMD[1]	SDA1

Type	Register	Configuration
	I2C_TIMING_CMD[2]	RACK
	I2C_TIMING_CMD[3]	UDB1
	I2C_TIMING_CMD[4]	SDB1
	I2C_TIMING_CMD[5]	RACK
	I2C_TIMING_CMD[6]	JMPN1
	I2C_TIMING_CMD[7]	P
	I2C_TIMING_CMD[8]	EXIT
	I2C_LOOP1	*n*
	I2C_DST1	3
Timing data preparation	I2C_DEV_ADDR	Slave address+'0', a total of 8 bits
	I2C_TX_FIFO	TXD0, TXD1, ..., TXDn in turn

Standard Timing – 7-Bit Addressing, Direct Read Operation

Figure 12-3 7-bit addressing, direct read timing

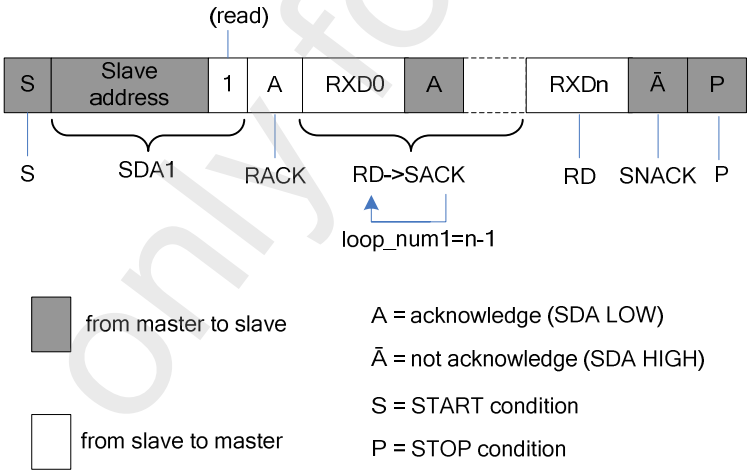


Table 12-3 describes the timing description configurations in Figure 12-3.

Table 12-3 7-bit addressing, direct read timing description configurations

Type	Register	Configuration
Timing format description	I2C_TIMING_CMD[0]	S
	I2C_TIMING_CMD[1]	SDA1

Type	Register	Configuration
	I2C_TIMING_CMD[2]	RACK
	I2C_TIMING_CMD[3]	RD
	I2C_TIMING_CMD[4]	SACK
	I2C_TIMING_CMD[5]	JMPN1
	I2C_TIMING_CMD[6]	RD
	I2C_TIMING_CMD[7]	SNACK
	I2C_TIMING_CMD[8]	P
	I2C_TIMING_CMD[9]	EXIT
	I2C_LOOP1	*n*–1
	I2C_DST1	3
Timing data preparation	I2C_DEV_ADDR	Slave address+'1', a total of 8 bits

NOTE

Write the read-back data RXD0, RXD1, …, and RXD*n* to I2C_RX_FIFO in turn.

Standard Timing – 10- Bit Addressing, Combined Read Operation

Figure 12-4 10-bit addressing, combined read timing

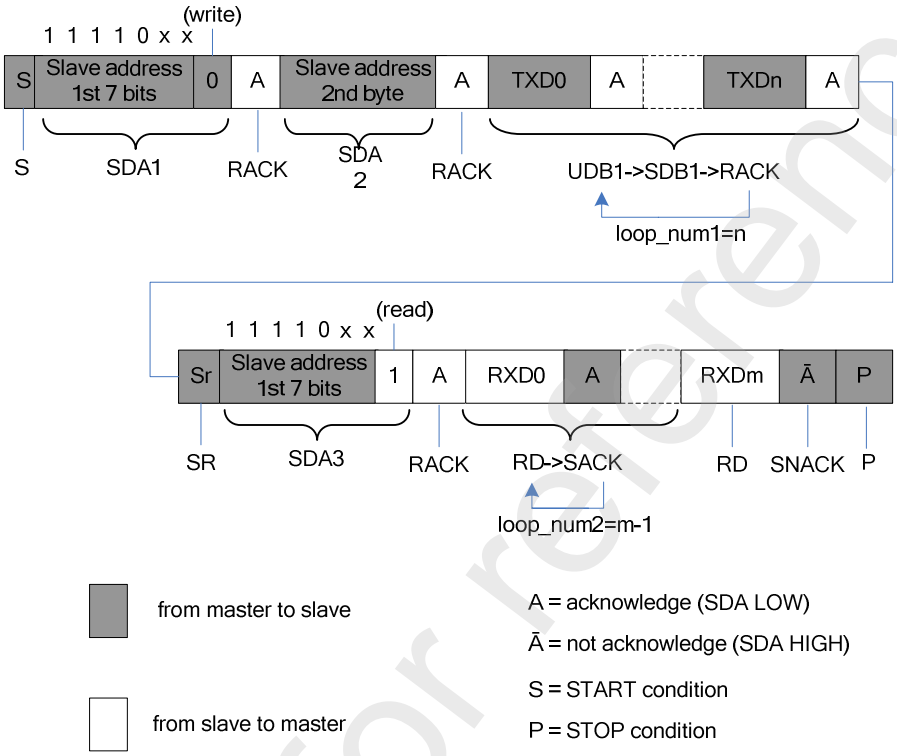


Table 12-4 describes the timing description configurations in Figure 12-4.

Table 12-4 10-bit addressing, combined read timing description configurations

Type	Register	Configuration
Timing format description	I2C_TIMING_CMD[0]	S
	I2C_TIMING_CMD[1]	SDA1
	I2C_TIMING_CMD[2]	RACK
	I2C_TIMING_CMD[3]	SDA2
	I2C_TIMING_CMD[4]	RACK
	I2C_TIMING_CMD[5]	UDB1
	I2C_TIMING_CMD[6]	WDB1
	I2C_TIMING_CMD[7]	RACK
	I2C_TIMING_CMD[8]	JMPN1
	I2C_TIMING_CMD[9]	SR
	I2C_TIMING_CMD[10]	SDA3

Type	Register	Configuration
	I2C_TIMING_CMD[11]	RACK
	I2C_TIMING_CMD[12]	RD
	I2C_TIMING_CMD[13]	SACK
	I2C_TIMING_CMD[14]	JMPN2
	I2C_TIMING_CMD[15]	RD
	I2C_TIMING_CMD[16]	SNACK
	I2C_TIMING_CMD[17]	P
	I2C_TIMING_CMD[18]	EXIT
	I2C_LOOP1	*n*
	I2C_DST1	5
	I2C_LOOP2	*m*–1
	I2C_DST2	12
Timing data preparation	I2C_DEV_ADDR	Write the first 7 bits of the slave address+'0' to dev_addr_byte1 Write the second byte of the slave address to dev_addr_byte2. Write the first 7 bits of the slave address+'1' to dev_addr_byte3.
	I2C_TX_FIFO	TXD0, TXD1, ..., TXDn in turn

NOTE

Write the read-back data RXD0, RXD1, …, and RXD*m* to I2C_RX_FIFO in turn.

Non-Standard Timing

Figure 12-5 shows a non-standard timing. In this timing, an acknowledgement is received only after 64 bytes data is transmitted continuously to the slave device.

Figure 12-5 Non-standard timing

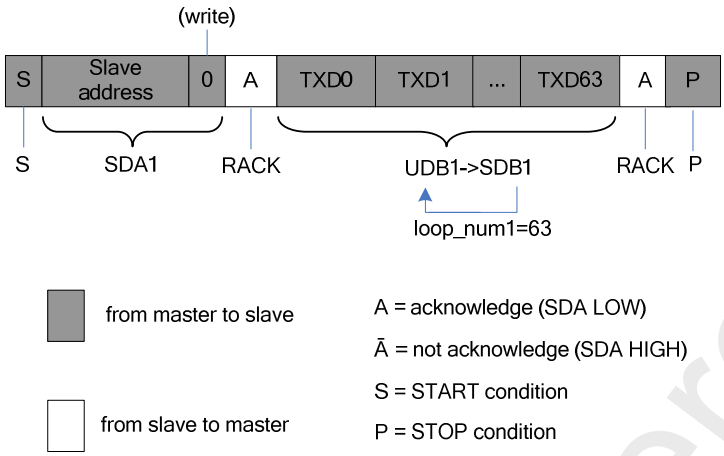


Table 12-5 describes the timing description configurations in Figure 12-5.

Table 12-5 Non-standard timing description configurations

Type	Register	Configuration
Timing format description	I2C_TIMING_CMD[0]	S
	I2C_TIMING_CMD[1]	SDA1
	I2C_TIMING_CMD[2]	RACK
	I2C_TIMING_CMD[3]	UDB1
	I2C_TIMING_CMD[4]	SDB1
	I2C_TIMING_CMD[5]	JMPN1
	I2C_TIMING_CMD[6]	RACK
	I2C_TIMING_CMD[7]	P
	I2C_TIMING_CMD[8]	EXIT
	I2C_LOOP1	63
	I2C_DST1	3
Timing data preparation	I2C_DEV_ADDR	(Slave address+'0'), a total of 8 bits
	I2C_TX_FIFO	TXD0, TXD1, ..., and TXD63 in turn

12.1.5 Operating Mode

12.1.5.1 Data Transmission in Non-DMA Mode (Write Operation in Interrupt Mode)

Perform the following steps:

Step 1 Configure I2C_HCNT and I2C_LCNT to enable the controller to work in the correct mode.

Step 2 Set I2C_TX_WATERMARK to 0x10.

Step 3 Configure I2C_GLB to enable the controller.

Step 4 Complete timing description based on the actual timing by referring to section 12.1.4 "Timing Description Principles."

Step 5 Set I2C_CTRL1 to 0x1 to start the controller.

Step 6 Set I2C_INTR_EN to 0x811.

Step 7 Query I2C_INTR_STAT in the interrupt service program. If I2C_INTR_STAT[arb_lost] or I2C_INTR_STAT[ack_bit_unmatch] is 1, an exception occurs; otherwise, if I2C_INTR_STAT[tx_lt_watermark] is 1, you can write up to 32 bytes data to be written to the TX FIFO.

- If there still is data to be written, set I2C_INTR_RAW to 0x10 to clear the tx_lt_watermark interrupt that triggers this interrupt handling process and wait until the next time the interrupt service program is triggered.
- If there is no data to be written, set I2C_INTR_EN to 0x1801 and wait for the all_cmd_done interrupt. When the all_cmd_done interrupt is received, all data has been written to the slave device.

Step 8 Set I2C_INTR_EN to 0x0 and I2C_INTR_RAW to 0x1fff to clear the interrupt and disable interrupt reporting, making preparation for switchover between operating modes.

----End

12.1.5.2 Data Transmission in Non-DMA Mode (Write Operation in Query Mode)

Perform the following steps:

Step 1 Configure I2C_HCNT and I2C_LCNT to enable the controller to work in the correct mode.

Step 2 Configure I2C_GLB to enable the controller.

Step 3 Complete timing description based on the actual timing by referring to section 12.1.4 "Timing Description Principles."

Step 4 Set I2C_CTRL1 to 0x1 to start the controller.

Step 5 Constantly query I2C_FIFO_STAT[tx_fifo_not_full] until it is 1 and write 1 byte data to be written to the TX FIFO. When all data to be written has be written to the TX FIFO, go to the next step.

Step 6 Constantly query I2C_INTR_RAW. If I2C_INTR_RAW[arb_lost_raw] or I2C_INTR_RAW[ack_bit_unmatch_raw] is 1, an exception occurs. If I2C_INTR_RAW[all_cmd_done_raw] is 1, all timings are complete.

Step 7 Set I2C_INTR_EN to 0x0 and I2C_INTR_RAW to 0x1fff to clear the interrupt and disable interrupt reporting, making preparation for switchover between operating modes.

----End

12.1.5.3 Data Transmission in Non-DMA Mode (Read Operation in Interrupt Mode)

Perform the following steps:

Step 1 Configure I2C_HCNT and I2C_LCNT to enable the controller to work in the correct mode.

Step 2 Set I2C_RX_WATERMARK to 0x10.

Step 3 Configure I2C_GLB to enable the controller.

Step 4 Complete timing description based on the actual timing by referring to section 12.1.4 "Timing Description Principles."

Step 5 Set I2C_CTRL1 to 0x1 to start the controller.

Step 6 Set I2C_INTR_EN to 0x1805.

Step 7 Query I2C_INTR_STAT in the interrupt service program. If I2C_INTR_STAT[arb_lost] or I2C_INTR_STAT[ack_bit_unmatch] is 1, an exception occurs. If no exception occurs, and I2C_INTR_STAT[all_cmd_done] is 1, all data has been read back. If no exception occurs and I2C_INTR_STAT[all_cmd_done] is 0, the rx_gt_watermark interrupt is generated, and you can read the 32 bytes read-back data from the RX FIFO. After reading the 32 bytes data, set I2C_INTR_RAW to 0x4 to clear the tx_lt_watermark interrupt that triggers this interrupt handling process and wait until the next time the interrupt service program is triggered.

Step 8 Set I2C_INTR_EN to 0x0 and I2C_INTR_RAW to 0x1fff to clear the interrupt and disable interrupt reporting, making preparation for switchover between operating modes.

----End

12.1.5.4 Data Transmission in Non-DMA Mode (Read Operation in Query Mode)

Perform the following steps:

Step 1 Configure I2C_HCNT and I2C_LCNT to enable the controller to work in the correct mode.

Step 2 Configure I2C_GLB to enable the controller.

Step 3 Complete timing description based on the actual timing by referring to section 12.1.4 "Timing Description Principles."

Step 4 Set I2C_CTRL1 to 0x1 to start the controller.

Step 5 Constantly query I2C_FIFO_STAT[rx_fifo_not_empty] until it is 1 and read 1 byte data from the RX FIFO. When all data are read back, go to the next step.

Step 6 Constantly query I2C_INTR_RAW. If I2C_INTR_RAW[arb_lost_raw] or I2C_INTR_RAW[ack_bit_unmatch_raw] is 1, an exception occurs. If I2C_INTR_RAW[all_cmd_done_raw] is 1, all timings are complete.

Step 7 Set I2C_INTR_EN to 0x0 and I2C_INTR_RAW to 0x1fff to clear the interrupt and disable interrupt reporting, making preparation for switchover between operating modes.

----End

12.1.5.5 Data Transmission in DMA Mode (Write Operation)

Perform the following steps:

Step 1 Obtain a DMAC channel.

Step 2 Configure and then start the DMAC channel.

Step 3 Configure I2C_HCNT and I2C_LCNT to enable the controller to work in the correct mode.

Step 4 Set I2C_TX_WATERMARK to 0x10.

Step 5 Configure I2C_GLB to enable the controller.

Step 6 Complete timing description based on the actual timing by referring to section 12.1.4 "Timing Description Principles."

Step 7 Set I2C_CTRL1 to 0x201 to start the controller.

Step 8 Wait for the DMAC completion interrupt.

Step 9 Constantly query I2C_INTR_RAW. If I2C_INTR_RAW[arb_lost_raw] or I2C_INTR_RAW[ack_bit_unmatch_raw] is 1, an exception occurs. If I2C_INTR_RAW[all_cmd_done_raw] is 1, all timings are complete.

Step 10 Set I2C_INTR_EN to 0x0 and I2C_INTR_RAW to 0x1fff to clear the interrupt and disable interrupt reporting, making preparation for switchover between operating modes.

----End

12.1.5.6 Data Transmission in DMA Mode (Read Operation)

Perform the following steps:

Step 1 Obtain a DMAC channel.

Step 2 Configure and then start the DMAC channel.

Step 3 Configure I2C_HCNT and I2C_LCNT to enable the controller to work in the correct mode.

Step 4 Set I2C_RX_WATERMARK to 0x10.

Step 5 Configure I2C_GLB to enable the controller.

Step 6 Complete timing description based on the actual timing by referring to section 12.1.4 "Timing Description Principles."

Step 7 Set I2C_CTRL1 to 0x301 to start the controller.

Step 8 Wait for the DMAC completion interrupt.

Step 9 Constantly query I2C_INTR_RAW. If I2C_INTR_RAW[arb_lost_raw] or I2C_INTR_RAW[ack_bit_unmatch_raw] is 1, an exception occurs. If I2C_INTR_RAW[all_cmd_done_raw] is 1, all timings are complete.

Step 10 Set I2C_INTR_EN to 0x0 and I2C_INTR_RAW to 0x1fff to clear the interrupt and disable interrupt reporting, making preparation for switchover between operating modes.

----End

12.1.5.7 Exception Handling Process

Perform the following steps:

Step 1 Set I2C_GLB[i2c_enable] to 0 to disable the controller.

Step 2 Set I2C_INTR_EN to 0x0 and I2C_INTR_RAW to 0x1fff to clear the interrupt and disable interrupt reporting, making preparation for switchover between operating modes.

----End

12.1.6 Register Summary

Hi3516C V300 provides two I²C units.

- The base address for I²C0 registers is 0x1211_0000.
- The base address for I²C1 registers is 0x1211_2000.

NOTE

The variable *n* in the offset addresses of I²C registers ranges from 0 to 31.

Table 12-6 Summary of I²C registers

Offset Address	Register	Description	Page
0x0000	I2C_GLB	I²C global configuration register	12-14
0x0004	I2C_HCNT	I²C high level duration register	12-15
0x0008	I2C_LCNT	I²C low level duration register	12-15
0x0010	I2C_DEV_ADDR	I²C component address register	12-16
0x0014	I2C_DATA_BUF	I²C data buffer register	12-16
0x0018	I2C_PATTERN_DATA1	I²C pattern data 1 register	12-17
0x001C	I2C_PATTERN_DATA2	I²C pattern data 2 register	12-17
0x0020	I2C_TX_FIFO	I²C TX FIFO data register	12-18
0x0024	I2C_RX_FIFO	I²C RX FIFO data register	12-18
0x0030 + *n* x 4	I2C_TIMING_CMD	I²C timing command register	12-18
0x00B0	I2C_LOOP1	I²C loop number 1 register	12-20
0x00B4	I2C_DST1	I²C jump destination 1 register	12-20
0x00B8	I2C_LOOP2	I²C loop number 2 register	12-21
0x00BC	I2C_DST2	I²C jump destination 2 register	12-21
0x00C0	I2C_LOOP3	I²C loop number 3 register	12-21
0x00C4	I2C_DST3	I²C jump destination 3 register	12-22

Offset Address	Register	Description	Page
0x00C8	I2C_TX_WATERMARK	I²C TX FIFO watermark register	12-22
0x00CC	I2C_RX_WATERMARK	I²C RX FIFO watermark register	12-23
0x00D0	I2C_CTRL1	I²C control register 1	12-23
0x00D8	I2C_FIFO_STAT	I²C FIFO status register	12-24
0x00E0	I2C_INTR_RAW	I²C raw interrupt register	12-25
0x00E4	I2C_INTR_EN	I²C interrupt enable register	12-26
0x00E8	I2C_INTR_STAT	I²C interrupt status register	12-27

12.1.7 Register Description

I2C_GLB

I2C_GLB is an I²C global configuration register.

Offset Address: 0x0000 | Register Name: I2C_GLB | Total Reset Value: 0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved		sda_hold_duration				reserved		i2c_enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:8]	RW	sda_hold_duration	SDA hold time duration The reference clock PCLK is 50 MHz. It is recommended that sda_hold_duration be 0.3 times i2c_low_duration. Note: It controls only the hold time duration of data sent from the host to the slave device.
[7:1]	RO	reserved	Reserved
[0]	RW	i2c_enable	I²C enable control 0: disabled. TX FIFO and RX FIFO are cleared. 1: enabled Note: If timing exceptions occur, disable and then enable the controller in case that residual data of the previous operation exists in the TX FIFO and RX FIFO.

I2C_HCNT

I2C_HCNT is an I^2C high level duration register.

Offset Address	Register Name	Total Reset Value
0x0004	I2C_HCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																i2c_high_duration															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	i2c_high_duration	SCL high level duration The reference clock PCLK is 50 MHz. It is recommended that i2c_high_duration be 1/2 of the SCL cycle in standard mode and 0.36 times of the SCL cycle in fast mode. Standard mode: i2c_high_duration = (F_{PCLK}/F_{SCL}) x 0.5 Fast mode: i2c_high_duration = (F_{PCLK}/F_{SCL}) x 0.36 (F_{SCL} is the SCL bus frequency.) If F_{SCL} is 400 kHz in fast mode, i2c_high_duration is calculated as follows: i2c_high_duration = (50 MHz/400 kHz) x 0.36 = 45

I2C_LCNT

I2C_LCNT is an I^2C low level duration register.

Offset Address	Register Name	Total Reset Value
0x0008	I2C_LCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																i2c_low_duration															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	i2c_low_duration	SCL low level duration The reference clock PCLK is 50 MHz. It is recommended that i2c_low_duration be 1/2 of the SCL cycle in standard mode and 0.64 times of the SCL cycle in fast mode. Standard mode: i2c_low_duration = (F_{PCLK}/F_{SCL}) x 0.5 Fast mode: i2c_low_duration = (F_{PCLK}/F_{SCL}) x 0.64 (F_{SCL} is the SCL bus frequency.) If F_{SCL} is 400 kHz in fast mode, i2c_low_duration is calculated as follows: i2c_scl_lcnt = (50 MHz/400 kHz) x 0.64 = 80

I2C_DEV_ADDR

I2C_DEV_ADDR is an I^2C component address register.

Offset Address	Register Name	Total Reset Value
0x0010	I2C_DEV_ADDR	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	dev_addr_byte4		dev_addr_byte3		dev_addr_byte2		dev_addr_byte1	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	dev_addr_byte4	Byte 4 of the component address
[23:16]	RW	dev_addr_byte3	Byte 3 of the component address
[15:8]	RW	dev_addr_byte2	Byte 2 of the component address
[7:0]	RW	dev_addr_byte1	Byte 1 of the component address

I2C_DATA_BUF

I2C_DATA_BUF is an I^2C data buffer register.

Offset Address	Register Name	Total Reset Value
0x0014	I2C_DATA_BUF	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	data_buf_byte4		data_buf_byte3		data_buf_byte2		data_buf_byte1	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	data_buf_byte4	Byte 4 of the data buffer

[23:16]	RW	data_buf_byte3	Byte 3 of the data buffer
[15:8]	RW	data_buf_byte2	Byte 2 of the data buffer
[7:0]	RW	data_buf_byte1	Byte 1 of the data buffer

I2C_PATTERN_DATA1

I2C_PATTERN_DATA1 is an I^{2}C pattern data 1 register.

Offset Address	Register Name	Total Reset Value
0x0018	I2C_PATTERN_DATA1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	pattern_data_byte4		pattern_data_byte3		pattern_data_byte2		pattern_data_byte1	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	pattern_data_byte4	Byte 4 of pattern data
[23:16]	RW	pattern_data_byte3	Byte 3 of pattern data
[15:8]	RW	pattern_data_byte2	Byte 2 of pattern data
[7:0]	RW	pattern_data_byte1	Byte 1 of pattern data

I2C_PATTERN_DATA2

I2C_PATTERN_DATA2 is an I^{2}C pattern data 2 register.

Offset Address	Register Name	Total Reset Value
0x001C	I2C_PATTERN_DATA2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	pattern_data_byte8		pattern_data_byte7		pattern_data_byte6		pattern_data_byte5	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RW	pattern_data_byte8	Byte 8 of pattern data
[23:16]	RW	pattern_data_byte7	Byte 7 of pattern data
[15:8]	RW	pattern_data_byte6	Byte 6 of pattern data
[7:0]	RW	pattern_data_byte5	Byte 5 of pattern data

I2C_TX_FIFO

I2C_TX_FIFO is an I^{2}C TX FIFO data register.

Offset Address	Register Name	Total Reset Value
0x0020	I2C_TX_FIFO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								tx_fifo							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	WO	tx_fifo	TX FIFO entry The written data is data to be transmitted.

I2C_RX_FIFO

I2C_RX_FIFO is an I^{2}C RX FIFO data register.

Offset Address	Register Name	Total Reset Value
0x0024	I2C_RX_FIFO	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								rx_fifo							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	rx_fifo	RX FIFO entry The read data is data received from the I^{2}C bus.

I2C_TIMING_CMD

I2C_TIMING_CMD is an I^{2}C timing command register.

Offset Address	Register Name	Total Reset Value
0x0030 + *n* x 4 (*n* = 0–31)	I2C_TIMING_CMD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												timing_cmd			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved
[4:0]	RW	timing_cmd	Timing command. *n* = 0, 1, 2, ..., 31. 0x00: EXIT (End. It is used to exit the logic.) 0x01: S (bus START) 0x02: WDA4 (Send dev_addr_byte4.) 0x03: WDA3 (Send dev_addr_byte3.) 0x04: WDA2 (Send dev_addr_byte2.) 0x05: WDA1 (Send dev_addr_byte1.) 0x06: WDB4 (Send data_buf_byte4.) 0x07: WDB3 (Send data_buf_byte3.) 0x08: WDB2 (Send data_buf_byte2.) 0x09: WDB1 (Send data_buf_byte1.) 0x0A: WPD8 (Send pattern_data_byte8.) 0x0B: WPD7 (Send pattern_data_byte7.) 0x0C: WPD6 (Send pattern_data_byte6.) 0x0D: WPD5 (Send pattern_data_byte5.) 0x0E: WPD4 (Send pattern_data_byte4.) 0x0F: WPD3 (Send pattern_data_byte3.) 0x10: WPD2 (Send pattern_data_byte2.) 0x11: WPD1 (Send pattern_data_byte1.) 0x12: RD (Receive 1 byte data.) 0x13: RACK (Receive low-level acknowledgement.) 0x14: RNACK (Receive high-level non-acknowledgement.) 0x15: RNC (Receive acknowledgement regardless of the level.) 0x16: SACK (Send low-level acknowledgement.) 0x17: SNACK (Send high-level non-acknowledgement.) 0x18: JMPN1 (Jump for limited times. The destination is specified by the DST1 register, and the number of jump times is specified by the LOOP1 register.) 0x19: JMPN2 (Jump for limited times. The destination is specified by the DST2 register, and the number of jump times is specified by the LOOP2 register.) 0x1A: JMPN3 (Jump for limited times. The destination is specified by the DST3 register, and the number of jump times is

			specified by the LOOP3 register.) 0x1B: UNDEF (undefined) 0x1C: UNDEF (undefined) 0x1D: UDB1 (Update date from the TX FIFO to data_buf_byte1.) 0x1E: SR (bus repeated START) 0x1F: P (bus STOP) **Note the following:** • When the UDB1 command is executed, if the TX FIFO is empty, the controller waits until the TX FIFO has data. During waiting, the controller does not change the status of the I²C bus. • When the RD command is executed, if the RX FIFO is full, the controller waits until the RX FIFO has spare space. During waiting, the controller does not change the status of the I²C bus.

I2C_LOOP1

I2C_LOOP1 is an I²C loop number 1 register.

Offset Address	Register Name	Total Reset Value
0x00B0	I2C_LOOP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	loop_num1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	loop_num1	Number of loops

I2C_DST1

I2C_DST1 is an I²C jump destination 1 register.

Offset Address	Register Name	Total Reset Value
0x00B4	I2C_DST1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																												dst_timing_cmd1			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved

[4:0]	RW	dst_timing_cmd1	Jump destination timing command register c vvv

I2C_LOOP2

I2C_LOOP2 is an I²C loop number 2 register.

Offset Address	Register Name	Total Reset Value
0x00B8	I2C_LOOP2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	loop_num2							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	loop_num2	Number of loops

I2C_DST2

I2C_DST2 is an I²C jump destination 2 register.

Offset Address	Register Name	Total Reset Value
0x00BC	I2C_DST2	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							dst_timing_cmd2
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved
[4:0]	RW	dst_timing_cmd2	Jump destination timing command register

I2C_LOOP3

I2C_LOOP3 is an I²C loop number 3 register.

Offset Address	Register Name	Total Reset Value
0x00C0	I2C_LOOP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	loop_num3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	loop_num3	Number of loops

I2C_DST3

I2C_DST3 is an I^{2}C jump destination 3 register.

Offset Address	Register Name	Total Reset Value
0x00C4	I2C_DST3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											dst_timing_cmd3				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	reserved	Reserved
[4:0]	RW	dst_timing_cmd3	Jump destination timing command register

I2C_TX_WATERMARK

I2C_TX_WATERMARK is an I^{2}C TX FIFO watermark register.

Offset Address	Register Name	Total Reset Value
0x00C8	I2C_TX_WATERMARK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											tx_watermark				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:0]	RW	tx_watermark	TX FIFO watermark. When data in the TX FIFO is less than that specified by tx_watermark, the tx_lt_watermark_raw raw interrupt is set to 1.

I2C_RX_WATERMARK

I2C_RX_WATERMARK is an I²C RX FIFO watermark register.

Offset Address	Register Name	Total Reset Value
0x00CC	I2C_RX_WATERMARK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							rx_watermark
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:0]	RW	rx_watermark	RX FIFO watermark. When data in the RX FIFO is more than that specified by rx_watermark, the rx_gt_watermark_raw raw interrupt is set to 1.

I2C_CTRL1

I2C_CTRL1 is I²C control register 1.

Offset Address	Register Name	Total Reset Value
0x00D0	I2C_CTRL1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved					dma_operation	reserved	start
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:8]	RW	dma_operation	DMA operation control 00: non-DMA mode 01: reserved 10: DMA write mode 11: DMA read mode
[7:1]	RO	reserved	Reserved

[0]	RW	start	Boot control. Writing 1 to this bit enables the state machine inside the controller to execute the timing command sequence. After execution is complete or an exception occurs, the logic clears this bit. 0: not boot 1: boot

I2C_FIFO_STAT

I2C_FIFO_STAT is an I^{2}C FIFO status register.

Offset Address	Register Name	Total Reset Value
0x00D8	I2C_FIFO_STAT	0x000A_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												tx_fifo_not_full	tx_fifo_not_empty	rx_fifo_not_full	rx_fifo_not_empty	reserved	tx_fifo_vld_num							reserved	rx_fifo_vld_num							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19]	RO	tx_fifo_not_full	TX FIFO full indicator 0: full 1: not full
[18]	RO	tx_fifo_not_empty	TX FIFO empty indicator 0: empty 1: not empty
[17]	RO	rx_fifo_not_full	RX FIFO full indicator 0: full 1: not full
[16]	RO	rx_fifo_not_empty	RX FIFO empty indicator 0: empty 1: not empty
[15]	RO	reserved	Reserved
[14:8]	RO	tx_fifo_vld_num	Valid data number in the TX FIFO
[7]	RO	reserved	Reserved

[6:0]	RO	rx_fifo_vld_num	Valid data number in the RX FIFO

I2C_INTR_RAW

I2C_INTR_RAW is an I^2C raw interrupt register.

Offset Address	Register Name	Total Reset Value
0x00E0	I2C_INTR_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			all_cmd_done_raw	arb_lost_raw	start_det_raw	stop_det_raw	reserved				tx_lt_watermark_raw	reserved	rx_gt_watermark_raw	reserved	ack_bit_unmatch_raw
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RWC	all_cmd_done_raw	Interrupt indicating that the EXIT command in the timing command sequence is executed 0: No interrupt is generated. 1: An interrupt is generated.
[11]	RWC	arb_lost_raw	Arbitration loss interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RWC	start_det_raw	Interrupt indicating that START is detected 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RWC	stop_det_raw	Interrupt indicating that STOP is detected 0: No interrupt is generated. 1: An interrupt is generated.
[8:5]	RO	reserved	Reserved
[4]	RWC	tx_lt_watermark_raw	Interrupt indicating that the data amount in the TX FIFO is less than the watermark during data transmission 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	reserved	Reserved

[2]	RWC	rx_gt_watermark_raw	Interrupt indicating that the data amount in the RX FIFO is greater than the watermark during data reception 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	reserved	Reserved
[0]	RWC	ack_bit_unmatch_raw	Interrupt indicating that the acknowledgement bit is not as expected 0: No interrupt is generated. 1: An interrupt is generated.

I2C_INTR_EN

I2C_INTR_EN is an I^{2}C interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x00E4	I2C_INTR_en	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			all_cmd_done_en	arb_lost_en	start_det_en	stop_det_en	reserved				tx_lt_watermark_en	reserved		rx_gt_watermark_en	reserved		ack_bit_unmatch_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RW	all_cmd_done_en	all_cmd_done interrupt enable 0: disabled 1: enabled
[11]	RW	arb_lost_en	arb_lost interrupt enable 0: disabled 1: enabled
[10]	RW	start_det_en	start_det interrupt enable 0: disabled 1: enabled

[9]	RW	stop_det_en	STOP interrupt enable 0: disabled 1: enabled
[8:5]	RO	reserved	Reserved
[4]	RW	tx_lt_watermark_en	tx_lt_watermark interrupt enable 0: disabled 1: enabled
[3]	RO	reserved	Reserved
[2]	RW	rx_gt_watermark_en	rx_gt_watermark interrupt enable 0: disabled 1: enabled
[1]	RO	reserved	Reserved
[0]	RW	ack_bit_unmatch_en	ack_bit_unmatch interrupt enable 0: disabled 1: enabled

I2C_INTR_STAT

I2C_INTR_STAT is an I^2C interrupt status register.

Offset Address	Register Name	Total Reset Value
0x00E8	I2C_INTR_STAT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																			all_cmd_done	arb_lost	start_det	stop_det	reserved				tx_lt_watermark	reserved	rx_gt_watermark	reserved	ack_bit_unmatch
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:13]	RO	reserved	Reserved
[12]	RO	all_cmd_done	Interrupt indicating that all timing commands are completed properly 0: No interrupt is generated. 1: An interrupt is generated.

[11]	RO	arb_lost	Arbitration loss interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[10]	RO	start_det	Interrupt indicating that START is detected 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	stop_det	Interrupt indicating that STOP is detected 0: No interrupt is generated. 1: An interrupt is generated.
[8:5]	RO	reserved	Reserved
[4]	RO	tx_lt_watermark	Interrupt indicating that the data amount in the TX FIFO is less than the watermark during data transmission 0: No interrupt is generated. 1: An interrupt is generated.
[3]	RO	reserved	Reserved
[2]	RO	rx_gt_watermark	Interrupt indicating that the data amount in the RX FIFO is greater than the watermark during data reception 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	reserved	Reserved
[0]	RO	ack_bit_unmatch	Interrupt indicating that the acknowledgement bit is not as expected 0: No interrupt is generated. 1: An interrupt is generated.

12.2 UART

12.2.1 Overview

The universal asynchronous receiver transmitter (UART) is an asynchronous serial communication interface. It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals. The UART is mainly used to interconnect the Hi3516C V300 with the UART of an external chip so that the two chips can communicate with each other.

Hi3516C V300 provides three UART units (UART0 to UART2).

- UART0: a two-wire UART for debugging and alarm reporting
- UART1: a four-wire UART for debugging, alarm reporting, and pan, tile, and zoom (PTZ) control

- UART2: a two-wire UART for debugging and alarm reporting

12.2.2 Features

The UART unit has the following features:

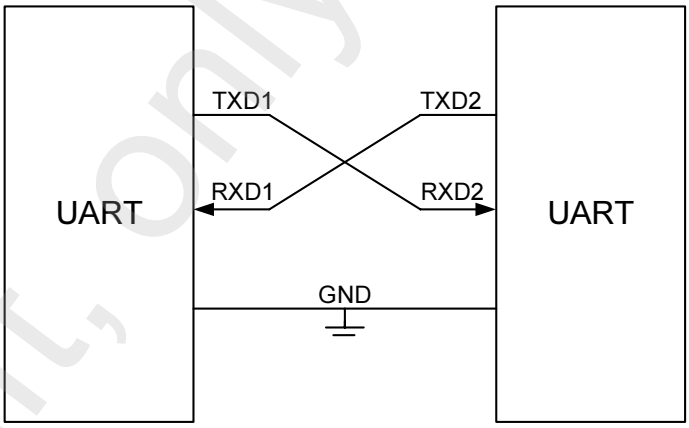
- Supports 64x8-bit transmit first-in, first-out (FIFO) and 64x12-bit RX FIFO.
- Supports programmable widths for the data bit and stop bit. The width of the data bit can be set to 5 bits, 6 bits, 7 bits, or 8 bits and width of the stop bit can be set to 1 bit or 2 bits by programming.
- Supports parity check or no check.
- Supports the programmable transfer rate.
- Supports RX FIFO interrupts, TX FIFO interrupts, RX timeout interrupts, and error interrupts.
- Supports the query of the raw interrupt status and the masked interrupt status.
- Allows the UART or the TX/RX function of the UART to be disabled by programming to reduce power consumption.
- Allows the UART clock to be disabled to reduce power consumption.
- Supports DMA operations.

12.2.3 Function Description

Application Block Diagram

Figure 12-6 shows the typical application of the UART.

Figure 12-6 Typical application block diagram of the UART

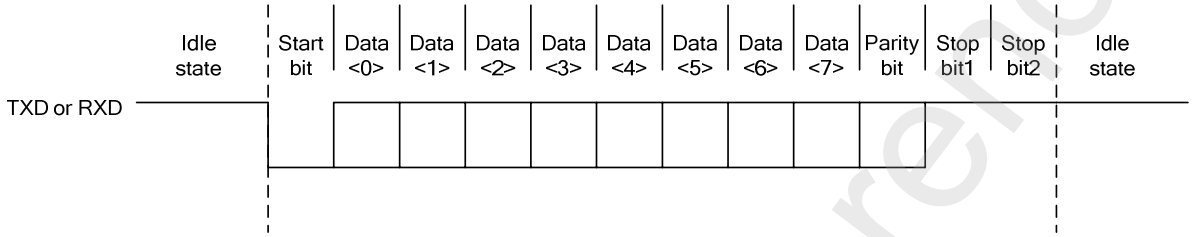


The UART serves as an asynchronous bidirectional serial bus. Through the UARTs connected by two data lines, a simplified and effective data transfer mode is implemented.

Function Principle

A frame transfer of the UART involves the start signal, data signal, parity bit, and stop signal, as shown in Figure 12-7. The data frame is output from the TXD end of one UART and then is input to the RXD end of the other UART.

Figure 12-7 Frame format of the UART



The definitions of the start signal, data signal, parity bit, and stop signal are as follows:

- Start signal (start bit)

  It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART does not transmit data, the level must remain high.

- Data signal (data bit)

  The data bit width can be set to 5 bits, 6 bits, 7 bits, or 8 bits according to the requirements in different applications.

- Parity bit

  It is a 1-bit error correction signal. The UART parity bit can be an odd parity bit, even parity bit, or stick parity bit. The UART can enable and disable the parity bit. For details, see the description of the UART_LCR_H register.

- Stop signal (stop bit)

  It is the stop bit of a data frame. The stop bit width can be set to 1 bit or 2 bits. The high level of TXD indicates the end of the data frame.

12.2.4 Operating Mode

12.2.4.1 Reference Clock and Reset

The UART reference clock source of Hi3516C V300 can be 24 MHz or 6 MHz, and the reference clock can be configured by setting PERI_CRG57 bit[19].

The UART reference clock can be enabled or disabled as required by configuring PERI_CRG57 bit[17:15].

The UART controller can be separately reset by configuring PERI_CRG57 bit[9:7].

NOTE

For details about the register PERI_CRG57, see the CRG section.

12.2.4.2 Baud Rate Configuration

The operating baud rate of the UART can be set by configuring the registers UART_IBRD and UART_FBRD. The baud rate is calculated as follows:

Current baud rate = Frequency of the UART reference clock/(16 x Clock divider). The frequency of the UART reference clock is 24 MHz by default.

NOTE

- Baud_Rate: The UART baud rates are 9600 bit/s, 14,400 bit/s, 19,200 bit/s, 38,400 bit/s, 57,600 bit/s, 76,800 bit/s, 115,200 bit/s, 230,400 bit/s, and 460,800 bit/s.
- $F_{UARTCLK}$: UART reference clock frequency. For Hi3516C V300, the reference clock frequency can be set to 24 MHz or 6 MHz by configuring PERI_CRG57 bit[19].
- BRD: baud rate frequency divider. It consists of two parts: BRD_I and BRD_F. BRD_I is the integer part, and BRD_F is the decimal part. BRD_I is configured by setting UART_IBRD, and BRD_F is configured by setting UART_FBRD.

The relationships between UART_IBRD/UART_FBRD and BRD_I/BRD_F are as follows:

UART_IBRD = BRD_I

UART_FBRD = Integer(BRD_F x 64 + 0.5)

For example, assume that $F_{UARTCLK}$ is 50 MHz and the expected UART baud rate (Baud_Rate) is 230,400 bit/s, the frequency divider BRD is 13.5634 (50 x 10^6/16 x 230400). In this case, BRD_I is 13, and BRD_F is 0.5634.

UART_IBRD and UART_FBRD can be calculated based on BRD_I and BRD_F as follows:

UART_IBRD = 13

UART_FBRD = Integer(0.5634 x 64 + 0.5) = Integer(36.5576) = 36

Therefore, to set the baud rate to 230,400 bit/s, you need to set UART_IBRD to 0xD and UART_FBRD to 0x24.

12.2.4.3 Data Transfer in Interrupt or Query Mode

Initialization

The initialization is implemented as follows:

Step 1 Configure the UART reference clock to deassert reset on the UART module.

Step 2 Write 0 to UART_CR bit[0] to disable the UART.

Step 3 Write to UART_IBRD and UART_FBRD to configure the transfer baud rate.

Step 4 Configure UART_CR and UART_LCR_H to set the UART operating mode.

Step 5 Configure UART_IFLS to set the thresholds of TX and RX FIFOs.

Step 6 If the driver runs in interrupt mode, set UART_IMSC to enable the corresponding interrupt; if the driver runs in query mode, disable the generation of corresponding interrupts.

Step 7 Write 1 to UART_CR bit[0] to enable the UART.

----End

Data Transmission

To transmit data, perform the following steps:

Step 1 Write the data to be transmitted to UART_DR and start data transmission.

Step 2 In query mode, check the TX_FIFO status by reading UART_FR bit[5] during the continuous data transmission. According to the TX_FIFO status, determine whether to transmit data to TX_FIFO. In interrupt mode, check the TX_FIFO status by reading the corresponding interrupt status bits and then determine whether to transmit data to TX_FIFO.

Step 3 Check whether the UART transmits all data by reading UART_FR bit[7]. If UART_FR bit[7] is 1, the UART transmits all data.

----End

Data Reception

To receive data, perform the following steps:

- In query mode, detect the RX_FIFO status by reading UART_FR[rxfe] during data reception and then determine whether to read data from the RX_FIFO according to the RX_FIFO status.
- In interrupt mode, determine whether to read data from RX_FIFO according to corresponding interrupt status bits.

12.2.4.4 Data Transfer in DMA Mode

Initialization

To initialize the UART, perform the following steps:

Step 1 Configure the UART reference clock to deassert reset on the UART module.

Step 2 Write 0 to UART_CR bit[0] to disable the UART.

Step 3 Write values to UART_IBRD and UART_FBRD to configure the data transfer rate.

Step 4 Configure UART_CR and UART_LCR_H to set the UART operating mode.

Step 5 Configure UART_IFLS to set the TX and RX FIFO thresholds.

Step 6 If the driver runs in interrupt mode, set UART_IMSC to enable corresponding interrupts. If the driver runs in query mode, disable the generation of corresponding interrupts.

Step 7 Write 1 to UART_CR bit[0] to enable the UART.

----End

Data Transfer

To transmit data, perform the following steps (the following is an example using the DMA to transmit data):

Step 1 Configure the DMA data channel, including the transfer source address, transfer destination address, number of data items to be transferred, and transfer type. For details, see the description in 3.6 "DMA."

Step 2 Set UART_DMACR to 0x2 to enable the DMA transfer function of the UART.

Step 3 Check whether the data is transferred completely based on the interrupt report status of the DMA. If all data is transferred, disable the DMA transfer function of the UART.

----End

Data Reception

To receive data, perform the following steps (the following is an example using the DMA to receive data):

Step 1 Configure the DMA data channel, including data transfer source and destination addresses, data receive area address, number of data items to be transferred, and transfer type.

Step 2 Set UART_DMACR to 0x1 to enable the DMA receive function of the UART.

Step 3 Check whether the data is received completely by querying the DMA status. If all data is received, disable the DMA receive function of the UART.

----End

12.2.5 Register Summary

Hi3516C V300 provides three UART units: UART0, UART1 and UART2. Their base addresses are as follows:

- The base address of UART0 registers is 0x1210_0000.
- The base address of UART1 registers is 0x1210_1000.
- The base address of UART2 registers is 0x1210_2000.

Table 12-7 describes the UART registers.

Table 12-7 Summary of UART registers

Offset Address	Register	Description	Page
0x000	UART_DR	Data register	12-34
0x004	UART_RSR	Receive status register or error clear register	12-35
0x018	UART_FR	Flag register	12-36
0x024	UART_IBRD	Integral baud rate register	12-37
0x028	UART_FBRD	Fractional baud rate register	12-37
0x02C	UART_LCR_H	Line control register	12-38
0x030	UART_CR	Control register	12-39
0x034	UART_IFLS	Interrupt FIFO threshold select register	12-41
0x038	UART_IMSC	Interrupt mask register	12-42
0x03C	UART_RIS	Raw interrupt status register	12-43

Offset Address	Register	Description	Page
0x040	UART_MIS	Masked interrupt status register	12-44
0x044	UART_ICR	Interrupt clear register	12-45
0x048	UART_DMACR	DMA control register	12-46

12.2.6 Register Description

UART_DR

UART_DR is a UART data register that stores the received data and the data to be transmitted. The receive status can be queried by reading this register.

Offset Address	Register Name	Total Reset Value
0x000	UART_DR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe	data							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:12]	RO	reserved	Reserved
[11]	RO	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. That is, a data segment is received when the RX FIFO is full.
[10]	RO	be	Break error 0: No break error occurs. 1: A break error occurs. That is, the time of RX data input signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[9]	RO	pe	Parity error 0: No parity error occurs. 1: A parity error occurs.
[8]	RO	fe	Frame error 0: No frame error occurs. 1: A frame error (namely, stop bit error) occurs.
[7:0]	RW	data	Data received and to be transmitted

UART_RSR

UART_RSR is a receive status register or error clear register.

- It acts as the receive status register when being read.
- It acts as the error clear register when being written.

You can query the receive status by reading UART_DR. The status information about the break, frame, and parity read from UART_DR has priority over that read from UART_RSR. That is, the status read from UART_DR changes faster than that read from UART_RSR.

UART_RSR is reset when any value is written to it.

Offset Address	Register Name	Total Reset Value
0x004	UART_RSR	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved				oe	be	pe	fe
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:4]	RO	reserved	Reserved
[3]	RW	oe	Overflow error 0: No overflow error occurs. 1: An overflow error occurs. When the FIFO is full, the next data segment cannot be written to the FIFO and an overflow occurs in the shift register. Therefore, the contents in the FIFO are valid. In this case, the CPU must read the data immediately to spare the FIFO.
[2]	RW	be	Break error 0: No break error occurs. 1: A break error occurs. A break error occurs when the time of the RX data signal keeping low is longer than a full word transfer. A full word consists of a start bit, a data bit, a parity bit, and a stop bit.
[1]	RW	pe	Parity error 0: No parity error occurs. 1: A parity error occurs when the received data is checked. In FIFO mode, the error is associated with the data at the top of the FIFO.
[0]	RW	fe	Frame error 0: No frame error occurs. 1: The stop bit of the received data is incorrect. The valid stop bit is 1.

UART_FR

UART_FR is a UART flag register.

Offset Address	Register Name	Total Reset Value
0x018	UART_FR	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								txfe	rxff	txff	rxfe	busy	reserved		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RO	txfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the TX holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the TX FIFO is empty.
[6]	RO	rxff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the RX holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the RX FIFO is full.
[5]	RO	txff	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the TX holding register is full. If UART_LCR_H [fen] is 1, this bit is set to 1 when the TX FIFO is full.
[4]	RO	rxfe	The definition of the bit is determined by the status of UART_LCR_H [fen]. If UART_LCR_H [fen] is 0, this bit is set to 1 when the RX holding register is empty. If UART_LCR_H [fen] is 1, this bit is set to 1 when the RX FIFO is empty.
[3]	RO	busy	UART busy/idle status 0: The UART is idle or data transmission is complete. 1: The UART is busy in transmitting data. If the bit is set to 1, the status is kept until the entire byte (including all stop bits) is transmitted from the shift register. Regardless of whether the UART is enabled, this bit is set to 1 when the TX FIFO is not empty.
[2:0]	RO	reserved	Reserved

UART_IBRD

UART_IBRD is an integral baud rate register.

Offset Address	Register Name	Total Reset Value
0x024	UART_IBRD	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	baud divint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	baud divint	Clock frequency divider corresponding to the integral part of the baud rate. All bits are cleared after reset.

UART_FBRD

UART_FBRD is a fractional baud rate register.

CAUTION

- The values of UART_IBRD and UART_FBRD can be updated only after the current data is transmitted and received completely.
- The minimum clock frequency divider is 1 and the maximum divider is 65,535 (2^{16} - 1). That is, UART_IBRD cannot be 0 and UART_FBRD is ignored if UART_IBRD is 0. Similarly, if UART_IBRD is equal to 65,535 (0xFFFF), UART_IBRD must be 0. If UART_FBRD is greater than 0, the data fails to be transmitted or received.

Offset Address	Register Name	Total Reset Value
0x028	UART_FBRD	0x00

Bit	7	6	5	4	3	2	1	0
Name	reserved		baud divfrac					
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:6]	RO	reserved	Reserved
[5:0]	RW	band divfrac	Clock frequency divider corresponding to the fractional part of the baud rate. All bits are cleared after reset.

UART_LCR_H

UART_LCR_H is a line control register. The registers UART_LCR_H, UART_IBRD, and UART_FBRD are combined to form a 30-bit register. If UART_IBRD and UART_FBRD are updated, UART_LCR_H must be updated at the same time.

Offset Address	Register Name	Total Reset Value
0x02C	UART_LCR_H	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								sps	wlen		fen	stp2	eps	pen	brk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RO	reserved	Reserved
[7]	RW	sps	Parity select When bit 1, bit 2, and bit 7 of this register are set to 1, the parity bit is 0 during transmission and detection. When bit 1 and bit 7 of this register are set to 1 and bit 2 is set to 0, the parity bit is 1 during transmission and detection. When bit 1, bit 2, and bit 7 are cleared, the stick parity bit is disabled.
[6:5]	RW	wlen	Count of bits in a transmitted or received frame 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
[4]	RW	fen	TX/RX FIFO enable 0: disabled 1: enabled
[3]	RW	stp2	2-bit stop bit at the end of a transmitted frame 0: There is no 2-bit stop bit at the end of the transmitted frame. 1: There is a 2-bit stop bit at the end of the transmitted frame. The RX logic does not check for the 2-bit stop bit during data reception.
[2]	RW	eps	Parity select during data transmission and reception 0: The odd parity is generated or checked during data transmission and reception. 1: The even parity is generated or checked during data transmission and reception. When UART_LCR_H[fen] is 0, this bit becomes invalid.
[1]	RW	pen	Parity enable 0: The parity is disabled.

			1: The parity is generated on the TX side and checked on the RX side.
[0]	RW	brk	Break transmit 0: invalid 1: After the current data transmission is complete, UTXD outputs low level continuously. **NOTE** This bit must retain 1 during the period of at least two full frames to ensure the break command is executed properly. In general, the bit must be set to 0.

UART_CR

UART_CR is a UART control register.

To configure UART_CR, perform the following steps:

Step 1 Write 0 to UART_CR[uarten] to disable the UART.

Step 2 Wait until the current data transmission or reception is complete.

Step 3 Clear UART_LCR_H[fen].

Step 4 Configure UART_CR.

Step 5 Write 1 to UART_CR[uarten] to enable the UART.

----End

Offset Address	Register Name	Total Reset Value
0x030	UART_CR	0x0300

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ctsen	rtsen	reserved		rts	dtr	rxe	txe	lbe	reserved						uarten
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	ctsen	CTS hardware flow control enable 0: disabled 1: enabled. Data is transmitted only when the nUARTCTS signal is valid.
[14]	RW	rtsen	RTS hardware flow control enable 0: disabled 1: enabled. The data reception request is raised only when the RX FIFO has available space.
[13:12]	RO	reserved	Reserved
[11]	RW	rts	Request transmit

			This bit is the inversion of the status output signal nUARTRTS of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[10]	RW	dtr	Data transmit ready This bit is the inversion of the status output signal nUARTDTR of the UART modem. 0: The output signal retains. 1: When this bit is set to 1, the output signal is 0.
[9]	RW	rxe	UART receive enable 0: disabled 1: enabled If the UART is disabled during data reception, the current data reception is stopped abnormally.
[8]	RW	txe	UART transmit enable 0: disabled 1: enabled If the UART is disabled during data transmission, the current data transmission is stopped abnormally.
[7]	RW	lbe	Loopback enable 0: disabled 1: UARTTXD is looped back to UARTRXD.
[6:1]	RO	reserved	Reserved
[0]	RW	uarten	UART enable 0: disabled 1: enabled If the UART is disabled during data reception and transmission, the data transfer is stopped abnormally.

UART_IFLS

UART_IFLS is an interrupt FIFO threshold select register. It is used to set a threshold for triggering a FIFO interrupt (UART_TXINTR or UART_RXINTR).

Offset Address	Register Name	Total Reset Value
0x034	UART_IFLS	0x0012

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										rxiflsel			txiflsel		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Bits	Access	Name	Description
[15:6]	RO	reserved	Reserved
[5:3]	RW	rxiflsel	RX interrupt FIFO threshold select. An RX interrupt is triggered when any of the following conditions is met: 000: RX FIFO ≥ 1/8 full 001: RX FIFO ≥ 1/4 full 010: RX FIFO ≥ 1/2 full 011: RX FIFO ≥ 3/4 full 100: RX FIFO ≥ 7/8 full 101–111: reserved
[2:0]	RW	txiflsel	TX interrupt FIFO threshold select. A TX interrupt is triggered when any of the following conditions is met: 000: TX FIFO ≤ 1/8 full 001: TX FIFO ≤ 1/4 full 011: TX FIFO ≤ 3/4 full 010: TX FIFO ≤ 1/2 full 100: TX FIFO ≤ 7/8 full 101–111: reserved

UART_IMSC

UART_IMSC is an interrupt mask register. It is used to mask interrupts.

Offset Address	Register Name	Total Reset Value
0x038	UART_IMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeim	beim	peim	feim	rtim	txim	rxim	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RW	oeim	Mask status of the overflow error interrupt 0: masked 1: not masked
[9]	RW	beim	Mask status of the break error interrupt 0: masked 1: not masked
[8]	RW	peim	Mask status of the parity interrupt 0: masked 1: not masked
[7]	RW	feim	Mask status of the frame error interrupt 0: masked 1: not masked
[6]	RW	rtim	Mask status of the RX timeout interrupt 0: masked 1: not masked
[5]	RW	txim	Mask status of the TX interrupt 0: masked 1: not masked
[4]	RW	rxim	Mask status of the RX interrupt 0: masked 1: not masked
[3:0]	RO	reserved	Reserved

UART_RIS

UART_RIS is a raw interrupt status register. The contents of this register are not affected by the UART_IMSC register.

Offset Address	Register Name	Total Reset Value
0x03C	UART_RIS	0x0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeris	beris	peris	feris	rtris	txris	rxris	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oeris	Status of the raw overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	beris	Status of the raw break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	peris	Status of the raw parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	feris	Status of the raw error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtris	Status of the raw RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txris	Status of the raw TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxris	Status of the raw RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

UART_MIS

UART_MIS is a masked interrupt status register. The contents of this register are the results obtained after the raw interrupt status is ANDed with the interrupt mask status.

Offset Address	Register Name	Total Reset Value
0x040	UART_MIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oemis	bemis	pemis	femis	rtmis	txmis	rxmis	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	RO	oemis	Status of the masked overflow error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	bemis	Status of the masked break error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	pemis	Status of the masked parity interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[7]	RO	femis	Status of the masked error interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[6]	RO	rtmis	Status of the masked RX timeout interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[5]	RO	txmis	Status of the masked TX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[4]	RO	rxmis	Status of the masked RX interrupt 0: No interrupt is generated. 1: An interrupt is generated.
[3:0]	RO	reserved	Reserved

UART_ICR

UART_ICR is an interrupt clear register. When 1 is written to it, the corresponding interrupt is cleared. Writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x044	UART_ICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved					oeic	beic	peic	feic	rtic	txic	rxic	reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:11]	RO	reserved	Reserved
[10]	WO	oeic	Overflow error interrupt clear 0: invalid 1: cleared
[9]	WO	beic	Break error interrupt clear 0: invalid 1: cleared
[8]	WO	peic	Parity interrupt clear 0: invalid 1: cleared
[7]	WO	feic	Error interrupt clear 0: invalid 1: cleared
[6]	WO	rtic	RX timeout interrupt clear 0: invalid 1: cleared
[5]	WO	txic	TX interrupt clear 0: invalid 1: cleared
[4]	WO	rxic	RX interrupt clear 0: invalid 1: cleared
[3:0]	RO	reserved	Reserved

UART_DMACR

UART_DMACR is a DMA control register. It is used to enable or disable the DMAs of the TX and RX FIFOs.

Offset Address	Register Name	Total Reset Value
0x048	UART_DMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													dmaonerr	txdmae	rxdmae
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:3]	RO	reserved	Reserved
[2]	RW	dmaonerr	DMA enable for the RX channel when the UART error interrupt (UARTEINTR) occurs. 0: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is valid. 1: When UARTEINTR is valid, the DMA output request (UARTRXDMASREQ or UARRTXDMABREQ) of the RX channel is invalid.
[1]	RW	txdmae	TX FIFO DMA enable 0: disabled 1: enable
[0]	RW	rxdmae	RX FIFO DMA enable 0: disabled 1: enable

12.3 SPI

12.3.1 Overview

The serial peripheral interface (SPI) controller implements serial-to-parallel conversion and parallel-to-serial conversion, and serves as a master to communicate with peripherals in synchronous and serial modes. The SPI controller supports three types of peripheral interfaces including the SPI, TI synchronous serial interface, and MicroWire interface.

12.3.2 Features

CAUTION

- Hi3516C V300 has two serial peripheral interfaces (SPIs). SPI0 supports a chip select (CS), whereas SPI1 supports two CSs.
- Hi3516C V300 SPIs are master interfaces. The working reference clock is 100 MHz. SPI_CLK output by the SPI supports the maximum working frequency of 50 MHz.

The SPI controller has the following features:

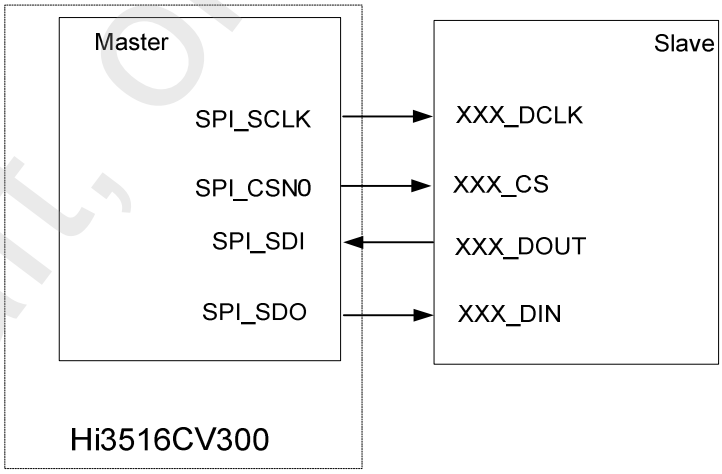
- Supports programmable frequency of the interface clock.
- Supports two separate FIFOs. One acts as an RX FIFO and the other one acts as a TX FIFO. Each of them is 16-bit wide and 256-location deep.
- Supports programmable serial data frame length: 4 bits to 16 bits.
- Provides internal loopback test mode.
- Supports the direct memory access (DMA) operation.
- Supports three types of peripheral interfaces including the SPI, MicroWire interface, and TI synchronous serial interface.
- Supports SPI in full-duplex mode and configurable clock polarity and phase.
- Supports MicroWire in half-duplex mode.
- Supports TI synchronous serial interface in full-duplex mode.

12.3.3 Function Description

Typical Application

Figure 12-8 shows the application block diagram when the SPI is connected to a slave device. The default CS pin SPI_CSN0 is used.

Figure 12-8 Application block diagram when the SPI is connected to a single slave device



12.3.4 Peripheral Bus Timings

The meanings of the abbreviations and acronyms in Figure 12-9 to Figure 12-16 are as follows:

- MSB: most significant bit
- LSB: least significant bit
- Q: Q is an undefined signal

SPI

NOTE

SPO indicates the polarity of SPICLKOUT and SPH indicates the phase of SPICLKOUT. They correspond to SPICR0 bit[7:6].

1. **SPO = 0, SPH = 0**

Figure 12-9 shows the SPI single frame format.

Figure 12-9 SPI single frame format (SPO = 0, SPH = 0)

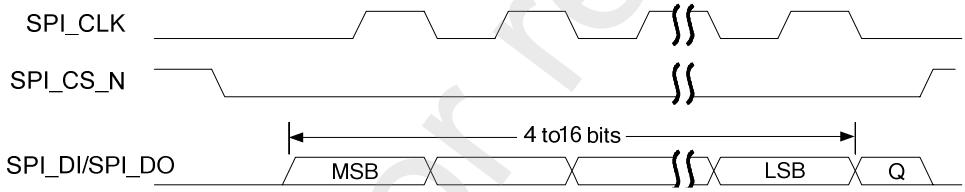
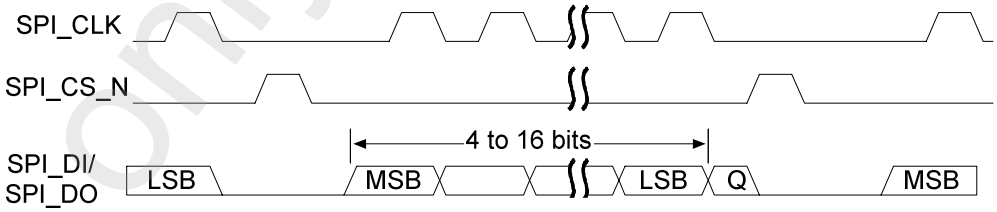


Figure 12-10 shows the SPI continuous frame format.

Figure 12-10 SPI continuous frame format (SPO = 0, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the RX data line SPI_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. At this time, both the master and slave data become

valid. The SPI_CLK pin changes to high level in the next half SPI_CLK clock cycle. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For continuous transfer, the SPI_CS_N signal must pull up the SPI_CLK clock by one clock cycle between the transfers of two words. When SPH is 0, the slave select pin fixes the data of the internal serial device register. Therefore, the master device must pull up the SPI_CS_N signal between the transfers of two words in continuous transfer. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

2. **SPO = 0, SPH = 1**

Figure 12-11 shows the SPI single frame format.

Figure 12-11 SPI single frame format (SPO = 0, SPH = 1)

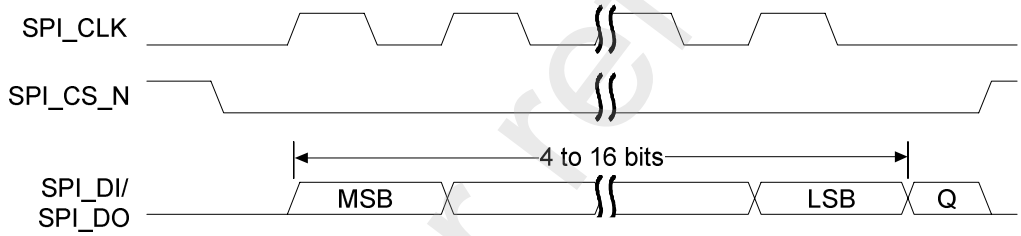
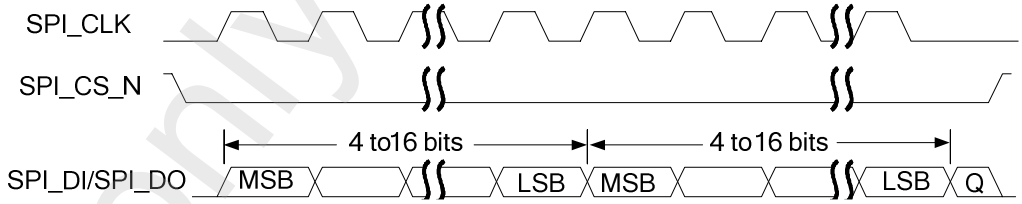


Figure 12-12 shows the SPI continuous frame format.

Figure 12-12 SPI continuous frame format (SPO = 0, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. The master and slave data become valid on their respective transfer line half SPI_CLK clock cycle later. In addition, SPI_CLK becomes valid from the first rising edge. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

For a continuous transfer, SPI_CS_N remains low between the transfers of two words. When the continuous transfer ends, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

3. **SPO = 1, SPH = 0**

Figure 12-13 shows the SPI single frame format.

Figure 12-13 SPI single frame format (SPO = 1, SPH = 0)

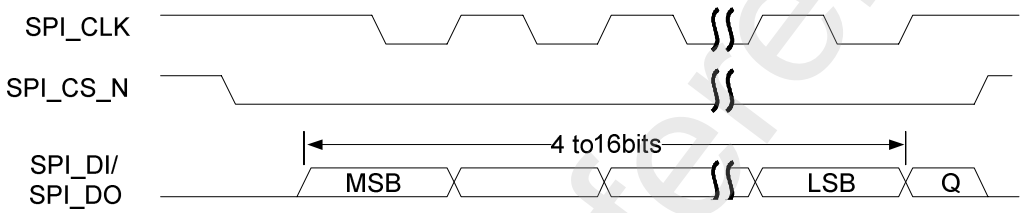
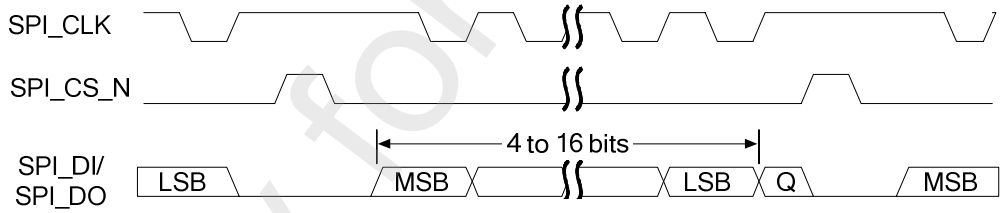


Figure 12-14 shows the SPI continuous frame format.

Figure 12-14 SPI continuous frame format (SPO = 1, SPH = 0)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. The data from the slave device is transferred to the RX data line SPI_DI of the master device immediately. Half SPI_CLK clock cycle later, the valid master data is transmitted to SPI_DO. After another half SPI_CLK clock cycle, the SPI_CLK master pin is set to low. Then, data is captured on the falling edge and is transmitted on the rising edge of the SPI_CLK clock.

If a single word is transferred, SPI_CS_N is restored to high level after one SPI_CLK clock since the data of the last bit is captured.

For a continuous transfer, the SPI_CS_N signal must be pulled up between the transfers of two words. This is because that when SPH is 0, the slave select pin fixes the data of the internal serial device register. SPI_CS_N is restored to high level one SPI_CLK clock later after the last bit is captured.

4. **SPO = 1, SPH = 1**

Figure 12-15 shows the SPI single frame format.

Figure 12-15 SPI single frame format (SPO = 1, SPH = 1)

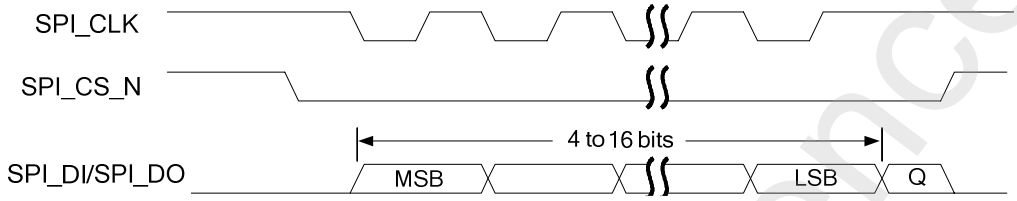
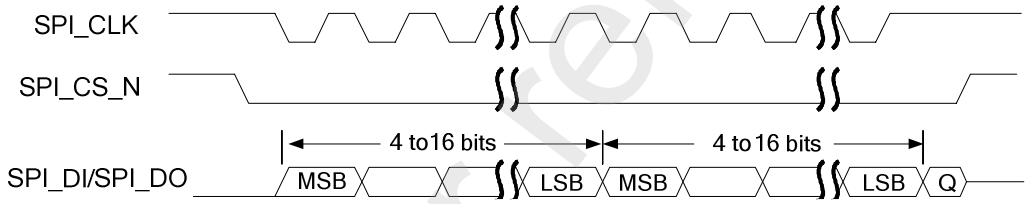


Figure 12-16 shows the SPI continuous frame format.

Figure 12-16 SPI continuous frame format (SPO = 1, SPH = 1)



When the SPI is idle in this mode:

- The SPI_CLK signal is set to high.
- The SPI_CS_N signal is set to high.
- The TX data line SPI_DO is forced to low.

When the SPI is enabled and valid data is ready in the TX FIFO, data transfer starts if the SPI_CS_N signal is set to low. Half SPI_CLK clock cycle later, the master data and slave data are valid on respective transfer line. In addition, SPI_CLK becomes valid from a falling edge of SPI_CLK. Then, data is captured on the rising edge and is transmitted on the falling edge of the SPI_CLK clock. If a single word is being transmitted, SPI_CS_N is restored to high level one SPI_CLK clock cycle later after the last bit is captured.

For a continuous transfer, the SPI_CS_N signal remains low. SPI_CS_N is restored to high level one SPI_CLK clock cycle after the last bit is captured. For a continuous transfer, SPI_CS_N remains low during transfer. The method of ending data transfer is the same as that in single transfer mode.

5. **Interface timings**

Figure 12-17 SPI timings

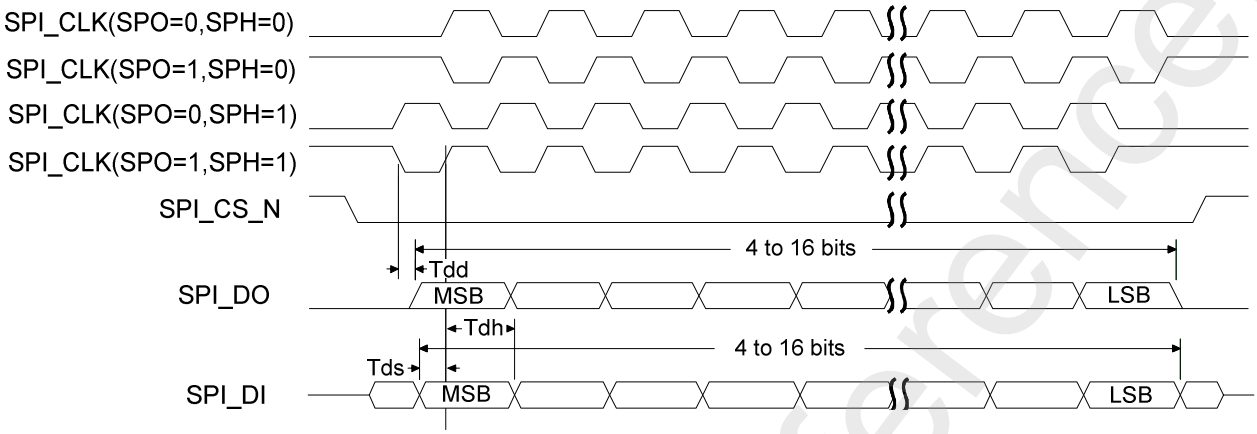


Table 12-8 Timing parameters of the SPI

Parameter	Description	Min	Max	Unit
Tdd	Output data delay	–3.5	5	ns
Tds	Input control signal setup time	23	None	ns
Tdh	Input control signal hold time	0	None	ns

TI Synchronous Serial Interface

Figure 12-18 shows the TI synchronous serial single frame format.

Figure 12-18 TI synchronous serial single frame format

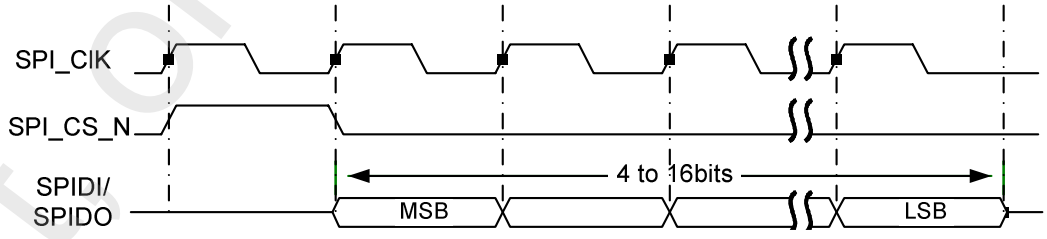
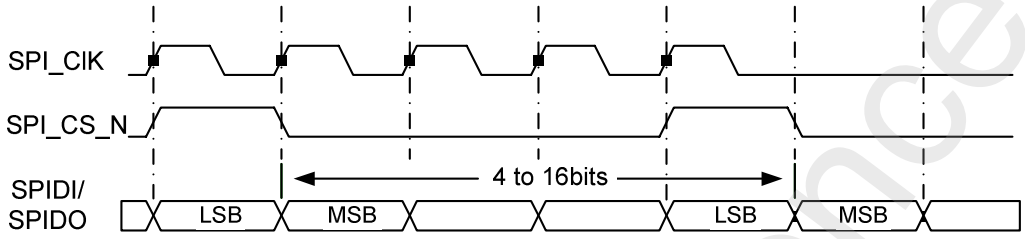


Figure 12-19 shows the TI synchronous serial continuous frame format.

Figure 12-19 TI synchronous serial continuous frame format



When the SPI is idle in this mode:

- The SPI_CK signal is set to low.
- The SPI_CS_N signal is set to low.
- The transfer data line SPI_DO retains high impedance.

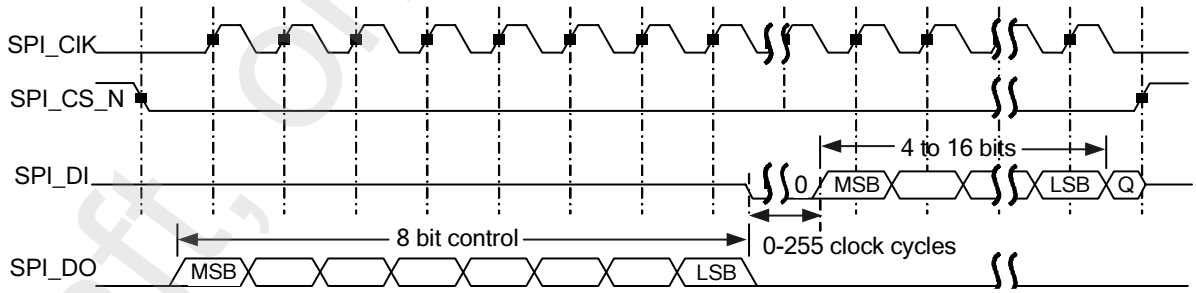
If there is data in the TX FIFO, SPI_CS_N generates a high-level pulse in one SPI_CK clock cycle. Then, the data to be transmitted is transferred from the TX FIFO to the TX logic serial shift register. In addition, the MSBs of the data frames with the length of 4–16 bits are shifted and output from SPI_DO on the next rising edge of the SPI_CK clock. Similarly, the MSB of the data received from the external serial slave device is shifted and input from the SPI_DI pin.

The SPI and off-chip serial device stores the data in the serial shift register on the falling edge of the SPI_CK clock. The RX serial register transmits the data to the RX FIFO on the rising edge of the first SPI_CK clock after receiving the LSB.

National Semiconductor Microwire Interface

Figure 12-20 shows the national semiconductor microwire single frame format.

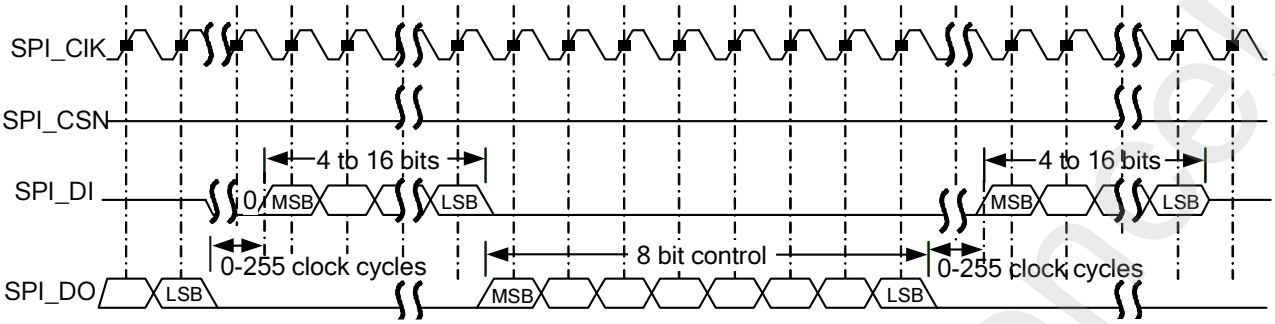
Figure 12-20 National semiconductor microwire single frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

Figure 12-21 shows the national semiconductor microwire continuous frame format.

Figure 12-21 National semiconductor microwire continuous frame format



0 to 255 clock cycles can be delayed between the end of SPI_DO LSB and the start of SPI_DI MSB.

The microwire format is similar to the SPI format because both of them use the technology of transferring master-slave information. The only difference is that the SPI works in full-duplex mode and the microwire interface works in half-duplex mode. Before the SPI transmits serial data to the external chip, an 8-bit control word needs to be added. In this process, the SPI does not receive any data. After data transfer is complete, the external chip decodes the received data. One clock cycle later after 8-bit control information is transmitted, the slave device starts to respond to the required data. The returned data length is 4 bits to 16 bits, and the length of the entire frame is 13 bits to 25 bits.

When the SPI is idle in this mode:

- The SPI_CLK signal is set to low.
- The SPI_CS_N signal is set to high level.
- The TX data signal SPI_DO is forced to low level.

Writing one control byte to the TX FIFO starts a data transfer. The data transfer is triggered on a falling edge of SPI_CS_N. The data of the TX FIFO is sent to the serial shift register. The MSB of the 8-bit control frame is transmitted to the SPI_DO pin. During frame transfer, SPI_CS_N remains low. Whereas SPI_DI retains high impedance.

The off-chip serial slave device latches the data to the serial shift register on each rising edge of the SPI_CLK clock. After the slave device latches the data of the last bit, the slave device starts to decode the received data in the next clock cycle. Then, the slave device provides the data required by the SPI. Each bit is written to SPI_DI on the falling edge of the SPI_CK clock. For a single data transfer, SPI_CS_N is pulled up at the end of the frame one clock cycle after the last bit is written to the RX serial register. In this way, the RX data is transmitted to the RX FIFO.

The start and end for a continuous data transfer are the same as those for a signal data transfer. During the continuous data transfer, SPI_CS_N retains low and the data transferred is continuous. The control word of the next frame is adjacent to the LSB of the previous frame. When the LSB of the frame is latched to the SPI, each received value is originated from the receive shift register on the falling edge of the SPI_CLK clock.

12.3.5 Operating Mode

Working Modes

The SPI working modes include the data transmission in the interrupt or query mode and the data transmission in the DMA mode.

Clock and Reset

The frequency of the output SPI clock is calculated as follows:

$F_{sspclkout} = F_{sspclk}/[CPSDVSR \times (1 + SCR)]$

Fsspclk is the working reference clock of the SPI and its value is 100 MHz.

For details about CPSDVSR and SCR, query the corresponding registers.

The SPI of Hi3516C V300 supports separately soft reset, which is controlled by the PERI_CRG57 bit[6:5] register. To disable the soft reset on the SPI, write 0 to corresponding bits. To enable soft-reset on the SPI, write 1 to corresponding bits. The default value is 0 when the SPI is powered on.

Interrupts

The SPI has five interrupts. Four of them have separate interrupts sources and maskable and active high.

- SPIRXINTR

  RX FIFO interrupt request. When there are four or more valid data segments in the RX FIFO, the interrupt is set to 1.

- SPITXINTR

  TX FIFO interrupt request. When there are four or less valid data segments in the TX FIFO, the interrupt is set to 1.

- SPIRORINTR

  RX overrun interrupt request. When the FIFO is full and new data is written to the FIFO, the FIFO is overrun and the interrupt is set to 1. In this case, the data is written to the RX shift register rather than the FIFO.

- SPIRTINTR

  RX timeout interrupt request. When the RX FIFO is not empty and the SPI is idle for more than a fixed 32-bit cycle, the interrupt is set to 1.

  It indicates that data in the RX FIFO needs to be transmitted. When the RX FIFO is empty or new data is transmitted to SPIRXD, the interrupt is cleared. The interrupt can also be cleared by writing to the SPIICR[RTIC] register.

- SPIINTR

  Combined interrupt. This interrupt is obtained by performing an OR operation on the preceding four interrupts. If any of the preceding four interrupts is set to 1 and enabled, SPIINTR is set to 1.

For details about how to connect the SPIINTR of SPI, see "Interrupts" in this section.

Initialization

The initialization is implemented as follows:

Step 1 Write 0 to SPICR1[1] to disable the SPI.

Step 2 Write to SPICR0 to set the parameters such as the frame format and transfer data bit width.

Step 3 Configure SPICPSR to set the required clock divider.

Step 4 In the interrupt mode, configure SPIIMSC to enable the corresponding interrupts or disable the generation of corresponding interrupts in query or DMA mode.

Step 5 Configure SPITXFIFOCR and SPIRXFIFOCR in interrupt or DMA mode.

Step 6 Configure SPIDMACR to enable the DMA function of the SPI in DMA mode.

----End

Data Transfer in Query Mode

The full status of the TX or RX FIFO is not considered, because the depth of the TX FIFO or RX FIFO is 512.

Perform the following steps:

Step 1 Write 1 to SPICR1[1] to enable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Poll SPISR until SPISR[4] is 0, SPISR[0] is 1, and SPISR[2] is 1. If SPISR[4] is 0, the bus is busy; if SPISR[0] is 1, the TX FIFO is empty; if SPISR[2] is 1, the RX FIFO is not empty.

Step 4 Read data until the RX FIFO is empty. You can check whether the RX FIFO is empty by querying SPISR[2].

CAUTION

The SPI/Microwire has full-duplex features. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 5 Write 0 to SPICR1[1] to disable the SPI.

----End

Data Transfer in Interrupt Mode

Perform the following steps:

Step 1 Write 1 to SPICR1[1] to disable the SPI.

Step 2 Write the data to be transmitted to SPIDR continuously.

Step 3 Wait for the interrupt SPIRXINTR and read data in cyclic mode until all data is read.

Note that the full-duplex features of the SPI/Microwire. That is, a data segment is received after a data segment is transmitted. Even if only data is transmitted, the RX FIFO must be cleared.

Step 4 Write 0 to SPICR1[1] to disable the SPI.

----End

Data Transfer in DMA Mode

Perform the following steps:

Step 1 Obtain a DMAC channel.

Step 2 Write 1 to SPICR1[1] to disable the SPI.

Step 3 Transmit data.

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SPI TX FIFO for the data transfer.
3. Check whether all data is transmitted by viewing the DMA interrupt. If all data is transmitted, disable the DMA transmit function of the SPI.

Step 4 Receive data

1. Configure the parameters of the configuration register and control register related to the DMAC channel.
2. Start the DMAC and respond to the DMA request of the SSP RX FIFO for the data transfer.
3. Check whether all data is received by viewing the DMA interrupt. If all data is received, disable the DMA receive function of the SPI.

Step 5 Write 0 to SPICR1[1] to disable the SPI.

----End

12.3.6 Register Summary

Table 12-9 describes the registers.

- The base address of SPI registers is 0x1212_0000.
- The base address of SPI registers is 0x1212_1000.

Table 12-9 Summary of SPI registers

Offset Address	Register	Description	Page
0x000	SPICR0	Control register 0	12-58
0x004	SPICR1	Control register 1	12-59
0x008	SPIDR	Data register	12-60

Offset Address	Register	Description	Page
0x00C	SPISR	Status register	12-61
0x010	SPICPSR	Clock divider register	12-61
0x014	SPIIMSC	Interrupt mask register	12-62
0x018	SPIRIS	Raw interrupt status register	12-63
0x01C	SPIMIS	Masked interrupt status register	12-63
0x020	SPIICR	Interrupt clear register	12-64
0x024	SPIDMACR	DMA control register	12-64
0x028	SPITXFIFOCR	TX FIFO control register	12-65
0x02C	SPIRXFIFOCR	RX FIFO control register	12-66

12.3.7 Register Description

SPICR0

SPICR0 is SPI control register 0.

Offset Address	Register Name	Total Reset Value
0x000	SPICR0	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCR								SPH	SPO	FRF		DSS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	SCR	Serial clock rate, ranging from 0 to 255. The value of the SCR is used to generate the TX and RX bit rates of the SPI. The formula is as follows: FSSPCLK/(CPSDVSR (1 + SCR). CPSDVSR is an even ranging from 2 to 254, and it is configured by SPICPSR.
[7]	RW	SPH	SPI output clock phase. For details, see section 12.3.4 "Peripheral Bus Timings."
[6]	RW	SPO	SPI output clock polarity. For details, see section 12.3.4 "Peripheral Bus Timings."
[5:4]	RW	FRF	Frame format select. 00: Motorola SPI frame format 01: TI synchronous serial frame format 10: National microwire frame format 11: reserved

[3:0]	RW	DSS	Data width 0x3: 4 bits 0x8: 9 bits 0xD: 14 bits 0x4: 5 bits 0x9: 10 bits 0xE: 15 bits 0x5: 6 bits 0xA: 11 bits 0xF: 16 bits 0x6: 7 bits 0xB: 12 bits 0x7: 8 bits 0xC: 13 bits Other values: reserved

SPICR1

SPICR1 is SPI control register 1.

Offset Address	Register Name	Total Reset Value
0x004	SPICR1	0x7F00

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WaitEn	WaitVal							reserved	mode_altasens	reserved	BigEnd	reserved	MS	SSE	LBM
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15]	RW	WaitEn	Wait enable. This bit is valid when the SPICR0[FRF] is set to the national microwire frame format. 0: disabled 1: enabled
[14:8]	RW	WaitVal	Number of waiting beats between read and write when in the national microwire frame format. When WaitEn is 1 and the frame format is national microwire, WaitVal is valid.
[7]	RW	reserved	Reserved

[6]	RO	mode_altasens	0: The CS signal is automatically generated by the chip logic based on the selected timing. 1: The CS signal is controlled by the SPI enable when the Motorola SPI frame format is used. If the SPI is enabled, the CS signal is pulled down; otherwise, the CS signal is pulled up.
[5]	RO	reserved	Reserved
[4]	RW	BigEnd	Data endian mode 0: little endian 1: big endian
[3]	RW	reserved	Reserved
[2]	RW	MS	Master or slave mode. This bit can be changed only when the SPI is disabled. 0: master mode (default value) 1: reserved
[1]	RW	SSE	SPI enable 0: disabled 1: enabled
[0]	RW	LBM	Loopback mode 0: A normal serial port operation is enabled. 1: The output of the TX serial shift register is connected to the input of the RX serial shift register.

SPIDR

SPIDR is a data register.

Offset Address	Register Name	Total Reset Value
0x008	SPIDR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:0]	RW	DATA	TX or RX FIFO Read: RX FIFO Write: TX FIFO If the data is less than 16 bits, the data must be aligned to the right. The TX logic ignores the unused upper bits, and the RX logic automatically aligns the data to the right.

SPISR

SPISR is a status register.

Offset Address	Register Name	Total Reset Value
0x00C	SPISR	0x0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											BSY	RFF	RNE	TNF	TFE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bits	Access	Name	Description
[15:5]	RW	reserved	Reserved
[4]	RW	BSY	SPI busy flag 0: idle 1: busy
[3]	RW	RFF	Whether the RX FIFO is full 0: not full 1: full
[2]	RW	RNE	Whether the RX FIFO is not empty 0: empty 1: not empty
[1]	RW	TNF	Whether the TX FIFO is not full 0: full 1: not full
[0]	RW	TFE	Whether the TX FIFO is empty 0: not empty 1: empty

SPICPSR

SPICPSR is a clock divider register.

Offset Address	Register Name	Total Reset Value
0x010	SPICPSR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								CPSDVSR							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:8]	RW	reserved	Reserved

[7:0]	RW	CPSDVSR	Clock divider. The value must be an even ranging from 2 to 254. It depends on the frequency of the SPI reference clock.

SPIIMSC

SCIIMSC is an interrupt mask register. The value 0 indicates an interrupt is masked and the value1 indicates an interrupt is not masked.

Offset Address	Register Name	Total Reset Value
0x014	SPIIMSC	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXIM	RXIM	RTIM	RORIM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RW	reserved	Reserved
[3]	RW	TXIM	TX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the TX FIFO. 1: The interrupt is not masked when only half of or less data is left in the TX FIFO.
[2]	RW	RXIM	RX FIFO interrupt mask 0: The interrupt is masked when only half of or less data is left in the RX FIFO. 1: The interrupt is not masked when only half of or less data is left in the RX FIFO.
[1]	RW	RTIM	RX timeout interrupt mask 0: masked 1: not masked
[0]	RW	RORIM	RX overflow interrupt mask 0: masked 1: not masked When the value is 1, the hardware stream control function is enabled. That is, when the RX FIFO is full, the SPI stops transmitting data.

SPIRIS

SPIRIS is a raw interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x018	SPIRIS	0x0008

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXRIS	RXRIS	RTRIS	RORRIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXRIS	Raw TX FIFO interrupt status
[2]	RO	RXRIS	Raw RX FIFO interrupt status
[1]	RO	RTRIS	Raw RX timeout interrupt status
[0]	RO	RORRIS	Raw RX overflow interrupt status

SPIMIS

SPIMIS is a masked interrupt status register. The value 0 indicates no interrupts are generated, and the value 1 indicates interrupts are generated.

Offset Address	Register Name	Total Reset Value
0x01C	SPIMIS	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												TXMIS	RXMIS	RTMIS	RORMIS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:4]	RO	reserved	Reserved
[3]	RO	TXMIS	Status of the masked TX FIFO interrupt
[2]	RO	RXMIS	Status of the masked RX FIFO interrupt
[1]	RO	RTMIS	Status of the masked RX timeout interrupt
[0]	RO	RORMIS	Status of the masked RX overflow interrupt

SPIICR

SCIICR is an interrupt clear register. Writing 1 clears an interrupt, and writing 0 has no effect.

Offset Address	Register Name	Total Reset Value
0x020	SPIICR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														RTIC	RORIC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	RO	reserved	Reserved
[1]	RO	RTIC	RX timeout interrupt clear
[0]	RO	RORIC	RX overflow interrupt clear

SPIDMACR

SCIDMACR is a DMA control register.

Offset Address	Register Name	Total Reset Value
0x024	SPIDMACR	0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														TXDMAE	RXDMAE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[15:2]	WO	reserved	Reserved
[1]	WO	TXDMAE	DMA TX FIFO enable 0: disabled 1: enabled
[0]	WO	RXDMAE	DMA RX FIFO enable 0: disabled 1: enabled

SPITXFIFOCR

SPITXFIFOCR is a TX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x028	SPITXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										TXINTSize			DMATXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved
[5:3]	RW	TXINTSize	Threshold for generating the TX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the value of TXINTSize, TXRIS is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMATXBRSize	Threshold for generating the TX FIFO request DMA transfer burst. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – DMATXBRSize), DMATXBREQ is valid. The width of the TX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 128

SPIRXFIFOCR

SPIRXFIFOCR is an RX FIFO control register.

Offset Address	Register Name	Total Reset Value
0x02C	SPIRXFIFOCR	0x0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved										RXINTSize			DMARXBRSize		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bits	Access	Name	Description
[15:6]	RW	reserved	Reserved
[5:3]	RW	RXINTSize	Threshold for generating the RX FIFO request interrupt. That is, when the number of data segments in the TX FIFO is less than or equal to the configured value (256 – RXINTSize), RXRIS is valid. The width of the RX FIFO is 16 bits. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 64 111: 64
[2:0]	RW	DMARXBRSize	Burst transfer threshold. When this threshold is reached, the RX FIFO asks the DMA to perform a burst transfer. That is, when number of data segments in the TX FIFO is less than or equal to the value of DMARXBRSize, DMARXBREQ is valid. 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 224

12.4 3-Wire SPI

12.4.1 Overview

Hi3516C V300 provides one 3-wire SPI for interconnection with the MN34120 sensor.

12.4.2 Operating Mode

The 3-wire SPI uses the APB clock as the internal working clock. To initialize the SPI interface clock, you need to calculate the SPI clock ratio based on the required frequency of the SPI clock and write the value to the SPI_3WIRE_COEF0 register.

For example, if the required frequency of the SPI clock is 1 MHz, spi_clk_div is calculated as follows: spi_clk_div = (50 MHz/1 MHz)/2 – 1 = 24 (0x18 in hexadecimal). Therefore, spi_clk_div needs to be set to 0x18.

To read the SPI data, perform the following steps:

Step 1 Write the address of the read register to SPI_3WIRE_COEF1[spi_add], and write 1 to SPI_3WIRE_COEF1[spi_rw].

Step 2 Write 1 to SPI_3WIRE_COEF2[start] to start the read operation.

Step 3 Query SPI_3WIRE_COEF2[spi_busy] until this bit is 0.

Step 4 Read the required data from SPI_3WIRE_COEF2[spi_rdata].

----End

To write the SPI data, perform the following steps:

Step 1 Write the address and data of the write register to SPI_3WIRE_COEF1[spi_add] and SPI_3WIRE_COEF1[spi_wdata], and write 0 to SPI_3WIRE_COEF1[spi_rw].

Step 2 Write 1 to SPI_3WIRE_COEF2[start] to start the write operation.

Step 3 Query SPI_3WIRE_COEF2[spi_busy] until this bit is 0.

----End

12.4.3 spi_3wire_reg Register Summary

Table 12-10 describes the 3-wire SPI registers.

Table 12-10 Summary of 3-wire SPI registers (base address: 0x1212_2000)

Offset Address	Register	Description	Page
0x0000	SPI_3WIRE_COEF0	3-Wire SPI configuration register 0	12-68
0x0004	SPI_3WIRE_COEF1	3-Wire SPI configuration register 1	12-68
0x000C	SPI_3WIRE_COEF2	3-Wire SPI configuration register 2	12-69

12.4.4 spi_3wire_reg Register Description

SPI_3WIRE_COEF0

SPI_3WIRE_COEF0 is 3-wire SPI configuration register 0.

Offset Address	Register Name	Total Reset Value
0x0000	SPI_3WIRE_COEF0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								spi_clk_div							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	spi_clk_div	SPI clock ratio. The value range is 1−255. spi_clk_div is used for generating the SPI clock. spi_clk_div is calculated as follows: spi_clk_div = (FAPBCLK/FSPICLK)/2 − 1 where FAPBCLK is the APB clock frequency. For example, the bus clock frequency is 50 MHz and the expected frequency of the SPI clock is 1 MHz, spi_clk_div is calculated as follows: spi_clk_div = (50 MHz/1 MHz)/2 – 1 =24

SPI_3WIRE_COEF1

SPI_3WIRE_COEF1 is 3-wire SPI configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0004	SPI_3WIRE_COEF1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	spi_rw	spi_add															spi_wdata															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	spi_rw	SPI read/write operation select 0: write 1: read
[30:16]	RW	spi_add	SPI operation address
[15:0]	RW	spi_wdata	SPI write data

SPI_3WIRE_COEF2

SPI_3WIRE_COEF2 is 3-wire SPI configuration register 2.

Offset Address	Register Name	Total Reset Value
0x000C	SPI_3WIRE_COEF2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														spi_busy	start	spi_rdata															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	spi_busy	SPI operating status bit 0: The SPI bus is idle. 1: The SPI bus is busy.
[16]	RW	start	SPI read/write operation start. The operation can be started only when spi_busy is 0. The read back value is 0, which is meaningless.
[15:0]	RO	spi_rdata	SPI read data

12.5 eMMC/SD/SDIO Controller

12.5.1 Function Description

Functional Block Diagram

The eMMC/SD/SDIO controller (MMC controller for short) controls the read/write operations on the secure digital (SD) card and embedded multimedia card (eMMC), and supports various extended devices such as Bluetooth and Wi-Fi devices based on the secure digital input/output (SDIO) protocol. Hi3516C V300 provides four MMC controllers.

Table 12-11 describes the functional signals and pins corresponding o the four MMC controller of Hi3516C V300.

Table 12-11 Functional signals and pins corresponding o the four MMC controller of Hi3516C V300

MMC Controller	Functional Signal	Pin
MMC0	SDIO0_CCLK_OUT	SDIO0_CCLK_OUT

MMC Controller	Functional Signal	Pin
	SDIO0_CARD_POWER_EN	SDIO0_CARD_POWER_EN
	SDIO0_CARD_DETECT	SDIO0_CARD_DETECT
	SDIO0_CCMD	SDIO0_CCMD
	SDIO0_CDATA0	SDIO0_CDATA0
	SDIO0_CDATA1	SDIO0_CDATA1
	SDIO0_CDATA2	SDIO0_CDATA2
	SDIO0_CDATA3	SDIO0_CDATA3
MMC1	SDIO1_CCLK_OUT	RMII_CLK
	SDIO1_CARD_POWER_EN	RMII_RX_DV
	SDIO1_CARD_DETECT	MDIO
	SDIO1_CCMD	RMII_RXD1
	SDIO1_CDATA0	RMII_TXD0
	SDIO1_CDATA1	RMII_TXD1
	SDIO1_CDATA2	RMII_RXD0
	SDIO1_CDATA3	RMII_TX_EN
MMC2	EMMC_CLK	SFC_CLK
	EMMC_CMD	SFC_CSN
	EMMC_DATA0	SFC_WP_IO2
	EMMC_DATA1	SFC_SIO_IO0
	EMMC_DATA2	SFC_HOLD_IO3
	EMMC_DATA3	SFC_SOI_IO1
	EMMC_RST_N	SYS_RSTN_OUT
MMC3	SDIO2_CCLK_OUT	GPIO1_0
	SDIO2_CCMD	GPIO1_6
	SDIO2_CDATA0	GPIO1_5
	SDIO2_CDATA1	GPIO1_2
	SDIO2_CDATA2	GPIO1_3
	SDIO2_CDATA3	GPIO1_1

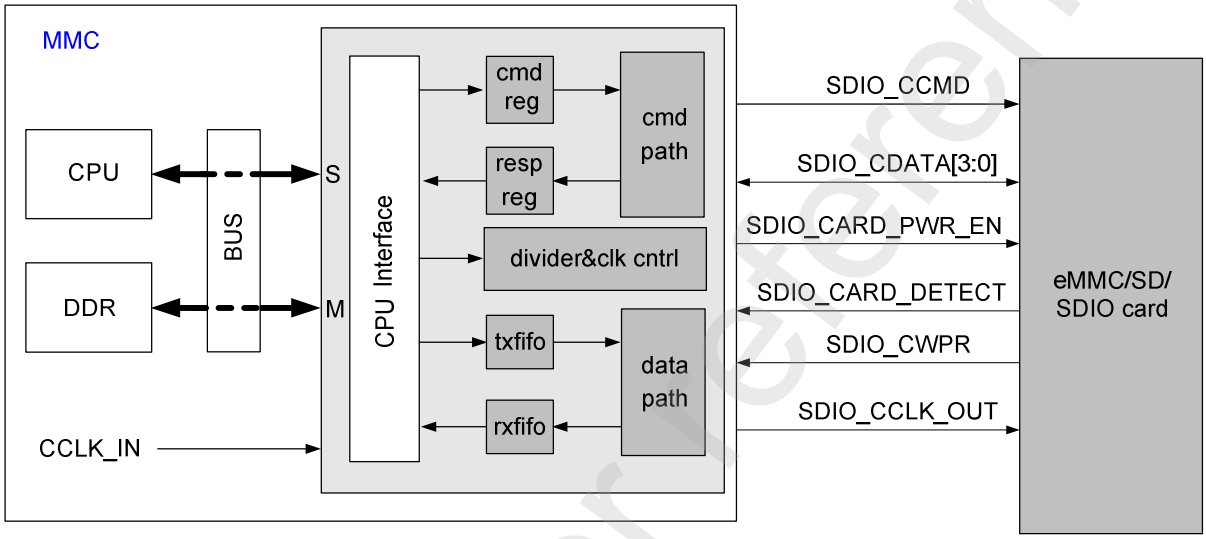
The MMC0/MMC1/MMC3 controller controls the devices that comply with the following protocols:

- Secure Digital Memory (SD mem-version 2.0)
- Secure Digital I/O (SDIO-version 2.0)

The MMC2 controller controls the devices that comply with the MultiMediaCard (eMMC-version 4.41, eMMC-version 4.5)

Figure 12-22 shows the functional block diagram of the MMC controller.

Figure 12-22 Functional block diagram of the MMC controller



NOTE

S indicates slave interface and M indicates master interface.

The MMC controller has the following features:

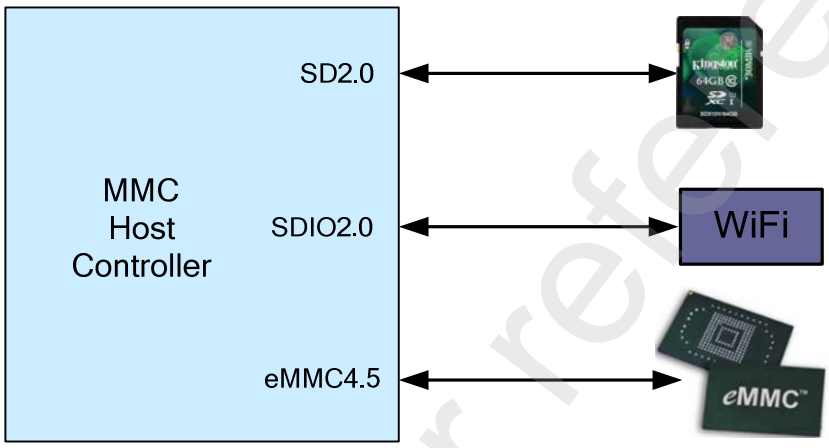
- Supports the SD card or eMMC with maximum 2 TB capacity.
- Transfers data by using the internal direct memory access controller (IDMAC).
- Supports configurable burst size during DMA transfer and configurable FIFO threshold.
- Supports FIFO overflow and underflow interrupts to avoid errors during data transfer.
- Supports the cyclic redundancy check (CRC) generation and check for data and commands.
- Supports programmable frequency of the interface clock.
- Disables the MMC clock and interface clock in low-power mode.
- Supports 1-bit or 4-bit data width based on the connected component.
- Reads or writes data blocks with the size of 1 byte to 65,535 bytes.
- Reads/writes stream data from/to the MMC card.
- Supports the suspend operation, resume operation, and read wait operation on the SDIO card.

- Supports default speed, high speed, 4-bit DDR SDRAMs, the GO_PRE_IDLE_STATE command, and hardware reset for eMMC 4.41.
- Supports 4-bit HS200 (1.8 V IO voltage), CMD21, CMD49, and the voltage of 3.3 V or 1.8 V for eMMC 4.5.

Typical Application

Figure 12-23 shows the typical application circuit of the MMC controller.

Figure 12-23 Typical application circuit of the MMC controller



Commands and Responses

All interactions between the MMC controller and the card, including initializing the card, reading/writing to registers, querying the status, and transferring data, are implemented by using commands.

A MMC command is a segment of 48-bit serial data consisting of a start bit, a transmission bit, a command sequence, a CRC bit, and an end bit. After receiving a command, the card returns a 48-bit or a 136-bit response based on the command type.

Figure 12-24 Format of an MMC command

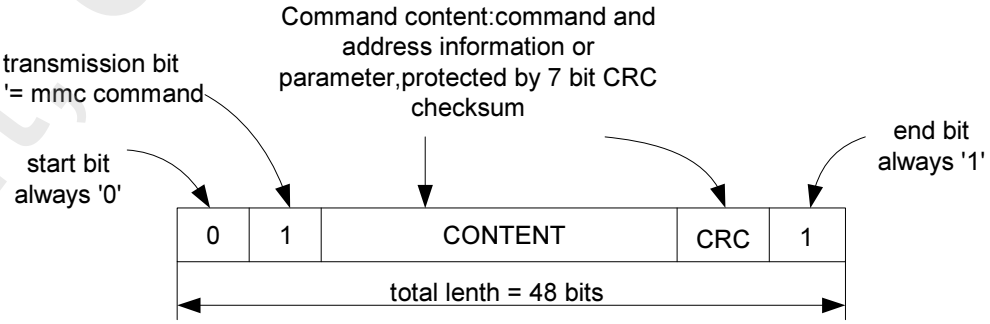
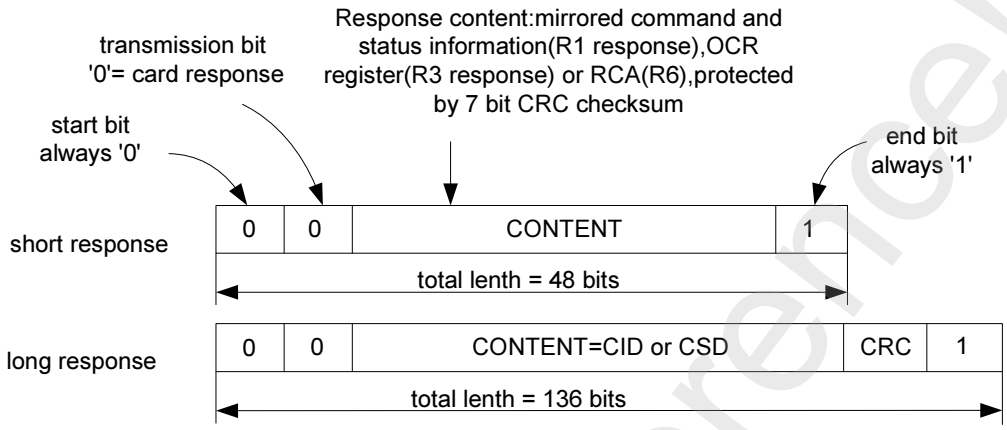


Figure 12-25 Format of the response to an MMC command



Commands are classified into the following two types based on whether data is transferred:

- Non-data transfer command

  The MMC controller transmits/receives commands to/from the card through the command signal line.

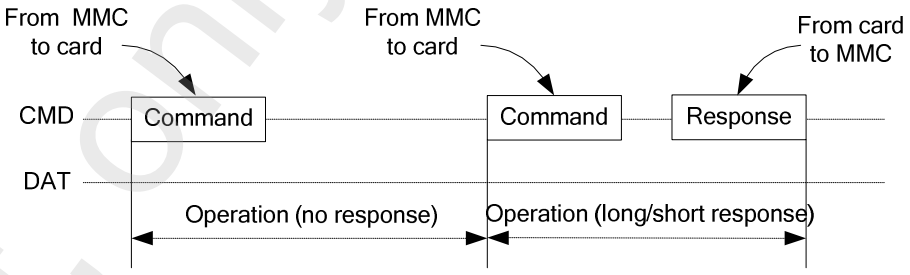
- Data transfer command

  Besides the interaction on the command line, data is also transferred through the data lines DAT0 to DAT3.

1. Non-data transfer command

Figure 12-26 shows the operations between the MMC controller and the card by running a non-data transfer command.

Figure 12-26 Operations by running an MMC non-data transfer command



2. Data transfer command

The MMC supports the following data transfer commands:

- Stream data read/write command

  Only the MMC card supports the stream data read/write command. In this case, only the data line DAT0 is used for data transfer, and no CRC check is performed.

- Single-block read/write command

After this command is executed, one single data block is read and written each time. No stop command is required for stopping each data transfer.

- Multi-block read/write command
  - Predefined block count mode

    Before the multi-block read/write command is executed, the block count command is transmitted to specify the number of data blocks to be transferred.
  - Open-ended mode

    After a read/write command is transmitted, a stop command is required for stopping data transfer at the end of data transfer.

  The difference between the two modes lies on how the MMC controller notifies the card of the end of each data transfer. The SD card supports only the open-ended mode, whereas the MMC supports both modes.

  The multi-block read/write command for the SDIO card is different from the preceding two modes. To be specific, the command parameter contains the number of data blocks to be transferred when the read/write command is transmitted.

Responses are classified into the following three types:

- Command without response

  For example, the card reset command.
- Short response command

  For example, the data transfer command and card status query command.
- Long response command

  This type of commands are used to read only the information about the card identification (CID) and card specific data (CSD) registers of a card.

Data Transfer

The single-block read/write command and the multi-block read/write command are widely used during data transfer. The data block during the data transfer of the SD card and eMMC is 512 bytes; the block size during the data transfer of the SDIO card can be customized

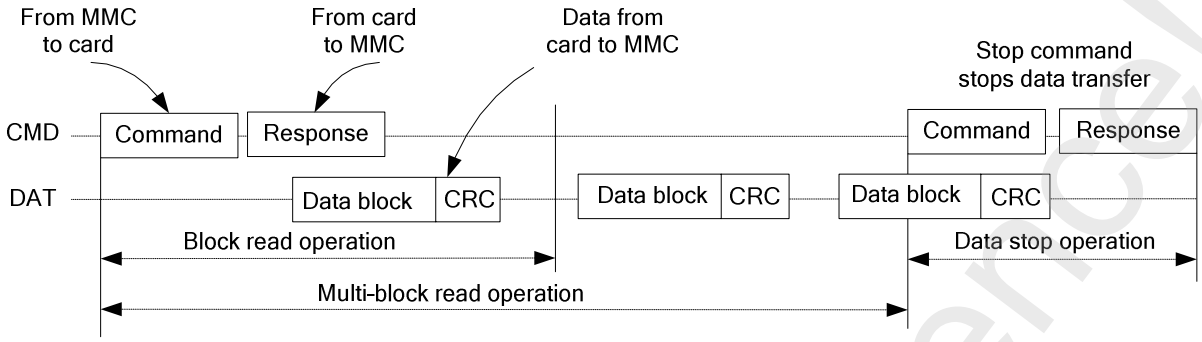
NOTE

During the data transfer by using the block read/write command, the total data amount to be transferred must be an integral multiple of the block size.

All data transfer commands are short response commands with data transferred through data lines. Figure 12-27 and Figure 12-28 show the relationships among the commands, responses, and timings of data lines.

1. Single-block and multi-block read operations

Figure 12-27 Single-block and multi-block read operations

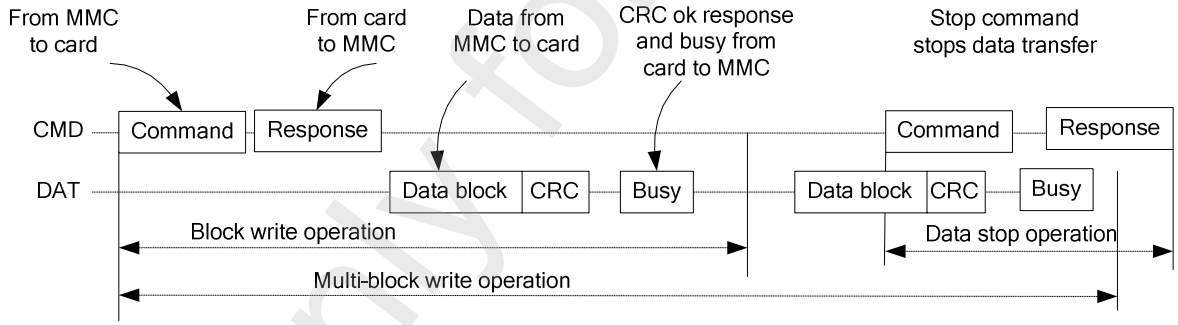


The MMC controller transmits a single-block or multi-block command to a card. When a response is being received, data is received by blocks. Each data block contains a CRC check bit for ensuring the integrity of the transferred data.

In a single-block read operation, the data transfer is completed after the MMC controller receives a data block. In a multi-block read operation, the MMC controller needs to transmit a stop command to end the data transfer after receiving multiple data blocks only in open-ended mode.

2. Single-block and multi-block read operations

Figure 12-28 Single-block and multi-block write operations



The MMC controller transmits a single-block or multi-block command to a card. After receiving a response, the MMC controller starts to transmit data to the card by blocks. Each data block contains a CRC bit. The card performs CRC on each data block and transfers the CRC status to the MMC controller. This ensures that data is transferred properly.

In a single-block write operation, the data transfer is completed after the MMC controller transmits a data block. In a multi-block write operation, the MMC controller needs to transmit a stop command to end the data transfer after transmitting multiple data blocks only in open-ended mode. After a write operation, the card may be busy in programming the flash memory. The MMC controller can perform the next operation on the card only after it confirms that the card is not busy by querying the status of the signal line DAT0.

3. Data transfer format

During the block read/write operations, the 1- or 4-bit data line can be used to transfer data between the MMC controller and the card. Before a data transfer command is

transmitted, the data transfer widths of the MMC controller and card must be the same (1 bit or 4 bits). You can set the data bit width of the MMC controller by configuring MMC_CTYPE and set the data bit width of the card by transmitting the corresponding command.

Figure 12-29 shows the data transfer format in 1-bit mode, and Figure 12-30 shows the data transfer format in 4-bit mode.

Figure 12-29 Data transfer format in 1-bit mode

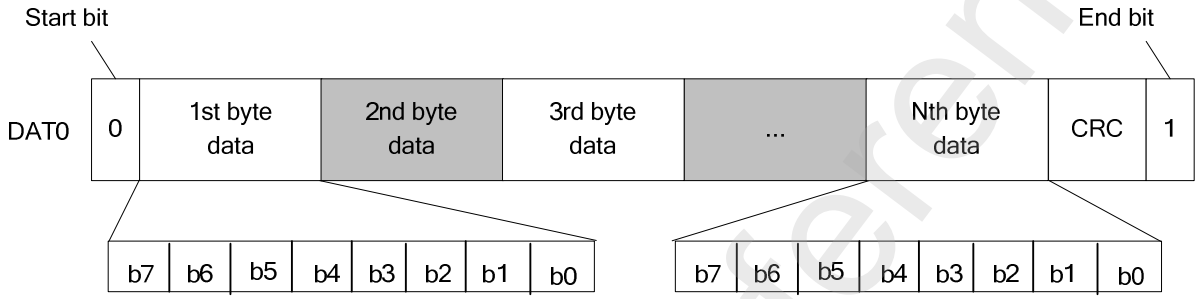


Figure 12-30 Data transfer format in 4-bit mode

12.5.2 Application Notes

NOTE

For details about clock reset registers, see section 3.2.7 "Register Description."

Clock Gating

When the software completes the current command or data transfer and does not start a new data transfer, the SDIO_CCLK_OUT clock can be disabled if the MMC controller is idle.

Perform the following steps:

Step 1 Read MMC_STATUS.

Step 2 If both MMC_STATUS[Command fsm_states] and MMC_STATUS[data_state_mc_busy] are 0, write 0 to MMC_CTRL to mask the MMC interrupt and enable the DMA request, and

go to Step 3. If any of [Command fsm_states] and [data_state_mc_busy] is not 0, wait with delay, and go to Step 1.

Step 3 Write 0 to PERI_CRG49 bit[1] to disable the MMC0 clock, and write 0 to PERI_CRG49 bit[9] to disable the MMC1 clock. Write 0 to PERI_CRG49 bit[17] to disable the MMC2 clock, and write 0 to PERI_CRG50 bit[1] to disable the MMC3 clock.

NOTE

To enable the MMC0 clock, write 1 to PERI_CRG49 bit[1]. To enable the MMC1 clock, write 1 to PERI_CRG49 bit[9]. To enable the MMC2 clock, write 1 to PERI_CRG49 bit[17]. To enable the MMC3 clock, write 1 to PERI_CRG50 bit[1].

----End

Soft Reset

If the MMC controller cannot be restored to the idle state due to data transfer exceptions, you can write 1 to PERI_CRG49 bit[0] to soft reset MMC0, write 1 to PERI_CRG49 bit[8] to soft reset MMC1, write 1 to PERI_CRG49 bit[16] to soft reset MMC2, and write 1 to PERI_CRG50 bit[0] to soft reset MMC3. In addition, you can query MMC_STATUS[Data_busy] to check whether the MMC controller is idle.

Before using the MMC controller, you are advised to soft-reset the MMC controller after hot-swapping the card.

Configuring the Working Clock

Before using the MMC controller, you need to configure the frequency of its working clock. Configure MMC0 by setting PERI_CRG49 bit[5:4], configure MMC1 by setting PERI_CRG49 bit[13:12], configure MMC2 by setting PERI_CRG49 bit[21:20], and configure MMC3 by setting PERI_CRG50 bit[5:4].

Configuring the Interface Clock

Clock frequencies vary according to the MMCs complying with different protocols and the status of MMCs. The MMC controller provides an internal even frequency divider that generates appropriate interface clocks by dividing the frequency of the working clock. The relationship between the frequencies of the working clock CCLK_IN and the interface clock SDIO_CCLK_OUT of the MMC controller is as follows:

$F_{SDIO\_CCLK\_OUT} = F_{CCLK\_IN}/(2 \times clk\_divider)$

Where, clk_divider is the value of MMC_CLKDIV[clk_divider]. Clock frequencies vary according to card types. The maximum value of $F_{SDIO\_CCLK\_OUT}$ is 50 MHz.

Before changing the clock frequency of an MMC, ensure that no data or command is being transferred. In addition, to avoid the occurrence of glitches in the output clock of the MMC, you need to perform the following steps:

Step 1 Disable the interface clock.

Set MMC_CLKENA to 0x0000_0000, set MMC_CMD[Start_cmd], MMC_CMD[Update_clk_regs_only], and MMC_CMD[Wait_prvdata_complete] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 2 Set the clock divider.

Configure MMC_CLKDIV based on the required clock frequency, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

Step 3 Enable the interface clock again.

Set MMC_CLKENA to 0x0000_0001, set MMC_CMD[Start_cmd] and MMC_CMD[Update_clk_regs_only] to 1, and wait until MMC_CMD[Start_cmd] is cleared automatically.

----End

CAUTION

The values of MMC_CMD and MMC_CMD are loaded only after MMC_CLKDIV[Start_cmd] and MMC_CLKENA[Update_clk_only] are set to 1. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically. If a command is being executed, a hardware locked error (HLE) interrupt is generated. In this case, you need to clear the interrupt, and then transmit a command again.

When a command is being executed or data is being transferred, the clock parameter values of the card cannot be changed.

Initialization

Before commands and data are exchanged between a card and the MMC controller, the MMC controller needs to be initialized. Perform the following steps:

Step 1 Configure the frequency of the working clock of the MMC controller. For details, see "Working Clock Configuration" in section 12.5.2 "Application Notes."

Step 2 Soft-reset the MMC controller after the card is powered on and the command and data signal lines are pulled up and become stable. For details, see "Soft Reset" in section 12.5.2 "Application Notes."

Step 3 Clear interrupts. Set all bits of MMC_RINTSTS bit[15:0] to 1 to clear raw interrupt status bits.

Step 4 Configure MMC_INTMASK. Set all bits of MMC_INTMASK bit[15:0] to 1 to enable all interrupt sources.

If data is transferred in DMA mode, set MMC_INTMASK bit[4] and MMC_INTMASK bit[5] to 0 to mask the TX/RX FIFO data request interrupts.

Step 5 Set MMC_CTRL[Int_enable] to 1 to enable the MMC interrupt.

Step 6 Configure the timeout parameter register MMC_TMOUT.

Step 7 Configure the FIFO parameter register MMC_FIFOTH.

----End

After the preceding steps, the interface clock can be configured and commands can be transmitted to the card.

Non-Data Transfer Command

If the MMC controller receives a response (correct response, error response, or timeout response) after transmitting a command, the MMC controller sets MMC_RINTSTS bit[2] to 1. Short responses are stored in MMC_RESP0, and long responses are stored in MMC_RESP0 to MMC_RESP3. MMC_RESP3 bit[31] is the MSB, and MMC_RESP0 bit[0] is the LSB. After a command is transmitted, its error status is reflected by the response command and the corresponding error bit of MMC_RINTSTS.

To transmit a non-data transfer command, perform the following steps:

Step 1 Set the corresponding command parameters of MMC_CMDARG.

Step 2 Configure the command register MMC_CMD based on the description in Table 12-12.

Step 3 Wait until the MMC controller runs the command. If the command is executed, the MMC controller clears MMC_CMD[Start_cmd] automatically.

Step 4 Check whether an HLE interrupt is generated by MMC_RINTSTS bit[12].

Step 5 Wait until the command is executed. If the MMC controller receives a response (correct response, error response, or timeout response), the MMC controller sets MMC_RINTSTS bit[2] to 1. This indicates that the command is executed.

Step 6 Check whether there is any response exception and read the response value if necessary.

You can check the response timeout error, response CRC error, and response error by reading MMC_RINTSTS bit[8], MMC_RINTSTS bit[6], and MMC_RINTSTS bit[1] respectively.

----End

CAUTION

The values of MMC_CMD, MMC_CMDARG, MMC_BYTCNT, and MMC_BLKSIZ are loaded only after MMC_CMDARG[Start_cmd] is set to 1 and MMC_CMD[Update_clock_registers_only] is set to 0. After the values are loaded successfully, the MMC controller clears MMC_CMD[Start_cmd] automatically.

If other commands are being executed, an HLE interrupt is generated. In this case, you need to perform the preceding operations again. When a non-data transfer command is executed, the values of MMC_BYTCNT and MMC_BLKSIZ are ignored.

Table 12-12 Default values of MMC_CMD when a non-data transfer command is executed

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
data_transfer_expected	0	Indicates a non-data transfer command.
card_number	0	-

Parameter	Value	Description
cmd_index	Cmd index	Command index
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
response_length	0	Indicates that this bit is set to 1 when the response is a long response.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
Wait_prvdata_complete	1 or 0	Indicates that the MMC controller must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status during data transfer or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Reading a Single Data Block or Multiple Data Blocks

To read a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the number of bytes to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for reading data to MMC_CMDARG.

Step 5 Configure MMC_CMD according to the description in Table 12-13.

For the SD card or eMMC, you need to read a single data block by running CMD17, and read multiple data blocks by running CMD18; for the SDIO card, you need to read a single data block or multiple data blocks by running CMD53.

The MMC controller starts to run commands after MMC_CMD is written. After commands are transferred to the bus, the cmd_done interrupt is generated.

Step 6 Check the values of MMC_RINTSTS bit[5] and MMC_RINTSTS bit[10]. If any or both of them are 1, read the data in the FIFO by reading MMC_DATA. This ensures that the MMC controller can receive the subsequent data. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. In this case, you can transmit a stop command to stop the data transfer by using the software.

Step 7 If MMC_RINTSTS bit[3] is 1, data transfer is complete. In this case, read the remaining data in the FIFO by reading MMC_DATA.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."

----End

Table 12-13 Default values of MMC_CMD when a single data block or multiple data blocks are read

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."
transfer_mode	0	Indicates block transfer.
read/write	0	Indicates that data is read from the card.
response_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	Indicates the command index.
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Writing a Single Data Block or Multiple Data Blocks

To write a single data block or multiple data blocks, perform the following steps:

Step 1 Write 1 to MMC_CTRL[fifo_reset] to reset the FIFO pointer, and query and wait until this bit is cleared automatically.

Step 2 Write the size of the data to be transmitted to MMC_BYTCNT.

Step 3 Write the block size to MMC_BLKSIZ.

Step 4 Write the start address for writing data to MMC_CMDARG.

Step 5 Write data to the FIFO by writing to MMC_DATA. The FIFO needs to be filled with data completely at the very beginning.

Step 6 Configure MMC_CMD according to the description in Table 12-14.

For the SD card or eMMC, you need to write a single data block by running CMD24, and write multiple data blocks by running CMD25; for the SDIO card, you need to write a single data block or multiple data blocks by running CMD53.

Step 7 Check the values of MMC_RINTSTS bit[4] and MMC_RINTSTS bit[10]. If any or both of them are 1, fill the FIFO with data by writing to MMC_DATA. In addition, check data error interrupts, that is, check the values of MMC_RINTSTS bit[7], MMC_RINTSTS bit[9], MMC_RINTSTS bit[13], and MMC_RINTSTS bit[15]. If necessary, you can transmit a stop command to stop the data transfer by using the software. If MMC_RINTSTS bit[3] is 1, data transfer is complete.

Step 8 If MMC_CMD[Send_auto_stop] is set to 1 during the command execution, the MMC controller automatically transmits a stop command to stop the data transfer. For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."

Step 9 Query and wait until the value of MMC_STATUS[data_busy] is changed from 1 to 0.

----End

Table 12-14 Default values of MMC_CMD when a single data block or multiple data blocks are written

Parameter	Value	Description
Start_cmd	1	Indicates that a command starts to be transmitted.
Update_clock_registers_only	0	Indicates a non-clock parameter update command.
card_number	0	-
send_initialization	0	Indicates that this bit is set to 1 when a command is a card reset command such as CMD0.
stop_abort_cmd	0	Indicates that this bit is set to 1 when a command is a data transfer stop command such as CMD12.
send_auto_stop	0 or 1	For details, see "Configuration for Using the Auto-Stop Function" in section 12.5.2 "Application Notes."
transfer_mode	0	Indicates block transfer.

Parameter	Value	Description
read_write	1	Indicates that data is written to the card.
response_length	0	Indicates that all responses to data commands are short responses.
data_transfer_expected	1	Indicates a data transfer command.
response_expect	1	Indicates that this bit is set to 0 when a command is not responded, such as CMD0, CMD4, or CMD15.
cmd_index	Cmd index	-
Wait_prvdata_complete	1 or 0	Indicates that the master device must wait until the current data transfer command is executed before transmitting another command. You are advised to set this bit to the fixed value 1 except that the command is used for querying the card status or stopping the current data transfer.
Check_response_crc	1 or 0	Indicates whether the MMC controller checks the responded CRC bit.

Reading/Writing Stream Data

The modes of reading/writing stream data are the same as those of reading/writing data blocks, except that MMC_CMD[Transfer_mode] needs to be set to 1. During a stream data transfer, the auto-stop function is required.

Transferring Data by Using the IDMAC

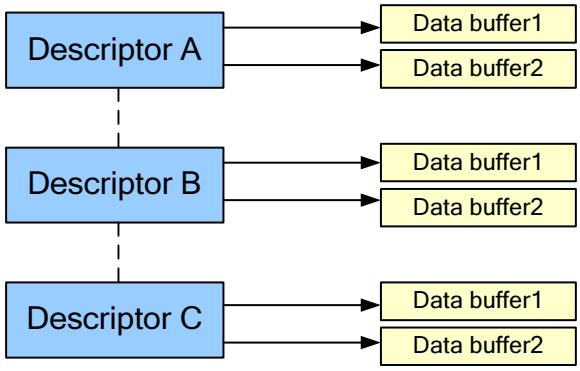
The MMC controller has an embedded IDMAC that transfers data from the original address to the destination address based on the specified descriptor.

Descriptor

The IDMAC supports the following two types of descriptors:

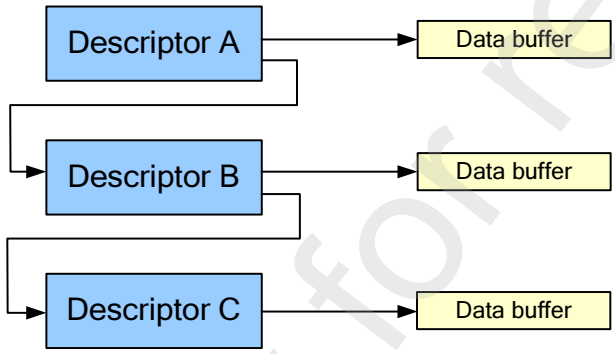
- Dual-buffer descriptor. For this type of descriptor, the span between two descriptors is determined by the DSL bit of MMC_BMOD. Figure 12-31 shows the structure of the dual-buffer descriptor.

Figure 12-31 Structure of the dual-buffer descriptor



- Linked descriptor. For this type of descriptor, each descriptor points to a unique buffer and the next descriptor. Figure 12-32 shows the structure of the linked descriptor.

Figure 12-32 Structure of the linked descriptor



Each descriptor must be word-aligned, and each descriptor contains 16-byte control and status information. Figure 12-33 shows the internal structure of 32-bit descriptors.

Figure 12-33 Internal structure of 32-bit descriptors

DES0 is used to protect the control and status information. Table 12-15 describes the definition of each bit.

Table 12-15 Definition of each bit of DES0

Bits	Register	Description
31	OWN	Indicates the attributes of the descriptor. 0: The descriptor belongs to the CPU. 1: The descriptor belongs to the IDMAC. After data is transferred by using the IDMAC, the IDMAC clears this bit.
30	CES	Indicates the error status when a card is read. 0: No error occurs. 1: An error occurs.
29:6	RES	Reserved
5	ER	Indicates the link end of the descriptor. 0: The descriptor is not the last one on the link. 1: The descriptor is the last one on the link. This bit is valid only for the dual-buffer descriptor.
4	CH	Indicates the definition of the second address in DES3. 0: The second address in DES3 is the address of the second buffer. 1: The second address in DES3 is the address of the next descriptor. When this bit is 1, DES1[25:13] must be 0.
3	FS	Indicates that the descriptor contains the first data buffer when this bit is 1. If the size of the first data buffer is 0, the next descriptor contains the start data.
2	LD	Indicates that the descriptor points to the last data buffer when this bit is 1.
1	DIC	Indicates that the data transfer completion interrupt is masked when this bit is 1.
0	RES	Reserved

DES1 is used to specify the buffer size. Table 12-16 describes the definition of each bit of DES1.

Table 12-16 Definition of each bit of DES1

Bits	Register	Description
31: 26	RES	Reserved
25: 13	BS2	Indicates the number of bytes in the second data buffer. This value must be an integral multiple of 4. This bit is invalid when DES0[4] is 1.
12: 0	BS1	Indicates the number of bytes in the first data buffer. This value

Bits	Register	Description
		must be an integral multiple of 4.

DES2 is the address pointer of the first data buffer. Table 12-17 describes the definition of each bit of DES2.

Table 12-17 Definition of each bit of DES2

Bits	Register	Description
31: 0	BAP1	Indicates the physical address of the first data buffer. The address must be word-aligned.

DES3 indicates the second address. Table 12-18 describes the definition of each bit of DES3.

Table 12-18 Definition of each bit of DES3

Bits	Register	Description
31: 0	BAP2	Indicates the physical address of the second data buffer when dual-buffer descriptors are used, or indicates the physical address of the next descriptor when DES0[4] is 1.

Initialization

Perform the following steps:

Step 1 Configure MMC_BMOD to set bus parameters.

Step 2 Configure MMC_IDINTEN to mask unnecessary registers.

Step 3 Create TX/RX descriptor linked lists, configure MMC_DBADDR, and set the start address.

Step 4 The IDMAC attempts to obtain descriptors from the descriptor linked lists.

----End

Transmission

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, set DES0 bit[31] (OWN bit) to 1, and provide data buffers.

Step 2 Write data commands to MMC_CMD.

Step 3 Set TX_Wmark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC

enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from data buffers to the internal FIFO of the MMC controller when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Reception

Perform the following steps:

Step 1 Create the descriptors DES0 to DES3 by using the CPU, and set the DES0 bit[31] (OWN bit) to 1.

Step 2 Write read commands to MMC_CMD.

Step 3 Set RX_WMark by using MMC_FIFOTH.

Step 4 The IDMAC obtains descriptors and check whether the value of the OWN bit is 1. If the OWN bit is not 1, wait until the CPU releases descriptors. During this process, the IDMAC enters the suspend state. Therefore, the CPU needs to configure MMC_PLDMND to enable the IDMAC to obtain descriptors again.

Step 5 The IDMAC transfers data from the internal FIFO of the MMC controller to the external data buffers when the OWN bit is 1.

Step 6 If the interrupts are enabled, the corresponding bit of the IDMAC status register MMC_IDSTS is updated and the OWN bit is cleared after data transfer.

----End

Auto-Stop Function Configuration

When multiple data blocks are read or written, a stop command is required to stop each data transfer. The stop command can be transmitted in non-data transfer command mode or by using the auto-stop function.

The auto-stop function is applicable in the following scenarios:

- SD card

  Multi-block read/write operation by running CMD18 or CMD25

- eMMC
  - Stream data read/write operation
  - Multi-block read/write operation in open-ended mode by running CMD18 or CMD25

Before using the auto-stop function of the MMC controller, you are advised to perform the followings steps:

Step 1 Set MMC_CMD[Send_auto_stop] to 1 during the block transfer command operation.

Step 2 After data transfer, the MMC controller automatically transmits a stop command to enable the card to restore to the corresponding state.

Step 3 Read MMC_RINTSTS[auto_cmd_done] to check whether the stop command is executed. The response is stored in MMC_RESP1.

----End

Stopping or Aborting the Data Transfer

The stop command is used to interrupt the data transfer between the MMC controller and the card, whereas the abort command is used to interrupt the I/O data transfer only in SDIO_IOONLY or SDIO_COMBO mode.

The two commands are used as follows:

- Stop command

  This command can be transmitted at any time during data transfer, because this command is used to stop the data transfer. In this case, you need to set MMC_CMD bit[5:0] to CMD12, MMC_CMD bit[14] to 1, and MMC_CMD bit[13] to 0.

- Abort command

  This command is available only for SDIO_IOONLY or SDIO_COMBO. To abort the data transfer, you need to configure the CCCR[ASx] register of the SDIO card by running the CMD52 command.

Suspend and Resume Operations

An SDIO card can store the data of a maximum of seven functional devices. The MMC controller can suspend the data transfer of a device by performing the suspend operation. Then the SD interface bus is available for another device with higher priority. After the device with higher priority transfers data, the MMC controller can resume the suspended data transfer of the previous device.

The suspend and resume operations are implemented by configuring the corresponding bits of the CCCR register of the SDIO card. The CCCR register is written or read by running the CMD52 command.

To implement a suspend operation, perform the following steps:

Step 1 Query the SBS bit of the CCCR register to check whether the SDIO card supports suspend and resume operations.

Step 2 Query the FSx and bus status (BS) bits of the CCCR register to check whether the functional device to be suspended is transferring data.

If the BS bit is 1, the device specified by the FSx bit is transferring data.

Step 3 Set the bus release (BR) bit of the CCCR register to 1 to suspend the current data transfer.

Step 4 Check whether the BS and the BR bits of the CCCR register are cleared.

The BS bit retains 1 when the data bus is being used. The BR bit retains 1 before the bus is released completely. When both the BR and BS bits are 0, the data transfer of the selected functional device is suspended.

Step 5 If the current read operation is suspended, MMC_CTRL[Abort_read_data] needs to be set to 1 to restart the data transfer function of the MMC controller after the suspend operation. Then MMC_CTRL[Abort_read_data] is cleared automatically.

Step 6 Read MMC_TCBCNT to query the number of transferred bytes.

----End

To implement a resume operation, perform the following steps:

Step 1 Query the transfer status of the card to check whether the bus is idle.

Step 2 If the card is disconnected, run the CMD7 command to select it. The card status can be queried by running the CMD52 or CMD53 command.

Step 3 Check whether the device to be resumed is ready for data transfer by querying the RF bit of the CCCR register. If the RF bit is 1, the device is ready for data transfer.

Step 4 Run the CMD52 command to write the device ID to the FS bit of the CCCR register to resume the data transfer, and enable the MMC controller to enter the data transfer state (that is, write the block size to MMC_BLKSIZ, and write the amount of remaining data to be transferred to MMC_BYTCNT).

For details about the configuration of MMC_CMDARG, see Table 12-19. The configuration of MMC_CMD is similar to the configuration during block transfer.

Step 5 The data transfer is resumed after the CMD52 command is transmitted successfully. Read the resume data flag (DF) bit of the SDIO device. If this bit is 1, data transfer starts when the transfer function is resumed. If this bit is 0, no data is ready for transferring.

Step 6 If the DF bit is 0, the MMC generates a data timeout error interrupt a period of time later during data read.

----End

Table 12-19 Reference configuration of MMC_CMDARG when the resume operation is performed

MMC_CMDARG	Value	Description
Bit[31]	1	Indicates the read/write flag.
Bit[30:28]	0	Indicates the ID of a functional device that accesses the CCCR register.
Bit[27]	1	Indicates the real-time flag, that is, write-to-read.
Bit[26]	None	-
Bit[25:9]	0x0D	Indicates the register address.
Bit[8]	None	-
Bit[7:0]	ID of the functional device that is resumed	Indicates write data.

CAUTION

The MMC controller cannot be woken up after the system enters the low-power mode.

Read Wait Operation

The read wait operation is performed to suspend the data transfer of the device that is using the SDIO card. The MMC controller determines the duration of pausing the data transfer.

To implement a read wait operation, perform the following steps:

Step 1 Check whether the card supports the read wait operation.

You can read the SRW bit of the CCCR register by running the CMD52 command. If the SRW bit is 1, all the devices supporting the card support the read wait operation.

Step 2 Set MMC_CTRL[Read_wait] to 1.

Step 3 If you want to resume the data transfer, clear MMC_CTRL[Read_wait].

----End

12.5.3 Register Summary

Table 12-20 describes the MMC registers.

Table 12-20 Summary of MMC registers (the base addresses for MMC0, MMC1, MMC2, and MMC3 are 0x100C_0000, 0x100D_0000, 0x100E_0000, and 0x100F_0000 respectively)

Offset Address	Register	Description	Page
0x0000	MMC_CTRL	MMC control register	12-92
0x0004	MMC_PWREN	Power_en control register	12-93
0x0008	MMC_CLKDIV	Clock divider register	12-94
0x0010	MMC_CLKENA	Clock enable register	12-94
0x0014	MMC_TMOUT	Timeout register	12-95
0x0018	MMC_CTYPE	Card type register	12-96
0x001C	MMC_BLKSIZ	Block size configuration register	12-96
0x0020	MMC_BYTCNT	Block transfer count register	12-97
0x0024	MMC_INTMASK	Interrupt mask register	12-97
0x0028	MMC_CMDARG	Command parameter register	12-98
0x002C	MMC_CMD	Command register	12-98
0x0030	MMC_RESP0	Response register 0	12-102
0x0034	MMC_RESP1	Response register 1	12-102
0x0038	MMC_RESP2	Response register 2	12-102
0x003C	MMC_RESP3	Response register 3	12-103
0x0040	MMC_MINTSTS	Masked interrupt status register	12-103

Offset Address	Register	Description	Page
0x0044	MMC_RINTSTS	Raw interrupt status register	12-104
0x0048	MMC_STATUS	Status register	12-105
0x004C	MMC_FIFOTH	FIFO threshold register	12-106
0x0050	MMC_CDETECT	Card detection register	12-108
0x0054	MMC_WRTPRT	Card write protection register	12-108
0x005C	MMC_TCBCNT	Count of bytes transmitted to the card register	12-109
0x0060	MMC_TBBCNT	Count of bytes transmitted from the bus interface unit (BIU) FIFO register	12-109
0x0064	MMC_DEBNCE	Dejitter count register	12-110
0x0074	MMC_UHS_REG	UHS-1 register	12-110
0x0078	MMC_CARD_RSTN	eMMC reset control register	12-111
0x0080	MMC_BMOD	Bus mode register	12-111
0x0084	MMC_PLDMND	Poll demand register	12-112
0x0088	MMC_DBADDR	Base address register of the descriptor linked list	12-112
0x008C	MMC_IDSTS	IDMAC status register	12-113
0x0090	MMC_IDINTEN	IDMAC interrupt enable register	12-114
0x0094	MMC_DSCADDR	Address register of the current descriptor	12-115
0x0098	MMC_BUFADDR	Address register of the current data buffer	12-115
0x0100	MMC_CARDTHRCTL	Threshold control register	12-119
0x0108	MMC_UHS_REG_EXT	UHS extension register	12-117
0x010C	MMC_DDR_REG	eMMC 4.5 DDR start bit detection control register	12-118
0x0110	MMC_ENABLE_SHIFT	Phase shift register	12-118
0x0200	MMC_DATA	Data register (entrance address of the FIFO)	12-119

12.5.4 Register Description

MMC_CTRL

MMC_CTRL is a MMC control register.

Offset Address	Register Name	Total Reset Value
0x0000	MMC_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved						use_internal_dmac		reserved															abort_read_data	send_irq_response	read_wait	reserved	int_enable	reserved	dma_reset	fifo_reset	controller_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25]	RW	Use_internal_dmac	Whether to transfer data by using the IDMAC 0: The CPU transfers data by using the slave interface. 1: The CPU transfers data by using the IDMAC.
[24:9]	RO	reserved	Reserved
[8]	RW	Abort_read_data	Whether to abort the data transfer during data read 0: invalid 1: After transmitting a suspend command during data read, the software polls the card to check when suspend occurs. After the suspend occurs, the software sets the bit to 1. This enables the data transfer state machine to be restored to idle state for the next block transfer. After the state machine restores to the idle status, this bit is cleared automatically.
[7]	RW	Send_irq_response	TX interrupt response control 0: invalid 1: An interrupt request (IRQ) response is transmitted automatically. After the response is transmitted, this bit is cleared automatically. To wait for the interrupt generated by the MMC controller, the host transmits the CMD40 command and waits for the interrupt response from the MMC controller. If you do not want the host to keep in the interrupt wait state, set this bit to 1 and transmit the CMD40 command to restore the host to the idle state.

[6]	RW	Read_wait	Read wait control 0: disabled 1: enabled This bit is valid only for the SDIO card that supports the read wait function.
[5]	RW	reserved	Reserved.
[4]	RW	Int_enable	Global interrupt enable 0: disabled 1: enabled The interrupt output is valid only when this bit is valid and the interrupt source is enabled.
[3]	RO	reserved	Reserved
[2]	RW	Dma_reset	Soft reset control for the IDMAC 0: invalid 1: reset the internal DMA interface This bit is automatically reset after two AHB clock cycles.
[1]	RW	Fifo_reset	Soft reset control for the internal FIFO 0: invalid 1: reset the FIFO pointer This bit is reset automatically after the reset operation is complete.
[0]	RW	Controller_reset	Soft reset control for the controller 0: invalid 1: reset the eMMC/SD/SDIO host module

MMC_PWREN

MMC_PWREN is a Power_en control register.

Offset Address	Register Name	Total Reset Value
0x0004	MMC_PWREN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								Power_enable
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved

[0]	RW	Power_enable	Power control 0: power off 1: power on

MMC_CLKDIV

MMC_CLKDIV is a clock divider register that shows the ratio of the frequency of the module output clock to the frequency of the input clock. For example, if the module input clock is 40 MHz and the register value is set to 1, the output clock is 20 MHz.

The clock divider is 2 x N. If the value of *N* is 0x0, it indicates no frequency division (2 x 0 = 0); if the value of *N* is 0x1, the frequency is divided by 2; if the value of *N* is 0xFF, the frequency is divided by 510.

Offset Address	Register Name	Total Reset Value
0x0008	MMC_CLKDIV	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								clk_divider0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RW	clk_divider0	Clock divider 0. The clock divider is 2 x *n*. If the value of *n* is 0, it indicates no frequency division; if the value of *n* is 1, the frequency is divided by 2; if the value of *n* is 0xFF, the frequency is divided by 510.

MMC_CLKENA

MMC_CLKENA is a clock enable register.

Offset Address	Register Name	Total Reset Value
0x0010	MMC_CLKENA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																cclk_low_power	reserved														cclk_enable

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	cclk_low_power	Card low-power control for disabling the card clock 0: non lower-power mode 1: low-power mode When the card is idle, the card clock is disabled. This function is used only for the SD card and eMMC, because the card clock of the SDIO card must be retained for detecting interrupts.
[15:1]	RW	reserved	Reserved
[0]	RW	cclk_enable	Card clock enable 0: disabled 1: enabled

MMC_TMOUT

MMC_TMOUT is a timeout register.

Offset Address	Register Name	Total Reset Value
0x0014	MMC_TMOUT	0xFFFF_FF40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_timeout																								response_timeout							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	data_timeout	Timeout during the data transfer of the card, in unit of the mmc_clk cycle of the card. The timeout is also the data starvation timeout of the CPU.
[7:0]	RW	response_timeout	Response timeout, in unit of the mmc_clk cycle of the card.

MMC_CTYPE

MMC_CTYPE is a card type register.

Offset Address	Register Name	Total Reset Value
0x0018	MMC_CTYPE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															card_width_0	reserved															card_width_1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	card_width_0	Bus width of the card. It must be set to 0. 0: non 8-bit mode 1: 8-bit mode Note the following: If bit[16] is 1, the card is set to 8-bit mode, and the value of bit[0] is ignored. If bit[16] is 0, the card is set to 1-bit mode or 4-bit mode, depending on the value of bit[0].
[15:1]	RW	reserved	Reserved
[0]	RW	card_width_1	Bus width of the card 0: 1-bit mode 1: 4-bit mode

MMC_BLKSIZ

MMC_BLKSIZ is a block size configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	MMC_BLKSIZ	0x0000_0200

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																block_size															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	block_size	Block size. The initial size of each block is 512 bytes.

MMC_BYTCNT

MMC_BYTCNT is a block transfer count register.

Offset Address	Register Name	Total Reset Value
0x0020	MMC_BYTCNT	0x0000_0200

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	Byte_count							
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:0]	RW	Byte_count	Number of transferred bytes. The number must be an integral multiple of the block size. If the data transfer is not block transfer, this register must be set to 0. In this case, the software needs to transmit a stop or an abort command to control the data transfer.

MMC_INTMASK

MMC_INTMASK is an interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0024	MMC_INTMASK	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				sdio_int_mask	int_mask		
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	sdio_int_mask	SDIO interrupt mask 0: masked 1: enabled

[15:0]	RW	int_mask	Interrupt mask 0: masked 1: enabled Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation-by-host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_CMDARG

MMC_CMDARG is a command parameter register.

Offset Address	Register Name	Total Reset Value
0x0028	MMC_CMDARG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cmd_arg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cmd_arg	Command parameter that is transferred to the card. The command parameter is related to the protocol, and each command corresponds to a command parameter.

MMC_CMD

MMC_CMD is a command register.

Offset Address	Register Name	Total Reset Value
0x002C	MMC_CMD	0x2000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	start_cmd	reserved	use_hold_reg	volt_switch	boot_mode	disable_boot	expect_boot_ack	enable_boot	reserved		update_clock_registes_only		card_number				send_initialization	stop_abort_cmd	wait_prvdata_complete	send_auto_stop	transfer_mode	read_write	data_transfer_expected	check_response_crc	response_length	response_expect	cmd_index					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	start_cmd	Start control 0: do not start 1: start a command After the command is transferred to the card interface unit (CIU), this bit is cleared. The CPU does not allow modifications to this register. Otherwise, an HLE interrupt is generated. After transmitting a command, the CPU queries this bit, and transmits the next command when the value of this bit changes to 0.
[30]	RW	reserved	Reserved
[29]	RW	use_hold_reg	Whether to use the hold register 0: The CMD and DATA signals transmitted to the MMC do not pass through the hold register. 1: The CMD and DATA signals transmitted to the MMC pass through the hold register.
[28]	RW	volt_switch	Voltage switching enable 0: disabled 1: enabled
[27]	RW	boot_mode	Boot mode 0: boot mode 1: alternative boot mode
[26]	RW	disable_boot	Boot disable If the software enables this bit and the Start_cmd bit at the same time, the controller aborts the boot operation. The Enable_boot and Disable_boot bits cannot be enabled at the same time.

[25]	RW	expect_boot_ack	Boot response enable If the software enables this bit and the Enable_boot bit at the same time, the controller detects the boot response signal in "0–1–0" sequence.
[24]	RW	enable_boot	Boot enable This bit is available when the boot mode is mandatory. If the software enables this bit and the Start_cmd bit, the controller pulls down the CMD signal to start the boot process. The Enable_boot and Disable_boot bits cannot be enabled at the same time.
[23:22]	RO	reserved	Reserved
[21]	RW	update_clock_registers_only	Automatic update 0: The normal command sequence is used. That is, the values of MMC_CMD, MMC_CMDARG, MMC_TMOUT, MMC_CTYPE, MMC_BLKSIZ, and MMC_BYTCNT are transferred from the BIU to the CIU. The CIU uses the new values of registers when running new commands. 1: No command is transmitted, and only the clock register values in the card clock domain are updated. The values of MMC_CLKDIV and MMC_CLKENA are transferred to the card clock domain. The card clock can be changed (frequency change and clock enable) even no command is transmitted. Each time the card clock is changed; this bit must be set to 1. In this case, no command is transmitted to the card, and no command done interrupt is generated.
[20:16]	RW	card_number	Serial number of the card that is being used
[15]	RW	send_initialization	Whether to transmit the initialization sequence 0: do not transmit the initialization sequence before transmitting the Send_initialization command (high level in 80 clock cycles) 1: transmit the initialization sequence before transmitting the Send_initialization command When a card is powered on, the initialization sequence must be transmitted for initialization before any command is transmitted. That is, this bit must be set to 1.
[14]	RW	stop_abort_cmd	Whether to transmit the stop/abort command when data is being transferred in open-ended mode or in fixed length mode. 0: do not transmit the stop/abort command 1: transmit the stop/abort command for stopping the current data transfer

[13]	RW	wait_prvdata_complete	Whether to transmit a command immediately 0: transmit a command immediately even though the previous data transfer is not complete 1: transmit a command only when the previous data transfer is complete The typical value is 0. If this bit is set to 0, the transfer status can be read during data transfer, and the interrupt transfer is supported.
[12]	RW	send_auto_stop	Whether to transmit the stop command 0: do not transmit the stop command after data transfer 1: transmit the stop command after data transfer In non-data transfer mode, this bit is ignored.
[11]	RW	transfer_mode	Transfer mode 0: block transfer mode 1: stream transfer mode In non-data transfer mode, this bit is ignored.
[10]	RW	read_write	Read/write control 0: read data from the card 1: write data to the card In non-data transfer mode, this bit is ignored.
[9]	RW	data_transfer_expected	Data transfer indicator 0: No data is output from the card. 1: Data is output from the card.
[8]	RW	check_response_crc	Whether to perform the CRC check 0: Do not check the CRC response. 1: Check the CRC response. No valid CRC is returned when some commands are responded. To prevent the host from performing CRC, the software needs to disable this function based on related commands.
[7]	RW	response_length	Response length 0: Short responses are output from the card 1: Long responses are output from the card The length of a long response is 128 bits, whereas the length of a short response is 32 bits.
[6]	RW	response_expect	Whether to output response 0: No response is output from the card. 1: Responses are output from the card.
[5:0]	RW	cmd_index	Command index

MMC_RESP0

MMC_RESP0 is response register 0.

Offset Address	Register Name	Total Reset Value
0x0030	MMC_RESP0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response0	Bit[31:0] of a response

MMC_RESP1

MMC_RESP1 is response register 1.

Offset Address	Register Name	Total Reset Value
0x0034	MMC_RESP1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response1	Bit[63:32] of a long response After the CIU transmits an auto-stop command, the corresponding response is stored in this register, and the response to the previous command is still stored in MMC_RESP0. The auto-stop command is available only during data transfer, and the corresponding response is always a short response.

MMC_RESP2

MMC_RESP2 is response register 2.

Offset Address	Register Name	Total Reset Value
0x0038	MMC_RESP2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response2																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response2	Bit[95:64] of a long response

MMC_RESP3

MMC_RESP3 is response register 3.

Offset Address	Register Name	Total Reset Value
0x003C	MMC_RESP3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	response3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	response3	Bit[127:96] of a long response

MMC_MINTSTS

MMC_MINTSTS is a masked interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0040	MMC_MINTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sdio_interrupt	int_status														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RO	sdio_interrupt	SDIO Interrupt mask status The SDIO interrupt is valid only when MMC_INTMASK [sdio_int_mask] is enabled. 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card.
[15:0]	RO	int_status	Status of each interrupt Bit[15]: end-bit error (read)/write no CRC (EBE)

			Bit[14]: auto command done (ACD) Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DTO) Bit[8]: response timeout (RTO) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_RINTSTS

MMC_RINTSTS is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0044	MMC_RINTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															sdio_interrupt	int_status															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16]	RW	sdio_interrupt	SDIO raw status of an interrupt 0: No SDIO interrupt is output from the card. 1: An SDIO interrupt is output from the card. The value of the interrupt status bit is independent of the interrupt mask status.
[15:0]	RW	int_status	Raw status of each interrupt. Writing 1 clears the bits, and writing 0 has no effect. The value of the interrupt status bit is independent of the interrupt mask status. Bit[15]: end-bit error (read)/write no CRC (EBE) Bit[14]: auto command done (ACD)

			Bit[13]: start-bit error (SBE) Bit[12]: hardware locked write error (HLE) Bit[11]: FIFO underrun/overrun error (FRUN) Bit[10]: data starvation by the host timeout (HTO) Bit[9]: data read timeout (DRTO)/Boot Data Start (BDS) Bit[8]: response timeout (RTO)/Boot Ack Received (BAR) Bit[7]: data CRC error (DCRC) Bit[6]: response CRC error (RCRC) Bit[5]: RX FIFO data request (RXDR) Bit[4]: TX FIFO data request (TXDR) Bit[3]: data transfer over (DTO) Bit[2]: command done (CD) Bit[1]: response error (RE) Bit[0]: card detect (CD)

MMC_STATUS

MMC_STATUS is a status register.

Offset Address	Register Name	Total Reset Value
0x0048	MMC_STATUS	0x0000_0106

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				fifo_count												response_index					data_state_mc_busy	data_busy	reserved	commandfsm_states					fifo_full	fifo_empty	fifo_tx_watermark	fifo_rx_watermark	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0

Bits	Access	Name	Description
[31:30]	RO	reserved	Reserved
[29:17]	RO	fifo_count	FIFO count
[16:11]	RO	response_index	Serial number of the previous response, including the response to the auto-stop command
[10]	RO	data_state_mc_busy	0: The data TX/RX state machine is idle. 1: The data TX/RX state machine is busy.
[9]	RO	data_busy	This field value depends on the reverse level of DATA0. 0: idle (DATA0 is high level) 1: busy (DATA0 is low level)
[8]	RO	reserved	Reserved

[7:4]	RO	commandfsm_states	Status of the command state machine 0x0: idle 0x1: send init sequence 0x2: Tx cmd start bit 0x3: Tx cmd tx bit 0x4: Tx cmd index + arg 0x5: Tx cmd crc7 0x6: Tx cmd end bit 0x7: Rx resp start bit 0x8: Rx resp IRQ response 0x9: Rx resp tx bit 0xA: Rx resp cmd idx 0xB: Rx resp data 0xC: Rx resp crc7 0xD: Rx resp end bit 0xE: Cmd path wait NCC 0xF: wait, CMD-to-response turnaround
[3]	RO	fifo_full	FIFO full flag 0: empty 1: full
[2]	RO	fifo_empty	FIFO empty flag 0: not empty 1: empty
[1]	RO	fifo_tx_watermark	Whether the FIFO reaches the TX threshold 0: no 1: yes
[0]	RO	fifo_rx_watermark	Whether the FIFO reaches the RX threshold 0: no 1: yes

MMC_FIFOTH

MMC_FIFOTH is a FIFO threshold register.

Offset Address	Register Name	Total Reset Value
0x004C	MMC_FIFOTH	0x60FF_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		Multiple_Transaction_Size		rx_wmark												reserved				tx_wmark											
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:28]	RW	Multiple_Transaction_Size	Transferred burst length 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 110: 128 111: 256
[27:16]	RW	rx_wmark	FIFO threshold during data read. If the data amount in the FIFO is above the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: rx_wmark ≤ FIFO_DEPTH – 2 Recommendation: A request is raised when the value of [(FIFO_DEPTH/2) – 1] is above the threshold. Note: FIFO_DEPTH = 256
[15:12]	RW	reserved	Reserved

[11:0]	RW	tx_wmark	FIFO threshold during data transmission. If the data amount in the FIFO is below the threshold, a DMA request is enabled. After a data transfer, a DMA request is raised for transferring the remaining data no matter whether the threshold is reached. In non-DMA mode, the RXDR interrupt is enabled. If the data amount in the FIFO is not above the threshold after a data transfer, no interrupt is generated. In this case, the software needs to read the remaining data by querying the DTD interrupt. If a data transfer is complete in DMA mode, the DMA raises a single transfer request to read data until the DTD interrupt is generated even though the remaining data amount is below the threshold. Restriction: tx_wmark ≤ FIFO_DEPTH – 2 Recommendation: This field must be less than or equal to FIFO_DEPTH/2. Note: FIFO_DEPTH = 256

MMC_CDETECT

MMC_CDETECT is a card detection register.

Offset Address	Register Name	Total Reset Value
0x0050	MMC_CDETECT	0x0000_0001

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								card_detect_n
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	1

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	card_detect_n	Card detection signal The value depends on the SDIO_CARD_DETECT pin.

MMC_WRTPRT

MMC_WRTPRT is a card write protection register.

Offset Address	Register Name	Total Reset Value
0x0054	MMC_WRTPRT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															write_protect
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	write_protect	Card write protection signal The value depends on the SDIO_CWPR pin.

MMC_TCBCNT

MMC_TCBCNT is a count of bytes transmitted to the card register.

Offset Address	Register Name	Total Reset Value
0x005C	MMC_TCBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_card_byte_count																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_card_byte_count	Count of bytes transmitted from the CIU to the card When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_TBBCNT

MMC_TBBCNT is a count of bytes transmitted from the BIU FIFO register.

Offset Address	Register Name	Total Reset Value
0x0060	MMC_TBBCNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trans_fifo_byte_count																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trans_fifo_byte_count	Count of bytes transferred between the CPU/DMA and BIU FIFO When this register is accessed through a 32-bit AHB, the 32-bit data needs to be read at a time. This avoids the read-coherency error.

MMC_DEBNCE

MMC_DEBNCE is a dejitter count register.

Offset Address	Register Name	Total Reset Value
0x0064	MMC_DEBNCE	0x00FF_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								debounce_count																							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved
[23:0]	RW	debounce_count	Number of bus clock cycles used by the dejitter filter logic. Generally, the dejitter duration ranges from 5 ms to 25 ms.

MMC_UHS_REG

MMC_UHS_REG is a UHS-1 register.

Offset Address	Register Name	Total Reset Value
0x0074	MMC_UHS_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved															ddr_reg	reserved															volt_reg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RW	reserved	Reserved
[16]	RW	ddr_reg	DDR mode control 0: non-DDR mode 1: DDR mode

[15:1]	RW	reserved	Reserved
[0]	RW	volt_reg	Voltage mode control 0: 3.3 V 1: 1.8 V

MMC_CARD_RSTN

MMC_CARD_RSTN is an eMMC reset control register.

Offset Address	Register Name	Total Reset Value
0x0078	MMC_CARD_RSTN	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															card_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:1]	RW	reserved	Reserved
[0]	RW	card_reset	eMMC reset. The control pin is CARD_RESET. 0: reset 1: deassert reset

MMC_BMOD

MMC_BMOD is a bus mode register.

Offset Address	Register Name	Total Reset Value
0x0080	MMC_BMOD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					pbl			de	dsl					fb	swr
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	RO	reserved	Reserved
[10:8]	RW	pbl	Length of the IDMAC burst transfer 000: 1 001: 4 010: 8

			011: 16 100: 32 101: 64 110: 128 111: 256
[7]	RW	de	IDMAC enable 0: disabled 1: enabled
[6:2]	RW	dsl	Span between two descriptors, that is, number of words between two non-linked descriptors. This bit is valid only for the dual-buffer descriptor.
[1]	RW	fb	Fixed burst length type 0: single and INCR burst types 1: single, INCR4, INCR8, and INCR16 burst types
[0]	RW	swr	Soft reset control for the internal register of the IDMAC 0: not reset 1: reset After reset, this bit is automatically cleared one clock cycle later.

MMC_PLDMND

MMC_PLDMND is a poll demand register.

Offset Address	Register Name	Total Reset Value
0x0084	MMC_PLDMND	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pd																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	pd	If DES0[OWN] is 0, the IDMAC enters the suspend state. The CPU can write any value to this register to enable the IDMAC to obtain descriptors again.

MMC_DBADDR

MMC_DBADDR is a base address register of the descriptor linked list.

Offset Address	Register Name	Total Reset Value
0x0088	MMC_DBADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sdl																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sdl	Start address of the descriptor linked list, that is, the base address of the first descriptor, which is word-aligned

MMC_IDSTS

MMC_IDSTS is an IDMAC status register.

Offset Address	Register Name	Total Reset Value
0x008C	MMC_IDSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																fsm				eb				ais	nis	reserved			ces	du	reserved		fbe	ri	ti
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16:13]	RO	fsm	Current state of the IDMAC state machine 0x0: DMA_IDLE 0x1: DMA_SUSPEND 0x2: DESC_RD 0x3: DESC_CHK 0x4: DMA_RD_REQ_WAIT 0x5: DMA_WR_REQ_WAIT 0x6: DMA_RD 0x7: DMA_WR 0x8: DESC_CLOSE Other values: reserved
[12:10]	RW	eb	Bus error type 001: The transmit operation is aborted. 010: The receive operation is aborted. Other values: reserved

[9]	RW	ais	Abnormal total interrupt. The value of this bit is obtained after the values of FBE, DU, and CES bits are ORed. Writing 1 clears this bit.
[8]	RW	nis	Normal total interrupt. The value of this bit is obtained after the values of the TI and RI bits are ORed. Writing 1 clears this bit.
[7:6]	RO	reserved	Reserved
[5]	RW	ces	Card error indicator. This bit indicates the card status when data is being received.
[4]	RW	du	Descriptor invalid interrupt. When DES0[OWN] is 0, this bit is set to 1. Writing 1 clears this bit.
[3]	RO	reserved	Reserved
[2]	RW	fbe	Fatal bus error interrupt. If this bit is set to 1, the IDMAC stops all accesses through the bus. Writing 1 clears this bit.
[1]	RW	ri	Receive done interrupt. This bit indicates that the data of a descriptor is received. Writing 1 clears this bit.
[0]	RW	ti	Transmit done interrupt. This bit indicates that a descriptor finishes transmitting data. Writing 1 clears this bit.

MMC_IDINTEN

MMC_IDINTEN is an IDMAC interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0090	MMC_IDINTEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						ai	ni	reserved				ces	du	reserved		fbe	ri	ti
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9]	RW	ai	Abnormal interrupt enable 0: disabled 1: The FBE, DU, and CES interrupts are enabled.
[8]	RW	ni	Normal interrupt enable 0: disabled 1: The TI and RI interrupts are enabled.
[7:6]	RO	reserved	Reserved

[5]	RW	ces	Card error interrupt enable 0: disabled 1: enabled
[4]	RW	du	Descriptor invalid interrupt enable 0: disabled 1: enabled
[3]	RO	reserved	Reserved
[2]	RW	fbe	Fatal bus error interrupt enable 0: disabled 1: enabled
[1]	RW	ri	RX interrupt enable 0: disabled 1: enabled
[0]	RW	ti	TX interrupt enable 0: disabled 1: enabled

MMC_DSCADDR

MMC_DSCADDR is an address register of the current descriptor.

Offset Address	Register Name	Total Reset Value
0x0094	MMC_DSCADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	had																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	had	Descriptor pointer. The value is automatically refreshed during data transfer. The register points to the start address of the descriptor that will be used by the IDMAC.

MMC_BUFADDR

MMC_BUFADDR is an address register of the current data buffer.

Offset Address	Register Name	Total Reset Value
0x0098	MMC_BUFADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	hba																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	hba	Data buffer pointer. The value is automatically refreshed during data transfer. The register points to the start address of the data buffer that is being used by the IDMAC.

MMC_CARDTHRCTL

MMC_CARDTHRCTL is a threshold control register.

Offset Address	Register Name	Total Reset Value
0x0100	MMC_CARDTHRCTL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				cardrdthreshold												reserved														BsyClrIntEn	cardrdthr_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RW	reserved	Reserved
[27:16]	RW	cardrdthreshold	Read threshold The maximum value is 512.
[15:2]	RW	reserved	Reserved
[1]	RW	BsyClrIntEn	Busy clear interrupt enable 0: disabled 1: enabled
[0]	RW	cardrdthr_en	Read threshold enable 0: disabled 1: enabled

MMC_UHS_REG_EXT

MMC_UHS_REG_EXT is a UHS extension register.

Offset Address	Register Name	Total Reset Value
0x0108	MMC_UHS_REG_EXT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	clk_drv_phase_ctrl	reserved	clk_smpl_phase_ctrl	reserved			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:23]	RW	clk_drv_phase_ctrl	clk_in_drv clock phase control 000: 0° 001: 45° 010: 90° 011: 135° 100: 180° 101: 225° 110: 270° 111: 315°
[22:19]	RO	reserved	Reserved
[18:16]	RW	clk_smpl_phase_ctrl	clk_in_sample clock phase control 000: 0° 001: 45° 010: 90° 011: 135° 100: 180° 101: 225° 110: 270° 111: 315°
[15:0]	RO	reserved	Reserved

MMC_DDR_REG

MMC_DDR_REG is an eMMC 4.5 DDR start bit detection control register.

Offset Address	Register Name	Total Reset Value
0x010C	MMC_DDR_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																half_start_bit															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	half_start_bit	DWC_mobile_storage internal start bit detection mechanism control. For eMMC 4.5 components, the start bit can be: 0: full cycle 1: non-full cycle Set this bit to 1 for the preceding eMMC 4.5 components, and set it to 0 for SD cards. When SATRT_BIT_SAMPLING_DDR or ASYNC_SAMPLE_DATA_PATH is set to 1, this bit is ignored.

MMC_ENABLE_SHIFT

MMC_ENABLE_SHIFT is a phase shift register.

Offset Address	Register Name	Total Reset Value
0x0110	MMC_ENABLE_SHIFT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														Enable Phase Shift Register	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RW	reserved	Reserved

[1:0]	RW	Enable Phase Shift Register	Phase shift control 00: default phase shift 01: Phase shift on the next rising edge 10: Phase shift on the next falling edge 11: Reserved

MMC_DATA

MMC_DATA is a data register (entrance address of the FIFO). The FIFO overflow must be read first before the data is read from or written to the FIFO.

Offset Address	Register Name	Total Reset Value
0x0200	MMC_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	data	Address for reading/writing to the FIFO. If the address ranges from 0x200 to 0x200 + FIFO_DEPTH, the FIFO is selected.

12.6 IR Interface

12.6.1 Overview

The infrared (IR) module receives data over the IR interface.

12.6.2 Features

The IR module has the following features:

- Allows you to disable the IR receive module by using software.
- Supports two operating modes:
  - Mode 0: supports decoding in four formats (including NEC with simple repeat code, NEC with full repeat code, SONY, and TC9012), error detection on received data, and IR wakeup.
  - Mode 1: supports the symbol level width detection in any data format.
- In mode 0, supports the RX data overflow interrupt, RX data frame format error interrupt, RX data frame interrupt, key release interrupt, and combined interrupt.
- In mode 1, supports the RX symbol overflow interrupt, RX symbol interrupt, symbol timeout interrupt, and combined interrupt.

- Supports the query of the raw interrupt status and the masked interrupt status.
- Supports interrupt clear and mask (write to clear).
- Supports IR wakeup.

12.6.3 Function Description

The IR module receives infrared signals transmitted by the infrared remote control, decodes the signals, and then transmits the decoded signals to the CPU system. When the chip is in the low-power state (the CPU is at a low frequency), the IR module generates an interrupt after receiving a complete frame, and transmits the interrupt to the CPU. In this way, the IR wake function is implemented.

The analysis of the signals transmitted by various infrared remote controls shows that the lead codes in the infrared commands vary according to remote controls. In addition, the subsequent control commands and the bits of command codes are also different. This is because infrared remote controls are not designed based on a unified infrared remote control standard. The basic encoding principles, however, are the same. That is, the pulses with different periods and duty ratios are used to represent 0 and 1. The duty ratios and pulse cycles may vary according to remote controls. Based on preceding differences, the code formats of the infrared data are classified into NEC with simple repeat code, NEC with full repeat code, TC9012 code, and SONY code.

Table 12-21 to Table 12-23 describe the code formats of the received infrared data.

NOTE

The values in Table 12-21 to Table 12-23 are tested before and may not be accurate. Therefore, they are only for reference.

Table 12-21 Code formats of the received infrared data (NEC with simple repeat code)

Data Format		NEC with Simple Repeat Code			
		uPD6121G	D6121/BU5777/D1913	LC7461M-C13	AEHA
Lead code (10 µs)	LEAD_S	900	900	900	337.6
	LEAD_E	450	450	450	168.8
Bit0 (10 µs)	B0_L	56	56	56	42.2
	B0_H	56	56	56	42.2
Bit1 (10 µs)	B1_L	56	56	56	42.2
	B1_H	169	169	169	126.6
Simple repeat code (10 µs)	SLEAD_S	900	900	900	337.6
	SLEAD_E	225	225	225	337.6
Burst (10 µs)		55	55	55	42.2
Frame length (10 µs)		108,00	10,800	10,800	8,777.6 – 12,828.8
Valid data bit		32	32	42	48

Table 12-22 Code formats of the received infrared data (NEC with full repeat code)

Data Format		NEC with Full Repeat Code						
		uPD6121G	LC7461M-C13	MN6024-C5D6	MN6014-C6D6	MATNEW	MN6030	PANASONIC
Lead code (10 µs)	LEAD_S	900	900	337.6	349.2	348.8	349	352
	LEAD_E	450	450	337.6	349.2	374.4	349	352
Bit 0 (10 µs)	B0_L	56	56	84.4	87.3	43.6	87.3	88
	B0_H	56	56	84.4	87.3	43.6	87.3	88
Bit 1 (10 µs)	B1_L	56	56	84.4	87.3	43.6	87.3	88
	B1_H	169	169	253.2	174.6	130.8	261.9	264
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None	None	None
	SLEAD_E							
Burst (10 µs)		55	55	84.4	87.3	43.6	87.3	88
Frame length (10 µs)		10,800	10,800	10,130	10,470	12,413.6 – 16,594.4	10,500	10,400
Valid data bit		32	42	22	24	48	22	22

Table 12-23 Code formats of the received infrared data (TC9012 code and SONY code)

Data Format		TC9012	SONY			
		TC9012F/9243	SONY-D7C5	SONY-D7C6	SONY-D7C8	SONY-D7C13
Lead code (10 µs)	LEAD_S	450	240	240	240	240
	LEAD_E	450	60	60	60	60
Bit0 (10 µs)	B0_L	56	60	60	60	60
	B0_H	56	60	60	60	60
Bit1 (10 µs)	B1_L	56	120	120	120	120
	B1_H	169	60	60	60	60
Simple repeat code (10 µs)	SLEAD_S	None	None	None	None	None
	SLEAD_E					
Burst (10 µs)		56	None	None	None	None
Frame length (10 µs)		10,800	4500	4500	4500	4500
Valid data bit		32	12	13	15	20

12.6.3.1 NEC with Simple Repeat Code

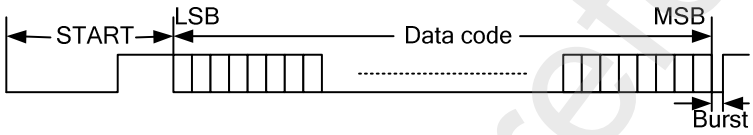
Frame Format

The NEC with simple repeat code consists of the following:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on specific code format. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

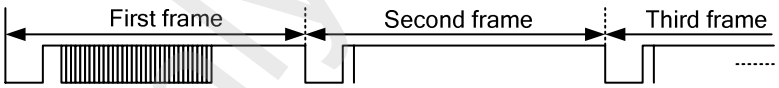
Figure 12-34 shows the frame format of transmitting a single NEC with simple repeat code.

Figure 12-34 Frame format for transmitting a single NEC with simple repeat code



If a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists only of a simple lead code and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). Figure 12-35 shows the frame format for transmitting NEC with simple repeat codes by pressing the key continuously.

Figure 12-35 Frame format for transmitting NEC with simple repeat codes by pressing the key continuously



Code Format

Figure 12-36 shows the definitions of bit0 and bit1 of the NEC with simple repeat code.

Figure 12-36 Definitions of bit0 and bit1 of the NEC with simple repeat code

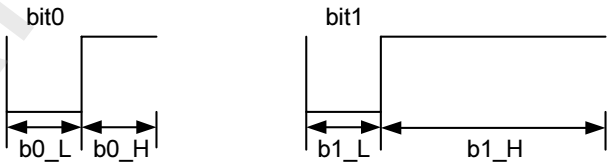


Figure 12-37 shows the format for transmitting a single NEC with simple repeat code. Figure 12-38 shows the format for transmitting consecutive NEC with simple repeat codes.

Figure 12-37 Format for transmitting a single NEC with simple repeat code

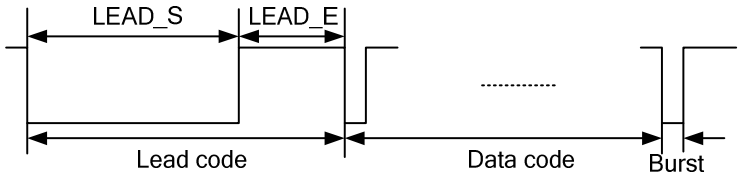
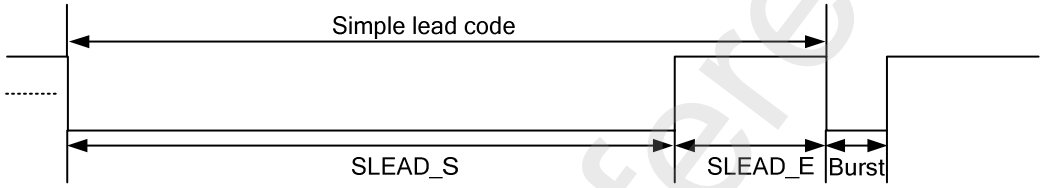


Figure 12-38 Code format for transmitting consecutive NEC with simple repeat codes



NOTE

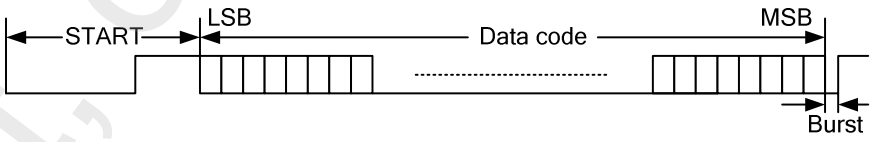
- The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 12-21 to Table 12-23.
- The frame length must be less than or equal to 160 ms. Otherwise, the simple lead code cannot be identified.

12.6.3.2 NEC with Full Repeat Code

Frame Format

The data format of the NEC with full repeat code consists of the following parts: START (lead code), data code, and burst. START (lead code): Consists of a start code (low level) and an end code (high level). Data code: The valid bits and the definition of each bit are determined by the specific code format. During data code reception, its LSB is received first. Burst signal: It is used to receive the last data bit. Figure 12-39 shows the frame format for transmitting a single NEC with full repeat code.

Figure 12-39 Frame format for transmitting a single NEC with full repeat code



If a complete data frame (first frame) is received after the key is held down for more than one frame length, the subsequently received data frame is still a complete data frame. That is, the first frame is transmitted repeatedly based on the frame length. Figure 12-40 shows the frame format for transmitting NEC with full repeat codes by pressing the key continuously.

Figure 12-40 Frame format for transmitting NEC with full repeat codes by pressing the key continuously

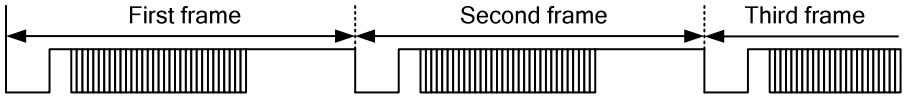


Figure 12-39 and Figure 12-40 show that the only difference between the NEC with simple repeat code and the NEC with full repeat code is the format of the repeat frame. For the NEC with simple repeat code, the simple lead code is transmitted; for the NEC with full repeat code, the complete frame is transmitted. That is, the first frame and the repeat frame are the same.

Code Format

Figure 12-41 shows the definitions of bit0 and bit1 of the NEC with full repeat code.

Figure 12-41 Definitions of bit0 and bit1 of the NEC with full repeat code

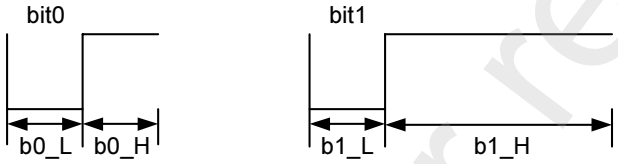
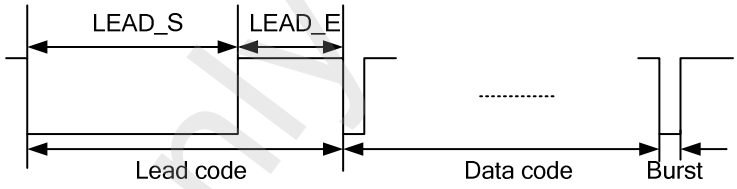


Figure 12-42 shows the format for transmitting a single NEC with full repeat code.

Figure 12-42 Format for transmitting a single NEC with full repeat code



NOTE

The pulse width of the high and low levels and the frame length depend on specific code formats. See Table 12-21 to Table 12-23.

12.6.3.3 TC9012 Code

Frame Format

CAUTION

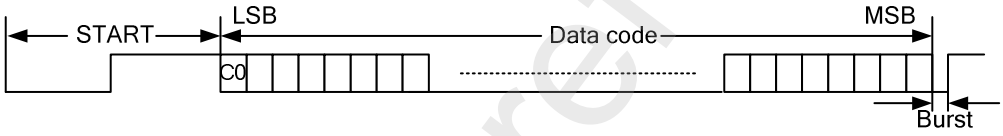
According to the features of the TC9012 code, the first bit of all key codes must be all 1s or all 0s. Otherwise, unnecessary frames are generated when the key are pressed continuously.

The TC9012 code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit depend on the specific code pattern. During data code reception, its LSB is received first.
- Burst signal: It is used to receive the last data bit.

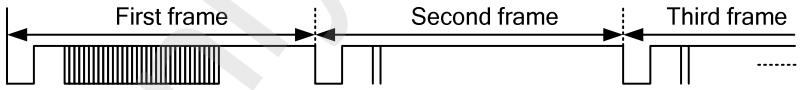
Figure 12-43 shows the frame format for transmitting a single TC9012 code.

Figure 12-43 Frame format for transmitting a single TC9012 code



When a complete data frame is received after the key is held down for more than one frame length, the subsequently received data frame consists of a lead code, a data bit, and a burst signal. The lead code also consists of a start code (low level) and an end code (high level). The data bit is the complement of the first data bit (C0) received in the previous frame. Figure 12-44 shows the frame format for transmitting TC9012 codes by pressing the key continuously.

Figure 12-44 Frame format for transmitting TC9012 codes by pressing the key continuously



Code Format

Figure 12-45 shows the definitions of bit0 and bit1 of the TC9012 code.

Figure 12-45 Definitions of bit0 and bit1 of the TC9012 code

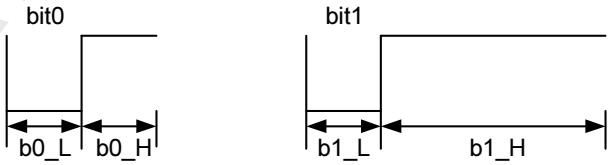


Figure 12-46 shows the format for transmitting a single TC9012 code.

Figure 12-46 Format for transmitting a single TC9012 code

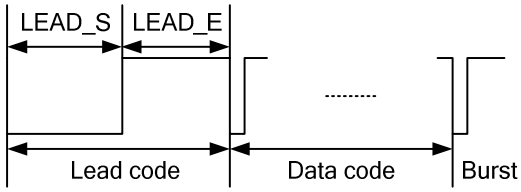


Figure 12-47 shows the format for transmitting consecutive TC9012 codes when C0 is 1.

Figure 12-47 Format for transmitting consecutive TC9012 codes (C0 = 1)

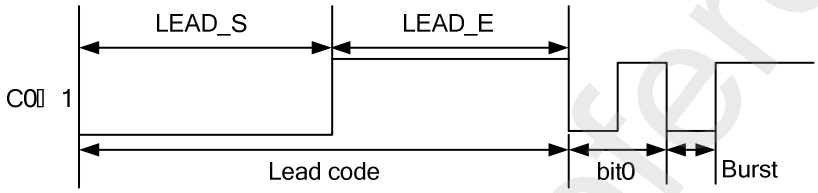
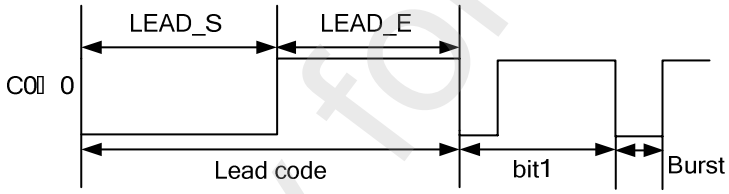


Figure 12-48 shows the format for transmitting consecutive TC9012 codes when C0 is 0.

Figure 12-48 Format for transmitting consecutiveTC9012 codes (C0 = 0)



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 12-21 to Table 12-23. In addition, the frame length must be less than or equal to 160 ms. Otherwise, the repeat frame cannot be identified.

12.6.3.4 SONY Code

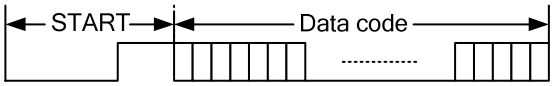
Frame Format

A SONY code consists of the following parts:

- Start code (lead code): Consists of a start code (low level) and an end code (high level).
- Data code: The valid bits and the definition of each bit are determined by the specific code pattern.

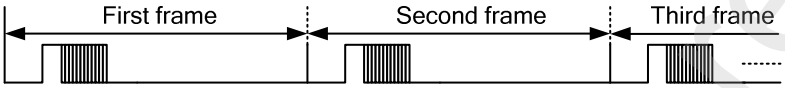
During reception, the LSB is received first. Figure 12-49 shows the frame format for transmitting a single SONY code.

Figure 12-49 Frame format for transmitting a single SONY code



When a complete data frame is received after the key is pressed for more than one frame length, the subsequently received data frame is also a complete data frame. Figure 12-50 shows the frame format for continuously transmitting SONY codes by pressing the key.

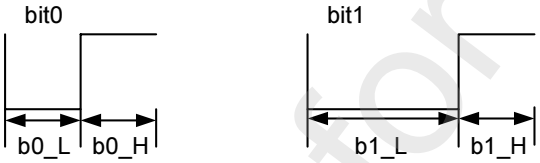
Figure 12-50 Frame format for continuously transmitting SONY codes by pressing the key



Code Format

Figure 12-51 shows the definitions of bit0 and bit1 of a SONY code.

Figure 12-51 Definitions of bit0 and bit1 of a SONY code



NOTE

The pulse width of the high level and low level and the frame length depend on specific code patterns. For details, see Table 12-21 to Table 12-23.

12.6.4 Operating Mode

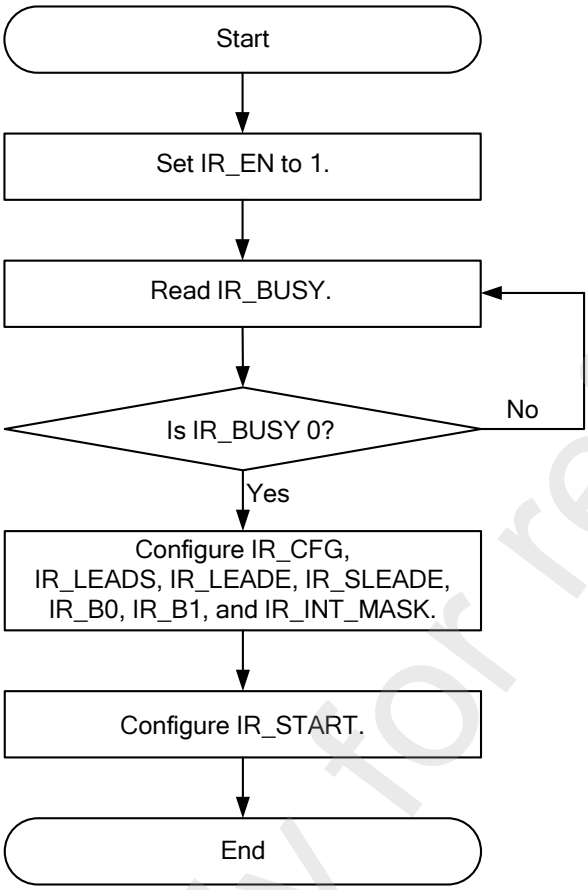
Soft Reset

When PERI_CRG57[4] is set to 1, the IR module is soft-reset separately. After reset, each configuration register is restored its default value. Therefore, these registers must be reinitialized.

Instances of Configuring Registers

Figure 12-52 shows the process of initializing the IR module.

Figure 12-52 Process of initializing the IR module



To initialize the IR module, perform the following steps:

Step 1 Select the address space of the IR module.

Step 2 Set IR_EN bit [0] to 1 to enable the IR receive module.

Step 3 Read IR_BUSY to check the current status of the IR module.

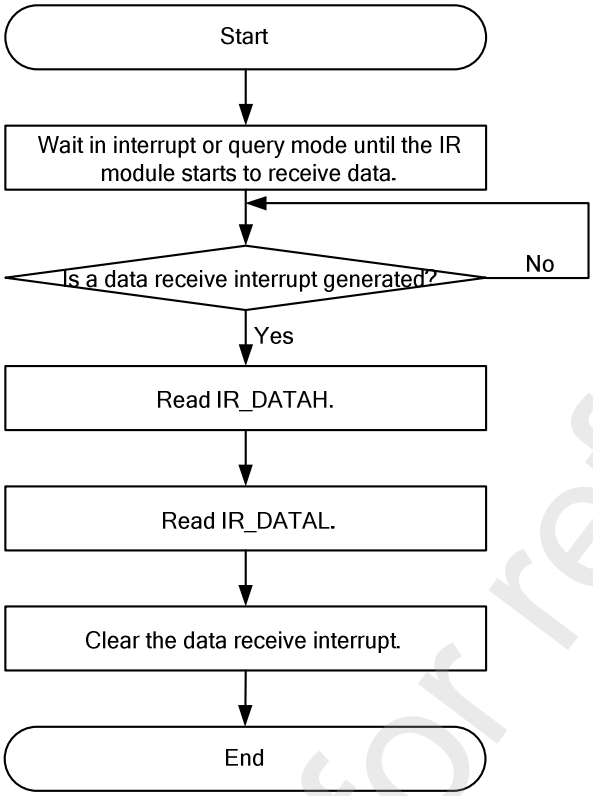
- If the value of IR_BUSY is 1, the IR module is busy. Then continue to read IR_BUSY. Note that configuring other control registers of the IR module by using software has no effect in this case.
- If the value of IR_BUSY is 0, the IR module is idle. Then go to Step 4.

Step 4 Configure IR_CFG, IR_LEADS, IR_LEADE, IR_SLEADE, IR_B0, IR_B1, and IR_INT_MASK. Note: You can update corresponding registers as required. If the registers are not updated, the original values are retained.

Step 5 Configure IR_STARTafter all IR control registers are configured. This is because IR_START is used to generate the start signal. If IR_START is configured, the IR module starts to receive infrared data based on the values of IR control registers.

----End

Figure 12-53 Process of reading the decoded data



To read the decoded data, perform the following steps:

Step 6 Select the address space of the IR module.

Step 7 Wait in interrupt or query mode until data frames are received.

- In interrupt mode, when the CPU receives an interrupt request signal from the IR module, read the value of IR_INT_STATUS[16]. If the value is 1, the IR module receives a data frame. Then, go to Step 8. If the value is 0, repeat Step 7 to wait for an interrupt.
- In query mode, continuously read the value of IR_INT_STATUS[0] by using software or read the value at intervals. If the value is 1, the IR module receives a data frame. Then, go to Step 8. If the value is 0, the IR module does not receive any data frame. Then, repeat Step 7 to continue the query.

Step 8 Read IR_DATAH. If the number of data bits in one frame is less than or equal to 32, skip this step.

Step 9 Read IR_DATAL.

Step 10 Clear the data receive interrupt.

----End

12.6.5 Register Summary

Table 12-24 describes IR registers.

Table 12-24 Summary of IR registers (base address: 0x120F_0000)

Offset Address	Register	Description	Page
0x000	IR_EN	IR receive enable control register	12-130
0x004	IR_CFG	IR configuration register	12-131
0x008	IR_LEADS	Lead code start bit margin configuration register (valid when IR_CFG[7] is 0 only)	12-132
0x00C	IR_LEADE	Lead code end bit margin configuration register (valid when IR_CFG[7] is 0 only)	12-133
0x010	IR_SLEADE	Simple lead code end bit margin configuration register (valid when IR_CFG[7] is 0 only)	12-135
0x014	IR_B0	Data 0 level judge margin configuration register (used only when IR_CFG[7] is 0)	12-136
0x018	IR_B1	Data 1 level judge margin configuration register (used only when IR_CFG[7] is 0)	12-137
0x01C	IR_BUSY	Configuration busy flag register	12-138
0x020	IR_DATAH	Upper 16-bit IR receive decoded data register (IR_CFG[7] = 0) or symbol count register in the symbol FIFO (IR_CFG[7] = 1)	12-138
0x024	IR_DATAL	Lower 32-bit IR receive decoded data register (IR_CFG[7] = 0) or IR received symbol width register (IR_CFG[7] = 1)	12-139
0x028	IR_INT_MASK	IR interrupt mask register	12-140
0x02C	IR_INT_STATUS	IR interrupt status register	12-142
0x030	IR_INT_CLR	IR interrupt clear register	12-143
0x034	IR_START	IR start configuration register	12-145

12.6.6 Register Description

IR_EN

IR_EN is an IR receive enable control register.

CAUTION

Before configuring other registers, you must set IR_EN[0] to 1 by using software. When IR_EN[0] is 0, other registers are read-only and the read values are their reset values.

Offset Address	Register Name	Total Reset Value
0x000	IR_EN	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved							ir_en
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	ir_en	IR receive module enable 0: disabled 1: enabled

IR_CFG

IR_CFG is an IR configuration register.

CAUTION

Before setting this register, you must set IR_BUSY bit[0] to 0 and set IR_EN bit[0] to 1. Otherwise, the original value is retained after configuration.

Offset Address	Register Name	Total Reset Value
0x004	IR_CFG	0x3E80_1F0B

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14	13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	ir_max_level_width				ir_format		ir_bits	ir_mode	ir_freq
Reset	0 0 1 1	1 1 1 0	1 0 0 0	0 0 0 0	0 0	0 1	1 1 1 1	0 0 0 0	1 0 1 1

Bits	Access	Name	Description
[31:16]	RW	ir_max_level_width	Invalid when IR_CFG[7] is 0. Indicates the maximum level width (in 10 μs) of a symbol whenIR_CFG[7] is 1. This width indicates the end of a symbol stream.
[15:14]	RW	ir_format	Indicates the data code format when IR_CFG[7] is 0.

			00: NEC with simple repeat code 01: TC9012 code 10: NEC with full repeat code 11: SONY code For details about the relationship between code types and code formats, see Table 12-21 to Table 12-23. Indicates the symbol format when IR_CFG[7] is 1. bit[15]: reserved The definitions of bit[14] are as follows: 0: The symbol is from low to high, and the symbol stream ends at the high level. 1: The symbol is from high to low, and the symbol stream ends at the low level.
[13:8]	RW	ir_bits	Indicates the number of data bits in a frame when IR_CFG[7] is 0. 0x00–0x2F: 1–48 data bits in a frame 0x30–0x3F: reserved If ir_bits is set to a value ranging from 0x30 to 0x3F by using software, the setting has no effect and the original value is retained. Indicates the symbol receive interrupt threshold when IR_CFG[7] is 1. bit[13]: reserved bit[12:8]: 0x0–0x1F. 0x0 indicates that an interrupt is reported when there is at least one symbol in the FIFO; 0x1F indicates that an interrupt is reported when there are at least 32 symbols in the FIFO, and so on.
[7]	RW	ir_mode	IR operating mode 0: The decoded complete data frames are output. 1: Only the symbol width is output.
[6:0]	RW	ir_freq	Frequency divider of the working clock. This register must be set to 0x17 if the IR reference clock is 24 MHz.

IR_LEADS

IR_LEADS is a lead code start bit margin configuration register (valid only when IR_CFG[7] = 0).

CAUTION

Before setting this register, you must set IR_BUSY[0] to 0 and set Register Description[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

The margin must be considered based on the typical value of the specific code type for accurately judging the start bit of the lead code. For details about the typical values of specific code types, see the values of LEAD_S in Table 12-21 to Table 12-23.

- For a pulse width whose typical value is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_S is 900, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 900 x 92% = 828 = 0x33C cnt_leads_max = 900 x 108% = 972 = 0x3CC

- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 as an example. If the typical value of LEAD_S is 240, the values of cnt_leads_min and cnt_leads_max are calculated as follows:

  cnt_leads_min = 240 x 80% = 192 = 0xC0 cnt_leads_max = 240 x 120% = 288 = 0x120

The basic configuration principle is as follows: cnt_leads_max is greater than or equal to cnt_leads_min, and cnt_leads_min is greater than cnt0_b_max and cnt1_b_max.

Offset Address	Register Name	Total Reset Value
0x008	IR_LEADS	0x033C_03CC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved								cnt_leads_min								reserved								cnt_leads_max							
Reset	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:16]	RW	cnt_leads_min	Minimum pulse width of the start bit of the lead code 0x000–0x007: reserved
[15:10]	RO	reserved	Reserved
[9:0]	RW	cnt_leads_max	Maximum pulse width of the start bit of the lead code 0x000–0x007: reserved

IR_LEADE

IR_LEADE is a lead code end bit margin configuration register (valid only when IR_CFG[7] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[0] to 0 and set IR_EN[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.

- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the lead code. The margin is about 8% of the type value. For details about the typical values of specific code types, see the values of LEAD_E in Table 12-21 to Table 12-23.

- For a pulse width whose typical value is greater than or equal to 400 (10 μs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of LEAD_E is 450, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 450 x 92% = 414 = 0x19E cnt_leade_max = 450 x 108% = 486 = 0x1E6

- For a pulse width whose typical value is less than 400 (10 μs precision), the recommended margin is 20% of the typical value. Take the SONY-D7C5 code as an example. If the typical value of LEAD_E is 60, the values of cnt_leade_min and cnt_leade_max are calculated as follows:

  cnt_leade_min = 60 x 80% = 48 = 0x030 cnt_leade_max = 60 x 120% = 72 = 0x048

The basic configuration principle is as follows: cnt_leade_max is greater than or equal to cnt_leade_min.

Offset Address	Register Name	Total Reset Value
0x00C	IR_LEADE	0x019E_01E6

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		cnt_leade_min		reserved		cnt_leade_max	
Reset	0 0 0 0	0 0 0 1	1 0 0 1	1 1 1 0	0 0 0 0	0 0 0 1	1 1 1 0	0 1 1 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_leade_min	Minimum pulse width of the end bit of the lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt_leade_max	Maximum pulse width of the end bit of the lead code 0x000–0x007: reserved

IR_SLEADE

IR_SLEADE is a simple lead code end bit margin configuration register (IR_CFG[7] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[0] to 0 and set IR_EN[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the NEC with simple repeat code, the margins of cnt_sleade and cnt_leade cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, the simple lead code cannot be identified. As a result, a frame format error occurs.
- This register must be configured only for the NEC with simple repeat code.

The margin must be considered based on the typical value of the specific code type for accurately judging the end bit of the simple lead code. For details about the typical values of specific code types, see the values of SLEAD_E in Table 12-21 to Table 12-23.

- For a pulse width whose typical value is greater than or equal to 225 (10 µs precision), the recommended margin is 8% of the typical value. Take the D6121 code as an example. If the typical value of SLEAD_E is 225, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 225 x 92% = 207 = 0xCF cnt_sleade_max = 225 x 108% = 243 = 0xF3

- For a pulse width whose typical value is less than 225 (10 µs precision), the recommended margin is 20% of the typical value. For example, if the typical value of SLEAD_E of a code type is 60, the values of cnt_sleade_min and cnt_sleade_max are calculated as follows:

  cnt_sleade_min = 60 x 80% = 48 = 0x30 cnt_sleade_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt_sleade_max is greater than or equal to cnt_sleade_min.

Offset Address	Register Name	Total Reset Value
0x010	IR_SLEADE	0x00CF_00F3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt_sleade_min								reserved								cnt_sleade_max							
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt_sleade_min	Minimum pulse width of the end bit of the simple lead code 0x000–0x007: reserved
[15:9]	RO	reserved	Reserved

[8:0]	RW	cnt_sleade_max	Maximum pulse width of the start bit of the simple lead code 0x000–0x007: reserved

IR_B0

IR_B0 is data 0 level judge margin configuration register (valid only when IR_CFG[7] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY[0] to 0 and set IR_EN[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type for accurately judging bit 0. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with full repeat code, NEC with simple repeat code, and TC9012 code, see the values of B0_H in Table 12-21 to Table 12-23. Take the D6121 code as an example. If the typical value of B0_H is 56 (10 µs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 56 x 80% = 45 = 0x2D cnt0_b_max = 56 x 120% = 67 = 0x43

- For details about the typical value of the SONY code, see the values of B0_L in Table 12-21 to Table 12-23. Take the SONY-D7C5 code as an example. If the typical value of B0_L is 60 (10 µs precision), the values of cnt0_b_min and cnt0_b_max are calculated as follows:

  cnt0_b_min = 60 x 80% = 48 = 0x30 cnt0_b_max = 60 x 120% = 72 = 0x48

The basic configuration principle is as follows: cnt0_b_max is greater than or equal to cnt0_b_min.

Offset Address	Register Name	Total Reset Value
0x014	IR_B0	0x002D_0043

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt0_b_min								reserved								cnt0_b_max							
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt0_b_min	Minimum pulse width of the level for judging bit0 0x000–0x007: reserved

[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt0_b_max	Maximum pulse width of the level for judging bit0 0x000–0x007: reserved

IR_B1

IR_B1 is data 1 judge level margin configuration register (valid only when IR_CFG[7] = 0).

CAUTION

- Before setting this register, you must set IR_BUSY bit[0] to 0 and set IR_EN bit[0] to 1. Otherwise, the original value of the register and the reserved value are retained after setting.
- For the preceding four code types, the margins for judging the levels of bit0 and bit1 cannot be overlapped. Otherwise, when the actual count value is within the overlapped range, bit1 cannot be identified and is regarded as bit0 by mistake.

A margin must be considered based on the typical value of the specific code type for accurately judging bit 1. The margin is about 20% of the typical value.

- For details about the typical values of the NEC with simple repeat code, NEC with simple repeat code, and TC9012 code, see the values of B1_H in Table 12-21 to Table 12-23. Take the D6121 code as an example. If the typical value of B1_H is 169 (10 µs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 169 x 80% = 135 = 0x87 cnt1_b_max = 169 x 120% = 203 = 0xCB

- For details about the typical value of the SONY code, see the values of B1_L in Table 12-21 to Table 12-23. Take the SONY-D7C5 code as an example. If the typical value of B1_L is 120 (10 µs precision), the values of cnt1_b_min and cnt1_b_max are calculated as follows:

  cnt1_b_min = 120 x 80% = 96 = 0x60 cnt1_b_max = 120 x 120% = 144 = 0x90

The basic configuration principle is as follows: cnt1_b_max is greater than or equal to cnt1_b_min.

Offset Address	Register Name	Total Reset Value
0x018	IR_B1	0x0087_00CB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								cnt1_b_min								reserved				cnt1_b_max											
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	1

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:16]	RW	cnt1_b_min	Minimum pulse width of the level for judging bit1

			0x000–0x007: reserved
[15:9]	RO	reserved	Reserved
[8:0]	RW	cnt1_b_max	Maximum pulse width of the level for judging bit1 0x000–0x007: reserved

IR_BUSY

IR_BUSY is a configuration busy flag register.

Offset Address	Register Name	Total Reset Value
0x01C	IR_BUSY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_busy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	ir_busy	Busy status flag 0: idle state. In this case, software can configure data. 1: busy state. In this state, software cannot configure data.

IR_DATAH

IR_DATAH is an upper 16-bit IR receive decoded data register (IR_CFG[7] = 0) or symbol count register in the symbol FIFO (IR_CFG[7] = 1)

The IR_DATAH register stores the upper 16 bits of the decoded data received by the IR, whereas IR_DATAL stores the lower 32 bits of the decoded data received by the IR. The data bits depend on the valid data bits in a frame and the specific code. For details, see the valid data bits in Table 12-21 to Table 12-23.

Data is stored as follows: The data is stored in IR_DATAH and IR_DATAL in sequence from MSB to LSB. That is, after IR_DATAL is full, the remaining data is stored in IR_DATAH. The unused upper bits are reserved. Data is read as follows: IR_DATAH and IR_DATAL are read in sequence.

The hardware receives all data bits without checking the definition of each data bit. The software is responsible for processing data bits.

Offset Address	Register Name	Total Reset Value
0x020	IR_DATAH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ir_datah															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	ir_datah	Indicates the upper 16 bits of the decoded data received by the IR module when IR_CFG[7] is 0. Indicates the symbol count in the symbol FIFO when IR_CFG[7] is 1. bit[15:6]: reserved bit[5:0]: number of symbols in the symbol FIFO

IR_DATAL

IR_DATAL is a lower 32-bit IR receive decoded data register (IR_CFG[7] = 0) or IR receive symbol width register (IR_CFG[7] = 1).

Offset Address	Register Name	Total Reset Value
0x024	IR_DATAL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ir_datal																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ir_datal	Indicates the lower 32 bits of the decoded data received by the IR module when IR_CFG[7] is 0. Indicates the width of the symbol received by the IR module when IR_CFG[7] is 1. The definitions of bit[31:16] are as follows: Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR when the symbol level is from low to high. Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low. The definitions of bit[15:0] are as follows: Indicates the low-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from low to high. Indicates the high-level width (a multiple of 10 μs) of the symbol received by the IR module when the symbol level is from high to low.

IR_INT_MASK

IR_INT_MASK is an IR interrupt mask register.

CAUTION

- Before setting this register, you must set IR_EN[0] to 1. Otherwise, the original value of the register is retained after setting.
- If all interrupts are masked, the IR wake-up function is unavailable.
- When IR_CFG[7] is 0, IR_INT_MASK bit[3:0] are valid; when IR_CFG[7] is 1, IR_INT_MASK bit[18:16] are valid.

The definitions of the interrupts related to the register are as follows:

- RX data overflow interrupt

  If the CPU does not fetch the current frame and the next frame is already received, the next frame overwrites the current frame and a raw RX data overflow error interrupt is reported.

- RX data frame format error interrupt

  If the received data frame is not complete or the data pulse width does not meet the margin requirements, a raw RX frame format error interrupt is reported.

- RX data frame interrupt

  After a complete frame data is received, a raw RX data frame interrupt is reported.

- Key release detection interrupt

  For the NEC with simple repeat code and TC9012 code, if the start synchronous code is not detected again within 160 ms after the previously detected start synchronous code, or a valid data frame rather than a simple lead code is detected, a raw key release detection interrupt is reported. Both the NEC with full repeat code and the SONY code do not support the key release detection interrupt.

- RX symbol overflow interrupt

  If the symbol FIFO is full because the CPU does not fetch the data in time and the subsequent symbol is already received, a raw RX symbol overflow error interrupt is reported.

- RX symbol interrupt

  If a complete symbol is received and the symbol count of the symbol FIFO is above the threshold configured by IR_CFG[ir_bits], a raw RX symbol interrupt is reported.

- Symbol timeout interrupt

  If no new symbol interrupt is received during the period configured by IR_CFG[ir_max_level_width] after a valid symbol is received, a raw symbol timeout interrupt is reported.

The hardware does not identify the interrupt priority. An interrupt is generated if one or more masked interrupt sources are valid.

Offset Address	Register Name	Total Reset Value
0x028	IR_INT_MASK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intm_overrun	intm_time_out	intm_symb_rcv	reserved												intm_release	intm_overflow	intm_frame_error	intm_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	RW	intm_overrun	Symbol overflow interrupt mask when IR_CFG[7] is 1 0: not masked 1: masked
[17]	RW	intm_time_out	Symbol timeout interrupt mask when IR_CFG[7] is 1 0: not masked 1: masked
[16]	RW	intm_symb_rcv	RX N symbol interrupt mask when IR_CFG[7] is 1 0: not masked 1: masked
[15:4]	RO	reserved	Reserved
[3]	RW	intm_release	Key release interrupt mask when IR_CFG[7] is 0 0: not masked 1: masked
[2]	RW	intm_overflow	RX data overflow interrupt mask when IR_CFG[7] is 0 0: not masked 1: masked
[1]	RW	intm_frame_error	RX data frame format error interrupt mask when IR_CFG[7] is 0 0: not masked 1: masked
[0]	RW	intm_rcv	RX data frame interrupt mask when IR_CFG[7] is 0 0: not masked 1: masked

IR_INT_STATUS

IR_INT_STATUS is an IR interrupt status register.

CAUTION

- When IR_CFG[7] is 0, IR_INT_STATUS bit[3:0] and IR_INT_STATUS bit[19:16] are valid.
- When IR_CFG[7] is 1, IR_INT_STATUS bit[10:8] and IR_INT_STATUS bit[26:24] are valid.

Offset Address	Register Name	Total Reset Value
0x02C	IR_INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved					intms_overrun	intms_time_out	intms_symb_rcv	reserved				intms_release	intms_overflow	intms_frame_error	intms_rcv	reserved				intrs_overrun	intrs_time_out	intrs_symb_rcv		reserved				intrs_release	intrs_overflow	intrs_frame_error	intrs_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:27]	RO	reserved	Reserved
[26]	RO	intms_overrun	Masked symbol overflow interrupt status when IR_CFG[7] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[25]	RO	intms_time_out	Masked symbol timeout interrupt status when IR_CFG[7] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[24]	RO	intms_symb_rcv	Masked RX symbol interrupt status when IR_CFG[7] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[23:20]	RO	reserved	Reserved
[19]	RO	intms_release	Masked key release interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[18]	RO	intms_overflow	Masked RX data overflow error interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.

[17]	RO	intms_frame_error	Masked RX data frame format error interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[16]	RO	intms_rcv	Masked RX data frame interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[15:11]	RO	reserved	Reserved
[10]	RO	intrs_overrun	Raw symbol overflow interrupt status when IR_CFG[7] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[9]	RO	intrs_time_out	Raw symbol timeout interrupt status when IR_CFG[7] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[8]	RO	intrs_symb_rcv	Raw RX symbol interrupt status when IR_CFG[7] is 1 0: No interrupt is generated. 1: An interrupt is generated.
[7:4]	RO	reserved	Reserved
[3]	RO	intrs_release	Raw key release interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[2]	RO	intrs_overflow	Raw RX data overflow error interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[1]	RO	intrs_frame_error	Raw RX data frame format error interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.
[0]	RO	intrs_rcv	Raw RX data frame interrupt status when IR_CFG[7] is 0 0: No interrupt is generated. 1: An interrupt is generated.

IR_INT_CLR

IR_INT_CLR is an IR interrupt clear register.

CAUTION

- When IR_CFG[7] is 0, IR_INT_CLR bit[3:0] are valid.
- When IR_CFG[7] is 1, IR_INT_CLR bit[18:16] are valid.

Offset Address: 0x030 | Register Name: IR_INT_CLR | Total Reset Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved													intc_overrun	intc_time_out	intc_symb_rcv	reserved												intc_release	intc_overflow	intc_framerr	intc_rcv
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:19]	RO	reserved	Reserved
[18]	WC	intc_overrun	When IR_CFG[7] is 1, this bit indicates whether the symbol overflow interrupt request is cleared. 0: no effect 1: cleared
[17]	WC	intc_time_out	When IR_CFG[7] is 1, this bit indicates whether the symbol timeout interrupt request is cleared. 0: no effect 1: cleared
[16]	WC	intc_symb_rcv	When IR_CFG[7] is 1, this bit indicates whether the RX symbol interrupt request is cleared. 0: no effect 1: cleared
[15:4]	RO	reserved	Reserved
[3]	WC	intc_release	When IR_CFG[7] is 0, this bit indicates whether the key release interrupt request is cleared. 0: no effect 1: cleared
[2]	WC	intc_overflow	When IR_CFG[7] is 0, this bit indicates whether the RX data overflow error interrupt request is cleared. 0: no effect 1: cleared

[1]	WC	intc_framerr	When IR_CFG[7] is 0, this bit indicates whether the RX data frame format error interrupt request is cleared. 0: no effect 1: cleared
[0]	WC	intc_rcv	When IR_CFG[7] is 0, this bit indicates whether the RX data frame interrupt request is cleared. 0: no effect 1: cleared If an RX data frame interrupt is generated and the software writes 1 to the bit without reading the data in IR_DATAL, the interrupt cannot be cleared.

IR_START

IR_START is an IR start configuration register.

After other registers are configured, IR_START can be started when any value is written to the corresponding address during the startup of the IR module.

Offset Address	Register Name	Total Reset Value
0x034	IR_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															ir_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	WO	ir_start	IR start configuration register

12.7 GPIO

12.7.1 Overview

Hi3516C V300 supports 9 groups of general purpose input/output (GPIO) pins, that is, GPIO0 to GPIO8. Each group of GPIO pins provides eight programmable input/output pins (GPIO8 has only three pins). Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes. As input, each GPIO pin can act as an interrupt source; as output, each GPIO pin can be set to 0 or 1 separately.

The GPIO can generate maskable interrupts based on the level or transition value. The general purpose input output interrupt (GPIOINTR) signal provides an indicator to the interrupt controller, indicating that an interrupt occurs.

CAUTION

- For details about the number of GPIO pins and multiplexing relationship between GPIO pins and other pins, see Hi3516CV300_PINOUT_EN.xlsx
- For the multiplexed GPIO pins that are output by default, note that the pins that connect to the chip and the components must be input.

12.7.2 Features

Each GPIO pin can be configured as input or output.

- As input, each GPIO pin can act as an interrupt source.
- As output, each GPIO can be set to 0 or 1 separately.

12.7.3 Operating Mode

Interface Reset

The GPIO is reset during chip power-on reset or system reset, and GPIO pins are in input state after being reset.

GPIO

Each pin can be configured as input or output. To configure a GPIO pin, perform the following steps:

Step 1 Enable the required GPIO pins by configuring corresponding pins according to the description of *Hi3516CV300_PINOUT_EN.xlsx*.

Step 2 Configure the GPIO as input or output by using the GPIO_DIR register.

Step 3 When the GPIO pins are in input mode, read the GPIO_DATA register to check the input signal value. When the GPIO pins are in output mode, write the output value to the GPIO_DATA register to control the output level of the GPIO pins.

----End

CAUTION

When the GPIO pins are in output mode, do not enable the GPIO interrupt. Otherwise, the GPIO interrupt will be generated when output signals meet interrupt generation conditions.

Interrupt Operation

The GPIO interrupt is controlled through seven registers (such as GPIO_IS). These registers enable you to select the interrupt source, interrupt edge (falling edge or rising edge), and interrupt trigger modes (level-sensitive mode or edge-sensitive mode). For details about the corresponding interrupt registers of the GPIO, see section 3.3 "Interrupt Systems."

When multiple interrupts are generated at the same time, these interrupts are combined into an interrupt and then reported. For details about the GPIO interrupt mapping, see section 3.3 "Interrupt Systems."

The GPIO_IS, GPIO_IBE, and GPIO_IEV registers determine the features of the interrupt source and interrupt trigger type.

GPIO_RIS and GPIO_MIS are used to read the raw interrupt status and masked interrupt status, respectively. GPIO_IEV controls the final report status of each interrupt. In addition, GPIO_IC is provided to clear the interrupt status.

Perform the following operations to configure GPIO pins to the interrupt mode:

Step 1 Select the edge-sensitive mode or level-sensitive mode by configuring the GPIO_IS register.

Step 2 Select the falling-/rising-edge-sensitive mode or high-/low-level-sensitive mode by configuring the GPIO_IEV register.

Step 3 If the edge-sensitive mode is selected, select single-edge-sensitive mode or dual-edge-sensitive mode by configuring the GPIO_IBE register.

Step 4 Write 0xFF to the GPIO_IC register to clear the interrupt.

Step 5 Set the GPIO_IE to 1 to enable the interrupt.

----End

CAUTION

Ensure that data in GPIO pins is stable during initialization to prevent pseudo interrupts.

The GPIO interrupts are controlled by seven registers. When one or more GPIO pins generate interrupts, a combined interrupt is output to the interrupt controller. The differences between the edge-sensitive mode and level-sensitive mode are as follows:

- Edge-sensitive mode: Software must clear this interrupt to enable superior interrupts.
- Level-sensitive mode: The external interrupt source must keep this level until the processor identifies this interrupt.

12.7.4 Register Summary

Table 12-25 lists the base addresses for 9 groups of GPIO registers.

Table 12-25 Base addresses for 9 groups of GPIO registers

Register	Base Address
GPIO8	0x1214_8000
GPIO7	0x1214_7000
GPIO6	0x1214_6000
GPIO5	0x1214_5000
GPIO4	0x1214_4000
GPIO3	0x1214_3000
GPIO2	0x1214_2000
GPIO1	0x1214_1000
GPIO0	0x1214_0000

Table 12-26 describes the offset addresses and definitions of a group of internal GPIO registers. GPIO0 to GPIO8 also have the same internal GPIO registers.

NOTE

- Register address of GPIO*n* = GPIO*n* base address + Offset address of the register
- The value of *n* ranges from 0 to 8.

Table 12-26 Summary of GPIO registers

Offset Address	Register	Description	Page
0x000–0x3FC	GPIO_DATA	GPIO data register	12-149
0x400	GPIO_DIR	GPIO direction control register	12-149
0x404	GPIO_IS	GPIO interrupt trigger register	12-150
0x408	GPIO_IBE	GPIO interrupt dual-edge trigger register	12-150
0x40C	GPIO_IEV	GPIO interrupt trigger event register	12-151
0x410	GPIO_IE	GPIO interrupt mask register	12-151
0x414	GPIO_RIS	GPIO raw interrupt status register	12-152
0x418	GPIO_MIS	GPIO masked interrupt status register	12-152
0x41C	GPIO_IC	GPIO interrupt clear register	12-153

12.7.5 Register Description

GPIO_DATA

GPIO_DATA is a GPIO data register. It is used to buffer the input or output data.

When the corresponding bit of the GPIO_DIR is configured as output, the values written to the GPIO_DATA register are sent to the corresponding pin (note that the pin multiplexing configuration must be correct). If the bit is configured as input, the value of the corresponding input pin is read.

CAUTION

If the corresponding bit of GPIO_DIR is configured as input, the pin value is returned after a valid read; if the corresponding bit is configured as output, the written value is returned after a valid read.

Through PADDR[9:2], the GPIO_DATA register masks the read and write operations on the register. The register corresponds to 256 address spaces. PADDR[9:2] corresponds to GPIO_DATA[7:0]. When the corresponding bit is high, it can be read or written. When the corresponding bit is low, no operations are supported. For example:

- If the address is 0x3FC (0b11_1111_1100), the operations on all the eight bits of GPIO_DATA bit[7:0] are valid.
- If the address is 0x200 (0b10_0000_0000), only the operation on GPIO_DATA bit[7] is valid.

Offset Address	Register Name	Total Reset Value
0x000–0x3FC	GPIO_DATA	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_data							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_data	Indicates the GPIO input data when the GPIO is configured as input; indicates the GPIO output data when the GPIO is configured as output. Each bit can be controlled separately. The register is used together with GPIO_DIR.

GPIO_DIR

GPIO_DIR is a GPIO direction control register. It is used to configure the direction of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x400	GPIO_DIR	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_dir							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_dir	GPIO direction control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit can be controlled separately. 0: input 1: output

GPIO_IS

GPIO_IS is a GPIO interrupt trigger register. It is used to configure the interrupt trigger mode.

Offset Address	Register Name	Total Reset Value
0x404	GPIO_IS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_is							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_is	GPIO interrupt trigger control register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: edge-sensitive mode 1: level-sensitive mode

GPIO_IBE

GPIO_IBE is a GPIO interrupt dual-edge trigger register. It is used to configure the edge trigger mode of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x408	GPIO_IBE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ibe							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ibe	GPIO interrupt edge control register. Bit[7:0] correspond to GPIO_DATA [7:0] respectively. Each bit is controlled independently. 0: single-edge-sensitive mode. The GPIO_IEV register controls whether the interrupt is rising-edge-sensitive or falling-edge-sensitive. 1: dual-edge-sensitive mode

GPIO_IEV

GPIO_IEV is a GPIO interrupt event register. It is used to configure the interrupt trigger event of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x40C	GPIO_IEV	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_iev							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_iev	GPIO interrupt trigger event register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: falling-edge-sensitive mode or low-level-sensitive mode 1: rising-edge-sensitive mode or high-level-sensitive mode.

GPIO_IE

GPIO_IE is a GPIO interrupt mask register. It is used to mask GPIO interrupts.

Offset Address	Register Name	Total Reset Value
0x410	GPIO_IE	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ie							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RW	gpio_ie	GPIO interrupt mask register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: masked 1: not masked

GPIO_RIS

GPIO_RIS is a GPIO raw interrupt status register. It is used to query the raw interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x414	GPIO_RIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ris							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_ris	GPIO raw interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the unmasked interrupt status. The status cannot be masked and controlled by the GPIO_IE register. 0: No interrupt occurs. 1: An interrupt is generated.

GPIO_MIS

GPIO_MIS is a GPIO masked interrupt status register. It is used to query the masked interrupt status of each GPIO pin.

Offset Address	Register Name	Total Reset Value
0x418	GPIO_MIS	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_mis							

Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	RO	gpio_mis	GPIO masked interrupt status register. Bit[7:0] correspond to GPIO_DATA [7:0], indicating the masked interrupt status. The status is controlled by the GPIO_IE register. 0: The interrupt is invalid. 1: The interrupt is valid.

GPIO_IC

GPIO_IC is a GPIO interrupt clear register. It is used to clear the interrupts generated by GPIO pins and clear the GPIO_RIS and GPIO_MIS registers.

Offset Address	Register Name	Total Reset Value
0x41C	GPIO_IC	0x00

Bit	7	6	5	4	3	2	1	0
Name	gpio_ic							
Reset	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[7:0]	WC	gpio_ic	GPIO interrupt clear register. Bit[7:0] correspond to GPIO_DATA [7:0]. Each bit is controlled separately. 0: no effect 1: cleared

12.8 USB 2.0 Host

12.8.1 Overview

The USB 2.0 host controller supports the high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) data transfer modes. It complies with the USB 2.0, open host controller interface (OHCI) V1.0a, and enhanced host controller interface (EHCI) V1.0 protocols. The USB 2.0 host controller has a root hub. As a part of the USB system, the root hub is used to extend the USB port. By using in the controller, the following functions are achieved:

- Controls and processes data transfer.
- Parses data packets and packages data.
- Encodes and decodes the signals transmitted through the USB port.
- Provide interfaces (such as the interrupt vector interface) for the driver.

The USB 2.0 device controller supports high-speed (480 Mbit/s) and full-speed (12 Mbit/s) data transfer modes. It also supports host/device intelligent switching.

12.8.2 Function Description

Logic Block Diagram

Figure 12-54 shows the logic block diagram of the USB 2.0 host controller.

Figure 12-54 Logic block diagram of the USB 2.0 host controller

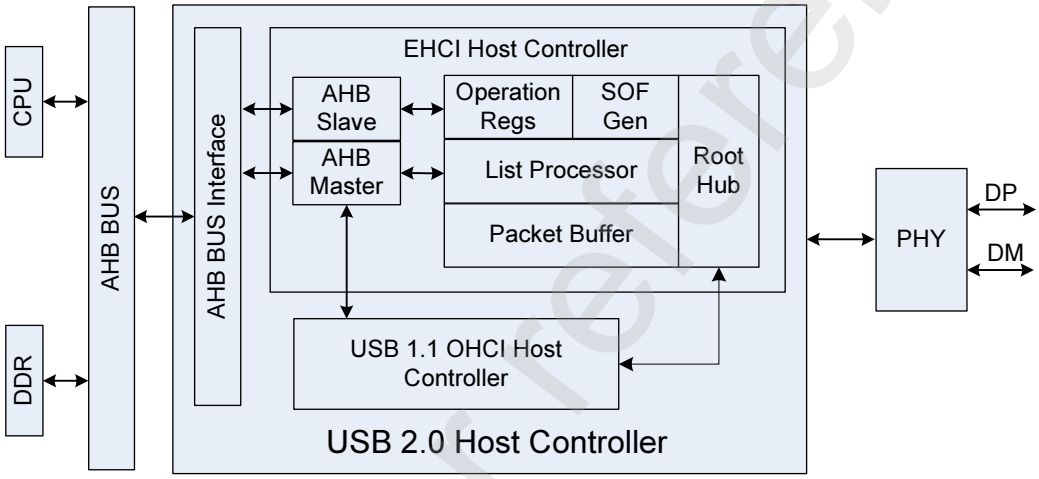
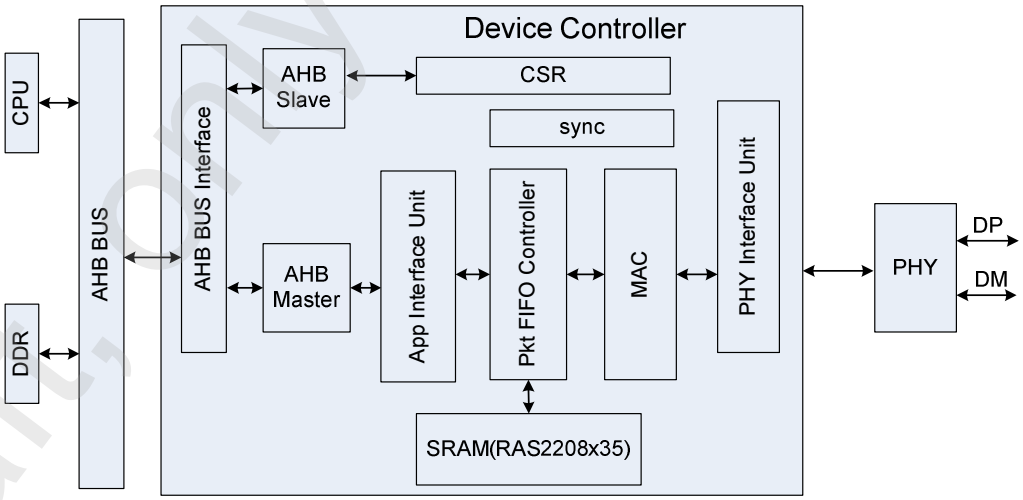


Figure 12-55 shows the logic block diagram of the USB 2.0 device.

Figure 12-55 Logic block diagram of the USB 2.0 device controller



NOTE

- UTMI: USB2.0 transceiver macrocell interface
- EHCI: enhanced host controller interface
- OHCI: open host controller interface

Typical Application

For details about the reference design of the USB 2.0 host controller, see the *Hi3516C V300 Hardware Design User Guide*.

Functions

The USB 2.0 host controller has the following features:

- Fully compatible with USB 2.0.
- Complies with OHCI V1.0a and EHCI V1.0 protocols.
- Supports high-speed, full-speed, and low-speed devices.
- Supports low-power solutions.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.
- Supports a maximum of 127 devices by using USB hubs

The USB 2.0 device controller has the following features:

- Complies with the USB 2.0 standard.
- Supports high-speed and full-speed devices.
- Supports four basic data transfer modes including control transfer, bulk transfer, isochronous transfer, and interrupt transfer.

Working Principle

The USB 2.0 host controller supports the following four standard transfer modes:

- Control transfer

  This mode applies to the data transfer between endpoints 0 of USB host and the USB device. For the USB devices of specific models, other endpoints may be used. The control transfer is bidirectional and the transferred data amount is small. Depending on the device and transfer speed, 8-byte data, 16-byte data, 32-byte data, or 64-byte data can be transferred.

- Bulk transfer

  This mode applies to the data transfer in bulk when there is no limit on the bandwidth and time interval. This mode is the best choice when the transfer speed is very low and many data transfers are delayed. Bulk transfer can be performed after all other types of data transfers are complete. In bulk transfer mode, data is transferred between the USB Host and USB Device without errors by using an error detection and retransmission mechanism.

- Isochronous transfer

  This mode applies to the stream data transfer with strict time requirements and strong error tolerance or the instant data transfer at a constant transfer rate. This mode provides a fixed bandwidth and time interval.

- Interrupt transfer

This mode applies to the data transfer when the data is scattered, unpredictable, and is of small volume. In this mode, the device is checked whether there is interrupt data to be sent at a fixed interval. The query frequency ranges from 1 ms to 255 ms and it depends on the device endpoint mode. The typical interrupt transfer mode is unidirectional and only input is available for the USB host.

12.8.3 Operating Mode

Host/Device Switching

You can configure the MISC_CTRL23[usb_chipid] to operate in host or device mode.

To enable the register to operate in host mode, set MISC_CTRL23[usb_chipid] to 0; to enable the register to operate in device mode, set MISC_CTRL23[usb_chipid] to 1.

Pin Polarity Control

The valid polarity of the USB PHY can be configured by setting MISC_CTRL23 [usb_host_pwren_pctrl].

Clock Gating

If the USB 2.0 host controller is not used, its clock can be disabled to reduce power consumption.

To disable the clock, perform the following steps:

Step 1 Write 1 to PERI_CRG46 [usb2_phy_port0_treq], PERI_CRG46[usb2_phy_req], PERI_CRG46[usb2_utmi0_srst_req], PERI_CRG46[usb2_otg_phy_srst_req], PERI_CRG46[usb2_hst_phy_srst_req], and PERI_CRG46[usb2_bus_srst_req] respectively to reset the USB controller and PHY.

Step 2 Set PERI_CRG46 [usb2_bus_cken] to 0 to disable the clocks of the USB 2.0 host controller.

----End

To enable the clock, perform the following steps:

Step 1 Deassert the reset on the USB controller and PHY. For details, see "Reset Deassert".

Step 2 Set PERI_CRG46 [usb2_bus_cken] to 1 to enable the USB 2.0 host clocks.

----End

Reset Deassert

By default, the USB controller and PHY are reset after power-on. To deassert reset, perform the following steps:

Step 1 Enable the reference clock and delay at least 10 μs until the clock is stable

Step 2 Write 0 to PERI_CRG46[usb2_phy_req] to deassert POR on the USB PHY, and wait at least 1 ms until the USB PHY PLL is stable.

Step 3 Write 0 to PERI_CRG46[usb2_phy_port0_treq] to deassert reset on the USB PHY UTMI, and wait at least 100 us until the USB PHY UTMI circuit is stable.

Step 4 Write 0 to PERI_CRG46[usb2_utmi0_srst_req], PERI_CRG46[usb2_otg_phy_srst_req], PERI_CRG46[usb2_hst_phy_srst_req], and PERI_CRG46[usb2_bus_srst_req] to deasert soft reset on the USB host controller, USB device controller, and USB bus.

----End

12.8.4 Register Summary

USB HOST Register

The USB 2.0 host controller includes the EHCI controller and OHCI controller. Table 12-27 and Table 12-28 describes USB 2.0 registers.

Table 12-27 Summary of EHCI registers (base address: 0x1012_0000)

Offset Address	Register	Description	Page
0x00	CAPVERSION	Controller version register	12-161
0x04	HCSPARAMS	Controller structure parameter register	12-161
0x08	HCCPARAMS	Controller specifications parameter register	12-162
0x10	USBCMD	USB command register	12-163
0x14	USBSTS	USB status register	12-165
0x18	USBINTR	USB interrupt enable register	12-167
0x1C	FRINDEX	Periodic linked list pointer register	12-168
0x24	PERIODICLISTBASE	Periodic linked list base address register	12-168
0x28	ASYNCLISTBASE	Non-periodic linked list base address register	12-169
0x50	CONFIGFLAG	Configuration flag register	12-169
0x54	PORTSC	Port status and control register	12-170
0x90	INSNREG00	Micro-frame length configuration register	12-161
0x94	INSNREG01	PBUF OUT/IN THRESHOLD register	12-173
0x98	INSNREG02	PBUF depth register	12-174
0x9C	INSNREG03	Controller configuration register 0	12-174
0xA0	INSNREG04	Controller configuration register 1	12-175
0xA4	INSNREG05	UTMI control and status register	12-176
0xA8	INSNREG06	AHB error status register	12-176
0xAC	INSNREG07	AHB error address register	12-177

Table 12-28 Summary of OHCI registers (base address: 0x1011_0000)

Offset Address	Register	Description	Page
0x00	HCREVERSION	Controller version register	12-178
0x04	HCCONTROL	Controller configuration register	12-178
0x08	HCCMDSTS	Controller command status register	12-179
0x0C	HCINTSTS	Interrupt status register	12-180
0x10	HCINTENABLE	Interrupt enable register	12-182
0x14	HCINTDISABLE	Interrupt disable register	12-183
0x18	HCCA	Controller communication physical address register	12-184
0x1C	PCED	Periodic linked list physical address register	12-185
0x20	CHED	Physical address register for the head endpoint descriptor of the control linked list	12-185
0x24	CCED	Physical address register for the current endpoint descriptor of the control linked list	12-186
0x28	BHED	Physical address register for the head endpoint descriptor of the batch linked list	12-186
0x2C	BCED	Physical address register for the current endpoint descriptor of the batch linked list	12-186
0x30	DH	Physical address register of the last descriptor	12-187
0x34	FSMPS	Maximum packet length and frame interval register	12-187
0x38	FMR	Remaining time counter register of the current frame	12-188
0x3C	FMNR	Frame ID counter register	12-189
0x40	PSR	Periodic linked list start register	12-189
0x44	LSTHRESHOLD	Low-speed transmission threshold register	12-190
0x48	RHDA	RH descriptor register A	12-190
0x4C	RHDB	RH descriptor register B	12-192
0x50	RHSTS	RH status register	12-192
0x54	RHPORTSTS	RH port status register	12-193

USB Device Register Overview

Table 12-29 describes the UBS device register overview.

Table 12-29 USB device register overview (base address: 0x1013_0000)

Offset Address	Name	Description	Page
0x0000	GOTGCTL	Device control and status register	12-195
0x0004	GOTGINT	Interrupt generation indicator register	12-198
0x0008	GAHBCFG	AHB configuration register	12-199
0x000C	GUSBCFG	USB configuration register	12-201
0x0010	GRSTCTL	Hardware reset register	12-202
0x0014	GINTSTS	Interrupt register	12-204
0x0018	GINTMSK	Interrupt mask register	12-206
0x0020	GRXSTSP	RX status register	12-209
0x0024	GRXFSIZ	RX FIFO depth register	12-210
0x0028	GNPTXFSIZ	Non-periodic TX FIFO depth register	12-210
0x002C	GNPTXSTS	Non-periodic TX FIFO/queue status register	12-211
0x0040	GSNPSID	Synopsys ID query register	12-212
0x0044	GHWCFG1	Hardware configuration register 1	12-212
0x0048	GHWCFG2	Hardware configuration register 2	12-213
0x004C	GHWCFG3	Hardware configuration register 3	12-214
0x0050	GHWCFG4	Hardware configuration register 4	12-216
0x005C	GDFIFOCFG	DFIFO software configuration register	12-218
0x0104 + 0x0004 x (FIFO_num – 1)	DIEPTXFN	IN endpoint TX FIFO depth register	12-218
0x0800	DCFG	Device configuration register	12-219
0x0804	DCTL	Device control register	12-220
0x0808	DSTS	Device status register	12-222
0x0810	DIEPMSK	Common interrupt mask register for IN endpoints	12-222
0x0814	DOEPMSK	Common interrupt mask register for OUT endpoints	12-224
0x0818	DAINT	Interrupt indicator register for all endpoints	12-225

Offset Address	Name	Description	Page
0x081C	DAINTMSK	Interrupt mask register for all endpoints	12-226
0x0820	DTKNQR1	IN token learning queue register 1	12-226
0x0824	DTKNQR2	IN token learning queue register 2	12-227
0x0830	DTKNQR3	IN token learning queue register 3	12-228
0x0834	DTKNQR4	IN token learning queue register 4	12-228
0x0828	DVBUSDIS	Device VBUS discharge time register	12-228
0x082C	DVBUSPULSE	Device VBUS pulsing time register	12-229
0x0830	DTHRCTL	Device threshold control register	12-229
0x0834	DIEPEMPMSK	FIFO empty interrupt mask register for device IN endpoints	12-231
0x0900	DIEPCTL0	Control register for device control IN endpoint 0	12-231
0x0B00	DOEPCTL0	Control register for device control OUT endpoint 0	12-232
0x0908 + (0x0020 x *n*)	DIEPINTn	Device IN endpoint-n interrupt register	12-233
0x0B08 + (0x0020 x *n*)	DOEPINTn	Device OUT endpoint-n interrupt register	12-235
0x0910	DIEPTSIZ0	Transfer size register for device IN endpoint 0	12-237
0x0B10	DOEPTSIZ0	Transfer size register for device OUT endpoint 0	12-238
0x0910 + (0x0020 x *n*)	DIEPTSIZn	Transfer size register for device IN Endpoint-n	12-239
0x0B10 + (0x0020 x *n*)	DOEPTSIZn	Transfer size register for device OUT endpoint-n	12-239
0x0914 + (0x0020 x *n*)	DIEPDMAN	Device IN endpoint-n DMA address register	12-240
0x0B14 + (0x0020 x *n*)	DOEPDMAN	Device OUT endpoint-n DMA address register	12-241
0x091C + (0x0020 x *n*)	DIEPDMABN	Device IN endpoint-n DMA buffer address register	12-241
0x0B1C + (0x0020 x *n*)	DOEPDMABN	Device OUT endpoint-n DMA buffer address register	12-242
0x0918	DTXFSTS0	IN endpoint 0 TX FIFO status register	12-242
0x0918 + (0x0020 x *n*)	DTXFSTSn	INendpoint *n* TX FIFO status register	12-242

NOTE

FIFO_num: number of FIFOs, ranging from 0 to 14

n: endpoint ID, ranging from 0 to 15

12.8.5 Register Description

12.8.5.1 EHCI Register Description

CAPVERSION

CAPVERSION is a controller version register.

Offset Address	Register Name	Total Reset Value
0x00	CAPVERSION	0x0100_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HCI_version																reserved								caplength							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	HCI_version	Controller version
[15:8]	-	reserved	Reserved
[7:0]	RO	caplength	Address length of the specifications information register, which is also the offset of the function access register

HCSPARAMS

HCSPARAMS is a controller structure parameter register.

Offset Address	Register Name	Total Reset Value
0x04	HCSPARAMS	0x0000_1111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								dbg_port_num				reserved				port_indicator	N_CC			N_PCC				port_routing_rule				reserved				port_power_control	N_PORTS			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:20]	RO	dbg_port_num	Debugging port ID (optional), starting from 1

[19:17]	-	reserved	Reserved
[16]	RO	port_indicator	Whether to support the port indicator control bit 0: not supported 1: supported
[15:12]	RO	N_CC	Number of OHCI controllers 0: There is no OHCI controller. The USB port supports only high-speed USB devices. *N*: There are *N* OHCI controllers. The USB port supports full-speed/low-speed devices. *N* ranges from 0x1 to 0xF.
[11:8]	RO	N_PCC	Number of ports supported by each OHCI controller. For example, if NPORTS = 6 and N_CC = 2, N_PCC = 3.
[7]	RO	port_routing_rule	Rule for mapping between the OHCI controller and ports. There is only one OHCI controller here, and all ports are mapped to this controller.
[6:5]	-	reserved	Reserved
[4]	RO	port_power_control	Whether the controller supports control over the port power 0: not supported 1: supported
[3:0]	RO	N_PORTS	Number of ports of the controller, ranging from 0x1 to 0xF

HCCPARAMS

HCCPARAMS is a controller specifications parameter register.

Offset Address	Register Name	Total Reset Value
0x08	HCCPARAMS	0x0000_A026

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved				EECP		isoc_scheduling_threshold	reserved	async_schedule_park_cap	programmable_frame_list_flag	addressing_cap
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 1 0	0 0 0 0	0 0 1 0	0	1	1	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved

[15:8]	RO	EECP	EHCI extended capability pointer, indicating whether the extended capability register exists 0x00: The extended capability register does not exist. Other values: offset address relative to the first EHCI extended capability during PCI configuration
[7:4]	RO	isoc_scheduling_threshold	Position of the real-time linked list that can be updated by software (relative to the current value). If bit[7] is 0, bit[6:4] indicate the number of micro-frames that can be buffered before the real-time descriptor status is updated. If bit[7] is 1, the driver considers that the controller has been buffering descriptors.
[3]	-	reserved	Reserved
[2]	RO	async_schedule_park_cap	Park feature of the async linked list 0: The async linked list does not support the park function. 1: The queue heads of the async linked list support the part function, and the function can be enabled or disabled by configuring the USBCMD register.
[1]	RO	programmable_frame_list_flag	Whether the flag linked list length is programmable 0: The length of the linked list is fixed at 1024 units, and the frame list size of the USBCMD register is 0 and read-only. 1: The length of the linked list can be configured by setting the frame list size register. Note that the address of the linked list must be physically consecutive.
[0]	RO	addressing_cap	Address bit width of the memory accessed by the controller 0: 32-bit 1: 64-bit

USBCMD

USBCMD is a USB COMMAND register.

Offset Address	Register Name	Total Reset Value
0x10	USBCMD	0x0008_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								interrupt_threshold_control								reserved				async_schedule_park_mode_enable	reserved	async_schedule_park_mode_count		light_HC_reset	interrupt_on_async_advance_doorbell	asynchronous_schedule_enable	periodic_schedule_enable	frame_list_size		HC_reset	run_stop
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	-	reserved	Reserved
[23:16]	RW	interrupt_threshold_control	Maximum rate for triggering interrupts by the controller 0x00: reserved 0x01: 1 micro-frame 0x02: 2 micro-frame 0x04: 4 micro-frame 0x08: 8 micro-frame 0x10: 16 micro-frame 0x20: 32 micro-frame 0x40: 64 micro-frame Other values: undefined
[15:12]	-	reserved	Reserved
[11]	RO	async_schedule_park_mode_enable	Park mode enable 0: disabled 1: enabled
[10]	-	reserved	Reserved
[9:8]	RW	async_schedule_park_mode_count	Number of transactions that the controller can handle successfully from the queue head
[7]	RW	light_HC_reset	Light reset on the controller, which does not affect the port status 0: not reset 1: reset

[6]	RW	interrupt_on_async_advance_doorbell	The software set this DoorBell register to 1 to instruct the controller to report an interrupt the next time the async linked list is processed. 0: invalid 1: valid
[5]	RW	asynchronous_schedule_enable	Async linked list enable 0: disabled. The controller does not provide the periodic linked list. 1: enabled
[4]	RW	periodic_schedule_enable	Periodic linked list enable 0: disabled. The controller does not provide the periodic linked list. 1: enabled
[3:2]	RW	frame_list_size	Length of the specified linked list 0x0: 1024 units (4096 bytes) 0x1: 512 units 0x2: 256 units 0x3: reserved
[1]	RW	HC_reset	Controller reset 0: not reset 1: reset
[0]	RW	run_stop	Whether the EHC handles the linked list 0: stop 1: run

USBSTS

USBSTS is a USB status register.

Offset Address	Register Name	Total Reset Value
0x14	USBSTS	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																asynchronous_schedule_status	periodic_schedule_status	reclamation	HC_halted	reserved						interrupt_on_async_advance	host_system_error	frame_list_rollover	port_change_interrupt	USB_error_interrupt	USB_interrupt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15]	RO	asynchronous_schedule_status	Real-time status of the async linked list 0: disabled 1: enabled
[14]	RO	periodic_schedule_status	Real-time status of the periodic linked list 0: disabled 1: enabled
[13]	RO	reclamation	This bit is set to 1 when the async linked list is empty. 0: invalid 1: valid
[12]	RO	HC_halted	Controller stop working flag bit 0: invalid 1: valid
[11:6]	-	reserved	Reserved
[5]	RWC	interrupt_on_async_advance	The driver enables the controller to report an interrupt the next time the async linked list is processed. 0: invalid 1: valid
[4]	RWC	host_system_error	This bit is set to 1 if a serious error occurs when the controller accesses the host system. In addition, the RUN_STOP bit is set to 0 to stop descriptor processing. 0: invalid 1: valid

[3]	RWC	frame_list_rollover	This bit is set to 1 when the frame list index changes from the maximum value to 0. 0: invalid 1: valid
[2]	RWC	port_change_interrupt	Port status change 0: valid 1: invalid
[1]	RWC	USB_error_interrupt	This bit is set to 1 when an error occurs during a transaction. 0: invalid 1: valid
[0]	RWC	USB_interrupt	This bit is set to 1 after the controller completes a transaction. 0: invalid 1: valid

USBINTR

USBINTR is a USB interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x18	USBINTR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										interrupt_on_async_advance_enable	host_system_error	frame_list_rollover_enable	port_change_interrupt_enable	USB_error_interrupt_enable	USB_interrupt_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	-	reserved	Reserved

[5]	RW	interrupt_on_async_advance_enable	Interrupt on async advance enable interrupt enable 0: disabled 1: enabled
[4]	RW	host_system_error	Host system error interrupt enable 0: disabled 1: enabled
[3]	RW	frame_list_rollover_enable	Frame list rollover enable interrupt enable 0: disabled 1: enabled
[2]	RW	port_change_interrupt_enable	Port change interrupt enable 0: disabled 1: enabled
[1]	RW	USB_error_interrupt_enable	USB error interrupt enable 0: disabled 1: enabled
[0]	RW	USB_interrupt_enable	USB interrupt enable 0: disabled 1: enabled

FRINDEX

FRINDEX is a periodic linked list pointer register.

Offset Address	Register Name	Total Reset Value
0x1C	FRINDEX	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				frame_index											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13:0]	RW	frame_index	Pointer to the periodic linked list. It is used for the controller to access the periodic linked list. This register is updated at an interval of 125 us.

PERIODICLISTBASE

PERIODICLISTBASE is a periodic linked list base address register.

Offset Address	Register Name	Total Reset Value
0x24	PERIODICLISTBASE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	0
Name	base_address																				reserved										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RW	base_address	Base address of the periodic linked list, corresponding to bit[32:12] of the memory address
[11:0]	-	reserved	Reserved

ASYNCLISTBASE

ASYNCLISTBASE is a non-periodic linked list base address register.

Offset Address	Register Name	Total Reset Value
0x28	ASYNCLISTBASE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	link_pointer_low																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RW	link_pointer_low	Address of the next queue head to be executed, corresponding to bit[31:5] of the memory address
[4:0]	-	reserved	Reserved

CONFIGFLAG

CONFIGFLAG is a configuration flag register.

Offset Address	Register Name	Total Reset Value
0x50	CONFIGFLAG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															config_flag
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	-	reserved	Reserved
[0]	RW	config_flag	Whether the port is taken over by the OHCI or EHCI controller 0: The port is taken over by the OHCI controller. 1: The port is taken over by the EHCI controller.

PORTSC

PORTSC is a port status and control register.

Offset Address	Register Name	Total Reset Value
0x54	PORTSC	0x0000_2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved									WKOC_E	WKDSCNNT_E	WKCNNNT_E	port_test_control				port_indicator_control		port_owner	port_power	line_state		reserved	prt_reset	suspend	force_port_resume	over_current_change	over_current_active	port_enable_change	port_enable	connect_status_change	current_connect_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:23]	-	reserved	Reserved
[22]	RW	WKOC_E	Overcurrent wakeup enable. For details about the operation mode, see section 4.3.1 in the EHCI protocol standard. 0: disabled 1: enabled

[21]	RW	WKDSCNNT_E	Disconnection wakeup enable. For details about the operation mode, see section 4.3.1 in the EHCI protocol standard. 0: disabled 1: enabled
[20]	RW	WKCNNNT_E	Connection wakeup enable. For details about the operation mode, see section 4.3.1 in the EHCI protocol standard. 0: disabled 1: enabled
[19:16]	RW	port_test_control	Test mode control 0x0: The test mode is invalid. 0x1: Test J_STATE 0x2: Test K_STATE 0x3: Test SE0_STATE 0x4: Test Packet 0x5: Test FORCE_ENABLE Other values: undefined
[15:14]	RW	port_indicator_control	This bit is invalid if P_INDICATOR is 0.
[13]	RW	port_owner	This bit is 0 when the ConfigFlag register changes from 0 to 1 and it 1 when the ConfigFlag register is 0. The software uses this bit to release the controller port permission. When the device connected to the port is not a high-speed device, the software writes 1 to this bit and the OHCI controller takes over the port. 0: The EHCI controller takes over the port. 1: The OHCI controller takes over the port.
[12]	RW	port_power	Controller port power control 0: off 1: on
[11:10]	RO	line_state	Line state, indicating the current logic state of D+(bit 11) and D-(bit 10). This register is valid only when the port is disabled and CCS is 1. 00: SE0, non-low-speed device 10: J state, non-low-speed device 01: K state, low-speed device, releasing port permissions 11: undefined
[9]	-	reserved	Reserved
[8]	RW	prt_reset	Port reset. Writing 1 to this bit starts bus reset, and writing 0 to this bit terminates bus reset. 0: The port is not reset. 1: The port is reset.

[7]	RW	suspend	Port standby status 0: The port is not in standby status. 1: The port is in standby status.
[6]	RW	force_port_resume	Port wakeup. This bit is set to 1 when the controller detects the change from the J state to K state in standby mode to drive the wakeup signal. 0: Wakeup is not detected on the port. 1: Wakeup is detected on the port (K state).
[5]	RWC	over_current_change	Port overcurrent status change 0: not changed 1: changed
[4]	RO	over_current_active	Port overcurrent status 0: no overcurrent 1: overcurrent
[3]	RWC	port_enable_change	Port enable status change 0: not changed 1: changed
[2]	RW	port_enable	Port enable status. The port can be enabled only by the controller but not software. 0: disabled 1: enabled
[1]	RWC	connect_status_change	Port connection status change 0: not changed 1: changed
[0]	RO	current_connect_status	Current port connection status 0: No device is connected to the port. 1: A device is connected to the port.

INSNREG00

INSNREG00 is a micro-frame length configuration register.

Offset Address	Register Name	Total Reset Value
0x90	INSNREG00	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												frame_correction				frame_counter															frame_couter_en
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:20]	RO	reserved	Reserved
[19:14]	RW	frame_correction	Micro-frame count correction, only for debugging
[13:1]	RW	frame_counter	Value of the micro-frame counter. This register is used only for emulation. In normal mode, the micro-frame length is 125 µs defined by the protocol. During emulation, you can change the micro-frame length by configuring this register as required to reduce the emulation time.
[0]	RW	frame_couter_en	Micro-frame length register enable 0: disabled 1: enabled

INSNREG01

INSNREG01 is a PBUF out/in threshold register.

Offset Address	Register Name	Total Reset Value
0x94	INSNREG01	0x0020_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	out_threshold																in_threshold															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	out_threshold	TX threshold. If the data amount in the PBUF is above the TX threshold, data starts to be transmitted.
[15:0]	RW	in_threshold	RX threshold. If the data amount in the PBUF is above the RX threshold, data is read from the PBUF.

INSNREG02

INSNREG02 is a PBUF depth register.

Offset Address	Register Name	Total Reset Value
0x98	INSNREG02	0x0000_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				pbuf_depth											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RW	pbuf_depth	PBUF depth.

INSNREG03

INSNREG03 is controller configuration register 0.

Offset Address	Register Name	Total Reset Value
0x9C	INSNREG03	0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	resume_clk_check_en	ignore_linestate	tx_tx_turnaround_delay			periodic_frame_list_fetch	time_available_offset							break_memory_transfer	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Access	Name	Description
[31:15]	RO	reserved	Reserved
[14]	RW	resume_clk_check_en	Clock check enable of the wakeup sequence 0: disabled 1: enabled
[13]	RW	ignore_linestate	Enable of ignoring line state check during SOF transmission in SE0_NAK test mode 0: disabled 1: enabled

[12:10]	RW	tx_tx_turnaround_delay	TX-TX turnaround delay addition
[9]	RW	periodic_frame_list_fetch	Instruction fetch interval of the periodic linked list 0: instruction fetch when the micro-frame ID is 0 1: instruction fetch for each micro-frame
[8:1]	RW	time_available_offset	Available time offset of the bus. The USB transmission starts only when the time before the EOF1 time point is sufficient.
[0]	RO	break_memory_transfer	Transfer enable. Data in the memory is packaged into large blocks and transmitted immediately when the PBUF IN/OUT threshold is reached. 0: disabled 1: enabled

INSNREG04

INSNREG04 is controller configuration register 1.

Offset Address	Register Name	Total Reset Value
0xA0	INSNREG04	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										auto_resume_en	nak_reload_fix_en	reserved		scaledwn_enum_time	hccparam_writable	hcsparam_writable	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5]	RW	auto_resume_en	When the controller is halted but the port is not woken up from the standby mode, port exceptions occur because the PHY does not output the clock. Setting this bit to 0 automatically wakes up the port when the controller is halted, preventing the preceding port exceptions. 0: enabled 1: disabled
[4]	RW	nak_reload_fix_en	NAK reload enable 0: enabled 1: disabled
[3]	RO	reserved	Reserved

[2]	RW	scaledwn_enum_time	Port enumeration time scale down enable 0: disabled 1: enabled
[1]	RW	hccparam_writable	HCCPARAMS bit[17], bit[15:4], and bit[2:0] write enable 0: disabled 1: enabled
[0]	RW	hcsparam_writable	HCSPARAMS register write enable 0: disabled 1: enabled

INSNREG05

INSNREG05 is a UTMI control and status register.

Offset Address	Register Name	Total Reset Value
0xA4	INSNREG05	0x0000_1000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														vbusy		vport				reserved											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RO	vbusy	If this bit is 1, the hardware is writing or reading. This bit is set to 0 when the read or write operation is complete.
[16:13]	RW	vport	Port ID. It cannot exceed the supported number of ports.
[12:0]	RO	reserved	Reserved

INSNREG06

INSNREG06 is an AHB error status register.

Offset Address	Register Name	Total Reset Value
0xA8	INSNREG06	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb_err_captured	reserved																			hbusrt_value				num_of_beat				num_of_successful_beat			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	ahb_err_captured	AHB bus error status 0: No error is detected. 1: An error is detected.
[30:12]	RO	reserved	Reserved
[11:9]	RO	hbusrt_value	hbrust value during the control phase when an AHB error occurs
[8:4]	RO	num_of_beat	Number of beats during a burst transfer when an AHB error occurs. The maximum number of beats is 16. 0x00–0x10: valid 0x11–0x1F: reserved
[3:0]	RO	num_of_successful_beat	Number of completed beats during a burst transfer when an AHB error occurs

INSNREG07

INSNREG07 is an AHB error address register.

Offset Address	Register Name	Total Reset Value
0xAC	INSNREG07	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ahb_master_error_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	ahb_master_error_addr	Address during the control phase when an AHB error occurs

12.8.5.2 OHCI Register Description

HCREVERSION

HCREVERSION is a controller version register.

Offset Address	Register Name	Total Reset Value
0x00	HCREVERSION	0x0000_0010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								revision							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Access	Name	Description
[31:8]	-	reserved	Reserved
[7:0]	RO	revision	Protocol version supported by the controller

HCCONTROL

HCCONTROL is a controller configuration register.

Offset Address	Register Name	Total Reset Value
0x04	HCCONTROL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																					remote_wakeup_enable	remote_wakeup_connected	interrupt_routing	HC_func_state		bulk_list_enable	control_list_enable	isochronous_enable	periodic_list_enable	control_bulk_service_ratio	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:11]	-	reserved	Reserved
[10]	RW	remote_wakeup_enable	Remote wakeup enable 0: disabled 1: enabled
[9]	RW	remote_wakeup_connected	Whether the controller supports remote wakeup 0: not supported 1: supported

[8]	RW	interrupt_routing	Interrupt source select for the HCINTERRUPTSTATUS register 0: normal host bus interrupt 1: system management interrupt
[7:6]	RW	HC_func_state	Working status of the controller 00: bus reset 01: wakeup 10: normal 11: standby
[5]	RW	bulk_list_enable	Batch transfer linked list processing enable for the next frame 0: disabled 1: enabled
[4]	RW	control_list_enable	Control transfer linked list processing enable for the next frame 0: disabled 1: enabled
[3]	RW	isochronous_enable	Real-time endpoint descriptor enable 0: disabled 1: enabled
[2]	RW	periodic_list_enable	Periodic linked list processing enable for the next frame 0: disabled 1: enabled
[1:0]	RW	control_bulk_service_ratio	Ratio of control endpoint descriptors to batch endpoint descriptors 00: 1:1 01: 2:1 10: 3:1 11: 4:1

HCCMDSTS

HCCMDSTS is a controller command status register.

Offset Address	Register Name	Total Reset Value
0x08	HCCMDSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														scheduling_overrun_count		reserved												ownership_change_request	bulk_list_filled	control_list_filled	HC_reset
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved
[17:16]	RW	scheduling_overrun_count	Scheduling overflow counter. The value increases by 1 each time a scheduling overflow error occurs.
[15:4]	-	reserved	Reserved
[3]	RW	ownership_change_request	Controller permission change request 0: There is no request. 1: There is a request.
[2]	RW	bulk_list_filled	When the batch transfer linked list has descriptors 0: no 1: yes
[1]	RW	control_list_filled	When the control transfer linked list has descriptors 0: no 1: yes
[0]	RW	HC_reset	Controller reset, which does not affect the root hub status 0: not reset 1: reset

HCINTSTS

HCINTSTS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0C	HCINTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	ownership_change	reserved																							root_hub_status_change	frame_num_overflow	unrecoverable_error	resume_detected	start_of_frame	writeback_done_head	scheduling_overrun
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30]	RW	ownership_change	Controller ownership change 0: invalid 1: valid
[29:7]	-	reserved	Reserved
[6]	RW	root_hub_status_change	This bit is set to 1 when the root hub status or root hub port status changes. 0: invalid 1: valid
[5]	RW	frame_num_overflow	Frame number overflow interrupt. This bit is set to 1 when hc_frame_num bit[15] changes from 1 to 0 or from 0 to 1. 0: invalid 1: valid
[4]	RW	unrecoverable_error	Interrupt indicating that an unrecoverable error occurs 0: invalid 1: valid
[3]	RW	resume_detected	Interrupt indicating that a wakeup signal is detected 0: invalid 1: valid
[2]	RW	start_of_frame	SOF flag 0: invalid 1: valid

[1]	RW	writeback_done_head	Write-back completion head flag 0: invalid 1: valid
[0]	RW	scheduling_overrun	Current frame scheduling overflow 0: Overflow does not occur. 1: Overflow occurs.

HCINTENABLE

HCINTENABLE is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x10	HCINTENABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	master_interrupt_en	ownership_change_en	reserved																						root_hub_status_change_en	frame_num_overflow_en	unrecoverable_error_en	resume_detected_en	start_of_frame_en	writeback_done_head_en	scheduling_overrun_en	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	master_interrupt_en	Controller master interrupt enable 0: disabled 1: enabled
[30]	RW	ownership_change_en	Controller ownership change interrupt enable 0: disabled 1: enabled
[29:7]	-	reserved	Reserved
[6]	RW	root_hub_status_change_en	Root hub status or root hub port status change interrupt enable 0: disabled 1: enabled
[5]	RW	frame_num_overflow_en	Frame number overflow interrupt enable 0: disabled 1: enabled

[4]	RW	unrecoverable_error_en	Unrecoverable error interrupt enable 0: disabled 1: enabled
[3]	RW	resume_detected_en	Wakeup interrupt enable 0: disabled 1: enabled
[2]	RW	start_of_frame_en	SOF interrupt enable 0: disabled 1: enabled
[1]	RW	writeback_done_head_en	Write-back completion head interrupt enable 0: disabled 1: enabled
[0]	RW	scheduling_overrun_en	Frame scheduling overflow interrupt enable 0: disabled 1: enabled

HCINTDISABLE

HCINTDISABLE is an interrupt disable register.

Offset Address	Register Name	Total Reset Value
0x14	HCINTDISABLE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	master_interrupt_disable	ownership_change_disable	reserved																						root_hub_status_change_disable	frame_num_overflow_disable	unrecoverable_error_disable	resume_detected_disable	start_of_frame_disable	writeback_done_head_disable	scheduling_overrun_disable	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	master_interrupt_disable	Controller master interrupt disable 0: ignored 1: disabled

[30]	RW	ownership_change_disable	Controller ownership change interrupt disable 0: ignored 1: disabled
[29:7]	-	reserved	Reserved
[6]	RW	root_hub_status_change_disable	Root hub status or root hub port status change interrupt disable 0: ignored 1: disabled
[5]	RW	frame_num_overflow_disable	Frame number overflow interrupt disable 0: ignored 1: disabled
[4]	RW	unrecoverable_error_disable	Unrecoverable error interrupt disable 0: ignored 1: disabled
[3]	RW	resume_detected_disable	Wakeup interrupt disable 0: ignored 1: disabled
[2]	RW	start_of_frame_disable	SOF interrupt disable 0: ignored 1: disabled
[1]	RW	writeback_done_head_disable	Write-back completion head interrupt disable 0: ignored 1: disabled
[0]	RW	scheduling_overrun_disable	Frame scheduling overflow interrupt disable 0: ignored 1: disabled

HCCA

HCCA is a controller communication physical address register.

Offset Address	Register Name	Total Reset Value
0x18	HCCA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	host_controller_communication_area																								reserved							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RW	host_controller_communication_area	Physical address for communications between the driver and controller
[7:0]	-	reserved	Reserved

PCED

PCED is a periodic linked list physical address register.

Offset Address	Register Name	Total Reset Value
0x1C	PCED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	period_current_ED																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	period_current_ED	Physical address of the current real-time or interrupt endpoint descriptor
[3:0]	-	reserved	Reserved

CHED

CHED is a physical address register for the head endpoint descriptor of the control linked list.

Offset Address	Register Name	Total Reset Value
0x20	CHED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	control_head_ED																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	control_head_ED	Physical address of the first endpoint descriptor of the control linked list

[3:0]	-	reserved	Reserved

CCED

CCED is a physical address register for the current endpoint descriptor of the control linked list.

Offset Address	Register Name	Total Reset Value
0x24	CCED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	control_current_Ed																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	control_current_Ed	Physical address of the current endpoint descriptor of the control linked list
[3:0]	-	reserved	Reserved

BHED

BHED is a physical address register for the head endpoint descriptor of the batch linked list.

Offset Address	Register Name	Total Reset Value
0x28	BHED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bulk_head_ED																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	bulk_head_ED	Physical address of the head endpoint descriptor of the batch linked list
[3:0]	-	reserved	Reserved

BCED

BCED is a physical address register for the current endpoint descriptor of the batch linked list.

Offset Address	Register Name	Total Reset Value
0x2C	BCED	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bulk_current_ED																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	bulk_current_ED	Physical address of the current endpoint descriptor of the batch linked list
[3:0]	-	reserved	Reserved

DH

DH is a physical address register of the last descriptor.

Offset Address	Register Name	Total Reset Value
0x30	DH	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	done_head																												reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:4]	RW	done_head	Physical address of the last descriptor
[3:0]	-	reserved	Reserved

FSMPS

FSMPS is a maximum packet length and frame interval register.

Offset Address	Register Name	Total Reset Value
0x34	FSMPS	0x2778_2EDF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_interval_toggle	FS_lagest_data_packet															reserved				frame_interval											
Reset	0	0	1	0	0	1	1	1	0	1	1	1	1	0	0	0	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1

Bits	Access	Name	Description
[31]	RW	frame_interval_toggle	This bit is inverted each time frame_interval is reloaded.
[30:16]	RW	FS_lagest_data_packet	Length of the largest packet at full speed
[15:14]	-	reserved	Reserved
[13:0]	RW	frame_interval	Bit interval between two frames

FMR

FMR is a remaining time counter register of the current frame.

Offset Address	Register Name	Total Reset Value
0x38	FMR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	frame_remaing_toggle	reserved																							frame_remaining							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	frame_remaing_toggle	This bit is loaded each time frame_remaining counts to 0.
[30:14]	-	reserved	Reserved
[13:0]	RW	frame_remaining	Remaining bit time count of the current frame, descending. The value of frame_interval is loaded each time frame_remaining counts to 0.

FMNR

FMNR is a frame number counter register.

Offset Address	Register Name	Total Reset Value
0x3C	FMNR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																FN															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	FN	Frame number counter, which increases by 1 for each frame

PSR

PSR is a periodic linked list start register.

Offset Address	Register Name	Total Reset Value
0x40	PSR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				periodic_start											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13:0]	RW	periodic_start	When the value of frame_remaining is the same as the value of this register, the processing of periodic linked list takes priority over that of control transfer linked list and batch transfer linked list.

LSTHRESHOLD

LSTHRESHOLD is a low-speed transmission threshold register.

Offset Address	Register Name	Total Reset Value
0x44	LSTHRESHOLD	0x0000_0628

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				LS_threshold											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0

Bits	Access	Name	Description
[31:12]	-	reserved	Reserved
[11:0]	RW	LS_threshold	The controller decides whether to start low-speed transmission of at most eight packets at a time before the SOF based on this register.

RHDA

RHDA is RH descriptor register A.

Offset Address	Register Name	Total Reset Value
0x48	RHDA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	poweron_to_powergood_time								reserved											no_overcurrent_protection	overcurrent_protection_mode	device_type	no_power_switching	power_switching_mode	number_downstream_ports							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:24]	RW	poweron_to_powergood_time	Wait time from the time when the port is powered on to when the power is stable. The unit is 2 ms. The driver cannot access the port of the root hub during the wait period.
[23:13]	-	reserved	Reserved
[12]	RW	no_overcurrent_protection	Whether to support reporting of the overcurrent protection event 0: supported 1: not supported
[11]	RW	overcurrent_protection_mode	Reporting mode of the overcurrent protection event 0: The overcurrent protection event is reported for all ports as a whole. 1: The overcurrent protection event for each port is reported separately.
[10]	RO	device_type	Whether the root hub is a compound device
[9]	RW	no_power_switching	Whether the port supports the switching power supply 0: supported 1: not supported, that is, constant power supply is used
[8]	RW	power_switching_mode	Port power switching mode 0: All ports use the same power supply. 1: Each port uses separate power supply.
[7:0]	RO	number_downstream_ports	Number of ports supported by the root hub

RHDB

RHDB is RH descriptor register B.

Offset Address	Register Name	Total Reset Value
0x4C	RHDB	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	port_power_control_mask																device_removable															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	port_power_control_mask	Whether the port is affected by global power supply when power_switch_mode is 1. The 16 bits indicate the status of at most 16 ports. 0: yes 1: no
[15:0]	RW	device_removable	Whether the port is removable. The 16 bits indicate the status of at most 16 ports. 0: yes 1: no

RHSTS

RHSTS is an RH status register.

Offset Address	Register Name	Total Reset Value
0x50	RHSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clear_remote_wakeup_enable	reserved													overcurrent_indicator_change	reserved	device_remote_wakeup_enable	reserved													overcurrent_indicator	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WC	clear_remote_wakeup_enable	Writing 1 clears device_remote_wakeup_enable, and writing 0 has no effect.
[30:18]	-	reserved	Reserved
[17]	WC	overcurrent_indicator_change	overcurrent_indicator change. Writing 1 clears overcurrent_indicator, and writing 0 has no effect. 0: invalid 1: valid
[16]	-	reserved	Reserved
[15]	RW	device_remote_wakeup_enable	Device standby wakeup enable 0: disabled 1: enabled. The connect_status_change interrupt is considered as the standby wakeup event.
[14:2]	-	reserved	Reserved
[1]	RW	overcurrent_indicator	Overcurrent status 0: working normally 1: overcurrent
[0]	-	reserved	Reserved

RHPORTSTS

RHPORTSTS is an RH port status register.

Offset Address	Register Name	Total Reset Value
0x54	RHPORTSTS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											port_reset_status_change	port_overcurrent_indicator_change	port_suspend_status_change	port_enable_status_change	connect_status_change	reserved						LS_device_attached	port_power_status	reserved				port_reset_status	port_overcurrent_status	port_suspend_status	port_enable_status	current_connect_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved
[20]	RW	port_reset_status_change	Port reset status change 0: unchanged 1: changed
[19]	RW	port_overcurrent_indicator_change	Port overcurrent indicator status change 0: unchanged 1: changed
[18]	RW	port_suspend_status_change	Port standby status change 0: unchanged 1: changed
[17]	RW	port_enable_status_change	Port enable status change 0: unchanged 1: changed
[16]	RW	connect_status_change	Port connection status change 0: unchanged 1: changed
[15:10]	-	reserved	Reserved
[9]	RW	LS_device_attached	Rate of the connected device 0: full-speed device 1: low-speed device

[8]	RW	port_power_status	Port power status 0: off 1: on
[7:5]	-	reserved	Reserved
[4]	RW	port_reset_status	Port reset 0: invalid 1: valid
[3]	RW	port_overcurrent_status	Port overcurrent indicator status 0: No overcurrent event occurs. 1: An overcurrent event occurs.
[2]	RW	port_suspend_status	Port standby status 0: not standby 1: standby
[1]	RW	port_enable_status	Port enable status 0: disabled 1: enabled
[0]	RW	current_connect_status	Current port connection status 0: No device is connected to the port. 1: A device is connected to the port.

12.8.5.3 USB Device Register Description

GOTGCTL

GOTGCTL is a device controller control and status register.

Offset Address	Register Name	Total Reset Value
0x0000	GOTGCTL	0x04C1_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				chirpen	multvalidbc					reserved	otgver	bsesvld	asesvld	dbnctime	conidsts	reserved				devhnpen	hstsethnpen	hnpreq	hstnegscs	bvalidovval	bvalidoven	avalidovval	avalidoven	vbvalidovval	vbvalidoven	sesreq	sesreqscs
Reset	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	RO	reserved	Reserved

[27]	RW	chirpen	Chirp on enable 0: disabled 1: enabled **NOTE** This bit is valid only when OTG_BC_SUPPORT is 1. If OTG_BC_SUPPORT is not 1, this bit is reserved.
[26:22]	RO	multvalidbc	BC ACA input Bit[26]: rid_float Bit[25]: rid_gnd Bit[24]: rid_a Bit[23]: rid_b Bit[22]: rid_c
[21]	RO	reserved	Reserved
[20]	RW	otgver	OTG version 0: OTG version 1.3 1: OTG version 2.0
[19]	RO	bsesvld	Transceiver status in device mode 0: B-session invalid 1: B-session valid
[18]	RO	asesvld	Transceiver status in host mode 0: A-session invalid 1: A-session valid
[17]	RO	dbnctime	Dejitter time 0: long dejitter time 1: short dejitter time
[16]	RO	conidsts	USB_ID status 0: The OTG works in A-device mode. 1: The OTG works in B-device mode.
[15:12]	RO	reserved	Reserved
[11]	RW	devhnpen	Device HNP enable 0: disabled 1: enabled
[10]	RW	hstsethnpen	Host HNP enable 0: disabled 1: enabled
[9]	RW	hnpreq	HNP request 0: no 1: yes

[8]	RO	hstnegscs	Host negotiation indicator 0: Host negotiation fails. 1: Host negotiation is successful.
[7]	RW	bvalidovval	Bvalid setting 0: Bvalid = 0 1: Bvalid = 1 When GOTGCTL[bvalidoven] is 1, this bit is valid.
[6]	RW	bvalidoven	Bvalid signal overwrite enable 0: Bvalid can be overwritten. 1: Bvalid cannot be overwritten.
[5]	RW	avalidovval	Avalid setting 0: Avalid = 0 1: Avalid = 1 When GOTGCTL[avalidoven] is 1, this bit is valid.
[4]	RW	avalidoven	Avalid signal overwrite enable 0: Avalid can be overwritten. 1: Avalid cannot be overwritten.
[3]	RW	vbvalidovval	vbusvalid setting 0: vbusvalid = 0 1: vbusvalid = 1 When GOTGCTL[vbvalidoven] is 1, this bit is valid.
[2]	RW	vbvalidoven	vbusvalid signal overwrite enable. 0: vbusvalid can be overwritten. 1: vbusvalid cannot be overwritten.
[1]	RW	sesreq	Session request 0: no 1: yes
[0]	RO	sesreqscs	Session request status 0: failure 1: success

GOTGINT

GOTGINT is an interrupt generation indicator register.

Offset Address	Register Name	Total Reset Value
0x0004	GOTGINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved											multvalipchng	dbncedone	adevtoutchg	hstnegdet	reserved							hstnegsucstschng	sesreqsucstschng	reserved						sesenddet	reserved	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:21]	RO	reserved	Reserved
[20]	RO	multvalipchng	An interrupt is generated when the value of at least one ACA pin changes. Setting this bit to 1 clears the interrupt. This bit is valid only when OTG_BC_SUPPORT is 1.
[19]	RO	dbncedone	An interrupt is generated when dejitter is successful after the device is connected. Setting this bit to 1 clears the interrupt. This bit is valid only when the HNP Capable or SRP Capable bit is set to 1.
[18]	RO	adevtoutchg	An interrupt is generated when waiting for the connection of device B times out. Setting this bit to 1 clears the interrupt.
[17]	RO	hstnegdet	An interrupt is generated when host negotiation is detected. Setting this bit to 1 clears the interrupt.
[16:10]	RO	reserved	Reserved
[9]	RO	hstnegsucstschng	An interrupt is generated when the host negotiation request fails or is successful. Setting this bit to 1 clears the interrupt.
[8]	RO	sesreqsucstschng	An interrupt is generated when the session request fails or is successful. Setting this bit to 1 clears the interrupt.
[7:3]	RO	reserved	Reserved
[2]	RO	sesenddet	An interrupt is generated when the session is over. Setting this bit to 1 clears the interrupt.
[1:0]	RO	reserved	Reserved

GAHBCFG

GAHBCFG is an AHB configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	GAHBCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								invdescendianness	ahbsingle	notialldmawrit	remmemsupp	reserved												nptxfemplvl	reserved	dmaen	hbstlen				glblintrmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24]	RW	invdescendianness	Inverse of the descriptor bit sequence 0: The descriptor byte sequence is consistent with the AHB master byte sequence. 1: When the AHB master byte sequence is big endian, the descriptor byte sequence is little endian. When the AHB master byte sequence is little endian, the descriptor byte sequence is big endian.
[23]	RW	ahbsingle	Bus single burst transfer for remaining data of DMA transfer 0: The remaining data is transmitted based on the INCR burst size. 1: The remaining data is transmitted based on the single burst size.
[22]	RW	notialldmawrit	System DMA done function enable for DMA write operations of all channels. It is valid only when GAHBCFG[RemMemSupp] is 1. 0: disabled 1: enabled
[21]	RW	remmemsupp	External memory access mode 0: not supported 1: supported. The device controller completes a data transfer and starts the next operation only after the sys_dma_done signal is valid.
[20:8]	RO	reserved	Reserved
[7]	RW	nptxfemplvl	Empty status level of the non-periodic TX FIFO 0: half empty. 1: empty.
[6]	RO	reserved	Reserved

[5]	RW	dmaen	DMA mode enable 0: The device controller works in slave mode. 1: The device controller works in DMA mode.
[4:1]	RW	hbstlen	Burst length/type for both the external and internal DMA modes In external DMA mode: 0x0: 1 word 0x1: 4 words 0x2: 8 words 0x3: 16 words 0x4: 32 words 0x5: 64 words 0x6: 128 words 0x7: 256 words Other values: reserved In internal DMA mode: 0x0: Single 0x1: INCR 0x3: INCR4 0x5: INCR8 0x7: INCR16 Other values: reserved
[0]	RW	glblintrmsk	Global interrupt mask 0: masked 1: not masked

GUSBCFG

GUSBCFG is a USB configuration register.

Offset Address	Register Name	Total Reset Value
0x000C	GUSBCFG	0x0000_1400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	corrupttxpkt	forcedevmode	forcehstmode	txenddelay	reserved											otgi2csel	phylpwrclksel	reserved	usbtrdtim				hnpcap	srpcap	reserved			fsintf	ulpi_utmi_sel	phyif	toutcal			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	WO	corrupttxpkt	Unexpected TX packet This bit is for debugging only and is always set to 0.
[30]	RW	forcedevmode	Forcible device mode 0: normal mode 1: forcible device mode
[29]	RW	forcehstmode	Forcible host mode 0: normal mode 1: forcible host mode
[28]	RW	txenddelay	TxEndDelay enable during standby wakeup (so that the opmode signal complies with the UTMI+ protocol 1.05) 0: disabled 1: enabled
[27:17]	RO	reserved	Reserved
[16]	RW	otgi2csel	UTMI or I^2C interface select 0: UTMI USB 1.1 full-speed interface 1: I^2C interface **NOTE** This bit is valid only when OTG_I2C_INTERFACE is 2. Reading this bit returns 0.
[15]	RW	phylpwrclksel	PHY low-power clock select 0: internal 480 MHz PLL clock 1: external 48 MHz clock
[14]	RO	reserved	Reserved

[13:10]	RW	usbtrdtim	USB turnaround time 0x5: This field is set to this value when the MAC interface is a 16-bit UTMI+ interface. 0x9: This field is set to this value when the MAC interface is an 8-bit UTMI+ interface. Other values: reserved
[9]	RW	hnpcap	HNP enable 0: disabled 1: enabled
[8]	RW	srpcap	SRP enable 0: disabled 1: enabled
[7:6]	RO	reserved	Reserved
[5]	RW	fsintf	Full-speed serial interface select 0: 6-pin unidirectional full-speed serial interface 1: 3-pin bidirectional full-speed serial interface
[4]	RW	ulpi_utmi_sel	Type of the interface between the controller and the PHY 0: UTMI+ interface 1: ULPI interface
[3]	RW	phyif	PHY interface bit width 0: 8 bits 1: 16 bits
[2:0]	RW	toutcal	HS/FS timeout (caused by the PHY) calibration High-speed operations: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times

GRSTCTL

GRSTCTL is a hardware reset register.

Offset Address	Register Name	Total Reset Value
0x0010	GRSTCTL	0x8000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	ahbidle	dmareq	reserved	txfnum	txfflsh	rxfflsh	intknqflsh	reserved	csftrst
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	ahbidle	Whether the AHB master state machine is idle 0: no 1: yes
[30]	RO	dmareq	DMA request signal status indicator 0: There is no DMA request. 1: The DMA request is being processed.
[29:11]	RO	reserved	Reserved
[10:6]	RW	txfnum	TX FIFO ID. 0x0: In shared FIFO mode, non-periodic TX FIFO 0 is flushed. In dedicated FIFO mode, TX FIFO 0 is flushed. 0x1: In shared FIFO mode, periodic TX FIFO 1 is flushed. In dedicated FIFO mode, TX FIFO 1 is flushed. 0x2: In shared FIFO mode, periodic TX FIFO 2 is flushed. In dedicated FIFO mode, TX FIFO 2 is flushed. 0xF: In shared FIFO mode, periodic TX FIFO 15 is flushed. In dedicated FIFO mode, TX FIFO 15 is flushed. 0x10: All TX FIFOs are flushed.
[5]	R_WS_SC	txfflsh	Flush of a single or all TX FIFOs. The flush operation is completed in eight 60 MHz clock cycles. Note that FIFOs cannot be flushed during transfer. 0: invalid 1: valid
[4]	RO	rxfflsh	Flush of all RX FIFOs. The flush operation is completed in eight 60 MHz clock cycles. Note that FIFOs cannot be flushed during transfer. 0: invalid 1: valid
[3]	R_WS_SC	intknqflsh	In token sequence learning queue flush This bit is valid only when OTG_EN_DED_TX_FIFO is 0. 0: invalid 1: valid
[2:1]	RO	reserved	Reserved
[0]	RW	csftrst	Soft reset on the device controller 0: not reset 1: reset

GINTSTS

GINTSTS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	GINTSTS	0x0800_0080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupint	sessreqint	reserved		lpm_int	reserved			resetdet	fetsusp	incomplpincompisoout	incompisoin	oepint	iepint	epmis	rstrdoneint	eopf	isooutdrop	enumdone	usbrst	usbsusp	erlysusp	reserved		goutnakeff	ginnakeff	nptxfemp	rxflvl	sof	reserved	modemis	curmod
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	wkupint	Wakeup interrupt. Setting this bit to 1 clears the interrupt. 0: invalid 1: valid
[30]	RWSC	sessreqint	Session request interrupt 0: invalid 1: valid
[29:28]	RO	reserved	Reserved
[27]	RWSC	lpm_int	LPM transfer interrupt 0: invalid 1: valid
[26:24]	-	reserved	Reserved
[23]	RWSC	resetdet	Reset detection in standby mode interrupt 0: invalid 1: valid
[22]	RWSC	fetsusp	Data fetch operation suspending interrupt 0: invalid 1: valid
[21]	RWSC	incomplpincompisoout	Real-time transfer incomplete interrupt, indicating that at lease one real-time OUT endpoint transfer is incomplete. 0: invalid 1: valid

[20]	RWSC	incompisoin	Real-time transfer incomplete interrupt, indicating that at lease one real-time IN endpoint transfer is incomplete. 0: invalid 1: valid
[19]	RO	oepint	OUT endpoint interrupt suspending 0: invalid 1: valid
[18]	RO	iepint	IN endpoint interrupt suspending 0: invalid 1: valid
[17]	RO	epmis	Endpoint mismatch interrupt 0: invalid 1: valid
[16]	RWSC	rstrdoneint	Status resume completion interrupt after low-power standby 0: invalid 1: valid
[15]	RWSC	eopf	Periodic transfer time limit reach interrupt within the current micro-frame duration 0: invalid 1: valid
[14]	RWSC	isooutdrop	Real-time OUT packet discard interrupt 0: invalid 1: valid
[13]	RWSC	enumdone	Enumeration completion interrupt 0: invalid 1: valid
[12]	RWSC	usbrst	USB device reset interrupt 0: invalid 1: valid
[11]	RWSC	usbsusp	USB device standby interrupt 0: invalid 1: valid
[10]	RWSC	erlysusp	Pre-standby interrupt. This bit is set to 1 when SE0 that lasts for 3 ms is detected on the bus. 0: invalid 1: valid
[9:8]	RO	reserved	Reserved

[7]	RO	goutnakeff	Global OUT NAK valid interrupt 0: invalid 1: valid
[6]	RO	ginnakeff	Global IN non-periodic NAK valid interrupt 0: invalid 1: valid
[5]	RO	nptxfemp	Non-periodic TX FIFO empty interrupt 0: invalid 1: valid
[4]	RO	rxflvl	RX FIFO non-empty interrupt 0: invalid 1: valid
[3]	RWSC	sof	SOF token interrupt 0: invalid 1: valid
[2]	RO	reserved	Reserved
[1]	RWSC	modemis	Mode mismatch interrupt 0: invalid 1: valid
[0]	RO	curmod	Current operating mode 0: device mode 1: host mode

GINTMSK

GINTMSK is a interrupt mask register.

Offset Address	Register Name	Total Reset Value
0x0018	GINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wkupintmsk	sessreqintmsk	reserved		lpm_intmsk	reserved			resetdetmsk	fetsuspmsk	incomplpmskincompisooutmsk	incompisoinmsk	oepintmsk	iepintmsk	epmismsk	rstrdoneintmsk	eopfmsk	isooutdropmsk	enumdonemsk	usbrstmsk	usbsuspmsk	erlysuspmsk	reserved		goutnakeffmsk	ginnakeffmsk	nptxfempmsk	rxflvlmsk	sofmsk	otgintmsk	modemismsk	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	wkupintmsk	Wakeup interrupt mask 0: invalid 1: valid
[30]	RW	sessreqintmsk	Session request interrupt mask 0: invalid 1: valid
[29:28]	-	reserved	Reserved
[27]	RW	lpm_intmsk	LPM transaction interrupt mask 0: invalid 1: valid
[26:24]	RO	reserved	Reserved
[23]	RW	resetdetmsk	Standby mode reset interrupt mask 0: invalid 1: valid
[22]	RW	fetsuspmsk	Data fetch suspending interrupt mask 0: invalid 1: valid
[21]	RW	incomplpmskincompisooutmsk	Incomplete real-time OUT transfer interrupt mask 0: invalid 1: valid
[20]	RW	incompisoinmsk	Incomplete real-time IN transfer interrupt mask 0: invalid 1: valid

[19]	RW	oepintmsk	OUT endpoint interrupt suspending mask 0: invalid 1: valid
[18]	RW	iepintmsk	IN endpoint interrupt suspending mask 0: invalid 1: valid
[17]	RW	epmismsk	Endpoint mismatch interrupt mask 0: invalid 1: valid
[16]	RW	rstrdoneintmsk	Mask of the status resume completion interrupt after low-power standby 0: invalid 1: valid
[15]	RW	eopfmsk	Mask of the periodic transfer time limit reach interrupt within the current micro-frame duration 0: invalid 1: valid
[14]	RW	isooutdropmsk	Real-time OUT packet discard interrupt mask 0: invalid 1: valid
[13]	RW	enumdonemsk	Enumeration completion interrupt mask 0: invalid 1: valid
[12]	RW	usbrstmsk	USB device reset interrupt mask 0: invalid 1: valid
[11]	RW	usbsuspmsk	USB device standby interrupt mask 0: invalid 1: valid
[10]	RW	erlysuspmsk	Pre-standby interrupt mask 0: invalid 1: valid
[9:8]	-	reserved	Reserved
[7]	RW	goutnakeffmsk	Global OUT NAK valid interrupt mask 0: invalid 1: valid

[6]	RW	ginnakeffmsk	Global IN non-periodic NAK valid interrupt mask 0: invalid 1: valid
[5]	RW	nptxfempmsk	Non-periodic TX FIFO empty interrupt mask 0: invalid 1: valid
[4]	RW	rxflvlmsk	RX FIFO non-empty interrupt mask 0: invalid 1: valid
[3]	RW	sofmsk	SOF token interrupt mask 0: invalid 1: valid
[2]	-	reserved	reserved
[1]	RW	modemismsk	Operation mode mismatch interrupt mask 0: invalid 1: valid
[0]	-	reserved	Reserved

GRXSTSP

GRXSTSP is an RX status register.

Offset Address	Register Name	Total Reset Value
0x0020	GRXSTSP	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved		fn	pktsts	dpid	bcnt		chnum_device mode
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:25]	RO	reserved	Reserved
[24:21]	RO	fn	ID of the micro-frame to which the current received packet belongs.

[20:17]	RO	pktsts	RX packet status 0x1: global OUT NAK (interrupt triggered) 0x2: received OUT data packet 0x3: OUT transfer completion (interrupt triggered) 0x5: SETUP transfer completion (interrupt triggered) 0x7: received SETUP data packet (interrupt triggered) Other values: reserved
[16:15]	RO	dpid	PID of the received OUT data packet. 00: DATA0 10: DATA1 01: DATA2 11: MDATA
[14:4]	RO	bcnt	Length of the received data packet, in byte
[3:0]	RO	chnum_devicemode	Endpoint ID of the current received packet

GRXFSIZ

GRXFSIZ is an RX FIFO depth register.

Offset Address	Register Name	Total Reset Value
0x0024	GRXFSIZ	0x0000_0211

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rxfdep															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	R/RW	rxfdep	RX FIFO depth. The unit is a 32-bit word. Its value range is 16−32768.

GNPTXFSIZ

GNPTXFSIZ is a non-periodic TX FIFO depth register.

Offset Address	Register Name	Total Reset Value
0x0028	GNPTXFSIZ	0x0100_0211

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ineptxf0dep																ineptxf0staddr															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	ineptxf0dep	Depth of IN endpoint TX FIFO 0. Its value range is 16−32768.
[15:0]	RW	ineptxf0staddr	Start address for the TX RAM of IN endpoint FIFO 0

GNPTXSTS

GNPTXSTS is a non-periodic TX FIFO and queue status register.

Offset Address	Register Name	Total Reset Value
0x002C	GNPTXSTS	0x0008_0100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved	nptxqtop							nptxqspcavail								nptxfspcavail															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:24]	RO	nptxqtop	Non-periodic TX request queue top Bit[30:27]: endpoint ID bit[26:25]: 00: IN/OUT token 01: zero-length transmit packet 10: PING/CSPLIT token 11: channel stop command Bit[24]: stop (the selected channel or endpoint is used for attempting)
[23:16]	RO	nptxqspcavail	Available space for the non-periodic TX request queue 0x0: The queue is full. 0x1: One address is available. 0x2: Two addresses are available. 0xn: *n* addresses ($0 \le n \le 8$) are available. Other values: reserved

[15:0]	RO	nptxfspcavail	Total available space for the non-periodic TX request queue 0x0: The TX FIFO is full. 0x1: One word is available. 0x2: Two words are available. 0xn: *n* words ($0 \leq n \leq 32768$) are available. 0x8000: 32768 words are available. Other values: reserved

GSNPSID

GSNPSID is a Synopsys ID query register.

Offset Address	Register Name	Total Reset Value
0x0040	GSNPSID	0x4F54_300A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	synopsysid																															
Reset	0	1	0	0	1	1	1	1	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:0]	RW	synopsysid	ID of the current DWC_otg version

GHWCFG1

GHWCFG1 is hardware configuration register 1.

Offset Address	Register Name	Total Reset Value
0x0044	GHWCFG1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epdir																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	epdir	Every two bits form a group, indicating the direction of an endpoint. bit[31:30]: direction of endpoint 15 bit[29:28]: direction of endpoint 14 ... bit[3:2]: direction of endpoint 1 bit[1:0]: direction of endpoint 0 (always bidirectional) 00: bidirectional (IN and OUT) endpoint

			01: IN endpoint 10: OUT endpoint 11: reserved

GHWCFG2

GHWCFG2 is hardware configuration register 2.

Offset Address	Register Name	Total Reset Value
0x0048	GHWCFG2	0x2284_D854

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				tknqdepth				reserved				nptxqdepth				reserved		multiprocintrpt		dynfifosizing		periosupport		reserved				numdeveps				fsphytype				hsphytype				singpnt		otgarch		otgmode			
Reset	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	1	1	0	0	0	0	1	0	1	0	1	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:26]	RO	tknqdepth	Depth of the IN token sequence learning queue in device mode The value range is 0−30.
[25:24]	-	reserved	Reserved
[23:22]	RO	nptxqdepth	Depth of the non-periodic request queue 00: 2 01: 4 10: 8 Other values: reserved
[21]	RO	reserved	Reserved
[20]	RO	multiprocintrpt	Multi-processor interrupt enable 0: disabled 1: enabled
[19]	RO	dynfifosizing	FIFO size dynamic configuration enable 0: disabled 1: enabled
[18]	RO	periosupport	Periodic OUT channel support in host mode 0: not supported 1: supported

[17:14]	RO	reserved	Reserved
[13:10]	RO	numdeveps	Number of device endpoints (excluding endpoint 0) The value range is 1−15.
[9:8]	RO	fsphytype	Type of the full-speed PHY interface 00: The full-speed interface is not supported. 01: The dedicated full-speed interface is supported. 10: FS pins share with UTMI+ pins. 11: FS pins share with ULPI pins.
[7:6]	RO	hsphytype	Type of the high-speed PHY interface 00: high-speed interface not supported 01: UTMI+ 10: ULPI 11: UTMI+ and ULPI
[5]	RO	singpnt	Application scenario 0: multi-point application (hub and split supported) 1: single-point application (hub and split not supported)
[4:3]	RO	otgarch	OTG architecture 00: slave only 01: external DMA 10: internal DMA Other values: reserved
[2:0]	RO	otgmode	Operating mode 011: SRP device 100: non-OTG device Other values: reserved

GHWCFG3

GHWCFG3 is hardware configuration register 3.

Offset Address	Register Name	Total Reset Value
0x004C	GHWCFG3	0x0501_51E8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dfifodepth																lpmmode	bcsupport	hsicmode	adpsupport	rsttype	reserved			otgen	pktsizewidth			xfersizewidth			
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1	1	0	1	0	0	0

Bits	Access	Name	Description
[31:16]	RO	dfifodepth	DFIFO depth. The value range is 32–32768.
[15]	RO	lpmmode	LPM mode 0: not supported 1: supported
[14]	RO	bcsupport	Whether the controller supports the battery charger 0: not supported 1: supported
[13]	RO	hsicmode	HSIC mode 0: not supported 1: supported
[12]	RO	adpsupport	ADP logic support 0: not supported 1: supported
[11]	RO	rsttype	Reset mode select 0: async reset 1: sync reset
[10:8]	RO	reserved	Reserved
[7]	RO	otgen	OTG function enable 0: disabled 1: enabled

[6:4]	RO	pktsizewidth	Bit width of the packet length counter 000: 4 bits 001: 5 bits 010: 6 bits 011: 7 bits 100: 8 bits 101: 9 bits 110: 10 bits Other values: reserved
[3:0]	RO	xfersizewidth	Bit width of the packet TX counter 0x0: 11 bits 0x1: 12 bits 0x8: 19 bits Other values: reserved

GHWCFG4

GHWCFG4 is user hardware configuration register 4.

Offset Address	Register Name	Total Reset Value
0x0050	GHWCFG4	0x4600_8020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	descdma	descdmaen	ineps				dedfifomode	sessendfltr	bvalidfltr	avalidfltr	vbusvalidfltr	iddgfltr	numctleps				phydatawidth			reserved					extndedhibernation	hibernation	ahbfreq	partialpwrdn	numdevperioeps			
Reset	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	descdma	Scatter/Gather DMA dynamic configuration 0: no dynamic configuration 1: dynamic configuration
[30]	RO	descdmaen	Scatter/Gather DMA enable 0: disabled 1: enabled

[29:26]	RO	ineps	Number of IN endpoints in device mode (including the control endpoint) 0: one IN endpoint 1: two IN endpoints ... 15: 16 IN endpoints
[25]	RO	dedfifomode	Enable of the dedicated TX FIFO for the IN endpoint 0: disabled 1: enabled
[24]	RO	sessendfltr	session_end filter enable 0: disabled 1: enabled
[23]	RO	bvalidfltr	b_valid filter enable 0: disabled 1: enabled
[22]	RO	avalidfltr	a_valid filter enable 0: disabled 1: enabled
[21]	RO	vbusvalidfltr	VBUS valid filter enable 0: disabled 1: enabled
[20]	RO	iddgfltr	IDDIG filter enable 0: disabled 1: enabled
[19:16]	RO	numctleps	Number of controlled endpoints excluding endpoint 0 The value range is 0−15.
[15:14]	RO	phydatawidth	Data width of the UTMI+ PHY/ULPI-to-internal UTMI+ wrapper 00: 8 bits 01: 16 bits 10: 8 bit or 16 bits, which is configured by using software Other values: reserved
[13:8]	-	reserved	Reserved
[7]	RO	extndedhibernation	Extended hibernation enable 0: disabled 1: enabled
[6]	RO	hibernation	Hibernation enable 0: disabled 1: enabled

[5]	RO	ahbfreq	Whether the minimum AHB frequency is lower than 60 MHz 0: no 1: yes
[4]	RO	partialpwrdn	Partial power down enable 0: disabled 1: enabled
[3:0]	RO	numdevperioeps	Number of real-time IN endpoints The value range is 0−15.

GDFIFOCFG

GDFIFOCFG is a DFIFO software configuration register.

Offset Address	Register Name	Total Reset Value
0x005C	GDFIFOCFG	0x0501_0511

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epinfobaseaddr																gdfifocfg															
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	epinfobaseaddr	Start address for the EP info controller
[15:0]	RW	gdfifocfg	DFIFO depth, which is dynamically configured

DIEPTXFN

DIEPTXFN is a device IN endpoint TX FIFO depth register.

NOTE

This register is valid only in dedicated FIFO mode.

Offset Address	Register Name	Total Reset Value
0x0104 + 0x0004 x (FIFO_num-1)	DIEPTXFN	0x0300_0251

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	inepntxfdep																inepntxfstaddr															
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1

Bits	Access	Name	Description
[31:16]	RW	inepntxfdep	Depth of the IN endpoint TX FIFO The value range is 16−32768.
[15:0]	RW	inepntxfstaddr	Start address for the IN endpoint FIFO*n* TX RAM

DCFG

DCFG is a device configuration register.

Offset Address	Register Name	Total Reset Value
0x0800	DCFG	0x8100_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	resvalid						perschintvl		descdma	epmiscnt						reserved			endevoutnak	perfrint	devaddr							ena32khzsusp	nzstsouthshk	devspd			
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RW	resvalid	Time when wakeup is detected valid in standby mode
[25:24]	RW	perschintvl	Time percentage for real-time linked list scheduling 00: 25% of (micro) frames 01: 50% of (micro) frames 10: 75% of (micro) frames 11: reserved
[23]	RW	descdma	Scatter/Gather DMA enable 0: disabled 1: enabled
[22:18]	RW	epmiscnt	IN endpoint mismatch statistics
[17:14]	RO	reserved	Reserved
[13]	RW	endevoutnak	NAK TX enable after OUT transfer is complete in Desc DMA mode 0: disabled 1: enabled
[12:11]	RW	perfrint	Real-time frame interval 1 00: 80% of the (micro) frame interval 01: 85% of the (micro) frame interval 10: 90% of the (micro) frame interval 11: 95% of the (micro) frame interval
[10:4]	RW	devaddr	Address allocated to the device during enumeration
[3]	RW	ena32khzsusp	32 kHz suspend mode enable 0: disabled 1: enabled

[2]	RW	nzstsouthshk	Non-zero-length status OUT handshake enable 0: disabled 1: enabled
[1:0]	RW	devspd	Device working mode 00: high speed 01: full speed (30 MHz or 60 MHz USB 2.0 PHY clock) 10: low speed 11: full speed (48 MHz USB 1.1 transceiver clock)

DCTL

DCTL is a device control register.

Offset Address	Register Name	Total Reset Value
0x0804	DCTL	0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														encontonbna	nakonbble	ignrfrmnum	gmc		reserved	pwronprgdone	cgoutnak	sgoutnak	cgnpinnak	sgnpinnak	tstctl			goutnaksts	gnpinnaksts	sftdiscon	rmtwkupsig
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Access	Name	Description
[31:18]	-	reserved	Reserved
[17]	RW	encontonbna	Continue on BNA enable 0: disabled 1: enabled
[16]	RW	nakonbble	NAK on Babble enable. Automatic NAK is configured when Babble is received. 0: disabled 1: enabled
[15]	RW	ignrfrmnum	Frame number ignore for real-time endpoints 0: disabled 1: enabled
[14:13]	RW	gmc	Number of packets to be transferred by the current endpoint 00: invalid 01: 1 packet 10: 2 packets 11: 3 packets

[12]	-	reserved	Reserved
[11]	RW	pwronprgdone	Register configuration completion after power-down wakeup
[10]	WO	cgoutnak	Global OUT NAK clear 0: invalid 1: valid
[9]	WO	sgoutnak	Global OUT NAK 0: invalid 1: valid
[8]	WO	cgnpinnak	Global non-periodic IN NAK clear 0: invalid 1: valid
[7]	WO	sgnpinnak	Global non-periodic IN NAK configuration 0: invalid 1: valid
[6:4]	RW	tstctl	Test mode 000: test mode disabled 001: Test_J mode 010: Test_K mode 011: Test_SE0_NAK mode 100: Test_Packet mode 101: Test_Force_Enable Other values: reserved
[3]	RO	goutnaksts	Global OUT NAK status 0: Send handshake based on the FIFO status and NAK and STALL bit status. 1: Send NAK for all packets except control transfer.
[2]	RO	gnpinnaksts	Global non-periodic NAK status 0: Send NAK based on the TX FIFO status. 1: Send NAK for all non-periodic IN endpoints.
[1]	RW	sftdiscon	Soft disconnection 0: working normally 1: The controller sets phy_opmode_o to 01 and generates a disconnection event to the USB host.
[0]	RW	rmtwkupsig	Standby wakeup signal 0: invalid 1: valid

DSTS

DSTS is a device status query register.

Offset Address	Register Name	Total Reset Value
0x0808	DSTS	0x0007_FF08

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								devlnsts				soffn												reserved				errticerr		enumspd		suspsts	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0

Bits	Access	Name	Description
[31:24]	RO	reserved	Reserved
[23:22]	RO	devlnsts	Logic level of the current USB bus bit[23]: logic level of D+ bit[22]: logic level of D−
[21:8]	RO	soffn	Number of frames or micro-frames in the received SOF packets
[7:4]	-	reserved	Reserved
[3]	RO	errticerr	UTMI+ interface signal error 0: invalid 1: valid
[2:1]	RO	enumspd	Enumeration speed 00: high speed 01: full speed (30 MHz or 60 MHz PHY clock) 10: low speed. 11: full speed (48 MHz PHY clock).
[0]	RO	suspsts	Standby status. The controller enters standby mode if it detects that D+/D– has no action within a period of time. In this case, this bit is set to 1. When any action of D+/D– is detected or the driver wakes up the controller, this bit is cleared. 0: not standby 1: standby

DIEPMSK

DIEPMSK is a common interrupt mask register for IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0810	DIEPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																		nakmsk	reserved			bnainintrmsk	txfifoundrnmsk	reserved	inepnakeffmsk	intknepmismsk	intkntxfempmsk	timeoutmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:14]	-	reserved	Reserved
[13]	RW	nakmsk	NAK interrupt mask 0: masked 1: not masked
[12:10]	-	reserved	Reserved
[9]	RW	bnainintrmsk	BNA interrupt mask 0: masked 1: not masked
[8]	RW	txfifoundrnmsk	FIFO underrun interrupt mask 0: masked 1: not masked
[7]	-	reserved	Reserved
[6]	RW	inepnakeffmsk	IN endpoint NAK effective interrupt mask 0: masked 1: not masked
[5]	RW	intknepmismsk	IN token received and EP mismatch interrupt mask 0: masked 1: not masked
[4]	RW	intkntxfempmsk	IN token received when TX FIFO empty interrupt mask 0: masked 1: not masked
[3]	RW	timeoutmsk	Timeout interrupt mask 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB bus error interrupt mask 0: masked 1: not masked

[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completed interrupt mask 0: masked 1: not masked

DOEPMSK

DOEPMSK is a common interrupt mask register for OUT endpoints.

Offset Address	Register Name	Total Reset Value
0x0814	DOEPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																	nyetmsk	nakmsk	bbleerrmsk	reserved		bnaoutintrmsk	outpktermsk	reserved	back2backsetupmsk	stsphsercvdmsk	outknepdismsk	setupmsk	ahberrmsk	epdisbldmsk	xfercomplmsk
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:15]	-	reserved	Reserved
[14]	RW	nyetmsk	NYET interrupt mask 0: masked 1: not masked
[13]	RW	nakmsk	NAK interrupt mask 0: masked 1: not masked
[12]	RW	bbleerrmsk	Babble error interrupt mask 0: masked 1: not masked
[11:10]	-	reserved	Reserved
[9]	RW	bnaoutintrmsk	BNA interrupt mask 0: masked 1: not masked

[8]	RW	outpkterrmsk	OUT packet error interrupt mask 0: masked 1: not masked
[7]	-	reserved	Reserved
[6]	RW	back2backsetupmsk	Back-to-back setup packets received interrupt mask 0: masked 1: not masked
[5]	RW	stsphsercvdmsk	Status phase received interrupt mask 0: masked 1: not masked
[4]	RW	outtknepdismsk	OUT token received when endpoint disabled interrupt mask 0: masked 1: not masked
[3]	RW	setupmsk	Setup phase done interrupt mask 0: masked 1: not masked
[2]	RW	ahberrmsk	AHB bus error interrupt mask 0: masked 1: not masked
[1]	RW	epdisbldmsk	Endpoint disabled interrupt mask 0: masked 1: not masked
[0]	RW	xfercomplmsk	Transfer completed interrupt mask 0: masked 1: not masked

DAINT

DAINT is an interrupt register for all device endpoints.

Offset Address	Register Name	Total Reset Value
0x0818	DAINT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	outepint																inepint															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	outepint	OUT endpoint interrupt

			Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RO	inepint	IN endpoint interrupt Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DAINTMSK

DAINTMSK is an interrupt mask register for all endpoints.

Offset Address	Register Name	Total Reset Value
0x081C	DAINTMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	outepmsk																inepmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RW	outepmsk	OUT endpoint interrupt mask Bit 16: OUT endpoint 0 ... Bit 31: OUT endpoint 15
[15:0]	RW	inepmsk	IN endpoint interrupt mask Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DTKNQR1

DTKNQR1 is IN token learning queue register 1.

Offset Address	Register Name	Total Reset Value
0x0820	DTKNQR1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																								wrapbit	reserved			intknwptr			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	eptkn	Endpoint ID of a token. Every four bits form a group to indicate the endpoint ID of a token. Bit[31:28]: endpoint ID of token 5 Bit[27:24]: endpoint ID of token 4 … Bit[15:12]: endpoint ID of token 1 Bit[11:8]: endpoint ID of token 0
[7]	RO	wrapbit	Write pointer wrap. This bit is set to 1 when the write pointer is wrapped, and it is cleared when the learning queue is cleared.
[6:5]	-	reserved	Reserved
[4:0]	RO	intknwptr	IN token queue write pointer

DTKNQR2

DTKNQR2 is IN token learning queue register 2.

Offset Address	Register Name	Total Reset Value
0x0824	DTKNQR2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Endpoint ID of a token. Every four bits form a group to indicate the endpoint ID of a token. Bit[31:28]: endpoint ID of token 13 Bit[27:24]: endpoint ID of token 12 … Bit[7:4]: endpoint ID of token 7 Bit[3:0]: endpoint ID of token 6

DTKNQR3

DTKNQR3 is IN token learning queue register 3.

Offset Address	Register Name	Total Reset Value
0x0830	DTKNQR3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Endpoint ID of a token. Every four bits form a group to indicate the endpoint ID of a token. Bit[31:28]: endpoint ID of token 21 Bit[27:24]: endpoint ID of token 20 … Bit[7:4]: endpoint ID of token 15 Bit[3:0]: endpoint ID of token 14

DTKNQR4

DTKNQR4 is IN token learning queue register 4.

Offset Address	Register Name	Total Reset Value
0x0834	DTKNQR4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eptkn																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	eptkn	Endpoint ID of a token. Every four bits form a group to indicate the endpoint ID of a token. Bit[31:28]: endpoint ID of token 29 Bit[27:24]: endpoint ID of token 28 … Bit[7:4]: endpoint ID of token 23 Bit[3:0]: endpoint ID of token 22

DVBUSDIS

DVBUSDIS is a VBUS discharge time register.

Offset Address	Register Name	Total Reset Value
0x0828	DVBUSDIS	0x0000_17D7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																dvbusdis															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	1

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	dvbusdis	VBUS discharge time. The counting clock is 60 MHz/1024.

DVBUSPULSE

DVBUSPULSE is a VBUS pulsing time register.

Offset Address	Register Name	Total Reset Value
0x082C	DVBUSPULSE	0x0000_05B8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																				dvbuspulse											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	0

Bits	Access	Name	Description
[31:12]	RO	reserved	Reserved
[11:0]	RO	dvbuspulse	VBUS pulsing time. The counting clock is 60 MHz/1024.

DTHRCTL

DTHRCTL is a threshold control register.

Offset Address	Register Name	Total Reset Value
0x0830	DTHRCTL	0x0C10_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				arbprken	reserved			rxthrlen							rxthren	reserved				ahbthrratio				txthrlen						isothren	nonisothren
Reset	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:28]	-	reserved	Reserved
[27]	RW	arbprken	Arbitrator parking enable, FIFO threshold for control IN endpoints in internal DMA mode to prevent underrun. 0: disabled 1: enabled
[26]	-	reserved	Reserved
[25:17]	RW	rxthrlen	RX FIFO threshold
[16]	RW	rxthren	RX threshold enable 0: disabled 1: enabled
[15:13]	-	reserved	Reserved
[12:11]	RW	ahbthrratio	AHB threshold ratio, which is the ratio of the AHB threshold to the MAC threshold in the TX channel 00: AHB threshold = MAC threshold 01: AHB threshold = MAC threshold/2 10: AHB threshold = MAC threshold/4 11: AHB threshold = MAC threshold/8
[10:2]	RW	txthrlen	TX FIFO threshold
[1]	RW	isothren	ISO IN endpoint threshold enable 0: disabled 1: enabled
[0]	RW	nonisothren	Non-ISO IN endpoint threshold enable 0: disabled 1: enabled

DIEPEMPMSK

DIEPEMPMSK is a FIFO empty interrupt mask register for IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0834	DIEPEMPMSK	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ineptxfempmsk															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RW	ineptxfempmsk	IN endpoint TX FIFO empty interrupt mask. Each bit corresponds to an endpoint. Bit 0: IN endpoint 0 ... Bit 15: IN endpoint 15

DIEPCTL0

DIEPCTL0 is a control register for control IN endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0900	DIEPCTL0	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epena	epdis	reserved		snak	cnak	txfnum				stall	reserved	eptype		naksts	reserved	usbactep	nextep			reserved								mps			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enable. This bit is cleared when the transfer is complete or the endpoint is disabled. 0: invalid 1: valid
[30]	RWSC	epdis	Endpoint disable 0: invalid 1: valid
[29:28]	-	reserved	Reserved
[27]	WO	snak	NAK configuration

[26]	WO	cnak	NAK clear
[25:22]	RW	txfnum	Number of TX FIFOs
[21]	RWSC	stall	Stall handshake, This bit is cleared after the endpoint receives the setup token packet.
[20]	-	reserved	Reserved
[19:18]	RO	eptype	Endpoint type. It is fixed at 0 for control endpoints.
[17]	RO	naksts	NAK status 0: non-NAK handshake TX 1: NAK handshake TX
[16]	-	reserved	Reserved
[15]	RO	usbactep	Endpoint activation. This bit is fixed at 1 for control endpoints.
[14:11]	RO	nextep	Next endpoint This field specifies the ID of the next endpoint that receives data.
[10:2]	-	reserved	Reserved
[1:0]	RW	mps	Minimum packet size 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes

DOEPCTL0

DOEPCTL0 is a control register for device control OUT endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0B00	DOEPCTL0	0x0000_8000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	epena	epdis	reserved		snak	cnak	reserved				stall	snp	eptype		naksts	reserved	usbactep	reserved											mps			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RWSC	epena	Endpoint enable. This bit is cleared after transfer is complete or the endpoint is disabled. 0: disabled 1: enabled

[30]	RO	epdis	Endpoint disable 0: enabled 1: disabled
[29:28]	-	reserved	Reserved
[27]	WO	snak	NAK configuration
[26]	WO	cnak	NAK clear
[25:22]	-	reserved	Reserved
[21]	RWSC	stall	Stall handshake. This bit is cleared after the endpoint receives the setup token packet.
[20]	RW	snp	Snooping mode. The controller does not check the packet before transmission.
[19:18]	RO	eptype	Endpoint type. It is fixed at 0 for control endpoints.
[17]	RO	naksts	NAK status 0: non-NAK handshake TX 1: NAK handshake TX
[16]	-	reserved	Reserved
[15]	RO	usbactep	Endpoint activation. This bit is fixed at 1 for control endpoints.
[14:2]	RO	reserved	Reserved
[1:0]	RW	mps	Minimum packet size 00: 64 bytes 01: 32 bytes 10: 16 bytes 11: 8 bytes

DIEPINTn

DIEPINTn is an interrupt register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0908 + (0x0020 x *n*) (*n* = 0–1)	DIEPINTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																StupPktRcvd	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	reserved	BNAIntr	TxfifoUndrn	TxFEmp	INEPNakEff	INTknEPMis	INTknTXFEmp	TimeOUT	AHBErr	EPDisbld	XferCompl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15]	RWSC	StupPktRcvd	Whether setup packets are received 0: invalid 1: valid
[14]	RWSC	NYETIntrpt	NYET interrupt, which is generated when the non-real-time OUT endpoint transmits the NYET packet 0: invalid 1: valid
[13]	RWSC	NAKIntrpt	NAK interrupt, which is generated when the controller transmits the NAK packet 0: invalid 1: valid
[12]	RWSC	BbleErrIntrpt	Babble error interrupt, which is generated when the endpoint receives the babble packet 0: invalid 1: valid
[11]	RWSC	PktDrpSts	Packet discard status interrupt, which is generated when the real-time OUT packet is discarded 0: invalid 1: valid
[10]	-	reserved	Reserved
[9]	RWSC	BNAIntr	Buffer not active interrupt, which is generated when the obtained description is not ready 0: invalid 1: valid

[8]	RWSC	TxfifoUndrn	FIFO underrun interrupt, which is generated when underrun occurs in the FIFO of the IN endpoint 0: invalid 1: valid
[7]	RO	TxFEmp	IN endpoint FIFO empty interrupt 0: invalid 1: valid
[6]	RWSC	INEPNakEff	IN endpoint NAK valid interrupt 0: invalid 1: valid
[5]	RWSC	INTknEPMis	IN endpoint token packet and endpoint mismatch interrupt 0: invalid 1: valid
[4]	RWSC	INTknTXFEmp	Interrupt indicating that the IN endpoint receives IN token packets when the TX FIFO is empty 0: invalid 1: valid
[3]	RWSC	TimeOUT	Latest IN transfer timeout interrupt of the IN endpoint 0: invalid 1: valid
[2]	RWSC	AHBErr	AHB bus error interrupt 0: invalid 1: valid
[1]	RWSC	EPDisbld	Endpoint disable interrupt 0: invalid 1: valid
[0]	RWSC	XferCompl	Transfer completion interrupt 0: invalid 1: valid

DOEPINTn

DOEPINTn is an interrupt register for OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B08 + (0x0020 x *n*) (*n* = 0–1)	DOEPINTn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																StupPktRcvd	NYETIntrpt	NAKIntrpt	BbleErrIntrpt	PktDrpSts	reserved	BNAIntr	OutPktErr	TxFEmp	Back2BackSETup	StsPhseRcvd	OUTTknEPdis	SetUp	AHBErr	EPDisbld	XferCompl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15]	RWSC	StupPktRcvd	Setup packet reception interrupt 0: invalid 1: valid
[14]	RWSC	NYETIntrpt	NYET interrupt, which is generated when the non-real-time OUT endpoint transmits the NYET packet 0: invalid 1: valid
[13]	RWSC	NAKIntrpt	NAK interrupt, which is generated when the controller transmits the NAK packet 0: invalid 1: valid
[12]	RWSC	BbleErrIntrpt	Babble error interrupt, which is generated when the endpoint receives the babble packet 0: invalid 1: valid
[11]	RWSC	PktDrpSts	Packet discard status interrupt, which is generated when the real-time OUT packet is discarded 0: invalid 1: valid
[10]	-	reserved	Reserved
[9]	RWSC	BNAIntr	BNA interrupt, which is generated when the obtained description is not ready 0: invalid 1: valid

[8]	RWSC	OutPktErr	FIFO overflow interrupt, which is generated when overflow occurs in the OUT endpoint 0: invalid 1: valid
[7]	RO	TxFEmp	IN endpoint FIFO empty interrupt 0: invalid 1: valid
[6]	RWSC	Back2BackSETup	OUT endpoint receiving back-to-back setup packet interrupt 0: invalid 1: valid
[5]	RWSC	StsPhseRcvd	All data transferred to the system memory by the OUT endpoint interrupt 0: invalid 1: valid
[4]	RWSC	OUTTknEPdis	OUT token packet received when OUT endpoint disabled interrupt 0: invalid 1: valid
[3]	RWSC	SetUp	Setup transfer completion interrupt 0: invalid 1: valid
[2]	RWSC	AHBErr	AHB bus error interrupt 0: invalid 1: valid
[1]	RWSC	EPDisbld	Endpoint disable interrupt 0: invalid 1: valid
[0]	RWSC	XferCompl	Transfer completion interrupt 0: invalid 1: valid

DIEPTSIZ0

DIEPTSIZ0 is a transfer size register for device IN endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0910	DIEPTSIZ0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved			PktCnt	reserved			XferSize
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:21]	-	reserved	Reserved
[20:19]	RW	PktCnt	Number of USB packets to be transferred for endpoint 0. The value decreases by 1 each time a packet is read from the TX FIFO.
[18:7]	RO	reserved	Reserved
[6:0]	RW	XferSize	Size of transferred data. The value decreases by 1 each time a packet is written to the TX FIFO from the system memory.

DOEPTSIZ0

DOEPTSIZ0 is a transfer size register for device OUT endpoint 0.

Offset Address	Register Name	Total Reset Value
0x0B10	DOEPTSIZ0	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved	SUPCnt	PktCnt		XferSize			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31]	RO	reserved	Reserved
[30:29]	RW	SUPCnt	Number of back-to-back setup packets that can be received by the endpoint 00: 0 packet 01: 1 packet 10: 2 packets 11: 3 packets Other values: reserved
[28:19]	RW	PktCnt	Number of USB packets to be transferred for endpoint *n*. The value decreases by 1 each time a packet is read from the TX FIFO.

[18:0]	RW	XferSize	Size of transferred data. The value decreases by 1 each time a packet is read from the RX FIFO to the system memory.

DIEPTSIZn

DIEPTSIZn is a transfer size register for device IN endpoint *n*.

Offset Address: 0x0910 + (0x0020 x *n*) (*n* = 0–1)

Register Name: DIEPTSIZn

Total Reset Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		mc		PktCnt												XferSize															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:29]	RW	mc	Packet count. For real-time IN endpoints, this register specifies the number of packets that must be transferred by each micro-frame; for non-real-time IN endpoints, it specifies the number of packets for instruction fetch of the controller. 00: 0 packet 01: 1 packet 10: 2 packets 11: 3 packets Other values: reserved
[28:19]	RW	PktCnt	Number of USB packets to be transferred for endpoint *n*. The value decreases by 1 each time a packet is read from the TX FIFO.
[18:0]	RW	XferSize	Size of transferred data. The value decreases by 1 each time a packet is written to the TX FIFO from the system memory.

DOEPTSIZn

DOEPTSIZn is a transfer size register for device OUT endpoint *n*.

Offset Address: 0x0B10 + (0x0020 x *n*) (*n* = 0–1)

Register Name: DOEPTSIZn

Total Reset Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved		rxdpid_supcnt		PktCnt												XferSize															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	-	reserved	Reserved
[30:29]	RW	rxdpid_supcnt	Received data PID for real-time OUT endpoints 00: DATA0 01: DATA 2 10: DATA 1 11: MDATA Number of back-to-back setup packets that can be received by the endpoint for control OUT endpoints 01: 1 packet 10: 2 packets 11: 3 packets Other values: reserved
[28:19]	RW	PktCnt	Number of USB packets to be transferred for endpoint *n*. The value decreases by 1 each time a packet is read from the TX FIFO.
[18:0]	RW	XferSize	Size of transferred data. The value decreases by 1 each time a packet is read from the RX FIFO to the system memory.

DIEPDMAN

DIEPDMAN is a DMA address register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0914 + (0x0020 x *n*) (*n* = 0–1)	DIEPDMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	Start address for storing or reading endpoint data in the system memory for IN endpoint *n*

DOEPDMAN

DOEPDMAN is a DMA address register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B14 + (0x0020 x n) (*n* = 0–1)	DOEPDMAN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dmaaddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dmaaddr	Start address for storing or reading endpoint data in the system memory for OUT endpoint *n*

DIEPDMABN

DIEPDMABN is a DMA buffer address register for device IN endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x091C + (0x0020 x *n*) (*n* = 0–1)	DIEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	Current DMA buffer address

DOEPDMABN

DOEPDMABN is a DMA buffer address register for device OUT endpoint *n*.

Offset Address	Register Name	Total Reset Value
0x0B1C + (0x0020 x *n*) (*n* = 0–1)	DOEPDMABN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMABufferAddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	DMABufferAddr	Current DMA buffer address

DTXFSTS0

DTXFSTS0 is an IN endpoint 0 TX FIFO status register.

Offset Address	Register Name	Total Reset Value
0x0918	DTXFSTS0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																INEPTxFSpcAvail															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	-	reserved	Reserved
[15:0]	RO	INEPTxFSpcAvail	Remaining space of the IN endpoint TX FIFO (in the unit of word) 0x0: 0 word, that is, the TX FIFO is full 0x1: one word 0x2: two words 0xn: *n* words (0 ≤ *n* ≤ 32,768) 0x8000: 32,768 words Other values: reserved

DTXFSTSn

DTXFSTSn is a TX FIFO status register for IN endpoints.

Offset Address	Register Name	Total Reset Value
0x0918 + (0x0020 x *n*) (*n* = 0–1)	DTXFSTSn	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																INEPTxFSpcAvail																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	INEPTxFSpcAvail	Remaining space of the IN endpoint TX FIFO (in the unit of word) 0x0: 0 word, that is, the TX FIFO is full 0x1: one word 0x2: two words 0xn: *n* words ($0 \le n \le 32,768$) 0x8000: 32,768 words Other values: reserved

12.9 LSADC

12.9.1 Overview

The low-speed ADC (LSADC) converts external analog signals into digits of specific ratios to measure analog signals. It can be used for electric quantity detection and key detection.

12.9.2 Features

The LSADC has the following features:

- 3.3 V/1.8 V power voltage
- Power-down mode
- Maximum scanning frequency of 200,000 times per second
- 10-bit sampling precision, 3-channel inputs
- Single scanning mode and continuous scanning mode
- Automatic interrupt reporting after scanning is complete

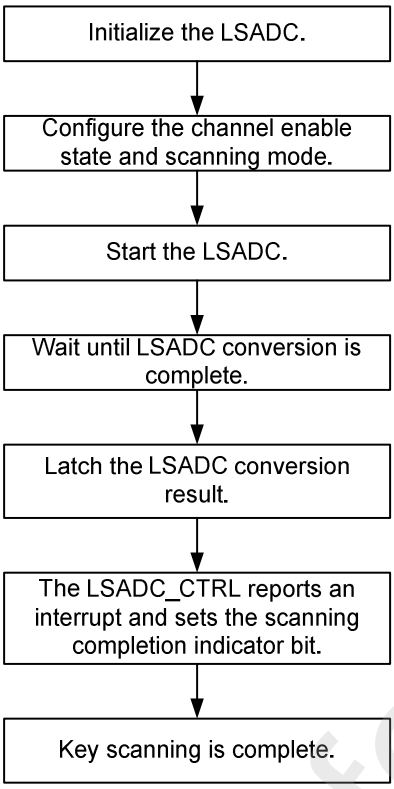
12.9.3 Operating Mode

Single Scanning Procedure

In single read mode (LSADC_CTRL0[model_sel] = 0), the CPU configures the ID of the channel to scanned, scanning mode, and key value mapping table and starts the LSADC to

complete a channel scanning. After channel scanning is complete, the system is notified of the scanning completion through interrupts, and the CPU can obtain the conversion result.

Figure 12-56 Single scanning procedure



Continuous Scanning Procedure

In continuous scanning mode (LSADC_CTRL0[model_sel] = 1), the CPU configures the continuous scanning interval (Tscan), glitch width (Tglitch), and valid channel ID (ch_vld) based on the application scenario, and starts the LSADC. The LSADC scans a valid channel within Tscan, and scans the next valid channel when the next scanning time reaches. After all valid channels are scanned, the LSADC cyclically scans them again. See Figure 12-58. Figure 12-57 illustrates channel polling in continuous scanning mode.

Figure 12-57 Channel polling in continuous scanning mode

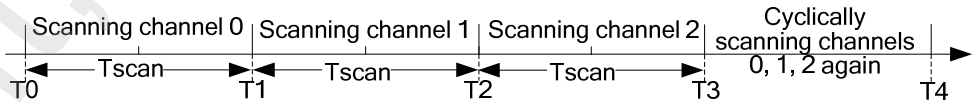
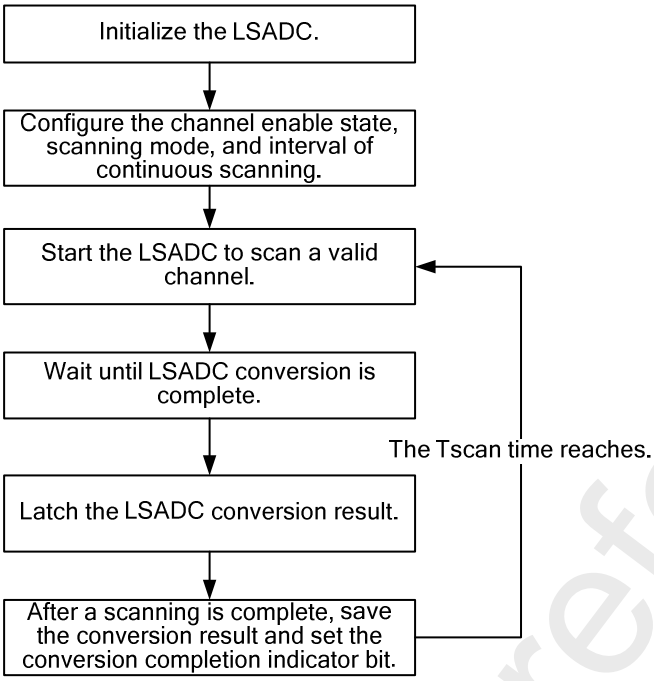


Figure 12-58 Continuous scanning procedure



Deglitch Procedure

The deglitch circuit adopts the majority decision algorithm. In the deglitch window, if the levels sampled by the ADC are the levels when keys are pressed, the value is considered as a valid key value; otherwise, a glitch signal is considered.

- In single scanning mode, the deglitch operation is not performed.
- In continuous scanning mode, the deglitch function is enabled. The deglitch time window Tglitch needs to be configured properly. For details, see the description of the LSADC_CTRL1 register.

Sampling Precision Configuration

The sampling precision can be configured as required by setting LSADC_CTRL9 [9:0].

- When the sampling precision is set to 10 bits, all 10 bits of the sampling result are valid.
- When the sampling precision is set to less than 10 bits, the corresponding upper bits of the sampling result are valid. For example, when the sampling precision is set to 8 bits, the upper 8 bits of the sampling result are valid.

12.9.4 Register Summary

Table 12-30 describes LSADC registers.

Table 12-30 Summary of LSADC registers (base address: 0x120E_0000)

Offset Address	Register	Description	Page
0x0000	LSADC_CTRL0	LSADC_CTRL configuration register	12-246
0x0004	LSADC_CTRL1	Deglitch configuration register	12-248
0x0008	LSADC_CTRL2	Scanning interval configuration register	12-248
0x0010	LSADC_CTRL4	Interrupt enable register	12-248
0x0014	LSADC_CTRL5	Interrupt status register	12-249
0x0018	LSADC_CTRL6	Interrupt clear register	12-250
0x001C	LSADC_CTRL7	Start configuration register	12-250
0x0020	LSADC_CTRL8	Stop configuration register	12-251
0x0024	LSADC_CTRL9	Conversion result precision register	12-251
0x0028	LSADC_CTRL10	lsadc_zero register	12-252
0x002C	LSADC_CTRL11	LSADC data hold register 1	12-252
0x0030	LSADC_CTRL12	LSADC data hold register 2	12-252
0x0034	LSADC_CTRL13	LSADC data hold register 3	12-253

12.9.5 Register Description

LSADC_CTRL0

LSADC_CTRL0 is an LSDAC_CTRL configuration register.

Offset Address	Register Name	Total Reset Value
0x0000	LSADC_CTRL0	0x0000_807F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								lsadc_data_delta				reserved		deglitch_bypass	reserved	lsadc_reset	power_down_model	model_sel	reserved		ch_c_vld	ch_b_vld	ch_a_vld	reserved				ch_c_eq_enable	ch_b_eq_enable	ch_a_eq_enable	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:24]	RW	reserved	Reserved

[23:20]	RW	lsadc_data_delta	Error range of the LSADC conversion result. In continuous scanning mode, if the difference between two conversion results falls within the error range, the two results are considered as the same.
[19:18]	RW	reserved	Reserved
[17]	RW	deglitch_bypass	Deglitch bypass (used in continuous scanning mode) 0: enabled 1: bypassed
[16]	RW	reserved	Reserved
[15]	RW	lsadc_reset	Whether the LSADC enters the reset status 0: The LSADC exits the reset status. 1: The LSADC enters the reset status.
[14]	RW	power_down_mode l	Whether power_down is supported 0: not supported 1: supported
[13]	RW	model_sel	Scanning mode of the LSADC_CTRL 0: single scanning mode 1: continuous scanning mode
[12:11]	RW	reserved	Reserved
[10]	RW	ch_c_vld	LSADC channel 2 validity 0: invalid 1: valid
[9]	RW	ch_b_vld	LSADC channel 1 validity 0: invalid 1: valid
[8]	RW	ch_a_vld	LSADC channel 0 validity 0: invalid 1: valid
[7:3]	RW	reserved	Reserved
[2]	RW	ch_c_eq_enable	LSADC channel 2 sampling equalization algorithm validity 0: invalid 1: valid
[1]	RW	ch_b_eq_enable	LSADC channel 1 sampling equalization algorithm validity 0: invalid 1: valid
[0]	RW	ch_a_eq_enable	LSADC channel 0 sampling equalization algorithm validity 0: invalid 1: valid

LSADC_CTRL1

LSADC_CTRL1 is a deglitch configuration register

Offset Address	Register Name	Total Reset Value
0x0004	LSADC_CTRL1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	glitch_sample																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	glitch_sample	Deglitch time window (in ms typically). When the LSADC conversion result is retained in the deglitch time window, the conversion result is considered as a valid value; otherwise, a glitch is considered. The deglitch time window cannot be 0 in continuous scanning mode.

LSADC_CTRL2

LSADC_CTRL2 is a scanning interval configuration register.

Offset Address	Register Name	Total Reset Value
0x0008	LSADC_CTRL2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	time_scan																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	time_scan	Interval of scanning two channels in continuous scanning mode (3 MHz clock domain N/3 MHz). The interval must be greater than the LSADC conversion time, that is, the configured value must be greater than or equal to 14. It cannot be set to 0 in continuous scanning mode.

LSADC_CTRL4

LSADC_CTRL4 is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x0010	LSADC_CTRL4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															int_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	int_enable	Scanned value valid interrupt enable 0: disabled 1: enabled

LSADC_CTRL5

LSADC_CTRL5 is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x0014	LSADC_CTRL5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																											lsadc_auto_busy	reserved	int_flag_inc	int_flag_inb	int_flag_ina
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:5]	RO	reserved	Reserved Writing to this field has no effect and reading this field returns 0.
[4]	RO	lsadc_auto_busy	LSADC busy indicator in automatic scanning mode 0: idle 1: busy
[3]	RO	reserved	Reserved
[2]	RO	int_flag_inc	Scanned value valid interrupt flag of channel 2
[1]	RO	int_flag_inb	Scanned value valid interrupt flag of channel 1

[0]	RO	int_flag_ina	Scanned value valid interrupt flag of channel 0

LSADC_CTRL6

LSADC_CTRL6 is an interrupt clear register.

Offset Address	Register Name	Total Reset Value
0x0018	LSADC_CTRL6	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved								clr_int_flag_inc	clr_int_flag_inb	clr_int_flag_ina
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	WO	clr_int_flag_inc	Channel 2 interrupt clear 0: not cleared 1: cleared
[1]	WO	clr_int_flag_inb	Channel 1 interrupt clear 0: not cleared 1: cleared
[0]	WO	clr_int_flag_ina	Channel 0 interrupt clear 0: not cleared 1: cleared

LSADC_CTRL7

LSADC_CTRL7 is a start configuration register.

Offset Address	Register Name	Total Reset Value
0x001C	LSADC_CTRL7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	start																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	start	LSADC_CTRL start signal. Writing any value to this register starts the LSADC_CTRL.

LSADC_CTRL8

LSADC_CTRL8 is a stop configuration register.

Offset Address	Register Name	Total Reset Value
0x0020	LSADC_CTRL8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	stop																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	stop	Automatic scanning stop. In automatic scanning mode, writing any value to this register stops automatic scanning of the LSADC_CTRL. Automatic scanning is restarted only after the start bit is enabled.

LSADC_CTRL9

LSADC_CTRL9 is a conversion result precision register.

Offset Address	Register Name	Total Reset Value
0x0024	LSADC_CTRL9	0x0000_03FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_active_bit									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved

[9:0]	RW	lsadc_active_bit	LSADC conversion result precision. 10'b1111111111: 10-bit precision 10'b1111111110: 9-bit precision … 10'b1000000000: 1-bit precision

LSADC_CTRL10

LSADC_CTRL10 is an lsadc_zero register.

Offset Address	Register Name	Total Reset Value
0x0028	LSADC_CTRL10	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_zero									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved
[9:0]	RW	lsadc_zero	LSADC value when no key is pressed

LSADC_CTRL11

LSADC_CTRL11 is LSADC data hold register 1.

Offset Address	Register Name	Total Reset Value
0x002C	LSADC_CTRL11	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_data_ina									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	lsadc_data_ina	Scanned value of LSADC channel 0

LSADC_CTRL12

LSADC_CTRL12 is LSADC data hold register 2.

Offset Address	Register Name	Total Reset Value
0x0030	LSADC_CTRL12	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_data_inb									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved
[9:0]	RO	lsadc_data_inb	Scanned value of LSADC channel 1

LSADC_CTRL13

LSADC_CTRL13 is LSADC data hold register 3.

Offset Address	Register Name	Total Reset Value
0x0034	LSADC_CTRL13	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																						lsadc_data_inc									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RW	reserved	Reserved
[9:0]	RO	lsadc_data_inc	Scanned value of LSADC channel 2

12.10 PWM

12.10.1 Overview

Hi3516C V300 has four independent pulse width modulation (PWM) outputs in one group.

12.10.2 Features

Each PWM output has the following features:

- Supports the optional 3 MHz, 24 MHz or 50 MHz clock source.
- Provides an internal 26-bit counter with configurable output frequency. The maximum frequency of the output square waves is 25 MHz (50 MHz/2), and the minimum frequency of the output square waves is 0.045 Hz (3 MHz/67108863).
- Allows you to set the number of high-level beats (26 bits).

- Provides a 10-bit internal counter and allows you to set the number of pulses. A maximum of 1023 pulses are supported. The number of output pulses can be fixed at a value and the always output mode is supported.
  - When pwmn_keep is set to 0 (PWM*n* indicates the PWM ID), PWM*n* outputs the square waves of a specific number, which depends on the setting of the pwmn_num register.
  - When pwmn_keep is set to 1, PWM*n* always outputs square waves.

12.10.3 Operating Mode

The internal working clock of the PWM module is 3 MHz, 24 MHz or 50 MHz. The following takes PWM0 as an example to configure 1-channel PWM output:

Step 1 Select an appropriate clock source, and calculate the number of required cycles and high-level beats.

Step 2 Write the corresponding values to PWM0_CFG0, PWM0_CFG1, and PWM0_CFG2.

Step 3 Set PWM0_CTRL[0] to 1 to enable the PWM output.

----End

For example, to output a 3 kHz waveform with 72.5% high levels and 10 pulses (the duty ratio is 72.5%), calculate the number of high levels as follows:

- If the 3 MHz clock is the source clock, Cycle = 3 MHz/1 kHz ≈ 1000 (0x00003E8 in hexadecimal)
- Number of high levels = Cycle x Duty ratio = 1000 x 72.5% = 725 (0x00002D5 in hexadecimal)

To output a desired waveform, perform the following steps:

Step 1 Write 0x2 to PERI_CRG14, select the 3 MHz clock as the PWM clock source, and enable the PWM clock.

Step 2 Read PWM0_STATE2[10] until it is 0. This indicates that the PWM module is idle and can output square waves.

Step 3 Write 0x0000_03E8 to PWM0_CFG0.

Step 4 Write 0x0000_02D5 to PWM0_CFG1.

Step 5 Write 0x0000_000A to PWM0_CFG2.

Step 6 Write 0x1 to PWM0_CTRL.

NOTE

The following steps can be skipped. They are used to check whether the square wave is output as expected.

Step 7 Read PWM0_STATE2[10] until it is 1. This indicates that the PWM module is outputting square waves.

Step 8 Read PWM0_STATE0 and compare the queried value with 0x0000_03E8.

Step 9 Read PWM0_STATE1 and compare the queried value with 0x0000_02D5.

Step 10 Read PWM0_STATE2[9:0] and compare the queried value with 0x0A. If PWM0_STATE2[10] is 1, the PWM module is outputting square waves. If PWM0_STATE2[10] is 0, the configured number of square waves are output.

----End

12.10.4 Register Summary

The registers of PWM*n* (*n* = 0−3) have the same functions but their base addresses are different. See Table 12-31.

Table 12-31 Base addresses for the registers of PWM*n*

Value of n	Base Address
0	0x1213_0000
1	0x1213_0020
2	0x1213_0040
3	0x1213_0060

Table 12-32 describes PWM0 registers as an example.

Table 12-32 Summary of PWM0 registers (base address: 0x1213_0000)

Offset Address	Register	Description	Page
0x0000	PWM0_CFG0	PWM0 configuration 0 register	12-255
0x0004	PWM0_CFG1	PWM0 configuration 1 register	12-256
0x0008	PWM0_CFG2	PWM0 configuration 2 register	12-256
0x000C	PWM0_CTRL	PWM0 control register	12-257
0x0010	PWM0_STATE0	PWM0 status 0 register	12-257
0x0014	PWM0_STATE1	PWM0 status 1 register	12-258
0x0018	PWM0_STATE2	PWM0 status 2 register	12-259

12.10.5 Register Description

PWM0_CFG0

PWM0_CFG0 is a PWM0 configuration 0 register.

Offset Address	Register Name	Total Reset Value
0x0000	PWM0_CFG0	0x0000_018F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_period																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:0]	RW	pwm0_period	Number of cycles for PWM0 **NOTE** The configured value must be greater than or equal to 2.

PWM0_CFG1

PWM0_CFG1 is a PWM0 configuration 1 register.

Offset Address	Register Name	Total Reset Value
0x0004	PWM0_CFG1	0x0000_00C7

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_duty																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:0]	RW	pwm0_duty	Number of level beats for PWM0. If the number is greater than or equal to the number of cycles, the output level is always high. **NOTE** The configured value must be greater than or equal to 1.

PWM0_CFG2

PWM0_CFG2 is a PWM0 configuration 2 register.

Offset Address	Register Name	Total Reset Value
0x0008	PWM0_CFG2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								pwm0_num							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:10]	RO	reserved	Reserved
[9:0]	RW	pwm0_num	Number of square waves output by PWM0

PWM0_CTRL

PWM0_CTRL is a PWM0 control register.

Offset Address	Register Name	Total Reset Value
0x000C	PWM0_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved																													pwm0_keep	pwm0_inv	pwm0_enable
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:3]	RO	reserved	Reserved
[2]	RW	pwm0_keep	PWM output mode 0: PWM0 outputs a fixed number of square waves. 1: PWM0 always outputs square waves.
[1]	RW	pwm0_inv	PWM output control 0: PWM0 outputs square waves in normal mode. 1: PWM0 outputs square waves in inverted mode.
[0]	RW	pwm0_enable	PWM enable 0: disabled 1: enabled

PWM0_STATE0

PWM0_STATE0 is a PWM0 status 0 register.

Offset Address	Register Name	Total Reset Value
0x0010	PWM0_STATE0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_period_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:0]	RO	pwm0_period_st	Number of count cycles for the internal module of PWM0

PWM0_STATE1

PWM0_STATE1 is a PWM0 status 1 register.

Offset Address	Register Name	Total Reset Value
0x0014	PWM0_STATE1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved								pwm0_duty_st																							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:26]	RO	reserved	Reserved
[25:0]	RO	pwm0_duty_st	Number of high level beats for the internal module of PWM0

PWM0_STATE2

PWM0_STATE2 is a PWM0 status 2 register.

Offset Address	Register Name	Total Reset Value
0x0018	PWM0_STATE2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved												pwm0_cnt_st								pwm0_keep_st	pwm0_busy	pwm0_period_st									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:22]	RO	reserved	Reserved
[21:12]	RO	pwm0_cnt_st	Number of remaining square waves output by PWM0. This field is valid only when the following conditions are met: pwm0_busy = 1, pwm0_keep_st = 0
[11]	RO	pwm0_keep_st	Square wave output mode for the internal module of PWM0 0: PWM0 outputs a fixed number of square waves. 1: PWM0 always outputs square waves.
[10]	RO	pwm0_busy	Working status of PWM0 0: Wave output is complete and PWM0 is idle. 1: PWM0 is outputting square waves.
[9:0]	RO	pwm0_period_st	Number of output square waves for the internal module of PWM0

Contents

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Tables

13 Security Modules

13.1 Cipher

13.1.1 Overview

The cipher module supports data encryption and decryption by following the data encryption standard (DES), 3DES, or advanced encryption standard (AES) algorithm. The DES, 3DES, and AES algorithms are implemented according to FIPS46-3 and FIPS 197 standards. The DES/3DES and AES operating modes comply with FIPS-81 and NIST special 800-38a standards.

The cipher module can encrypt or decrypt a large amount of data effectively. In addition, it encrypts and decrypts one or more blocks at one time.

13.1.2 Features

The cipher module has the following features:

- Supports the AES key length of 128 bits, 192 bit, or 256 bits. If keys are configured by the key management module, the key length can be set only to 128 bits.
- Supports the DES key length of 64 bits. The values for bit 0, bit 8, bit 16, bit 24, bit 32, bit 40, bit 48, and bit 56 represent the parity check values for eight bytes respectively. The parity check values are not used during encryption or decryption.
- Supports 3-key and 2-key modes for the 3DES algorithm. If keys are configured by the key management module, only the 2-key mode is supported.
- Supports the operating modes of counter with Cipher Block Chaining-Message Authentication Code (CCM), Galois/Counter Mode (GCM), electronic code book (ECB), cipher block chaining (CBC), 1-/8-/128-cipher feedback (CFB), 128-output feedback (OFB), and counter (CTR) for the AES algorithm. These operating modes comply with the NIST SP 800-38A standard.
- Supports the operating modes of ECB, CBC, 1/8/64-CFB, and 1/8/64-OFB for the DES or 3DES algorithm. These operating modes comply with the FIPS-81 standard.
- Encrypts and decrypts one or more blocks at one time in ECB, CBC, CFB, OFB or CTR operating mode.
- Encrypts and decrypts one or more blocks at one time in CTR operating mode using the AES algorithm.
- Provides eight encryption/decryption keys (64 bits, 128 bits, 192 bits, or 256 bits) configured by the CPU.

- Provides eight keys (fixed at 128 bits) configured by the key management module. The master CPU supports the write operation but not the read operation.
- Provides a single-block encryption/decryption channel and seven multi-block encryption/decryption channels. The single-block encryption/decryption channel can encrypt or decrypt a single block only at one time. In this case, the CPU writes data to the channel register and reads the results. For the multi-block encryption/decryption channel, the logic reads data from the DDR, and writes the encrypted or decrypted data to the DDR automatically.
- Supports weighted round robin policy for each channel. For a single-block channel, the weighted value is 1 by default; for a multi-block channel, the weighted value is configurable.
- Supports the same set of keys or different sets of keys for any channel.
- Keeps the data in the last incomplete block unprocessed when the data of the multi-block channels is not an integral multiple of encryption/decryption blocks.
- Supports byte address for the multi-block encryption/decryption channel.
- Supports the multi-linked-list structure for the multi-block encryption/decryption channel and supports the combination of data from multiple linked lists. The linked list length is 20 bits. That is, the maximum data amount is 1 MB minus 1.
- Queries the interrupt status and masks and clears interrupts.
- Separately processes and controls interrupts for each channel.
- Supports multi-packet interrupts and aging interrupts.

13.1.3 Function Description

The operating modes of the DES, 3DES, and AES algorithms comply with the FIPS-81 and NIST special 800-38a/c/d standards. In the DES, 3DES, and AES algorithms, the ECB, CBC, and CFB operating modes are identical; however, the CTR (for the AES algorithm only) and OFB operating modes are slightly different.

3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation.

Figure 13-1 shows the 3DES encryption of a 3-key operation and a 2-key operation.

Figure 13-1 3DES encryption of a 3-key operation and a 2-key operation

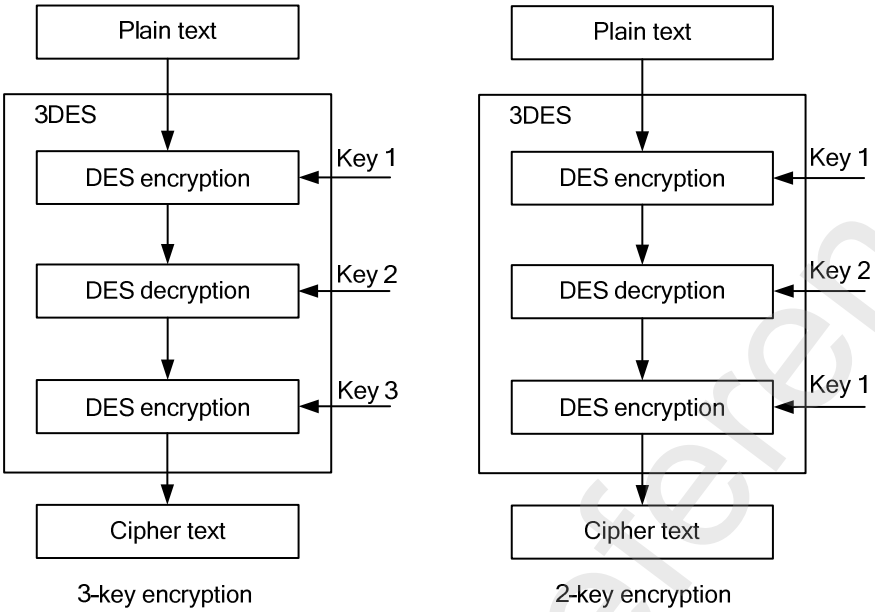
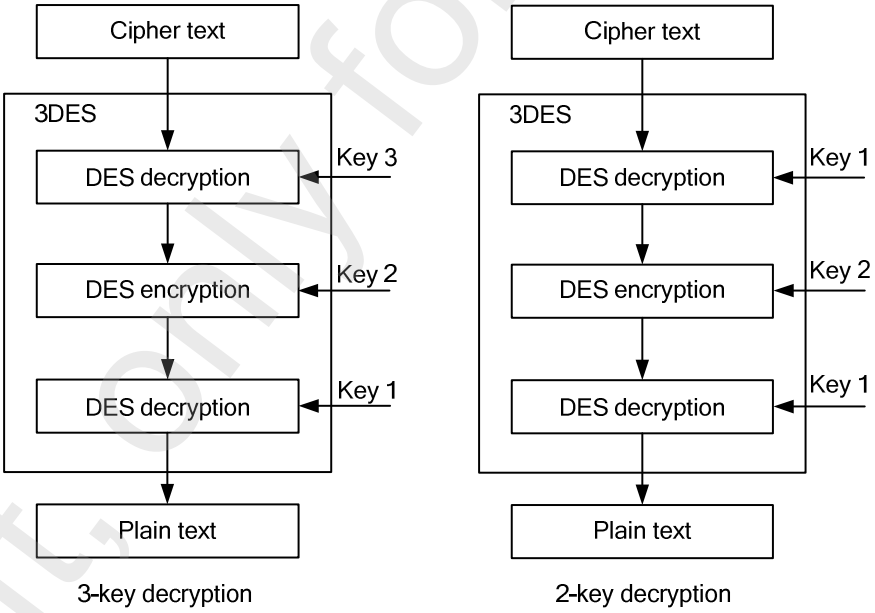


Figure 13-2 shows the 3DES decryption of a 3-key operation and a 2-key operation.

Figure 13-2 3DES decryption of a 3-key operation and a 2-key operation



ECB Mode

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent. With this feature, the plain text encryption and cipher text decryption can be performed concurrently. Figure 13-3 shows the ECB mode of the AES and DES algorithms, and Figure 13-4 shows the ECB mode of the 3DES algorithm.

Figure 13-3 ECB mode of the AES and DES algorithms

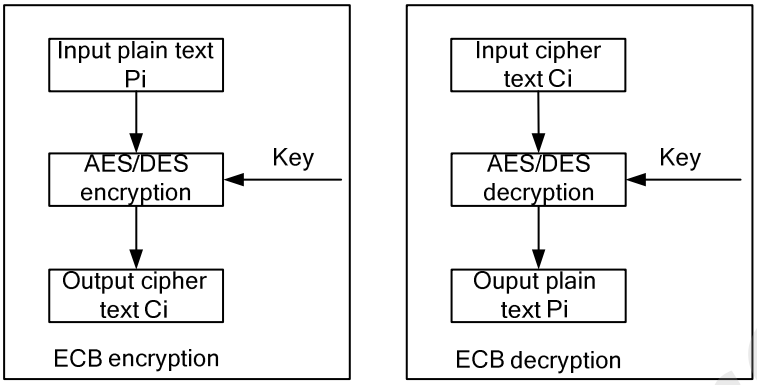
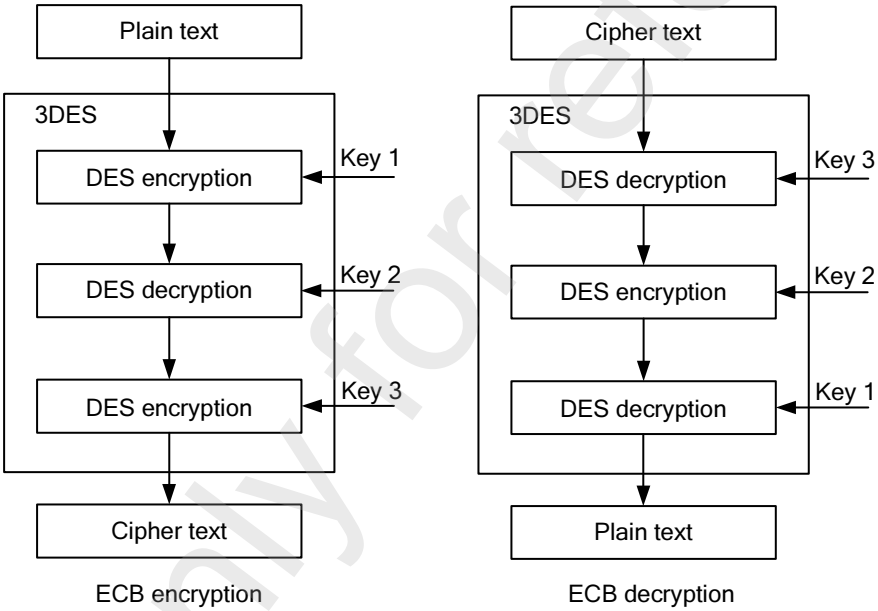


Figure 13-4 ECB mode of the 3DES algorithm



CBC Mode

In CBC mode, the encrypted input plain text block must be exclusively ORed with the input initialization vector (IV) before being encrypted. The encryption processing of each plain text block is related to the block processing result (cipher text) of the previous plain text. Therefore, encryption operations cannot be concurrently performed in CBC mode. The decryption operation, however, is independent of output plain text of the previous block. Therefore, decryption operations can be performed concurrently. Figure 13-5 shows the CBC mode of the AES and DES algorithms, and Figure 13-6 shows the CBC mode of the 3DES algorithm.

Figure 13-5 CBC mode of the AES and DES algorithms

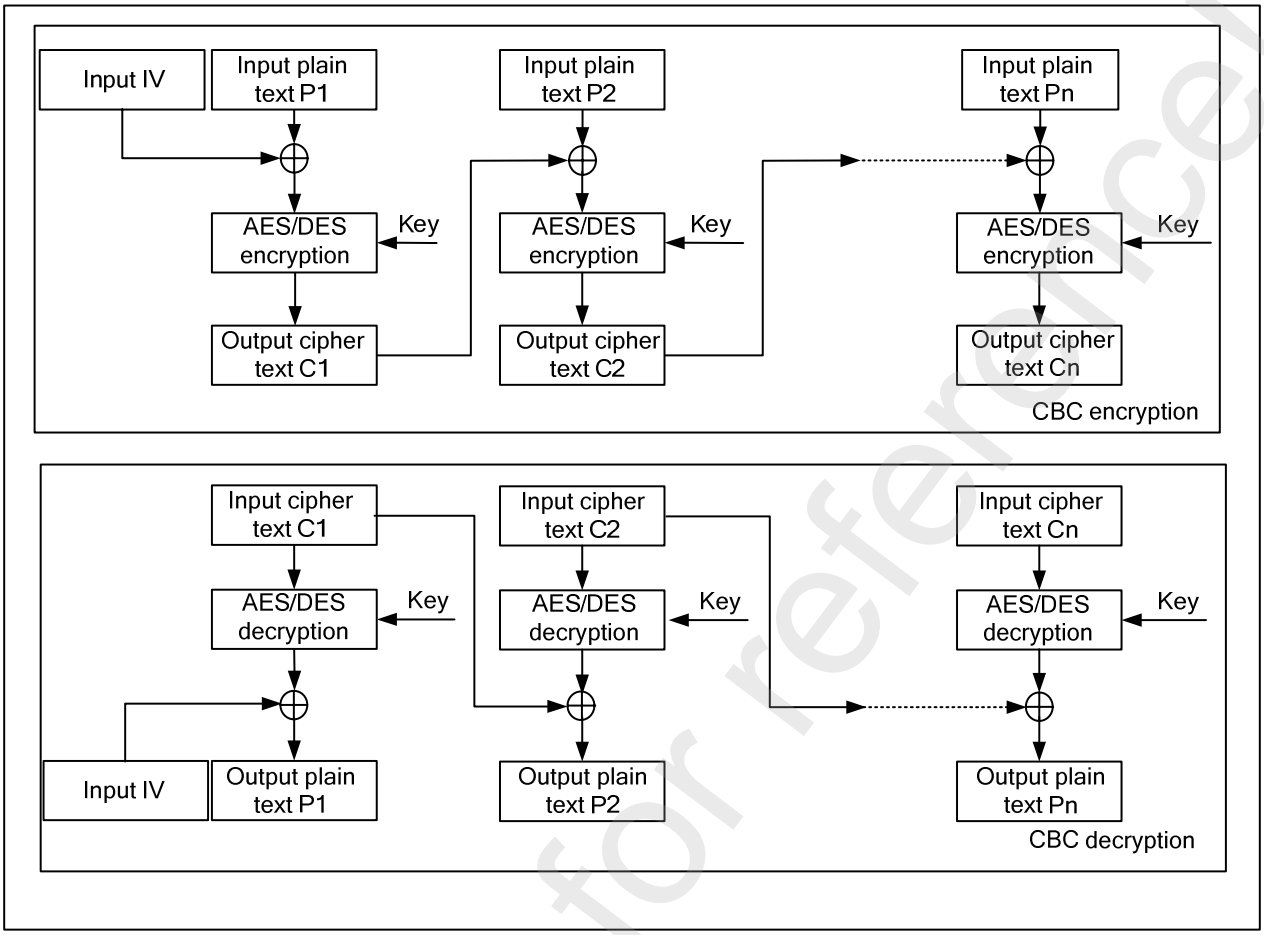
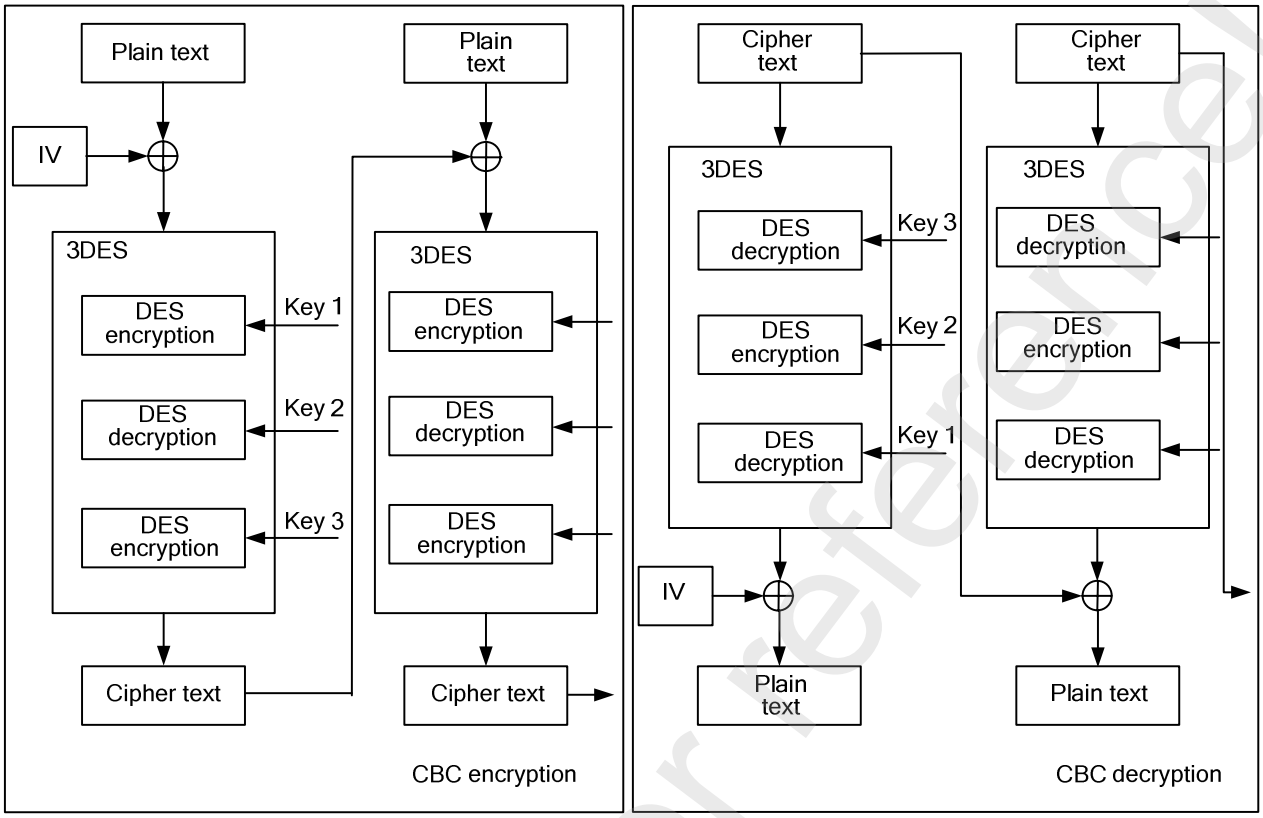


Figure 13-6 CBC mode of the 3DES algorithm



CFB Mode

The CFB mode is used to convert a block cipher into a stream cipher. This mode is implemented by selecting the operation bits of the CFB. The shift operation bits are represented by the letter s. The value of s is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 1 bit, 8 bits, or 128 bits for the AES algorithm

Figure 13-7 shows the s-bit CFB mode of the AES and DES algorithms, and Figure 13-8 shows the s-bit CFB mode of the 3DES algorithm.

Figure 13-7 S-bit CFB mode of the AES and DES algorithms

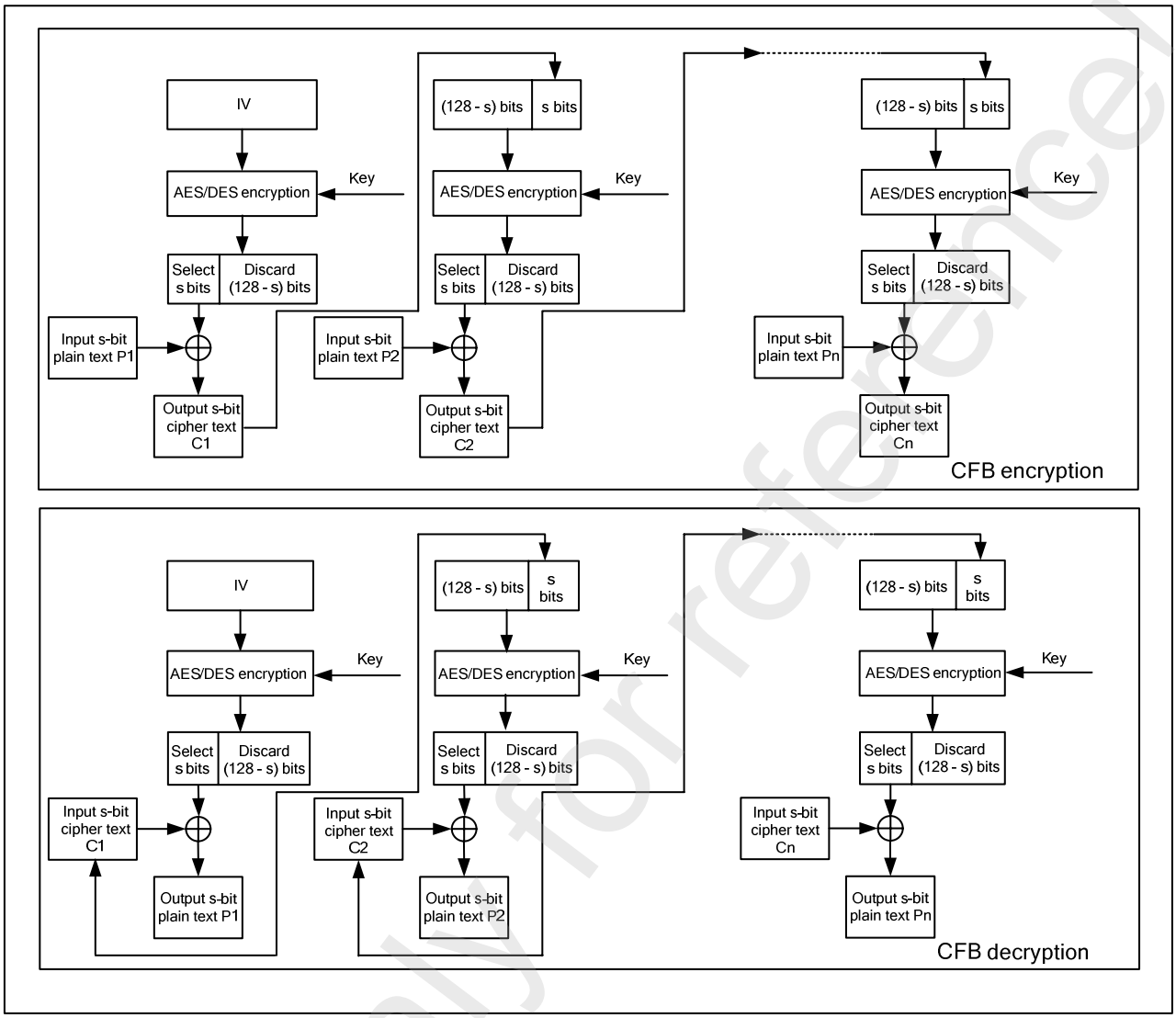
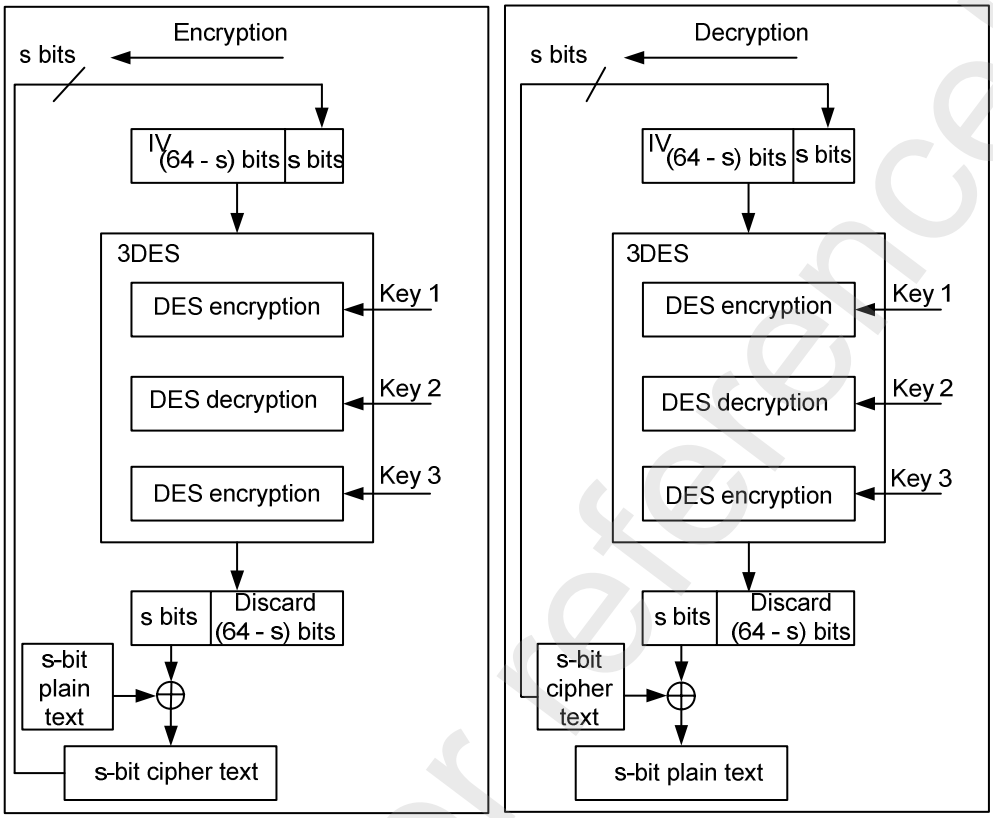


Figure 13-8 S-bit CFB mode of the 3DES algorithm



OFB Mode

In OFB mode, IVs serve as the inputs during encryption. If a same key is used, different IVs must be used to ensure operation security. The value of the s bit is as follows:

- 1 bit, 8 bits, or 64 bits for the DES or 3DES algorithm
- 128 bits for the AES algorithm

Figure 13-9 shows the OFB mode of the AES algorithm.

Figure 13-9 OFB mode of the AES algorithm

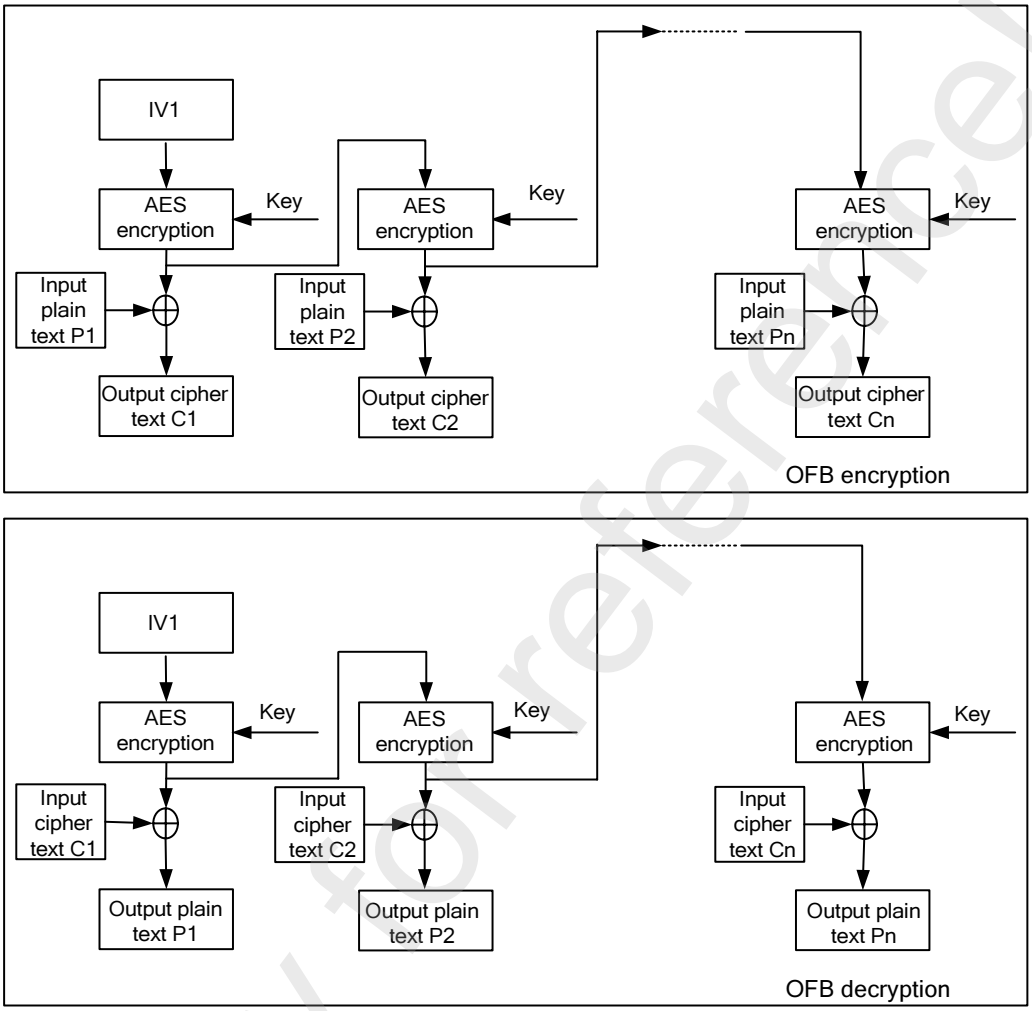


Figure 13-10 shows the s-bit OFB mode of the DES algorithm.

Figure 13-10 S-bit OFB mode of the DES algorithm

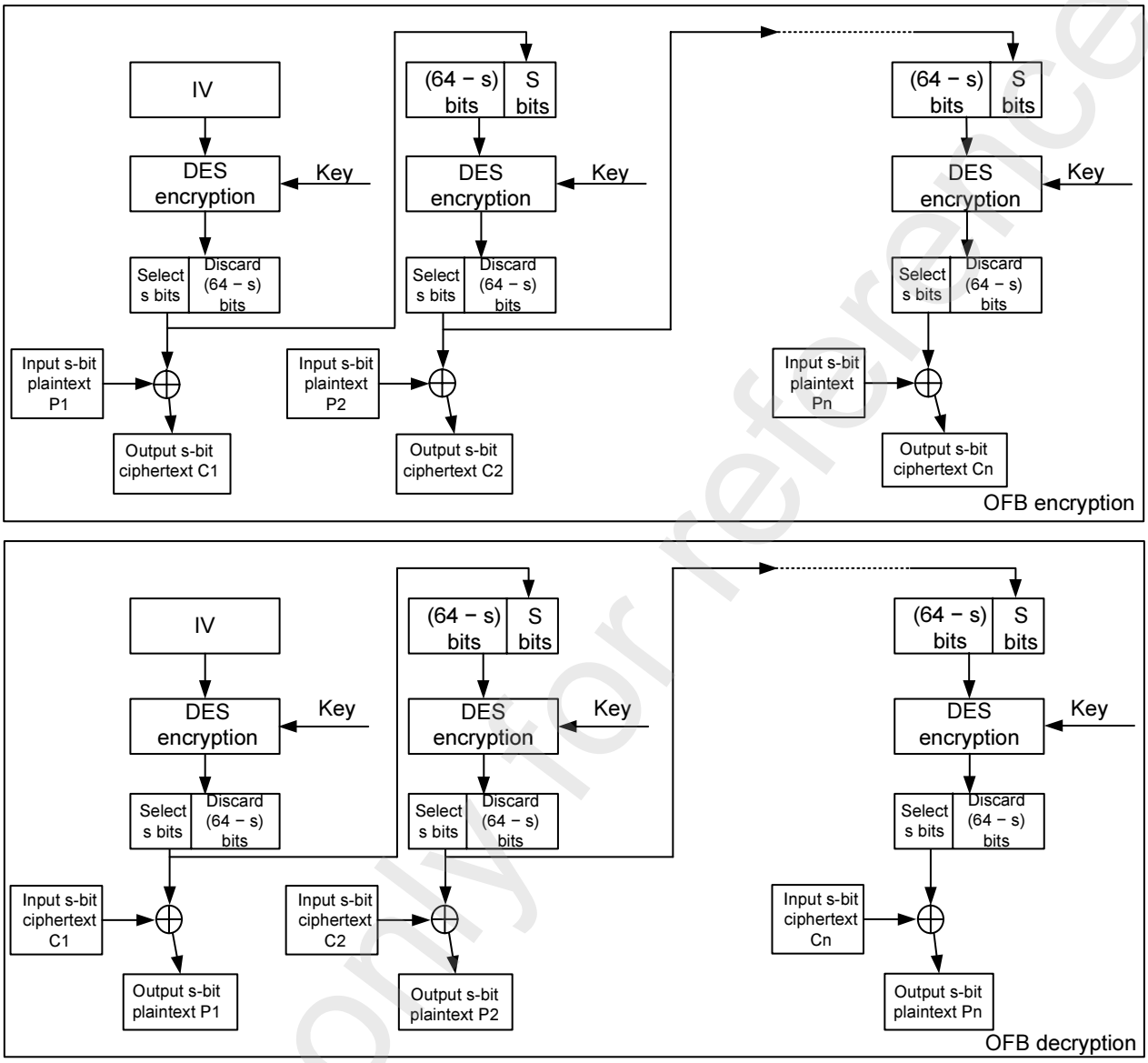
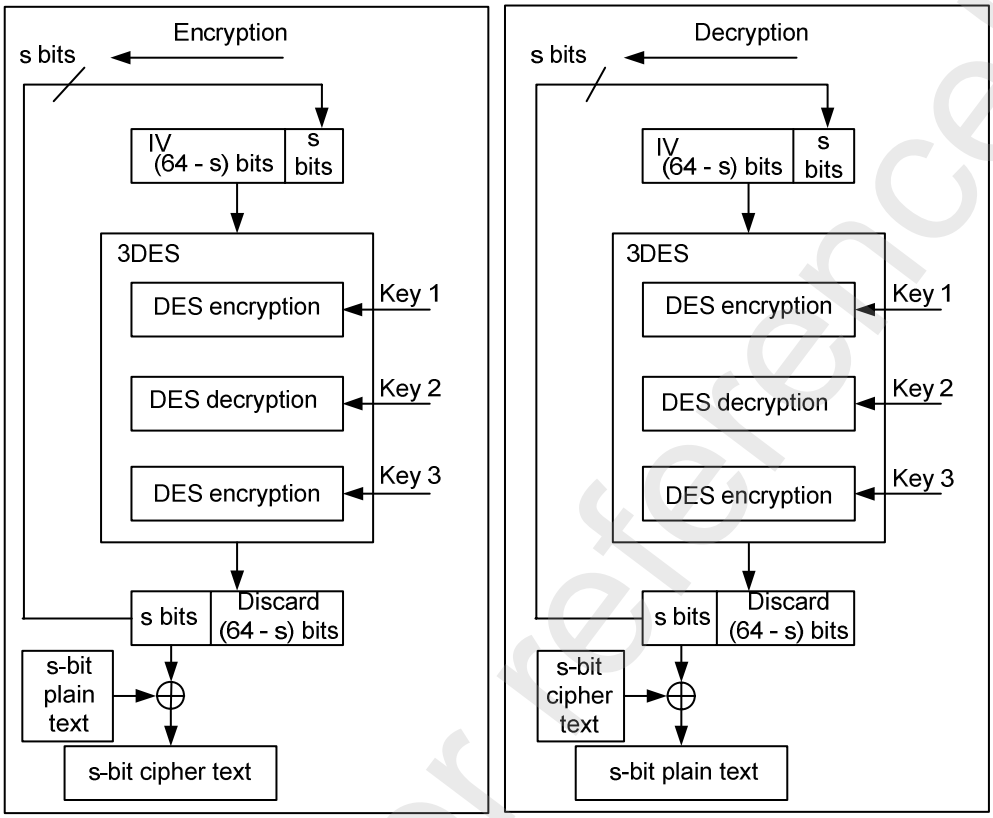


Figure 13-11 shows the s-bit OFB mode of the 3DES algorithm.

Figure 13-11 S-bit OFB mode of the 3DES algorithm



CTR Mode

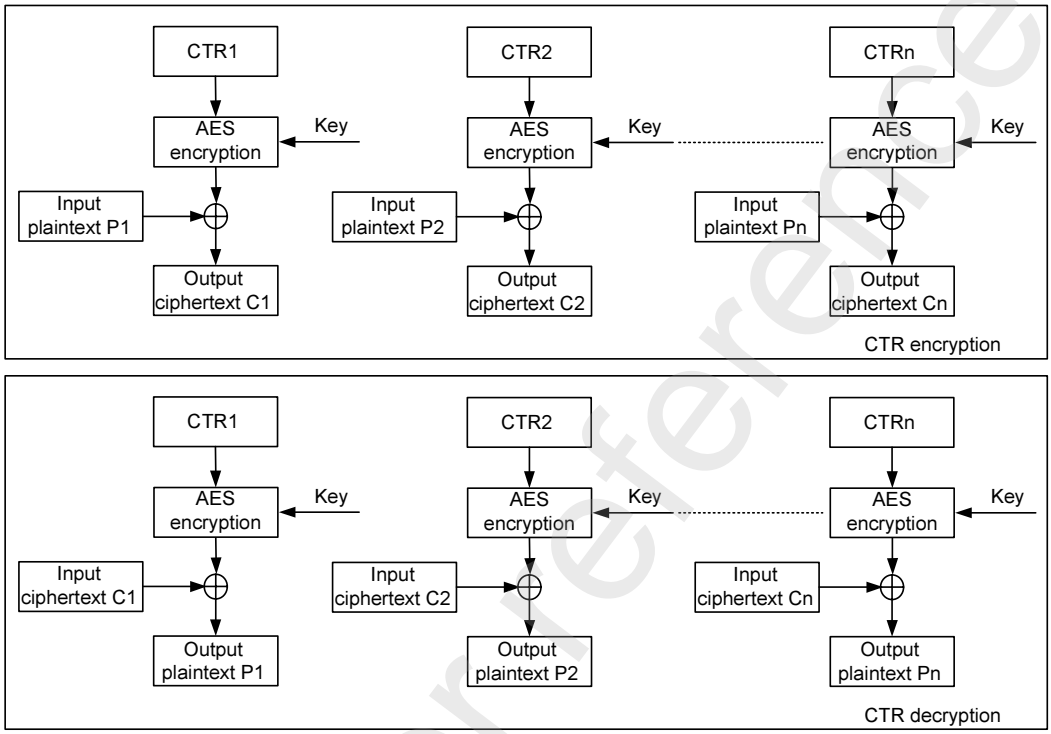
In CTR mode, different data segments are input to the cipher module by using the AES algorithm to ensure data security. Such data can be the count value CTRn. Therefore, CTRn determines the security of the CTR mode.

NOTE

CTRn is obtained by using the accumulation count mode.

Figure 13-12 shows the CTR mode of the AES algorithm.

Figure 13-12 CTR mode of the AES algorithm

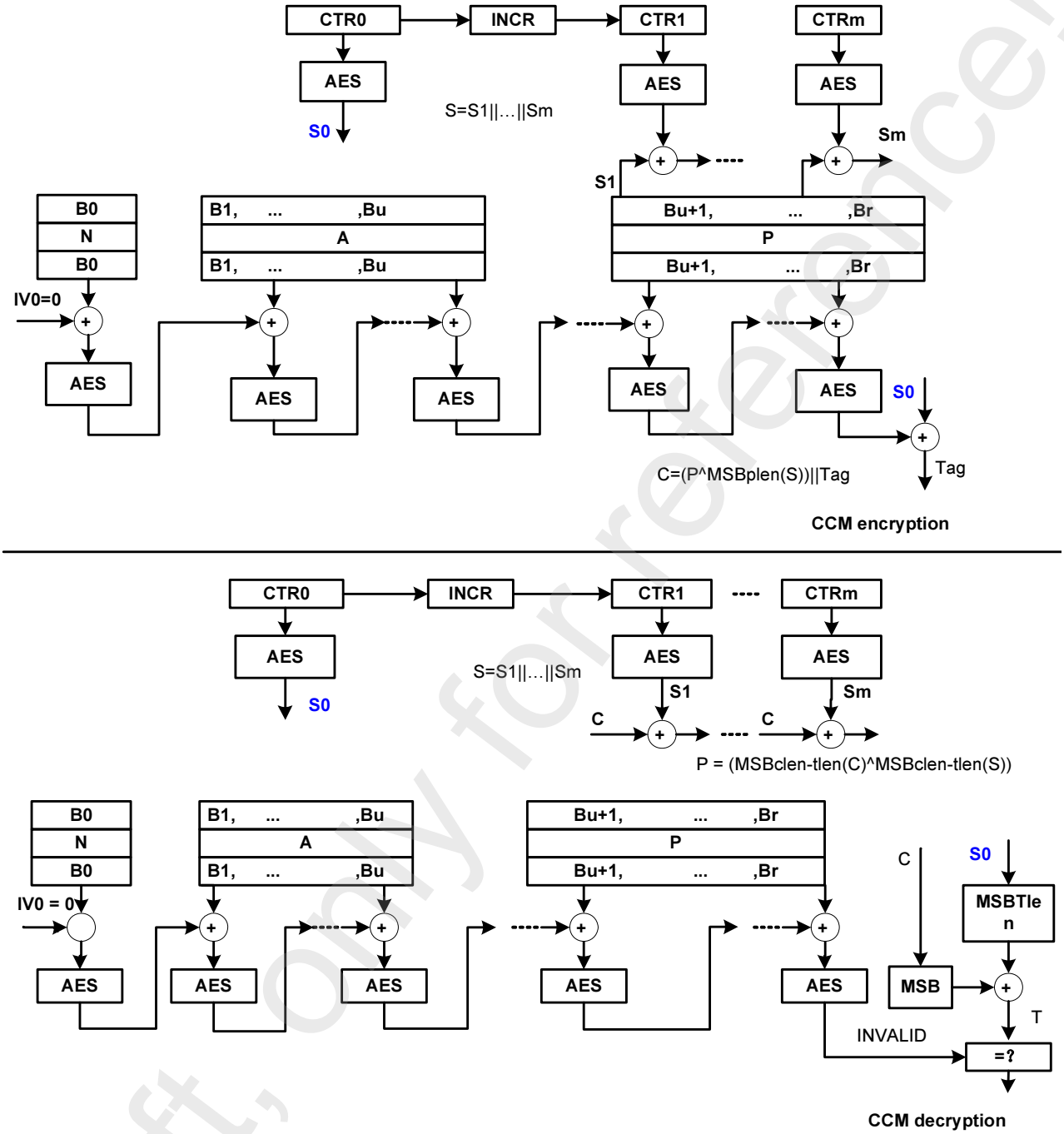


CCM Mode

The CCM mode of the AES algorithm consists of the AES CTR mode and AES CBC mode, which ensures data confidentiality and integrity.

Figure 13-13 shows the CCM mode of the AES algorithm.

Figure 13-13 CCM mode of the AES algorithm

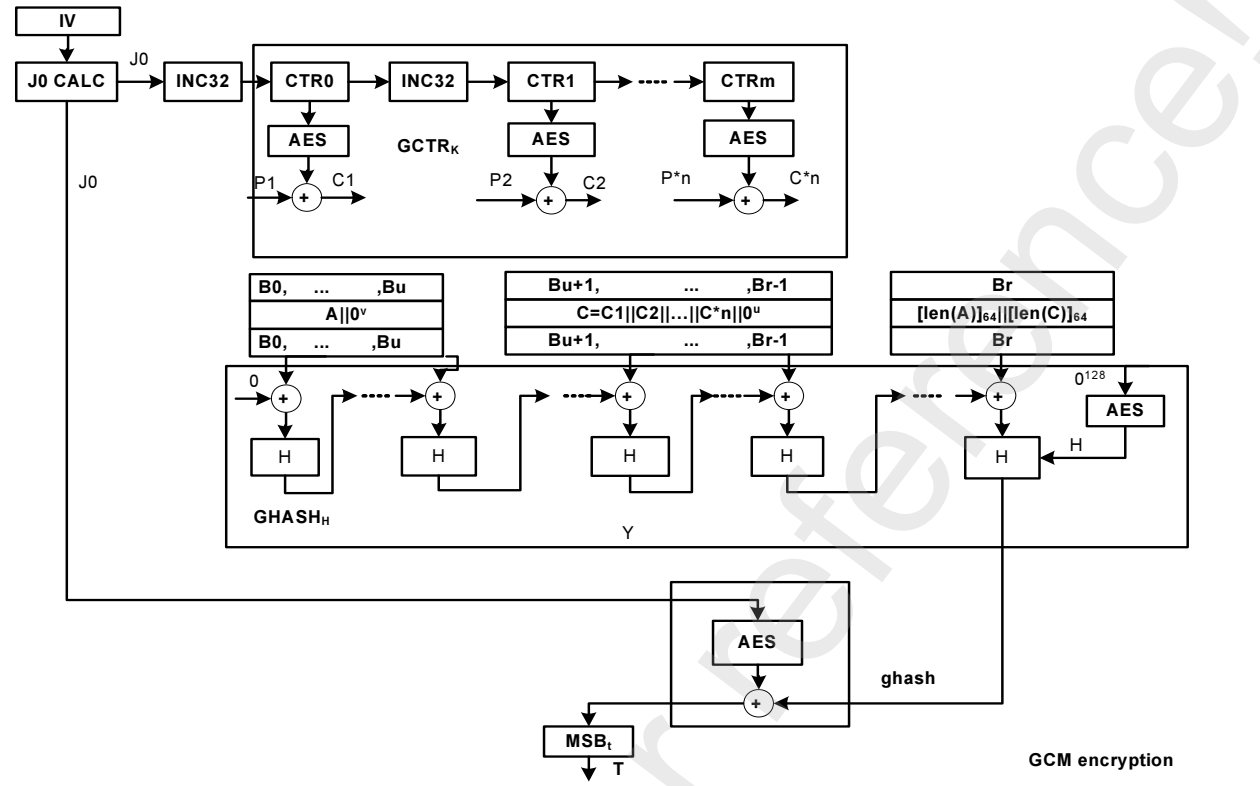


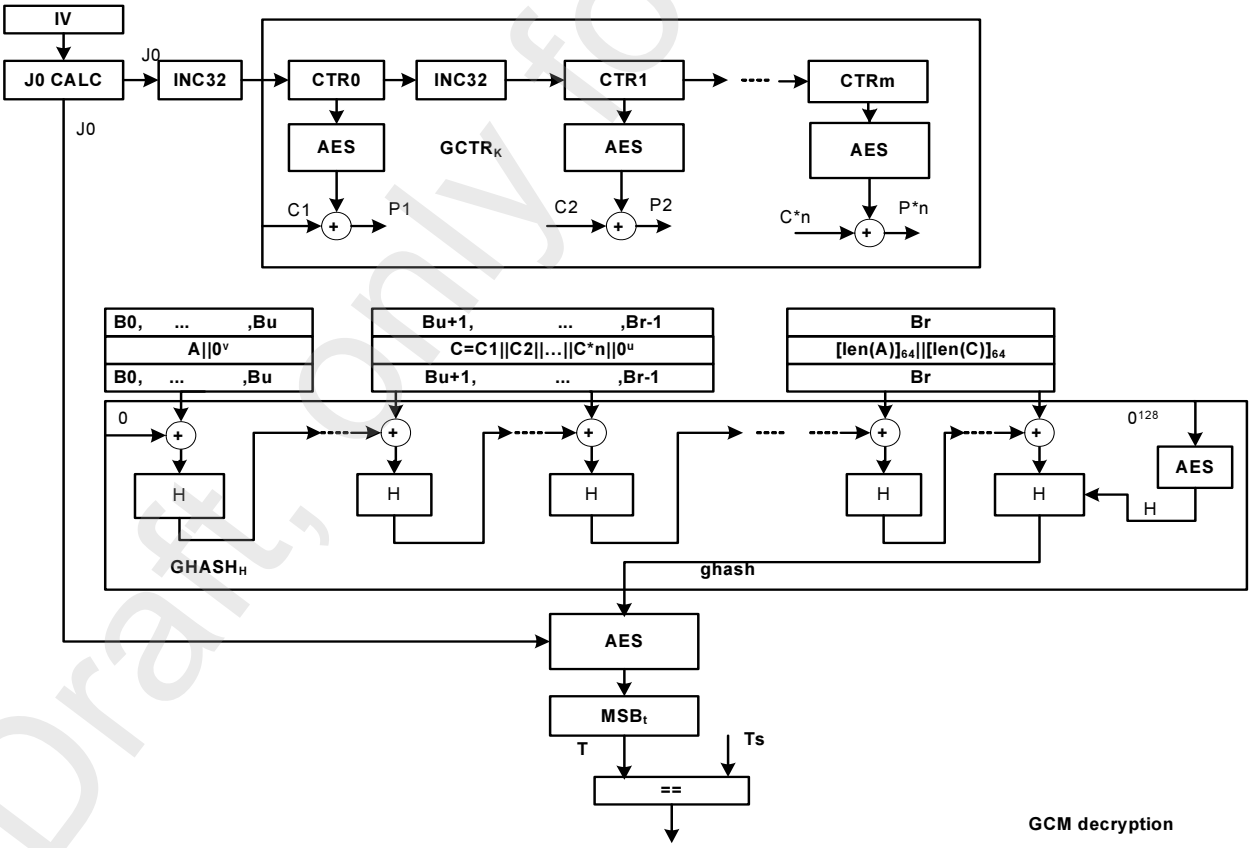
GCM Mode

The GCM mode of the AES algorithm consists of AES CTR and ghash, which ensures data confidentiality and integrity.

Figure 13-14 shows the GCM mode of the AES algorithm.

Figure 13-14 GCM mode of the AES algorithm





13.1.4 Operating Mode

Single-Block Operation Process of the Cipher Module

The cipher module provides channel 0 as the single-block encryption/decryption channel. A single-block operation is performed as follows:

Step 1 Check whether channel 0 is busy by querying the ch0_busy field of the configuration register CHAN0_CFG of channel 0. If channel 0 is not busy, configure data inputs and write related configuration information to the registers of channel 0.

Step 2 Write to the ch0_start field of CHAN0_CFG to enable channel 0 to start encryption or decryption.

----End

Check whether encryption and decryption of channel 0 are complete in either of following ways:

Step 1 Query the ch0_busy field. If ch0_busy indicates that channel 0 is not busy, encryption and decryption are complete.

Step 2 Check whether the interrupt of channel 0 is generated. If the interrupt is generated, encryption and decryption are complete. Read the registers CHAN0_CIPHER_DOUT and CHAN0_CIPHER_IVOUT of channel 0.

----End

Multi-Block Operation Process of the Cipher Module

The cipher module provides seven multi-block encryption/decryption channels. The weighted value of each channel can be set using software based on its rate. These channels automatically read data from the DDR, and write the encrypted or decrypted data to the DDR.

A multi-block operation is performed as follows:

Step 1 Initialize the channels, including setting the depth, start address, number of multi-packet interrupts, aging interrupt time of the input and output queues of each channel, and setting the control register of each channel.

Step 2 When data needs to be encrypted or decrypted, query CHANn_IBUF_CNT. If the value of this register is smaller than the value of CHANn_IBUF_NUM, add the header of the data linked list corresponding to the data to be encrypted or decrypted to the input queue, and go to Step 4; otherwise, go to step 3.

Step 3 Enable the interrupt corresponding to the input queue channel, wait for the generation of the interrupt, read CHANn_IEMPTY_CNT, write to this register to clear the interrupt, and add new data to the input queue.

Step 4 Add the linked list header of the output buffer to the output queue.

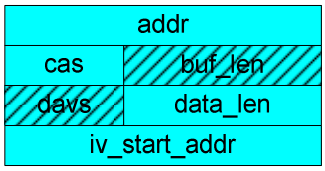
Step 5 Enable the interrupt corresponding to the output queue.

Step 6 Fetch data from the output queue, and write the number of currently received packets to CHANn_OFULL_CNT to clear the interrupt.

----End

Figure 13-15 shows the structure of the linked list header of a multi-block encryption/decryption channel.

Figure 13-15 Structure of the linked list header of a multi-block encryption/decryption channel

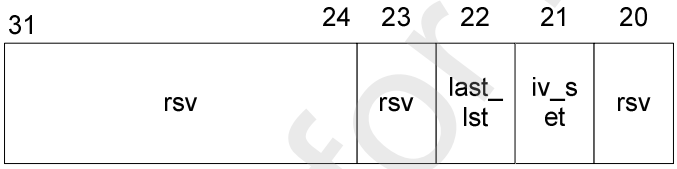


The field definitions are as follows:

- addr is the start address of the buffer pointer by the linked list header. The start address can be byte address.
- data_len is the length of the valid data pointed by the linked list header.
- cas is cipher control information.

Figure 13-16 shows the bits of cas.

Figure 13-16 Bits of cas



  - iv_set indicates that the IV of the data pointed by the current linked list header must be replaced. iv_start_addr indicates the start address of the IV in the DDR. This address must be aligned by word.
  - last_lst indicates that the data pointed by the current linked list header is the last linked list of a data block. If the logic encounters an incomplete encryption/decryption block after processing the linked list, the logic writes the incomplete block to the output buffer without performing encryption and decryption.

Clock Gating

When no encryption is required and the cipher module is idle, the cipher clock can be disabled by configuring the registers of the system controller, which reduces power consumption.

Soft Reset

The cipher module can be soft-reset by configuring the registers of the system controller.

13.1.5 Register Summary

Table 13-1 describes cipher registers.

NOTE

The variable *n* in the offset addresses indicates the channel ID and ranges from 1 to 7.

Table 13-1 Summary of cipher registers (base address: 0x1008_0000)

Offset Address	Register	Description	Page
0x0000–0x000C	CHAN0_CIPHER_DOUT	Cipher output register for channel 0 (for single-block encryption/decryption)	13-20
0x0010–0x001C	CHAN0_CIPHER_IVOUT	Operation complete IV output register of the cipher module	13-21
0x0020–0x008C	CHAN_CIPHER_IVOUT	IV output register for channels 1–7	13-22
0x0090–0x018C	CIPHER_KEY	CPU configuration key register of the cipher module	13-22
0x0840	CHAN0_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 0	13-24
0x0844	CHAN0_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 0	13-24
0x0848	CHAN1_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 1	13-24
0x084C	CHAN1_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 1	13-25
0x0850	CHAN2_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 2	13-25
0x0854	CHAN2_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 2	13-26
0x0858	CHAN3_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 3	13-26
0x085C	CHAN3_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 3	13-26
0x0860	CHAN4_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 4	13-27
0x0864	CHAN4_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 4	13-27
0x0868	CHAN5_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 5	13-28
0x086C	CHAN5_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 5	13-28
0x0870	CHAN6_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 6	13-28

Offset Address	Register	Description	Page
0x0874	CHAN6_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 6	13-29
0x0878	CHAN7_GCM_A_LEN_0	A length lower 32 bits register for the AES GCM of channel 7	13-29
0x087C	CHAN7_GCM_A_LEN_1	A length upper 32 bits register for the AES GCM of channel 7	13-30
0x0880	CHAN0_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 0	13-30
0x0884	CHAN0_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 0	13-30
0x0888	CHAN1_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 1	13-31
0x088C	CHAN1_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 1	13-31
0x0890	CHAN2_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 2	13-32
0x0894	CHAN2_GCM_PC_LEN_0	Payload length upper 32 bits register for the AES GCM of channel 2	13-32
0x0898	CHAN3_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 3	13-32
0x089C	CHAN3_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 3	13-33
0x08A0	CHAN4_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 4	13-33
0x08A4	CHAN4_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 4	13-34
0x08A8	CHAN5_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 5	13-34
0x08AC	CHAN5_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 5	13-34
0x08B0	CHAN6_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 6	13-35
0x08B4	CHAN6_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 6	13-35
0x08B8	CHAN7_GCM_PC_LEN_0	Payload length lower 32 bits register for the AES GCM of channel 7	13-36
0x08BC	CHAN7_GCM_PC_LEN_1	Payload length upper 32 bits register for the AES GCM of channel 7	13-36

Offset Address	Register	Description	Page
0x08C0	CHAN0_3_GCM_IV_LEN	IV length register for the AES GCM of channels 0−3	13-36
0x08C4	CHAN4_7_GCM_IV_LEN	IV length register for the AES GCM of channels 4−7	13-37
0x08CC	CHANn_GCM_IV_LEN_VLD	GCM IV length validity signal register	13-37
0x08D0	CHANn_GCM_TAG_VLD	GCM tag validity signal register	13-38
0x08D4	CHANn_GCM_GHASH_A_END	GCM A calculation end signal register	13-38
0x0900 + 0x10 x *n* + 0x00	CHANn_GCM_TAG_0	GCM tag register 0 for channel *n*	13-39
0x0900 + 0x10 x *n* + 0x04	CHANn_GCM_TAG_1	GCM tag register 1 for channel *n*	13-39
0x0900 + 0x10 x *n* + 0x08	CHANn_GCM_TAG_2	GCM tag register 2 for channel *n*	13-40
0x0900 + 0x10 x *n* + 0x0C	CHANn_GCM_TAG_3	GCM tag register 3 for channel *n*	13-40
0x1000	CHAN0_CIPHER_CTRL	Encryption/decryption control register for channel 0	13-40
0x1004−0x1010	CHAN0_CIPHER_IVIN	Cipher VI block input register for channel 0	13-42
0x1014−0x1020	CHAN0_CIPHER_DIN	128-bit block input register of the cipher module	13-43
0x1000 + *n* x 0x80	CHANn_IBUF_NUM	Input queue total depth register for channel n (n = 1–7) (linked list header count register)	13-44
0x1000 + *n* x 0x80 + 0x4	CHANn_IBUF_CNT	Pending data buffer count register for channel n in the input queue	13-44
0x1000 + *n* x 0x80 + 0x8	CHANn_IEMPTY_CNT	Processed data buffer count register for channel n in the input queue	13-45
0x1000 + *n* x 0x80 + 0xC	CHANn_INT_ICNTCFG	Input queue multi-packet interrupt threshold register for channel n	13-45
0x1000 + *n* x 0x80 + 0x10	CHANn_CIPHER_CTRL	Encryption/decryption control register for channel n	13-46
0x1000 + *n* x 0x80 + 0x14	CHANn_SRC_LST_SADDR	Input queue start address register for channel n	13-48
0x1000 + *n* x 0x80 + 0x18	CHANn_IAGE_TIMER	Input queue interrupt aging time configuration register for channel n	13-48

Offset Address	Register	Description	Page
0x1000 + *n* x 0x80 + 0x3C	CHANn_OBUF_NUM	Output queue total depth register for channel n (linked list header count register)	13-49
0x1000 + *n* x 0x80 + 0x40	CHANn_OBUF_CNT	Pending data buffer count register for channel n in the output queue	13-49
0x1000 + *n* x 0x80 + 0x44	CHANn_OFULL_CNT	Processed data buffer count register for channel n in the output queue	13-50
0x1000 + *n* x 0x80 + 0x48	CHANn_INT_OCNTCFG	Output queue multi-packet interrupt threshold register for channel n	13-50
0x1000 + *n* x 0x80 + 0x4C	CHANn_DEST_LST_SADDR	Output queue start address register for channel n	13-50
0x1000 + *n* x 0x80 + 0x50	CHANn_OAGE_TIMER	Output queue interrupt aging time configuration register for channel n	13-51
0x1400	INT_STATUS	Interrupt status register	13-52
0x1404	INT_EN	Interrupt enable register	13-53
0x1408	INT_RAW	Raw interrupt status register	13-54
0x140C	RST_STATUS	Reset status indicator register	13-55
0x1410	CHAN0_CFG	Channel 0 configuration register	13-55

13.1.6 Register Description

CHAN0_CIPHER_DOUT

CHAN0_CIPHER_DOUT is a cipher output register for channel 0 (for single-block encryption/decryption).

The data read from this register is the results of a single-block operation. The results of the AES algorithm are different from those of the DES or 3DES algorithm. The details are as follows:

- For the AES algorithm
  - If the 1-CFB mode is selected, the least significant bit (LSB) is valid, that is, CIPHER_DOUT bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- For the DES or 3DES algorithm
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DOUT bit[0] is valid.

- If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DOUT bit[7:0] is valid.
- If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.
- In other modes, lower 64 bits are valid, that is, CIPHER_DOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0000–0x000C	CHAN0_CIPHER_DOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_dout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_dout	128-bit block output of the cipher module. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0000 CIPHER_DOUT[63:32]: address 0x0004 CIPHER_DOUT[95:64]: address 0x0008 CIPHER_DOUT[127:96]: address 0x000C

CHAN0_CIPHER_IVOUT

CHAN0_CIPHER_IVOUT is an operation complete IV output register of the cipher module.

Note the following points when reading this register:

- This register can be ignored in ECB or CTR mode.
- If a single-block operation is performed, the data of this register is the vector output of the block. The data can be used as the vector input in the next block operation for the same data packet.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected (CIPHER_CTRL[cipher_mode] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.
- If a multi-block operation is performed, the data read from this register is the output vector of the last block operation.
  - If the AES algorithm is selected, 128 bits are valid.
  - If the DES or 3DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_IVOUT bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x0010–0x001C	CHAN0_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivout																															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan0_cipher_ivout	Vector output after the operation of the cipher module is complete. It can be ignored in ECB or CTR mode. Each address maps to a 32-bit data segment. CIPHER_DOUT[31:0]: address 0x0010 CIPHER_IVOUT[63:32]: address 0x0014 CIPHER_IVOUT[95:64]: address 0x0018 CIPHER_IVOUT[127:96]: address 0x001C

CHAN_CIPHER_IVOUT

CHAN_CIPHER_IVOUT is an IV output register for channels 1–7.

Offset Address	Register Name	Total Reset Value
0x0020–0x008C	CHAN_CIPHER_IVOUT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan_cipher_ivout																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chan_cipher_ivout	0x0020–0x002C: channel 1 0x0030–0x003C: channel 2 0x0040–0x004C: channel 3 0x0050–0x005C: channel 4 0x0060–0x006C: channel 5 0x0070–0x007C: channel 6 0x0080–0x008C: channel 7

CIPHER_KEY

CIPHER_KEY is a CPU configuration key register of the cipher module. The key is the configured value of the CPU, and the CPU can be read or written.

Note the following points when configuring this register:

- If the DES algorithm is selected, lower 64 bits are valid, that is, CIPHER_KEY[63:0] is valid.
- For the 3DES algorithm

  If a 3-key operation is performed (CIPHER_CTRL[key_length] = 0b00, 0b01, or 0b10), low 192 bits are valid.

  where

- CIPHER_KEY bit[63:0] indicates key 1.
- CIPHER_KEY bit[127:64] indicates key 2.
- CIPHER_KEY bit[191:128] indicates key 3.

If a 2-key operation is selected (CIPHER_CTRL[key_length] = 0b11), lower 128 bits are valid.

where

- CIPHER_KEY bit[63:0] indicates key 1.
- CIPHER_KEY bit[127:64] indicates key 2.

- For the AES algorithm
  - If a 128-bit key operation is performed, lower 128 bits are valid, that is, CIPHER_KEY bit[127:0] is valid.
  - If a 192-bit key operation is performed, lower 192 bits are valid, that is, CIPHER_KEY bit[191:0] is valid.
  - If a 256-bit key operation is performed, 256 bits are valid.

The cipher module allows you to configure eight keys. Each channel can use one key, and multiple channels can share one key.

Offset Address	Register Name	Total Reset Value
0x0090–0x018C	CIPHER_KEY	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cipher_key																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	cipher_key	Key input of the cipher module. Each address maps to a 32-bit data segment. CIPHER_KEY[31:0]: address 0x0090 CIPHER_KEY[63:32]: address 0x0094 CIPHER_KEY[95:64]: address 0x0098 CIPHER_KEY[127:96]: address 0x009C CIPHER_KEY[159: 128]: address 0x00A0 CIPHER_KEY[191:160]: address 0x00A4 CIPHER_KEY[223:192]: address 0x00A8 CIPHER_KEY[255:224]: address 0x00AC 0x0090–0x00AC: host_key0 0x00B0–0x00CC: host_key1 0x00D0–0x00EC: host_key2 0x00F0–0x010C: host_key3 0x0110–0x012C: host_key4 0x0130–0x014C: host_key5 0x0150–0x016C: host_key6 0x0170–0x018C: host_key7

CHAN0_GCM_A_LEN_0

CHAN0_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0840	CHAN0_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 0 (unit: 8 bits)

CHAN0_GCM_A_LEN_1

CHAN0_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0844	CHAN0_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 0 (unit: 8 bits)

CHAN1_GCM_A_LEN_0

CHAN1_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x0848	CHAN1_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 1 (unit: 8 bits)

CHAN1_GCM_A_LEN_1

CHAN1_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x084C	CHAN1_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 1 (unit: 8 bits)

CHAN2_GCM_A_LEN_0

CHAN2_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0850	CHAN2_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 2 (unit: 8 bits)

CHAN2_GCM_A_LEN_1

CHAN2_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0854	CHAN2_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 2 (unit: 8 bits)

CHAN3_GCM_A_LEN_0

CHAN3_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x0858	CHAN3_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 3 (unit: 8 bits)

CHAN3_GCM_A_LEN_1

CHAN3_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x085C	CHAN3_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 3 (unit: 8 bits)

CHAN4_GCM_A_LEN_0

CHAN4_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x0860	CHAN1_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 4 (unit: 8 bits)

CHAN4_GCM_A_LEN_1

CHAN4_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x0864	CHAN4_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 4 (unit: 8 bits)

CHAN5_GCM_A_LEN_0

CHAN5_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x0868	CHAN5_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan5_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 5 (unit: 8 bits)

CHAN5_GCM_A_LEN_1

CHAN5_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x086C	CHAN5_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan5_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 5 (unit: 8 bits)

CHAN6_GCM_A_LEN_0

CHAN6_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x0870	CHAN6_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan6_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 6 (unit: 8 bits)

CHAN6_GCM_A_LEN_1

CHAN6_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x0874	CHAN6_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan6_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 6 (unit: 8 bits)

CHAN7_GCM_A_LEN_0

CHAN7_GCM_A_LEN_0 is an A length lower 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x0878	CHAN7_GCM_A_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_a_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_a_len_0	Lower 32 bits of the A length for the AES GCM of channel 7 (unit: 8 bits)

CHAN7_GCM_A_LEN_1

CHAN7_GCM_A_LEN_1 is an A length upper 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x087C	CHAN7_GCM_A_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_a_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_a_len_1	Upper 32 bits of the A length for the AES GCM of channel 7 (unit: 8 bits)

CHAN0_GCM_PC_LEN_0

CHAN0_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0880	CHAN0_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 0 (unit: 8 bits)

CHAN0_GCM_PC_LEN_1

CHAN0_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 0.

Offset Address	Register Name	Total Reset Value
0x0884	CHAN0_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 0 (unit: 8 bits)

CHAN1_GCM_PC_LEN_0

CHAN1_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x0888	CHAN1_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 1 (unit: 8 bits)

CHAN1_GCM_PC_LEN_1

CHAN1_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 1.

Offset Address	Register Name	Total Reset Value
0x088C	CHAN1_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan1_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan1_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 1 (unit: 8 bits)

CHAN2_GCM_PC_LEN_0

CHAN2_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0890	CHAN2_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 2 (unit: 8 bits)

CHAN2_GCM_PC_LEN_1

CHAN2_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 2.

Offset Address	Register Name	Total Reset Value
0x0894	CHAN2_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan2_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan2_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 2 (unit: 8 bits)

CHAN3_GCM_PC_LEN_0

CHAN3_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x0898	CHAN3_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 3 (unit: 8 bits)

CHAN3_GCM_PC_LEN_1

CHAN3_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 3.

Offset Address	Register Name	Total Reset Value
0x089C	CHAN3_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan3_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan3_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 3 (unit: 8 bits)

CHAN4_GCM_PC_LEN_0

CHAN4_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x08A0	CHAN4_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 4 (unit: 8 bits)

CHAN4_GCM_PC_LEN_1

CHAN4_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 4.

Offset Address	Register Name	Total Reset Value
0x08A4	CHAN4_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan4_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 4 (unit: 8 bits)

CHAN5_GCM_PC_LEN_0

CHAN5_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x08A8	CHAN5_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 5 (unit: 8 bits)

CHAN5_GCM_PC_LEN_1

CHAN5_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 5.

Offset Address	Register Name	Total Reset Value
0x08AC	CHAN5_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan5_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 5 (unit: 8 bits)

CHAN6_GCM_PC_LEN_0

CHAN6_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x08B0	CHAN6_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 6 (unit: 8 bits)

CHAN6_GCM_PC_LEN_1

CHAN6_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 6.

Offset Address	Register Name	Total Reset Value
0x08B4	CHAN6_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan6_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan6_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 6 (unit: 8 bits)

CHAN7_GCM_PC_LEN_0

CHAN7_GCM_PC_LEN_0 is a payload length lower 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x08B8	CHAN7_GCM_PC_LEN_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_pc_len_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_pc_len_0	Lower 32 bits of the payload length for the AES GCM of channel 7 (unit: 8 bits)

CHAN7_GCM_PC_LEN_1

CHAN7_GCM_PC_LEN_1 is a payload length upper 32 bits register for the AES GCM of channel 7.

Offset Address	Register Name	Total Reset Value
0x08BC	CHAN7_GCM_PC_LEN_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan7_gcm_pc_len_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan7_gcm_pc_len_1	Upper 32 bits of the payload length for the AES GCM of channel 7 (unit: 8 bits)

CHAN0_3_GCM_IV_LEN

CHAN0_3_GCM_IV_LEN is an IV length register for the AES GCM of channels 0−3.

Offset Address	Register Name	Total Reset Value
0x08C0	CHAN0_3_GCM_IV_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				chan3_gcm_iv_len				reserved				chan2_gcm_iv_len				reserved				chan1_gcm_iv_len				reserved				chan0_gcm_iv_len			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved

[28:24]	RW	chan3_gcm_iv_len	IV length of channel 3
[23:21]	RO	reserved	Reserved
[20:16]	RW	chan2_gcm_iv_len	IV length of channel 2
[15:13]	RO	reserved	Reserved
[12:8]	RW	chan1_gcm_iv_len	IV length of channel 1
[7:5]	RO	reserved	Reserved
[4:0]	RW	chan0_gcm_iv_len	IV length of channel 0

CHAN4_7_GCM_IV_LEN

CHAN4_7_GCM_IV_LEN is an IV length register for the AES GCM of channels 4−7.

Offset Address	Register Name	Total Reset Value
0x08C4	CHAN4_7_GCM_IV_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved				chan3_gcm_iv_len				reserved				chan2_gcm_iv_len				reserved				chan1_gcm_iv_len				reserved				chan0_gcm_iv_len			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:29]	RO	reserved	Reserved
[28:24]	RW	chan7_gcm_iv_len	IV length of channel 7
[23:21]	RO	reserved	Reserved
[20:16]	RW	chan6_gcm_iv_len	IV length of channel 6
[15:13]	RO	reserved	Reserved
[12:8]	RW	chan5_gcm_iv_len	IV length of channel 5
[7:5]	RO	reserved	Reserved
[4:0]	RW	chan4_gcm_iv_len	IV length of channel 4

CHANn_GCM_IV_LEN_VLD

CHANn_GCM_IV_LEN_VLD is a GCM IV length validity signal register.

Offset Address	Register Name	Total Reset Value
0x08CC	CHANn_GCM_IV_LEN_VLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								chann_gcm_iv_len_vld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RO	chann_gcm_iv_len_vld	Whether the IV length of channel *n* is valid after the operation is started in AES GCM mode 0: invalid (the channel length is 0 or greater than 16 bytes) 1: valid

CHANn_GCM_TAG_VLD

CHANn_GCM_TAG_VLD is a GCM tag validity signal register.

Offset Address	Register Name	Total Reset Value
0x08D0	CHANn_GCM_TAG_VLD	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								chann_gcm_tag_vld							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RWC	chann_gcm_tag_vld	Whether the tag of channel *n* is valid in AES GCM mode 0: invalid 1: valid. Writing 1 clears this field.

CHANn_GCM_GHASH_A_END

CHANn_GCM_GHASH_A_END is a GCM A calculation end signal register.

Offset Address	Register Name	Total Reset Value
0x08D4	CHANn_GCM_GHASH_A_END	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																								chann_gcm_ghash_a_end							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:8]	RO	reserved	Reserved
[7:0]	RWC	chann_gcm_ghash_a_end	Whether the ghash of channel *n* is finished when the A length is not 0 in AES GCM mode 1: finished. Writing 1 clears this field. 0: not finished

CHANn_GCM_TAG_0

CHANn_GCM_TAG_0 is GCM tag register 0 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x00	CHANn_GCM_TAG_0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_0	GCM tag[31:0] for channel *n*

CHANn_GCM_TAG_1

CHANn_GCM_TAG_1 is GCM tag register 1 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x04	CHANn_GCM_TAG_1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_1	GCM tag[63:32] for channel *n*

CHANn_GCM_TAG_2

CHANn_GCM_TAG_2 is GCM tag register 2 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x08	CHANn_GCM_TAG_2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_2	GCM tag[95:64] for channel *n*

CHANn_GCM_TAG_3

CHANn_GCM_TAG_3 is GCM tag register 3 for channel *n*.

Offset Address	Register Name	Total Reset Value
0x0900 + 0x10 x *n* + 0x04	CHANn_GCM_TAG_3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chann_gcm_tag_3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	chann_gcm_tag_3	GCM tag[127:96] for channel *n*

CHAN0_CIPHER_CTRL

CHAN0_CIPHER_CTRL is an encryption/decryption control register for channel 0. Channel 0 is a single-block encryption/decryption channel.

Note the following points when configuring this register:

- Configure this register before configuring others registers of the cipher module.
- In the modes except the CFB mode of the AES algorithm, the CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes except the CFB and OFB modes of the DES and 3DES algorithms, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000	CHAN0_CIPHER_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																key_adder				key_sel	reserved	reserved		key_length			ivin_sel	width			alg_sel	mode			decrypt
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:17]	RO	reserved	Reserved
[16:14]	RW	key_adder	ID of the key used by the current channel 000: host_key0 001: host_key1 010: host_key2 011: host_key3 100: host_key4 101: host_key5 110: host_key6 111: host_key7
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: keys generated by the key management module
[12]	RO	reserved	Reserved
[11]	RO	reserved	Reserved
[10:9]	RW	key_length	Key length select For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RW	ivin_sel	Input select of CIPHER_IVIN 0: do not configure CIPHER_IVIN 1: configure CIPHER_IVIN

[7:6]	RW	width	Bit width control For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm
[3:1]	RW	mode	Operating mode select For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select 0: encryption 1: decryption

CHAN0_CIPHER_IVIN

CHAN0_CIPHER_IVIN is a cipher VI block input register for channel 0.

Assume that channel 0 is selected for the single-block encryption/decryption and the selected mode is not ECB mode (CIPHER_CTRL[mode] = 0b001, 0b010, 0b011, or 0b100).

- If you do not want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b0), CIPHER_IVIN can be ignored.
- If you want to configure the input vector (CIPHER_CTRL[ivin_sel] = 0b1), CIPHER_IVIN needs to be configured. If the AES algorithm is selected (CIPHER_CTRL [alg_sel] = 0b10), CIPHER_IVIN bit[127:0] is valid. If the DES or 3DES algorithm is selected (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11), lower 64 bits are valid, that is, CIPHER_IVIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1004–0x1010	CHAN0_CIPHER_IVIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_ivin																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_ivin	128-bit IV of the cipher module for channel 0 or the data input from the counter. Each address maps to a 32-bit data segment. CIPHER_IVIN[31:0]: address 0x1004 CIPHER_IVIN[63:32]: address 0x1008 CIPHER_IVIN[95:64]: address 0x100C CIPHER_IVIN[127:96]: address 0x1010

CHAN0_CIPHER_DIN

CHAN0_CIPHER_DIN is a 128-bit block input register of the cipher module.

Note the following points when configuring this register:

- If channel 0 is selected for the single-block operation, this register needs to be configured.
- Assume that the AES algorithm (CIPHER_CTRL[alg_sel] = 0b10) is selected.
  - If the 1-CFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 128-CFB mode is selected, 128 bits are valid.
  - In other modes, 128 bits are valid.
- Assume that the DES or the 3DES algorithm (CIPHER_CTRL[alg_sel] = 0b00, 0b01, or 0b11) is selected.
  - If the 1-CFB or 1-OFB mode is selected, the LSB is valid, that is, CIPHER_DIN bit[0] is valid.
  - If the 8-CFB or 8-OFB mode is selected, lower eight bits are valid, that is, CIPHER_DIN bit[7:0] is valid.
  - If the 64-CFB or 64-OFB mode is selected, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.
  - In other modes, lower 64 bits are valid, that is, CIPHER_DIN bit[63:0] is valid.

Offset Address	Register Name	Total Reset Value
0x1014–0x1020	CHAN0_CIPHER_DIN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	chan0_cipher_din																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	chan0_cipher_din	128-bit block input of the cipher module for channel 0. Each address maps to a 32-bit data segment. CIPHER_DIN[31:0]: address 0x1014 CIPHER_DIN[63:32]: address 0x1018 CIPHER_DIN[95:64]: address 0x101c CIPHER_DIN[127:96]: address 0x1020

CHANn_IBUF_NUM

CHANn_IBUF_NUM is an input queue total depth register for channel *n* (*n* = 1–7). This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80	CHANn_IBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ibuf_num	Input queue depth, that is, count of linked list headers configured for each channel

CHANn_IBUF_CNT

CHANn_IBUF_CNT is a pending data buffer count register for channel *n* in the input queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x4	CHANn_IBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ibuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ibuf_cnt	Count of buffers to be processed in the input queue

CHANn_IEMPTY_CNT

CHANn_IEMPTY_CNT is a processed buffer count register for channel *n* in the input queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x8	CHANn_IEMPTY_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iempty_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	iempty_cnt	Count of processed buffers in the input queue

CHANn_INT_ICNTCFG

CHANn_INT_ICNTCFG is an input queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the input queue processed by the logic is above the threshold, an input queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0xC	CHANn_INT_ICNTCFG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				int_icnt_cfg			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	int_icnt_cfg	Input queue multi-packet interrupt threshold

CHANn_CIPHER_CTRL

CHANn_CIPHER_CTRL is an encryption/decryption control register for channel *n*.

Note the following points when configuring this register:

- You must configure this register before performing encryption or decryption using the channel.
- In the modes other than the CFB mode of the AES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.
- In the modes other than the CFB and OFB modes of the DES or 3DES algorithm, CIPHER_CTRL[width] cannot be set to 01 or 10.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x10	CHANn_CIPHER_CTRL	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	weight		reserved	key_adder	key_sel	byte_seq	ts_vld	key_length	reserved	width	alg_sel	mode	decrypt
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:22]	RO	weight	Weighted value of the current channel, in the unit of 64 bytes
[21:17]	RO	reserved	Reserved
[16:14]	RW	key_adder	ID of the key used by the current channel. The key can be any one in the addresses 0–7.
[13]	RW	key_sel	Key select 0: keys configured by the CPU 1: keys generated by the key management module
[12:11]	RO	reserved	Reserved

[10:9]	RW	key_length	Key length select For the AES algorithm: 00: 128 bits 01: 192 bits 10: 256 bits 11: 128 bits For the DES algorithm: 00: 3 keys 01: 3 keys 10: 3 keys 11: 2 keys
[8]	RO	reserved	Reserved
[7:6]	RW	width	Bit width control For the DES or 3DES algorithm: 00: 64 bits 01: 8 bits 10: 1 bit 11: 64 bits For the AES algorithm: 00: 128 bits 01: 8 bits 10: 1 bit 11: 128 bits
[5:4]	RW	alg_sel	Algorithm select 00: DES algorithm 01: 3DES algorithm 10: AES algorithm 11: DES algorithm

[3:1]	RW	mode	Operating mode select For the AES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode 100: CTR mode Other values: ECB mode For the DES algorithm: 000: ECB mode 001: CBC mode 010: CFB mode 011: OFB mode Other values: ECB mode
[0]	RW	decrypt	Encryption/decryption select 0: encryption 1: decryption

CHANn_SRC_LST_SADDR

CHANn_SRC_LST_SADDR is an input queue start address register for channel n. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x14	CHANn_SRC_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	src_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	src_lst_saddr	Start address for the input queue

CHANn_IAGE_TIMER

CHANn_IAGE_TIMER is an input queue interrupt aging time configuration register for channel *n*. If overflow occurs in the aging time counter and the count of processed buffers in the input queue is greater than 0, an input queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x18	CHANn_IAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																iage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	iage_timer	Aging interrupt timer

CHANn_OBUF_NUM

CHANn_OBUF_NUM is an output queue total depth register for channel *n*. This register can be used to configure the count of linked list headers.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x3C	CHANn_OBUF_NUM	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_num															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	obuf_num	Total depth of the output queue

CHANn_OBUF_CNT

CHANn_OBUF_CNT is a pending data buffer count register for channel *n* in the output queue. When this register is written by using software, the logic adds the original value of the register and the written value. After the logic processes a buffer, the value of this register is decreased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x40	CHANn_OBUF_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																obuf_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved

[15:0]	RW	obuf_cnt	Count of buffers to be processed in the output queue

CHANn_OFULL_CNT

CHANn_OFULL_CNT is a processed buffer count register for channel *n* in the output queue. When this register is written by software, the logic subtracts the written value from the original value of this register. After the logic processes a buffer, the value of this register is increased by 1.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x44	CHANn_OFULL_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ofull_cnt																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	ofull_cnt	Count of processed buffers in the output queue

CHANn_INT_OCNTCFG

CHANn_INT_OCNTCFG is an output queue multi-packet interrupt threshold register for channel *n*. When the count of buffers in the output queue processed by the logic is above the threshold, an output queue interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x48	CHANn_INT_OCNTCFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																int_ocnt_cfg																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	int_ocnt_cfg	Output queue multi-packet interrupt threshold

CHANn_DEST_LST_SADDR

CHANn_DEST_LST_SADDR is an output queue start address register for channel *n*. The address must be aligned by word.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x4C	CHANn_DEST_LST_SADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dest_lst_saddr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dest_lst_saddr	Start address for the output queue

CHANn_OAGE_TIMER

CHANn_OAGE_TIMER is an output queue interrupt aging time configuration register for channel *n*. If overflow occurs in the aging time counter and the count of processed buffers in the output queue is greater than 0, an output queue processing complete interrupt is reported.

Offset Address	Register Name	Total Reset Value
0x1000 + *n* x 0x80 + 0x50	CHANn_OAGE_TIMER	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																oage_timer															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RW	oage_timer	Aging interrupt timer

INT_STATUS

INT_STATUS is an interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1400	INT_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_ibuf_int	ch6_ibuf_int	ch5_ibuf_int	ch4_ibuf_int	ch3_ibuf_int	ch2_ibuf_int	ch1_ibuf_int	ch0_ibuf_int	ch7_obuf_int	ch6_obuf_int	ch5_obuf_int	ch4_obuf_int	ch3_obuf_int	ch2_obuf_int	ch1_obuf_int	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RO	ch7_ibuf_int	Input queue data interrupt for channel 7
[14]	RO	ch6_ibuf_int	Input queue data interrupt for channel 6
[13]	RO	ch5_ibuf_int	Input queue data interrupt for channel 5
[12]	RO	ch4_ibuf_int	Input queue data interrupt for channel 4
[11]	RO	ch3_ibuf_int	Input queue data interrupt for channel 3
[10]	RO	ch2_ibuf_int	Input queue data interrupt for channel 2
[9]	RO	ch1_ibuf_int	Input queue data interrupt for channel 1
[8]	RO	ch0_ibuf_int	Data processing complete interrupt for channel 0
[7]	RO	ch7_obuf_int	Output queue data interrupt for channel 7
[6]	RO	ch6_obuf_int	Output queue data interrupt for channel 6
[5]	RO	ch5_obuf_int	Output queue data interrupt for channel 5
[4]	RO	ch4_obuf_int	Output queue data interrupt for channel 4
[3]	RO	ch3_obuf_int	Output queue data interrupt for channel 3
[2]	RO	ch2_obuf_int	Output queue data interrupt for channel 2
[1]	RO	ch1_obuf_int	Output queue data interrupt for channel 1
[0]	RO	reserved	Reserved

INT_EN

INT_EN is an interrupt enable register.

Offset Address	Register Name	Total Reset Value
0x1404	INT_EN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	int_en	reserved															ch7_ibuf_en	ch6_ibuf_en	ch5_ibuf_en	ch4_ibuf_en	ch3_ibuf_en	ch2_ibuf_en	ch1_ibuf_en	ch0_ibuf_en	ch7_obuf_en	ch6_obuf_en	ch5_obuf_en	ch4_obuf_en	ch3_obuf_en	ch2_obuf_en	ch1_obuf_en	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RW	int_en	Total interrupt enable for the cipher module
[30:16]	RO	reserved	Reserved
[15]	RW	ch7_ibuf_en	Input queue data interrupt enable for channel 7
[14]	RW	ch6_ibuf_en	Input queue data interrupt enable for channel 6
[13]	RW	ch5_ibuf_en	Input queue data interrupt enable for channel 5
[12]	RW	ch4_ibuf_en	Input queue data interrupt enable for channel 4
[11]	RW	ch3_ibuf_en	Input queue data interrupt enable for channel 3
[10]	RW	ch2_ibuf_en	Input queue data interrupt enable for channel 2
[9]	RW	ch1_ibuf_en	Input queue data interrupt enable for channel 1
[8]	RW	ch0_ibuf_en	Data processing complete interrupt enable for channel 0
[7]	RW	ch7_obuf_en	Output queue data interrupt enable for channel 7
[6]	RW	ch6_obuf_en	Output queue data interrupt enable for channel 6
[5]	RW	ch5_obuf_en	Output queue data interrupt enable for channel 5
[4]	RW	ch4_obuf_en	Output queue data interrupt enable for channel 4
[3]	RW	ch3_obuf_en	Output queue data interrupt enable for channel 3
[2]	RW	ch2_obuf_en	Output queue data interrupt enable for channel 2
[1]	RW	ch1_obuf_en	Output queue data interrupt enable for channel 1
[0]	RO	reserved	Reserved

INT_RAW

INT_RAW is a raw interrupt status register.

Offset Address	Register Name	Total Reset Value
0x1408	INT_RAW	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																ch7_obuf_raw	ch6_obuf_raw	ch5_obuf_raw	ch4_obuf_raw	ch3_obuf_raw	ch2_obuf_raw	ch1_obuf_raw	ch0_ibuf_raw	ch7_ibuf_raw	ch6_ibuf_raw	ch5_ibuf_raw	ch4_ibuf_raw	ch3_ibuf_raw	ch2_ibuf_raw	ch1_ibuf_raw	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15]	RWC	ch7_obuf_raw	Raw output queue data interrupt for channel 7
[14]	RWC	ch6_obuf_raw	Raw output queue data interrupt for channel 6
[13]	RWC	ch5_obuf_raw	Raw output queue data interrupt for channel 5
[12]	RWC	ch4_obuf_raw	Raw output queue data interrupt for channel 4
[11]	RWC	ch3_obuf_raw	Raw output queue data interrupt for channel 3
[10]	RWC	ch2_obuf_raw	Raw output queue data interrupt for channel 2
[9]	RWC	ch1_obuf_raw	Raw output queue data interrupt for channel 1
[8]	RWC	ch0_ibuf_raw	Raw data processing complete interrupt for channel 0
[7]	RWC	ch7_ibuf_raw	Raw input queue data interrupt for channel 7
[6]	RWC	ch6_ibuf_raw	Raw input queue data interrupt for channel 6
[5]	RWC	ch5_ibuf_raw	Raw input queue data interrupt for channel 5
[4]	RWC	ch4_ibuf_raw	Raw input queue data interrupt for channel 4
[3]	RWC	ch3_ibuf_raw	Raw input queue data interrupt for channel 3
[2]	RWC	ch2_ibuf_raw	Raw input queue data interrupt for channel 2
[1]	RWC	ch1_ibuf_raw	Raw input queue data interrupt for channel 1
[0]	RO	reserved	Reserved

RST_STATUS

RST_STATUS is a reset status indicator register.

Offset Address	Register Name	Total Reset Value
0x140C	RST_STATUS	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															rst_status
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	rst_status	Reset status indicator of the cipher module 0: The cipher module is being reset. 1: The cipher module is working properly.

CHAN0_CFG

CHAN0_CFG is channel 0 configuration register.

Offset Address	Register Name	Total Reset Value
0x1410	CHAN0_CFG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														ch0_busy	ch0_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	ch0_busy	Status signal of channel 0
[0]	RW	ch0_start	Encryption/Decryption start signal of channel 0

13.2 HASH

13.2.1 Overview

The hash is a module for implementing the SHA1, SHA256, HMAC_SHA1, and HMAC_SHA256 algorithms. The SHA1 and SHA256 algorithms comply with the FIPS 180-2 standard. The HMAC_SHA1 and HMAC_SHA256 algorithms comply with the RFC2104 standard.

The hash module can be used to authenticate data integrity and construct digital signatures.

13.2.2 Features

The hash module has the following features:

- Supports the SHA1, SHA256, HMAC_SHA1, and HMAC_SHA256 algorithms.
- Supports the input data configured by the CPU and read operation in DMA mode.
- Supports block-aligned total length of the input data (padded by software), that is, a multiple of 64 bytes. The total length is configured by software and the maximum value is $(2^{64} – 64)$ bytes. The message length after padding (by software) is used as the configured data length for the SHA1 and SHA256 algorithms, and the (padded message length + 64 bytes) is used as the configured data length for the HMAC_SHA1 and HMAC_SHA256 algorithms.
- Supports the 128-bit HMAC key configured by hardware (OTP Key Ctrl) or software.
- Supports configurable initial values for the SHA1 and SHA256 algorithms.

13.2.3 Function Description

The hash module is used to authenticate data integrity and construct digital signatures. The hash module can be set to the initial value update mode (the initial value needs to be configured in this mode) or non-initial value update mode by software. Then the message digest can be calculated by using the SHA1 or SHA256 algorithm. Software can start the HMAC_SHA1 or HMAC_SHA256 algorithm to calculate the MAC. The initial value cannot be configured.

13.2.4 Operating Mode

SHA1 Operation Process in CPU Mode

The CPU configures the input data. An SHA1 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[read_ctrl] to 1 and HASH_CTRL[sha_sel], HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 4 and step 5 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

SHA1 Operation Process in DMA Mode

The DMA reads the input data. An SHA1 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[read_ctrl], HASH_CTRL[sha_sel], HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

SHA256 Operation Process in CPU Mode

The CPU configures the input data. An SHA256 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[read_ctrl] and HASH_CTRL[sha_sel] to 1 and HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 4 and step 5 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

SHA256 Operation Process in DMA Mode

The DMA reads the input data. An SHA256 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel] to 1 and HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], HASH_CTRL[hardkey_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0. Set HASH_CTRL[sha_init_update_en] to 1 if the initial value needs to be updated.

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

HMAC_SHA1 Operation Process in CPU Mode

The CPU configures the input data. An HMAC_SHA1 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel], HASH_CTRL[small_end_en], and HASH_CTRL[sha_init_update_en] to 0 and HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], and HASH_CTRL[hardkey_sel] to 1 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 4 and step 5 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

HMAC_SHA1 Operation Process in DMA Mode

The DMA reads the input data. An HMAC_SHA1 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel], HASH_CTRL[small_end_en], HASH_CTRL[sha_init_update_en], HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], and HASH_CTRL[hardkey_sel] to 0 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT5[sha_out5]; if no, wait.

----End

HMAC_SHA256 Operation Process in CPU Mode

The CPU configures the input data. An HMAC_SHA256 operation in CPU mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[small_end_en] and HASH_CTRL[sha_init_update_en] to 0 and HASH_CTRL[read_ctrl], HASH_CTRL[sha_sel], HASH_CTRL[hmac_flag], and HASH_CTRL[hardkey_sel] to 1 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DATA_IN[data_in] by using the CPU.

Step 7 Repeat step 5 and step 6 until all the data required for calculation is input.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

HMAC_SHA256 Operation Process in DMA Mode

The DMA reads the input data. An HMAC_SHA256 operation in DMA mode is performed as follows:

Step 1 Check whether HASH_STATUS[hash_rdy] is 1. If yes, there is no calculation currently; if no, wait until the calculation is complete.

Step 2 Configure TOTAL_LEN1[total_len1] and TOTAL_LEN2[total_len2]. The configured message length must be 64-byte-aligned.

Step 3 Set HASH_CTRL[sha_sel] to 1 and HASH_CTRL[read_ctrl], HASH_CTRL[hmac_flag], HASH_CTRL[small_end_en], HASH_CTRL[sha_init_update_en], and HASH_CTRL[hardkey_sel] to 0 (the Cipher Hash Key Ctrl must first configure the key. If HASH_CTRL[hardkey_sel] is 0, the CPU must configure MCU_KEY0−3[mcu_key0−3]).

Step 4 Configure SHA_START[sha_start].

Step 5 Check whether HASH_STATUS[rec_rdy] is 1. If yes, go to the next step; if no, wait.

Step 6 Configure DMA_START_ADDR[dma_start_addr] by using the CPU.

Step 7 Configure DMA_LEN[dma_len] by using the CPU.

Step 8 Check whether HASH_STATUS[hash_rdy] is 1. If yes, read the calculation results from SHA_OUT1[sha_out1] to SHA_OUT8[sha_out8]; if no, wait.

----End

Clock Gating

When the hash calculation is not required, you can disable the clock of the hash module to reduce power consumption by configuring the system controller register.

Soft Reset

You can soft-rest the hash module by configuring the system controller register.

13.2.5 Register Summary

Table 13-2 describes hash registers.

Table 13-2 Summary of hash registers (base address: 0x1009_0000)

Offset Address	Register	Description	Page
0x0	TOTAL_LEN1	Hash message total length register (lower 32 bits)	13-62
0x4	TOTAL_LEN2	Hash message total length register (upper 32 bits)	13-62
0x8	HASH_STATUS	Status register	13-62
0xC	HASH_CTRL	Control register	13-63

Offset Address	Register	Description	Page
0x10	SHA_START	Calculation start register	13-64
0x14	DMA_START_ADDR	Read message start address register	13-65
0x18	DMA_LEN	DMA transfer length register	13-65
0x1C	DATA_IN	Input data register	13-66
0x20	REC_LEN1	RX message length register 1	13-66
0x24	REC_LEN2	RX message length register 2	13-67
0x30	SHA_OUT1	Hash output register 1	13-67
0x34	SHA_OUT2	Hash output register 2	13-67
0x38	SHA_OUT3	Hash output register 3	13-68
0x3C	SHA_OUT4	Hash output register 4	13-68
0x40	SHA_OUT5	Hash output register 5	13-68
0x44	SHA_OUT6	Hash output register 6	13-69
0x48	SHA_OUT7	Hash output register 7	13-69
0x4C	SHA_OUT8	Hash output register 8	13-70
0x70	MCU_KEY0	Key 0 (configured by MCU) register	13-70
0x74	MCU_KEY1	Key 1 (configured by MCU) register	13-70
0x78	MCU_KEY2	Key 2 (configured by MCU) register	13-71
0x7C	MCU_KEY3	Key 3 (configured by MCU) register	13-71
0x90	SHA_INIT1_UPDATE	SHA initial value register 1	13-71
0x94	SHA_INIT2_UPDATE	SHA initial value register 2	13-72
0x98	SHA_INIT3_UPDATE	SHA initial value register 3	13-72
0x9C	SHA_INIT4_UPDATE	SHA initial value register 4	13-72
0xA0	SHA_INIT5_UPDATE	SHA initial value register 5	13-73
0xA4	SHA_INIT6_UPDATE	SHA initial value register 6	13-73
0xA8	SHA_INIT7_UPDATE	SHA initial value register 7	13-73

Offset Address	Register	Description	Page
0xAC	SHA_INIT8_UPDATE	SHA initial value register 8	13-74

13.2.6 Register Description

TOTAL_LEN1

TOTAL_LEN1 is a hash message total length register (lower 32 bits).

Offset Address	Register Name	Total Reset Value
0x0	TOTAL_LEN1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_len1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	total_len1	SHA: lower bits of the padded message length (in byte) HMAC: lower bits of the length (in byte) of (i_key_pad + padded message)

TOTAL_LEN2

TOTAL_LEN2 is a hash message total length register (upper 32 bits).

Offset Address	Register Name	Total Reset Value
0x4	TOTAL_LEN2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	total_len2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	total_len2	SHA: upper bits of the padded message length (in byte) HMAC: upper bits of the length (in byte) of (i_key_pad + padded message)

HASH_STATUS

HASH_STATUS is an HASH status register.

Offset Address	Register Name	Total Reset Value
0x8	HASH_STATUS	0x0000_000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									error_state				rec_rdy	msg_rdy	dma_rdy	hash_rdy
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RO	len_err	Length correctness flag 0: correct 1: incorrect
[5:4]	RO	error_state	AHB bus status err_state[4] 0: No error occurs on the AHB. 1: An error occurs on the AHB. err_state[5] 0: The AHB slave is idle. 1: The AHB slave is busy.
[3]	RO	rec_rdy	Data RX ready flag for the internal logic (reg_rdy = msg_rdy & dma_rdy) 0: not ready 1: ready
[2]	RO	msg_rdy	Block calculation debugging information 0: The CPU channel is not ready to receive data. 1: The CPU channel is ready to receive data.
[1]	RO	dma_rdy	DMA debugging information 0: A data block is not completely read in DMA mode. 1: A data block is completely read in DMA mode.
[0]	RO	hash_rdy	TOTAL_LEN calculation completion signal 0: The calculation is not complete. 1: The calculation is complete.

HASH_CTRL

HASH_CTRL is an HASH control register.

Offset Address	Register Name	Total Reset Value
0xC	HASH_CTRL	0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									sha_init_update_en	small_end_en	hardkey_sel	hmac_flag	sha_sel		read_ctrl
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	sha_init_update_en	SHA initial value update enable. This bit is set to 0 for HMAC. 0: disabled. The default SHA initial value is used. 1: enabled. The value of sha_initn_update is used as the initial value when the SHA calculation starts.
[5]	RW	small_end_en	Word reverse order enable 0: big-endian mode 1: little-endian mode
[4]	RW	hardkey_sel	HMAC key select. This bit is set to 0 for the SHA. 0: kl_key (hardware key) 1: MCU key (software key)
[3]	RW	hmac_flag	Calculation mode select 0: SHA calculation 1: HMAC calculation
[2:1]	RW	sha_sel	Hash mode control 00: SHA1 mode 01: SHA256 mode Other values: reserved, Currently this field can be set to only 00 or 01.
[0]	RW	read_ctrl	Message transfer mode control 0: The message is read by the DMA. 1: The message is read by the CPU.

SHA_START

SHA_START is an SHA computing start register.

Offset Address	Register Name	Total Reset Value
0x10	SHA_START	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sha_start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	sha_start	Hash calculation start signal 0: not start 1: start

DMA_START_ADDR

DMA_START_ADDR is a read message start address register.

Offset Address	Register Name	Total Reset Value
0x14	DMA_START_ADDR	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dma_start_addr																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	dma_start_addr	Byte address. The address must be configured as word-aligned by software.

DMA_LEN

DMA_LEN is a DMA transfer length register.

Offset Address	Register Name	Total Reset Value
0x18	DMA_LEN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	segment_len1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	segment_len1	DMA transfer length (in byte), which must be word-aligned After the length is configured, data is read and calculated automatically by the internal logic.

DATA_IN

DATA_IN is an SHA computing input data register.

Offset Address	Register Name	Total Reset Value
0x1C	DATA_IN	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	data_in																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	data_in	The input data of the message digest needs to be determined through SHA computing, and the input data is configured by the CPU.

REC_LEN1

REC_LEN1 is RX message length register 1.

Offset Address	Register Name	Total Reset Value
0x20	REC_LEN1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	receive_byte_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	receive_byte_cnt	Number of bytes calculated by the hash module (64 bytes for each block). This register is cleared when the calculation starts.

REC_LEN2

REC_LEN2 is RX message length register 2.

Offset Address	Register Name	Total Reset Value
0x24	REC_LEN2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	receive_byte_cnt																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	receive_byte_cnt	Number of bytes calculated by the hash module (64 bytes for each block). This register is cleared when the calculation starts.

SHA_OUT1

SHA_OUT1 is hash output result register 1.

Offset Address	Register Name	Total Reset Value
0x30	SHA_OUT1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out1	Bits 0−31 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT2

SHA_OUT2 is hash output result register 2.

Offset Address	Register Name	Total Reset Value
0x34	SHA_OUT2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out2	Bits 32−63 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT3

SHA_OUT3 is hash output result register 3.

Offset Address	Register Name	Total Reset Value
0x38	SHA_OUT3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out3	Bits 64−95 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT4

SHA_OUT4 is hash output result register 4.

Offset Address	Register Name	Total Reset Value
0x3C	SHA_OUT4	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out4																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out4	Bits 96−127 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT5

SHA_OUT5 is hash output result register 5.

Offset Address	Register Name	Total Reset Value
0x40	SHA_OUT5	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out5																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out5	Bits 128−159 of the SHA1/SHA256 message digest output The reset terminal is removed, and the initial value is random.

SHA_OUT6

SHA_OUT6 is hash output result register 6.

Offset Address	Register Name	Total Reset Value
0x44	SHA_OUT6	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out6																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out6	This register does not apply to SHA1. This field indicates bits 160−191 of the SHA256 message digest output.

SHA_OUT7

SHA_OUT7 is hash output result register 7.

Offset Address	Register Name	Total Reset Value
0x48	SHA_OUT7	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out7																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out7	This register does not apply to SHA1. This field indicates bits 192−223 of the SHA256 message digest output.

SHA_OUT8

SHA_OUT8 is hash output result register 8.

Offset Address	Register Name	Total Reset Value
0x4C	SHA_OUT8	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_out8																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sha_out8	This register does not apply to SHA1. This field indicates bits 224−255 of the SHA256 message digest output.

MCU_KEY0

MCU_KEY0 is an HMAC input key register (bits 0−31, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x70	MCU_KEY0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	mcu_key0	HMAC input key register (bits 0−31, configured by the CPU) Reading this register returns 0.

MCU_KEY1

MCU_KEY1 is an HMAC input key register (bits 32−63, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x74	MCU_KEY1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	mcu_key1	HMAC input key register (bits 32−63, configured by the CPU) Reading this register returns 0.

MCU_KEY2

MCU_KEY2 is an HMAC input key register (bits 64−95, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x78	MCU_KEY2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	mcu_key2	HMAC input key register (bits 64−95, configured by the CPU) Reading this register returns 0.

MCU_KEY3

MCU_KEY3 is an HMAC input key register (bits 96−127, configured by the CPU).

Offset Address	Register Name	Total Reset Value
0x7C	MCU_KEY3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	mcu_key3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	mcu_key3	HMAC input key register (bits 96−127, configured by the CPU) Reading this register returns 0.

SHA_INIT1_UPDATE

SHA_INIT1_UPDATE is SHA initial value register 1.

Offset Address	Register Name	Total Reset Value
0x90	SHA_INIT1_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init1_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init1_update	SHA initial value (bits 0−31)

SHA_INIT2_UPDATE

SHA_INIT2_UPDATE is SHA initial value register 2.

Offset Address	Register Name	Total Reset Value
0x94	SHA_INIT2_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init2_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init2_update	SHA initial value (bits 32−63)

SHA_INIT3_UPDATE

SHA_INIT3_UPDATE is SHA initial value register 3.

Offset Address	Register Name	Total Reset Value
0x98	SHA_INIT3_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init3_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init3_update	SHA initial value (bits 64−95)

SHA_INIT4_UPDATE

SHA_INIT4_UPDATE is SHA initial value register 4.

Offset Address	Register Name	Total Reset Value
0x9C	SHA_INIT4_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init4_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init4_update	SHA initial value (bits 96−127)

SHA_INIT5_UPDATE

SHA_INIT5_UPDATE is SHA initial value register 5.

Offset Address	Register Name	Total Reset Value
0xA0	SHA_INIT5_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init5_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init5_update	SHA initial value (bits 128−159)

SHA_INIT6_UPDATE

SHA_INIT6_UPDATE is SHA initial value register 6.

Offset Address	Register Name	Total Reset Value
0xA4	SHA_INIT6_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init6_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init6_update	SHA initial value (bits 160−191)

SHA_INIT7_UPDATE

SHA_INIT7_UPDATE is SHA initial value register 7.

Offset Address	Register Name	Total Reset Value
0xA8	SHA_INIT7_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init7_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init7_update	SHA initial value (bits 192−223)

SHA_INIT8_UPDATE

SHA_INIT8_UPDATE is SHA initial value register 8.

Offset Address	Register Name	Total Reset Value
0xAC	SHA_INIT8_UPDATE	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sha_init8_update																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RW	sha_init8_update	SHA initial value (bits 224−255)

13.3 HISEC_TRNG_CTRL

13.3.1 Overview

HISEC_TRNG_CTRL is a module that generates true random numbers in compliance with the FIPS 140-1 random test standard.

13.3.2 Features

The HISEC_TRNG_CTRL module has the following features:

- Generates true random numbers.
- Supports three random number sources that can be configured by the CPU.
- Disables the random number sources.

13.3.3 Operating Mode

HISEC_TRNG_CTRL Operation Process

The HISEC_TRNG_CTRL operation process is as follows:

Step 1 Check whether HISEC_COM_TRNG_DATA_ST[trng_fifo_data_cnt] is greater than or equal to 1. If yes, go to the next step because there are random numbers; if no, wait.

Step 2 Read HISEC_COM_TRNG_FIFO_DATA[trng_fifo_data].

Step 3 Repeat step 1 and step 2 until the required number of random numbers are read.

----End

13.3.4 Register Summary

Table 13-3 describes HISEC_TRNG_CTRL registers.

Table 13-3 Summary of HISEC_TRNG_CTRL registers (base address: 0x120C_0000)

Offset Address	Register	Description	Page
0x0200	HISEC_COM_TRNG_CTRL	TRNG control register	13-76
0x0204	HISEC_COM_TRNG_FIFO_DATA	TRNG FIFO data register	13-77
0x0208	HISEC_COM_TRNG_DATA_ST	TRNG FIFO data register status register	13-77
0x020C	HISEC_COM_TRNG_ERR0_CNT	Count register for the number of times that data is detected as all 0s during RNG random number exception detection	13-78
0x0210	HISEC_COM_TRNG_ERR1_CNT	Count register for the number of times that data is detected as all 1s during RNG random number exception detection	13-79
0x0214	HISEC_COM_TRNG_ERR2_CNT	Count register for the number of times that the adjacent data segments are the same during RNG random number exception detection	13-79
0x0218	HISEC_COM_TRNG_ERR3_CNT	Count register for the number of times that the lower 32 bits of the adjacent 256-bit data are the same during RNG random number exception detection	13-79

13.3.5 Register Description

HISEC_COM_TRNG_CTRL

HISEC_COM_TRNG_CTRL is a TRNG control register.

Offset Address	Register Name	Total Reset Value
0x0200	HISEC_COM_TRNG_CTRL	0x0000_000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved														trng_cfg_lock	trng_sel	post_process_depth								post_process_enable	mix_enable	drop_enable	pre_process_enable	drbg_enable	cleardata	osc_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Bits	Access	Name	Description
[31:18]	RO	reserved	Reserved
[17]	RW	trng_cfg_lock	Lock signal of the trng_ctrl configuration (HISEC_COM_TRNG_CTRL[16:0]). The value 0 cannot be written after 1 is written. This bit can be reset only during the global reset. 0: unlocked 1: locked
[16]	RW	trng_sel	Output of the entropy source TRNG 0: The HiSilicon OSC analog random source data is selected for output. 1: The RO random source data is selected for output.
[15:8]	RW	post_process_depth	Post-processing mixing depth. A larger value indicates a better random effect and lower speed.
[7]	RW	post_process_enable	Pre-processing enable for the random number. If this function is enabled, the random number generation speed is decreased by the multiple of (post_process_depth + 1). 0: disabled 1: enabled
[6]	RW	mix_enable	Data mixing 0: disabled 1: enabled

[5]	RW	drop_enable	Enable for discarding data at different probabilities. If this function is enabled, the random number generation speed is decreased by 1/3. 0: disabled 1: enabled
[4]	RW	pre_process_enable	Pre-processing enable for the random number. If this function is enabled, the random number generation speed is decreased by 1/4. 0: disabled 1: enabled
[3]	RW	drbg_enable	DRBG post-processing enable 0: disabled 1: enabled
[2]	WC	cleardata	Writing 1 to this bit clears the random numbers in the FIFO.
[1:0]	RW	osc_sel	Random number source select 00: RNG is disabled. 01: Random number source 1 is used. 10: Random number source 2 is used. 11: Random number source 3 is used.

HISEC_COM_TRNG_FIFO_DATA

HISEC_COM_TRNG_FIFO_DATA is a TRNG FIFO data register.

Offset Address	Register Name	Total Reset Value
0x0204	HISEC_COM_TRNG_FIFO_DATA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	trng_fifo_data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	trng_fifo_data	The external interface can directly read this register, and the 32-bit data in the FIFO is returned.

HISEC_COM_TRNG_DATA_ST

HISEC_COM_TRNG_DATA_ST is a TRNG FIFO data register status register.

Offset Address	Register Name	Total Reset Value
0x0208	HISEC_COM_TRNG_DATA_ST	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3	2	1	0
Name	reserved				trng_fifo_data_cnt		reserved	low_ro_st1	low_ro_st0	low_osc_st1	low_osc_st0
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:8]	RO	trng_fifo_data_cnt	Number of random numbers in the FIFO
[7:4]	RO	reserved	Reserved
[3]	WC	low_ro_st1	If this bit is 1, the low-frequency oscillator clock always outputs 1 (there are 512 consecutive 1s in the hardware RO source during system clock detection). Writing this bit clears it.
[2]	WC	low_ro_st0	If this bit is 1, the low-frequency oscillator clock always outputs 0 (there are 512 consecutive 0s in the hardware RO source during system clock detection). Writing this bit clears it.
[1]	WC	low_osc_st1	If this bit is 1, the low-frequency oscillator clock always outputs 1. Writing this bit clears it.
[0]	WC	low_osc_st0	If this bit is 1, the low-frequency oscillator clock always outputs 0. Writing this bit clears it.

HISEC_COM_TRNG_ERR0_CNT

HISEC_COM_TRNG_ERR0_CNT is a count register for the number of times that data is detected as all 0s during RNG random number exception detection.

Offset Address	Register Name	Total Reset Value
0x020C	HISEC_COM_TRNG_ERR0_CNT	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	reserved				rng_err0_cnt			
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	rng_err0_cnt	Number of times that data is detected as all 0s during RNG random number exception detection

HISEC_COM_TRNG_ERR1_CNT

HISEC_COM_TRNG_ERR1_CNT is a count register for the number of times that data is detected as all 1s during RNG random number exception detection.

Offset Address	Register Name	Total Reset Value
0x0210	HISEC_COM_TRNG_ERR1_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rng_err1_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	rng_err1_cnt	Number of times that data is detected as all 1s during RNG random number exception detection

HISEC_COM_TRNG_ERR2_CNT

HISEC_COM_TRNG_ERR2_CNT is a count register for the number of times that the adjacent data segments are the same during RNG random number exception detection.

Offset Address	Register Name	Total Reset Value
0x0214	HISEC_COM_TRNG_ERR2_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rng_err2_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	rng_err2_cnt	Number of times that the adjacent data segments are the same during RNG random number exception detection

HISEC_COM_TRNG_ERR3_CNT

HISEC_COM_TRNG_ERR3_CNT is a count register for the number of times that the lower 32 bits of the adjacent 256-bit data are the same during RNG random number exception detection.

Offset Address	Register Name	Total Reset Value
0x0218	HISEC_COM_TRNG_ERR3_CNT	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																rng_err3_cnt															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	rng_err3_cnt	Number of times that the lower 32 bits of the adjacent 256-bit data are the same during RNG random number exception detection

13.4 RSA

13.4.1 Overview

The Rivest-Shamir-Adleman (RSA) is a public key encryption/decryption algorithm implemented through the modular exponentiation operation. The ciphertext is obtained as follows: $C = M^E \bmod N$. The plaintext is obtained as follows: $M=C^D \bmod N$. *M* indicates the plaintext, *C* indicates the ciphertext, *(N, E)* indicates the public key, and *(N, D)* indicates the private key.

The RSA module supports RSA 1024, RSA 2048, and RSA 4096 that comply with the PKCS#1 V1.5/2.1 standard.

The RSA module is used for data encryption/decryption and digital signature verification.

13.4.2 Features

The RSA module has the following features:

- Supports 1024-bit, 2048-bit, and 4096-bit keys.
- Supports the minimum performance of 10 operations per second (OPS) for the 2048-bit key.
- Supports key debugging by using CRC16.
- Clears the random access memories (RAMs) that store the internal RSA keys, packets, and results.

13.4.3 Function Description

The RSA module is used for data encryption/decryption and digital signature verification. The registers are configured by software. Then the RSA module is started to implement the modular exponentiation operation. The RSA module also uses CRC16 to calculate the key stored in the logic and outputs the result for checking whether the key is correct. The RSA module also clears the RAMs that store the internal keys, packets, and results.

13.4.4 Operating Mode

Encrypting/Decrypting Data by Using RSA

Data is encrypted/decrypted by using RSA as follows:

Step 1 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 2 Set SEC_RSA_MOD_REG[sec_rsa_key_width] to 1 and SEC_RSA_MOD_REG[sec_rsa_mod_sel], SEC_RSA_MOD_REG[sec_rsa_data0_clr], SEC_RSA_MOD_REG[sec_rsa_data1_clr], and SEC_RSA_MOD_REG[sec_rsa_data2_clr] to 0. When SEC_RSA_MOD_REG[sec_rsa_key_width] is 0 or 3, RSA 1024 is used; when the field value is 1, RSA 2048 is used; when the field value is 2, RSA 4096 is used.

Step 3 Configure SEC_RSA_WPKT_REG[sec_rsa_wpkt_reg]. The configured packet length must be the same as the key bit width configured in SEC_RSA_MOD_REG[sec_rsa_key_width].

Step 4 Configure SEC_RSA_WSEC_REG[sec_rsa_wsec_reg]. Set the key parameter N and then E/D. The length of each parameter must be the same as the key bit width configured in SEC_RSA_MOD_REG[sec_rsa_key_width].

Step 5 Set SEC_RSA_START_REG[sec_rsa_start_reg] to 1.

Step 6 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 7 Read SEC_RSA_RRSLT_REG[sec_rsa_rrslt_reg]. The length of the read result must be the same as the key bit width configured in SEC_RSA_MOD_REG[sec_rsa_key_width].

----End

Debugging the Key by Using CRC16

The key is debugged by using CRC16 as follows:

Step 1 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 2 Set SEC_RSA_MOD_REG[sec_rsa_data0_clr], SEC_RSA_MOD_REG[sec_rsa_data1_clr], and SEC_RSA_MOD_REG[sec_rsa_data2_clr] to 0, SEC_RSA_MOD_REG[sec_rsa_mod_sel] to 3, and SEC_RSA_MOD_REG[sec_rsa_key_width] to 1. When SEC_RSA_MOD_REG[sec_rsa_key_width] is 0 or 3, RSA 1024 is used; when the field value is 1, RSA 2048 is used; when the field value is 2, RSA 4096 is used.

Step 3 Set SEC_RSA_START_REG[sec_rsa_start_reg] to 1.

Step 4 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 5 Read the cyclic redundancy check (CRC) result from SEC_CRC16_REG[sec_rsa_crc16_dat].

----End

Clearing the RAM

The RAM is cleared as follows:

Step 1 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 2 Set SEC_RSA_MOD_REG[sec_rsa_mod_sel] to 2 and SEC_RSA_MOD_REG[sec_rsa_key_width], SEC_RSA_MOD_REG[sec_rsa_data0_clr], SEC_RSA_MOD_REG[sec_rsa_data1_clr], and SEC_RSA_MOD_REG[sec_rsa_data2_clr] to 1. If SEC_RSA_MOD_REG[sec_rsa_key_width] is 0 or 3, RSA 1024 is used; if the field value is 1, RSA 2048 is used; if the field value is 2, RSA 4096 is used. If SEC_RSA_MOD_REG[sec_rsa_data0_clr] is 1, the RAM that stores the RSA key is cleared; if the field value is 0, the RAM that stores the RSA key is not cleared. If SEC_RSA_MOD_REG[sec_rsa_data1_clr] is 1, the RAM that stores the RSA packet is cleared; if the field value is 0, the RAM that stores the RSA packet is not cleared. If SEC_RSA_MOD_REG[sec_rsa_data2_clr] is 1, the RAM that stores the RSA result is cleared; if the field value is 0, the RAM that stores the RSA result is not cleared.

Step 3 Set SEC_RSA_START_REG[sec_rsa_start_reg] to 1.

Step 4 Read and check whether SEC_RSA_BUSY_REG[sec_rsa_busy_reg] is 0. If yes, go to the next step; if no, wait.

Step 5 Read SEC_RSA_RPKT_REG[sec_rsa_rpkt_reg] to determine whether the RAM that stores the packet is cleared.

Step 6 Read SEC_RSA_RRSLT_REG[sec_rsa_rrslt_reg] to determine whether the RAM that stores the result is cleared.

Step 7 Check the key through CRC to determine whether the RAM that stores the key is cleared.

----End

13.4.5 Register Summary

Table 13-4 describes RSA registers.

Table 13-4 Summary of RSA registers (base address: 0x120B_0000)

Offset Address	Register	Description	Page
0x50	SEC_RSA_BUSY_REG	Busy status register for the SEC_RSA module	13-83
0x54	SEC_RSA_MOD_REG	Operating mode register for the SEC_RSA module	13-83
0x58	SEC_RSA_WSEC_REG	Key write operation register for the SEC_RSA module	13-84
0x5C	SEC_RSA_WPKT_REG	Packet write operation register for the SEC_RSA module	13-85
0x60	SEC_RSA_RPKT_REG	Packet read operation register for the SEC_RSA module	13-85
0x64	SEC_RSA_RRSLT_REG	Calculation result read operation register for the SEC_RSA module	13-86

Offset Address	Register	Description	Page
0x68	SEC_RSA_START_REG	Modular exponentiation operation configuration start register for the SEC_RSA module	13-86
0x6C	SEC_RSA_ADDR_REG	RAM address register for the key, packet, and result of the SEC_RSA module	13-86
0x70	SEC_RSA_ERROR_REG	Error alarm status register for the SEC_RSA module	13-87
0x74	SEC_CRC16_REG	Key CRC result register for the SEC_RSA module	13-88

13.4.6 Register Description

SEC_RSA_BUSY_REG

SEC_RSA_BUSY_REG is a busy status register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x50	SEC_RSA_BUSY_REG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1	0
Name	reserved								sec_rsa_busy_reg
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RO	sec_rsa_busy_reg	Busy status of the SEC_RSA module 0: idle 1: busy

SEC_RSA_MOD_REG

SEC_RSA_MOD_REG is an operating mode register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x54	SEC_RSA_MOD_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																									sec_rsa_data2_clr	sec_rsa_data1_clr	sec_rsa_data0_clr	sec_rsa_key_width		sec_rsa_mod_sel	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:7]	RO	reserved	Reserved
[6]	RW	sec_rsa_data2_clr	Clear enable for the RAM that stores the RSA result 0: not cleared 1: cleared
[5]	RW	sec_rsa_data1_clr	Clear enable for the RAM that stores the RSA packet 0: not cleared 1: cleared
[4]	RW	sec_rsa_data0_clr	Clear enable for the RAM that stores the RSA key 0: not cleared 1: cleared
[3:2]	RW	sec_rsa_key_width	Key bit width 00: 1024 bits 01: 2048 bits 10: 4096 bits 11: 1024 bits
[1:0]	RW	sec_rsa_mod_sel	Operating mode select 00: modular exponentiation encryption and decryption operation 01: reserved 10: The RAM is cleared. 11: The key is checked by using CRC16.

SEC_RSA_WSEC_REG

SEC_RSA_WSEC_REG is a key write operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x58	SEC_RSA_WSEC_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_wsec_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	sec_rsa_wsec_reg	CPU key configuration register. The number of configuration times is determined based on the configured bit width of the RSA key.

SEC_RSA_WPKT_REG

SEC_RSA_WPKT_REG is a packet write operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x5C	SEC_RSA_WPKT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_wpkt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	sec_rsa_wpkt_reg	CPU packet configuration register. The number of configuration times is determined based on the configured bit width of the RSA key.

SEC_RSA_RPKT_REG

SEC_RSA_RPKT_REG is a packet read operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x60	SEC_RSA_RPKT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_rpkt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sec_rsa_rpkt_reg	CPU packet read register. The number of configuration times is determined based on the configured bit width of the RSA key.

SEC_RSA_RRSLT_REG

SEC_RSA_RRSLT_REG is a calculation result read operation register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x64	SEC_RSA_RRSLT_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sec_rsa_rrslt_reg																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	sec_rsa_rrslt_reg	CPU calculation result register. The number of configuration times is determined based on the configured bit width of the RSA key.

SEC_RSA_START_REG

SEC_RSA_START_REG is a modular exponentiation operation configuration start register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x68	SEC_RSA_START_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																															sec_rsa_start_reg
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:1]	RO	reserved	Reserved
[0]	RW	sec_rsa_start_reg	CPU configuration start 0: not start 1: start

SEC_RSA_ADDR_REG

SEC_RSA_ADDR_REG is an RAM address register for the key, packet, and result of the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x6C	SEC_RSA_ADDR_REG	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Name	sec_rsa_addere_rslt		sec_rsa_addre_pkt		sec_rsa_addre_d		sec_rsa_addr_n	
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Bits	Access	Name	Description
[31:24]	RO	sec_rsa_addere_rslt	Result RAM address The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.
[23:16]	RO	sec_rsa_addre_pkt	Packet RAM address The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored or read. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.
[15:8]	RO	sec_rsa_addre_d	RAM address of the key parameter E/D The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.
[7:0]	RO	sec_rsa_addr_n	RAM address of the key parameter N The address offset is 4 bytes each time. That is, if the value of this field is 1, 4-byte data is stored. When the number of stored data segments reaches the maximum key bit width, the value of this field is 0 because the count value starts from 0.

SEC_RSA_ERROR_REG

SEC_RSA_ERROR_REG is an error alarm status register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x70	SEC_RSA_ERROR_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																														sec_rsa_err1	reserved
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:2]	RO	reserved	Reserved
[1]	RO	sec_rsa_err1	Alarm when the external input RSA key (N) is an even number (the odd/even feature of the key is not checked when the RAM that stores the key is cleared) 0: The external input key is normal. 1: The external input key (N) is an even number.
[0]	RO	reserved	Reserved

SEC_CRC16_REG

SEC_CRC16_REG is a key CRC result register for the SEC_RSA module.

Offset Address	Register Name	Total Reset Value
0x74	SEC_CRC16_REG	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																sec_rsa_crc16_dat																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:16]	RO	reserved	Reserved
[15:0]	RO	sec_rsa_crc16_dat	CRC result of the key

13.5 OTP Key Ctrl

13.5.1 Operating Mode

The one-time programming (OTP) Key Ctrl module is used to program and read keys in the OTP. The OTP Key Ctrl module supports the following working modes:

- Burning the key to the OTP
- Reading the key use status in the OTP
- Loading the key to the cipher or RSA key management module
- Loading the key to the hash

13.5.1.1 Burning the Key to the OTP

Before burning, the data in the OTP is 0. After burning is enabled, the OTP key control module burns the corresponding macro unit to 1 based on the key value and OTP address of the key (KL_CTRL[otp_key_add]).

The operation process of burning the key to the OTP is as follows:

Step 1 Assign values to KL_WKEY0, KL_WKEY1, KL_WKEY2, and KL_WKEY3.

Step 2 Query the status register KL_STA, and wait until KL_STA[ctrl_rdy] is 1 and KL_STA[ctrl_busy0], KL_STA[ctrl_busy1], and KL_STA[ctrl_busy2] are 0.

Step 3 Write the OTP address of the key to KL_CTRL[otp_key_add], and set KL_CTRL[work_mode] to 3'b010 to enable the mode of burning the key to the OTP.

Step 4 Write 1 to KL_CTRL[start] to start the operation.

Step 5 Query the status registers KL_STA and KL_STA1. Wait until KL_STA[key_wt_finish] is 1, indicating that the data has been burnt. At this time, the burning operation is complete. Note that if KL_STA[key_wt_error] is 1, the burning fails and the key address has been burned before. If KL_STA1[rd_back_check_err] is 1, errors occur during the burning operation. The related error information can be obtained by reading RBC_WKEY0_STA, RBC_WKEY1_STA, RBC_WKEY2_STA, and RBC_WKEY3_STA.

----End

13.5.1.2 Reading the Key Use Status in the OTP

After the key in the OTP is burnt, the corresponding key_stat bit is 1. Therefore, before burning the key, read the key_stat bit of the key at the corresponding address in the OTP to check the usage status and ensure that the address of the key to be burnt has not been used before.

Step 1 Query the status register KL_STA, and wait until KL_STA[ctrl_rdy] is 1 and KL_STA[ctrl_busy0], KL_STA[ctrl_busy1], and KL_STA[ctrl_busy2] are 0.

Step 2 Write 3'b000 to the control register KL_CTRL[work_mode] to enable the key lock status read back mode.

Step 3 Write 1 to KL_CTRL[start] to start the operation.

Step 4 Query the status registers KL_STA and KL_STA1 until KL_STA1[rd_key_st_finish] is 1, indicating that the operation is complete. key_stat[*n*] indicates the use status of key *n* (*n* is 0, 1,

2, or 3). The value 0 indicates that the key has not been burnt before, and the value 1 indicates that the key has been burnt.

----End

13.5.1.3 Loading the Key to the Cipher or RSA Key Management Module

The operation process of loading the key to the cipher is as follows:

Step 1 Query the status register KL_STA, and wait until KL_STA[ctrl_rdy] is 1 and KL_STA[ctrl_busy0], KL_STA[ctrl_busy1], and KL_STA[ctrl_busy2] are 0.

Step 2 Write the OTP address of the key to KL_CTRL[otp_key_add] and write 3'b001 to KL_CTRL[work_mode] to enable the function of loading the key to the cipher or RSA key management module.

Step 3 Write 1 to KL_CTRL[start] to start the operation.

Step 4 Query the status register KL_STA[cipher_rsa_kl_finish] until the value is 1, indicating that the operation of loading the key to the cipher or RSA key management module is complete. At this time, the operation is complete.

----End

13.5.1.4 Loading the Key to the Hash

The operation process of loading the key to the hash is as follows:

Step 1 Query the status register KL_STA, and wait until KL_STA[ctrl_rdy] is 1 and KL_STA[ctrl_busy0], KL_STA[ctrl_busy1], and KL_STA[ctrl_busy2] are 0.

Step 2 Write the OTP address of the key to KL_CTRL[otp_key_add] and write 3'b100 to KL_CTRL[work_mode] to enable the mode of loading the key to the hash.

Step 3 Write 1 to KL_CTRL[start] to start the operation.

Step 4 Query the status register KL_STA[hash_key_read_busy] until the value is 0, indicating that the operation of loading the key to the hash is complete. At this time, the operation is complete.

----End

13.5.2 OTP Key Ctrl Register Summary

Table 13-5 describes OTP key control registers.

Table 13-5 Summary of OTP key control registers (base address: 0x1207_0000)

Offset Address	Register	Description	Page
0x0000	KL_WKEY0	Key burning register 0	13-91
0x0004	KL_WKEY1	Key burning register 1	13-91
0x0008	KL_WKEY2	Key burning register 2	13-92
0x000C	KL_WKEY3	Key burning register 3	13-92

Offset Address	Register	Description	Page
0x0010	KL_CTRL	Key control register	13-92
0x0014	KL_STA	Status indicator register	13-93
0x001C	KL_STA1	Status indicator register 1	13-95
0x0020	RBC_WKEY0_STA	Key burning check status register 0	13-95
0x0024	RBC_WKEY1_STA	Key burning check status register 1	13-96
0x0028	RBC_WKEY2_STA	Key burning check status register 2	13-96
0x002C	RBC_WKEY3_STA	Key burning check status register 3	13-97

13.5.3 OTP Key Ctrl Register Description

KL_WKEY0

KL_WKEY0 is key burning register 0.

Offset Address	Register Name	Total Reset Value
0x0000	KL_WKEY0	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key0	Key[31:0] that are burnt to the OTP

KL_WKEY1

KL_WKEY1 is key burning register 1.

Offset Address	Register Name	Total Reset Value
0x0004	KL_WKEY1	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key1	Key[63:32] that are burnt to the OTP

KL_WKEY2

KL_WKEY2 is key burning register 2.

Offset Address	Register Name	Total Reset Value
0x0008	KL_WKEY2	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key2	Key[95:64] that are burnt to the OTP

KL_WKEY3

KL_WKEY3 is key burning register 3.

Offset Address	Register Name	Total Reset Value
0x000C	KL_WKEY3	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	WO	key3	Key[127:96] that are burnt to the OTP

KL_CTRL

KL_CTRL is a key control register.

Offset Address	Register Name	Total Reset Value
0x0010	KL_CTRL	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reserved																										otp_key_add		work_mode			start
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:6]	RO	reserved	Reserved
[5:4]	RW	otp_key_add	Address of the key in the OTP for burning or loading the key
[3:1]	RW	work_mode	Operating mode select 000: reading back the key lock status 001: loading the key to the cipher or RSA key management module 010: burning the key to the OTP 100: loading the key to the hash Other values: reserved
[0]	RW	start	Operation start. Writing 1 to this bit starts the operation. Reading back this bit has no effect. Note: A new operation can be initiated only when ctrl_busy1, ctrl_busy2 and ctrl_busy0 are 0 and ctrl_rdy is 1.

KL_STA

KL_STA is a status indicator register.

Offset Address	Register Name	Total Reset Value
0x0014	KL_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	key_wt_finish	key_wt_error	ctrl_busy1	ctrl_busy0	ctrl_rdy	reserved															ctrl_busy2	reserved									hash_key_read_busy	cipher_rsa_kl_finish	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31]	RO	key_wt_finish	Whether the operation of burning the key to the OTP is complete 0: not complete 1: complete
[30]	RO	key_wt_error	Whether an error occurs during the operation of burning the key to the OTP 0: No error occurs. The burning is successful. 1: An error occurs. The key address has been burnt before.
[29]	RO	ctrl_busy1	Controller busy signal 1. A new operation can be initiated only when ctrl_busy1, ctrl_busy2, and ctrl_busy0 are 0 and ctrl_rdy is 1.
[28]	RO	ctrl_busy0	Controller busy signal 0. A new operation can be initiated only when ctrl_busy1, ctrl_busy2, and ctrl_busy0 are 0 and ctrl_rdy is 1.
[27]	RO	ctrl_rdy	Controller ready signal. A new operation can be initiated only when ctrl_busy1, ctrl_busy2, and ctrl_busy0 are 0 and ctrl_rdy is 1.
[26:12]	RO	reserved	Reserved
[11]	RO	ctrl_busy2	Controller busy signal 2. A new operation can be initiated only when ctrl_busy1, ctrl_busy2, and ctrl_busy0 are 0 and ctrl_rdy is 1.
[10:2]	RO	reserved	Reserved
[1]	RO	hash_key_read_busy	Whether the operation of loading the key to the hash is complete 0: complete 1: not complete The hash encryption and decryption operations are started only after the loading operation is complete.

[0]	RO	cipher_rsa_kl_finish	Whether the operation of loading the key to the cipher or RSA key management module is complete 0: not complete 1: complete The cipher or RSA key management module can be started only after loading is complete.

KL_STA1

KL_STA1 is status indicator register 1.

Offset Address	Register Name	Total Reset Value
0x001C	KL_STA1	0x0000_0000

Bit	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9	8	7 6 5	4	3 2 1 0
Name	reserved						rd_back_check_err	reserved	rd_key_st_finish	key_stat
Reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0	0 0 0	0	0 0 0 0

Bits	Access	Name	Description
[31:9]	RO	reserved	Reserved
[8]	RO	rd_back_check_err	Check of the key burning result 0: The key burning is successful and the read back check is passed. 1: Errors occur during key burning and the read back check fails.
[7:5]	RO	reserved	Reserved
[4]	RO	rd_key_st_finish	Whether the operation of reading back the key lock indicator status is complete 0: complete 1: not complete
[3:0]	RO	key_stat	Key lock indicator. key_stat[*n*] indicates the use status of key *n* (*n* is 0, 1, 2, or 3). The value 0 indicates that the key has not been burnt before, and the value 1 indicates that the key has been burnt.

RBC_WKEY0_STA

RBC_WKEY0_STA is key burning check status register 0.

Offset Address	Register Name	Total Reset Value
0x0020	RBC_WKEY0_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_back_check_sta0																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rd_back_check_sta0	Check status of key bit[31:0]. If the corresponding bit is 1, an error occurs.

RBC_WKEY1_STA

RBC_WKEY1_STA is key burning check status register 1.

Offset Address	Register Name	Total Reset Value
0x0024	RBC_WKEY1_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_back_check_sta1																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rd_back_check_sta1	Check status of key bit[63:32]. If the corresponding bit is 1, an error occurs.

RBC_WKEY2_STA

RBC_WKEY2_STA is key burning check status register 2.

Offset Address	Register Name	Total Reset Value
0x0028	RBC_WKEY2_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_back_check_sta2																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rd_back_check_sta2	Check status of key bit[95:64]. If the corresponding bit is 1, an error occurs.

RBC_WKEY3_STA

RBC_WKEY3_STA is key burning check status register 3.

Offset Address	Register Name	Total Reset Value
0x002C	RBC_WKEY3_STA	0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rd_back_check_sta3																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Access	Name	Description
[31:0]	RO	rd_back_check_sta3	Check status of key bit[127:96]. If the corresponding bit is 1, an error occurs.

Contents

A Ordering Information

Figure A-1 shows the Hi3516C V300 mark.

Figure A-1 Hi3516C V300 mark

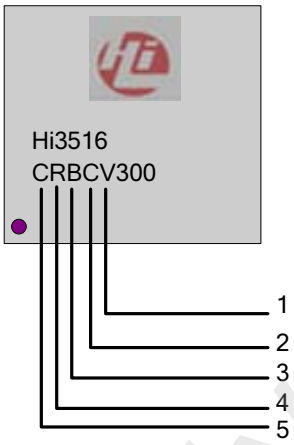


Table A-1 describes the Hi3516C V300 mark.

Table A-1 Meaning of the Hi3516C V300 mark

No.	Item	Description
1	Version number	It indicates the chip version number.
2	Temperature flag	The letter C stands for commercial. It indicates that the chip is for commercial use.
3	Package flag	The letter B indicates the ball grid array (BGA) package.
4	Environmental protection flag	The letter R stands for Restriction of Hazardous Substances (RoHS).
5	Product differentiation flag	It is the last digit of a chip name for differentiating one chip from another one.