PSoC® Creator™
Project Datasheet for LamellaDevice

Creation Time: 02/08/2021 10:53:32
User: PC1011900378\LocalAdmin
Project: LamellaDevice
Tool: PSoC Creator 4.2

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intl): 408.943.2600
http://www.cypress.com

Copyright

Trademarks

PSoC and CapSense are registered trademarks of Cypress Semiconductor Corporation. PSoC Creator is a trademark of Cypress Semiconductor Corporation. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Philips I2C Patent Rights

Purchase of I2C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I2C Patent Rights to use these components in an I2C system, provided that the system conforms to the I2C Standard Specification as defined by Philips. As from October 1st, 2006 Philips Semiconductors has a new trade name, NXP Semiconductors.

Disclaimer

CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. While reasonable precautions have been taken, Cypress assumes no responsibility for any errors that may appear in this document. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of a Cypress product in a life support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Flash Code Protection

Cypress products meet the specifications contained in their particular Cypress PSoC Datasheets. Cypress believes that its family of PSoC products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as 'unbreakable.'

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

Table of Contents

1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP series member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C58LP Device Series Block Diagram

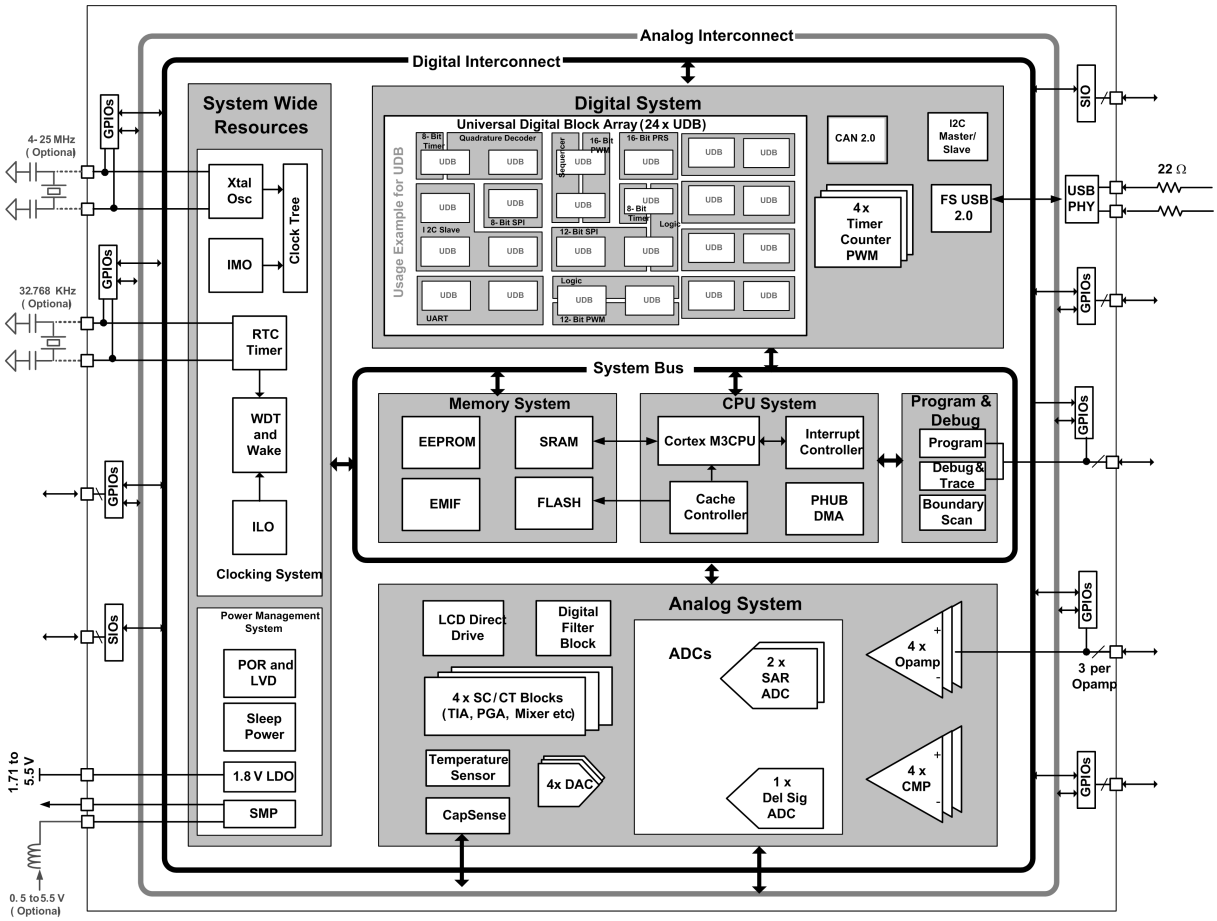


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5888LTI-LP097
Package Name	68-QFN
Family	PSoC 5LP
Series	CY8C58LP
Max CPU speed (MHz)	0
Flash size (kB)	256
SRAM size (kB)	64
EEPROM size (bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85
JTAG ID	0x2E161069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

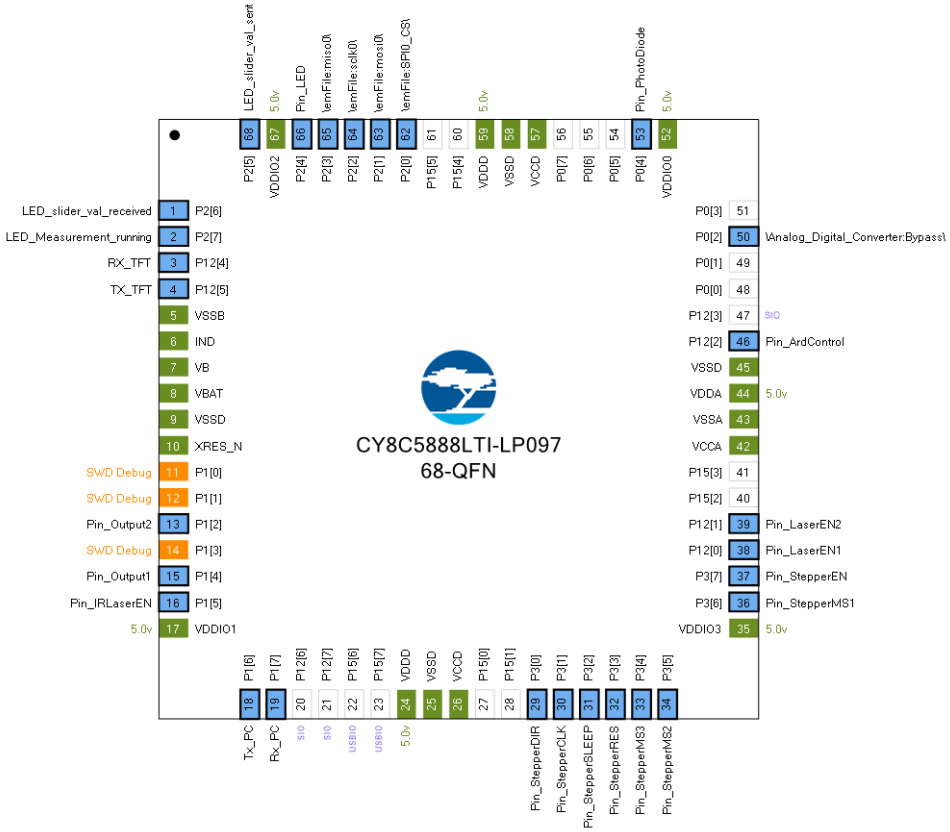
Resource Type	Used	Free	Max	% Used
Digital Clocks	4	4	8	50.00 %
Analog Clocks	1	3	4	25.00 %
CapSense Buffers	0	2	2	0.00 %
Digital Filter Block	0	1	1	0.00 %
Interrupts	6	26	32	18.75 %
IO	31	17	48	64.58 %
Segment LCD	0	1	1	0.00 %
CAN 2.0b	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	0	24	24	0.00 %
Timer	1	3	4	25.00 %
UDB				
Macrocells	67	125	192	34.90 %
Unique P-terms	135	249	384	35.16 %
Total P-terms	159			
Datapath Cells	7	17	24	29.17 %
Status Cells	10	14	24	41.67 %
StatusI Registers	6			
Sync Cells (x2)	1			
Routed Count7 Load/Enable	3			
Control Cells	3	21	24	12.50 %
Count7 Cells	3			
Opamp	0	4	4	0.00 %
Comparator	0	4	4	0.00 %
Delta-Sigma ADC	0	1	1	0.00 %
LPF	0	2	2	0.00 %
SAR ADC	1	1	2	50.00 %
Analog (SC/CT) Blocks	2	2	4	50.00 %
DAC				

Resource Type	Used	Free	Max	% Used
VIDAC	0	4	4	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[6]	LED_slider_-val_received	Software In/Out	Strong drive	HiZ Analog Unb
2	P2[7]	LED_-Measureme-nt_running	Software In/Out	Strong drive	HiZ Analog Unb
3	P12[4]	RX_TFT	Dgtl In	HiZ digital	HiZ Analog Unb
4	P12[5]	TX_TFT	Dgtl Out	Strong drive	HiZ Analog Unb
5	VSSB	VSSB	Dedicated		
6	IND	IND	Dedicated		
7	VB	VB	Dedicated		
8	VBAT	VBAT	Dedicated		
9	VSSD	VSSD	Power		
10	XRES_N	XRES_N	Dedicated		
11	P1[0]	Debug:SWD_IO	Reserved		
12	P1[1]	Debug:SWD_CK	Reserved		
13	P1[2]	Pin_Output2	Software In/Out	Strong drive	HiZ Analog Unb
14	P1[3]	Debug:SWV	Reserved		
15	P1[4]	Pin_Output1	Software In/Out	Strong drive	HiZ Analog Unb
16	P1[5]	Pin_IRLaserEN	Software In/Out	Strong drive	HiZ Analog Unb
17	VDDIO1	VDDIO1	Power		
18	P1[6]	Tx_PC	Dgtl Out	Strong drive	HiZ Analog Unb
19	P1[7]	Rx_PC	Dgtl In	HiZ digital	HiZ Analog Unb
20	P12[6]	SIO [unused]			HiZ Analog Unb
21	P12[7]	SIO [unused]			HiZ Analog Unb
22	P15[6]	USB IO [unused]			HiZ Analog Unb
23	P15[7]	USB IO [unused]			HiZ Analog Unb
24	VDDD	VDDD	Power		
25	VSSD	VSSD	Power		
26	VCCD	VCCD	Power		
27	P15[0]	GPIO [unused]			HiZ Analog Unb
28	P15[1]	GPIO [unused]			HiZ Analog Unb
29	P3[0]	Pin_-StepperDIR	Software In/Out	Strong drive	HiZ Analog Unb
30	P3[1]	Pin_-StepperCLK	Software In/Out	Strong drive	HiZ Analog Unb
31	P3[2]	Pin_-StepperSLEEP	Software In/Out	Strong drive	HiZ Analog Unb
32	P3[3]	Pin_-StepperRES	Software In/Out	Strong drive	HiZ Analog Unb
33	P3[4]	Pin_StepperMS3	Software In/Out	Strong drive	HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
34	P3[5]	Pin_StepperMS2	Software In/Out	Strong drive	HiZ Analog Unb
35	VDDIO3	VDDIO3	Power		
36	P3[6]	Pin_StepperMS1	Software In/Out	Strong drive	HiZ Analog Unb
37	P3[7]	Pin_StepperEN	Software In/Out	Strong drive	HiZ Analog Unb
38	P12[0]	Pin_LaserEN1	Software In/Out	Strong drive	HiZ Analog Unb
39	P12[1]	Pin_LaserEN2	Software In/Out	Strong drive	HiZ Analog Unb
40	P15[2]	GPIO [unused]			HiZ Analog Unb
41	P15[3]	GPIO [unused]			HiZ Analog Unb
42	VCCA	VCCA	Power		
43	VSSA	VSSA	Power		
44	VDDA	VDDA	Power		
45	VSSD	VSSD	Power		
46	P12[2]	Pin_ArdControl	Software In/Out	Strong drive	HiZ Analog Unb
47	P12[3]	SIO [unused]			HiZ Analog Unb
48	P0[0]	GPIO [unused]			HiZ Analog Unb
49	P0[1]	GPIO [unused]			HiZ Analog Unb
50	P0[2]	\Analog_-Digital_-Converter-:Bypass\	Analog	HiZ analog	HiZ Analog Unb
51	P0[3]	GPIO [unused]			HiZ Analog Unb
52	VDDIO0	VDDIO0	Power		
53	P0[4]	Pin_PhotoDiode	Analog	HiZ analog	HiZ Analog Unb
54	P0[5]	GPIO [unused]			HiZ Analog Unb
55	P0[6]	GPIO [unused]			HiZ Analog Unb
56	P0[7]	GPIO [unused]			HiZ Analog Unb
57	VCCD	VCCD	Power		
58	VSSD	VSSD	Power		
59	VDDD	VDDD	Power		
60	P15[4]	GPIO [unused]			HiZ Analog Unb
61	P15[5]	GPIO [unused]			HiZ Analog Unb
62	P2[0]	\emFile:SPI0_-CS\	Software In/Out	Strong drive	HiZ Analog Unb
63	P2[1]	\emFile:mosi0\	Dgtl Out	Strong drive	HiZ Analog Unb
64	P2[2]	\emFile:sclk0\	Dgtl Out	Strong drive	HiZ Analog Unb
65	P2[3]	\emFile:miso0\	Dgtl In	HiZ digital	HiZ Analog Unb
66	P2[4]	Pin_LED	Software In/Out	Strong drive	HiZ Analog Unb
67	VDDIO2	VDDIO2	Power		
68	P2[5]	LED_slider_-val_sent	Software In/Out	Strong drive	HiZ Analog Unb

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- HiZ analog = High impedance analog

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	48	GPIO [unused]			HiZ Analog Unb
P0[1]	49	GPIO [unused]			HiZ Analog Unb
P0[2]	50	\Analog_-Digital_-Converter-:Bypass\	Analog	HiZ analog	HiZ Analog Unb
P0[3]	51	GPIO [unused]			HiZ Analog Unb
P0[4]	53	Pin_PhotoDiode	Analog	HiZ analog	HiZ Analog Unb
P0[5]	54	GPIO [unused]			HiZ Analog Unb
P0[6]	55	GPIO [unused]			HiZ Analog Unb
P0[7]	56	GPIO [unused]			HiZ Analog Unb
P1[0]	11	Debug:SWD_IO	Reserved		
P1[1]	12	Debug:SWD_CK	Reserved		
P1[2]	13	Pin_Output2	Software In/Out	Strong drive	HiZ Analog Unb
P1[3]	14	Debug:SWV	Reserved		
P1[4]	15	Pin_Output1	Software In/Out	Strong drive	HiZ Analog Unb
P1[5]	16	Pin_IRLaserEN	Software In/Out	Strong drive	HiZ Analog Unb
P1[6]	18	Tx_PC	Dgtl Out	Strong drive	HiZ Analog Unb
P1[7]	19	Rx_PC	Dgtl In	HiZ digital	HiZ Analog Unb
P12[0]	38	Pin_LaserEN1	Software In/Out	Strong drive	HiZ Analog Unb
P12[1]	39	Pin_LaserEN2	Software In/Out	Strong drive	HiZ Analog Unb
P12[2]	46	Pin_ArdControl	Software In/Out	Strong drive	HiZ Analog Unb
P12[3]	47	SIO [unused]			HiZ Analog Unb
P12[4]	3	RX_TFT	Dgtl In	HiZ digital	HiZ Analog Unb
P12[5]	4	TX_TFT	Dgtl Out	Strong drive	HiZ Analog Unb
P12[6]	20	SIO [unused]			HiZ Analog Unb
P12[7]	21	SIO [unused]			HiZ Analog Unb
P15[0]	27	GPIO [unused]			HiZ Analog Unb
P15[1]	28	GPIO [unused]			HiZ Analog Unb
P15[2]	40	GPIO [unused]			HiZ Analog Unb
P15[3]	41	GPIO [unused]			HiZ Analog Unb
P15[4]	60	GPIO [unused]			HiZ Analog Unb
P15[5]	61	GPIO [unused]			HiZ Analog Unb
P15[6]	22	USB IO [unused]			HiZ Analog Unb
P15[7]	23	USB IO [unused]			HiZ Analog Unb
P2[0]	62	\emFile:SPI0_-CS\	Software In/Out	Strong drive	HiZ Analog Unb
P2[1]	63	\emFile:mosi0\	Dgtl Out	Strong drive	HiZ Analog Unb
P2[2]	64	\emFile:sclk0\	Dgtl Out	Strong drive	HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P2[3]	65	\emFile:miso0\	Dgtl In	HiZ digital	HiZ Analog Unb
P2[4]	66	Pin_LED	Software In/Out	Strong drive	HiZ Analog Unb
P2[5]	68	LED_slider_-val_sent	Software In/Out	Strong drive	HiZ Analog Unb
P2[6]	1	LED_slider_-val_received	Software In/Out	Strong drive	HiZ Analog Unb
P2[7]	2	LED_-Measureme-nt_running	Software In/Out	Strong drive	HiZ Analog Unb
P3[0]	29	Pin_-StepperDIR	Software In/Out	Strong drive	HiZ Analog Unb
P3[1]	30	Pin_-StepperCLK	Software In/Out	Strong drive	HiZ Analog Unb
P3[2]	31	Pin_-StepperSLEEP	Software In/Out	Strong drive	HiZ Analog Unb
P3[3]	32	Pin_-StepperRES	Software In/Out	Strong drive	HiZ Analog Unb
P3[4]	33	Pin_StepperMS3	Software In/Out	Strong drive	HiZ Analog Unb
P3[5]	34	Pin_StepperMS2	Software In/Out	Strong drive	HiZ Analog Unb
P3[6]	36	Pin_StepperMS1	Software In/Out	Strong drive	HiZ Analog Unb
P3[7]	37	Pin_StepperEN	Software In/Out	Strong drive	HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- HiZ analog = High impedance analog
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
\Analog_Digital_-Converter:Bypass\	P0[2]	Analog	HiZ Analog Unb
\emFile:miso0\	P2[3]	Dgtl In	HiZ Analog Unb
\emFile:mosi0\	P2[1]	Dgtl Out	HiZ Analog Unb
\emFile:sclk0\	P2[2]	Dgtl Out	HiZ Analog Unb
\emFile:SPI0_CS\	P2[0]	Software In/Out	HiZ Analog Unb
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
GPIO [unused]	P0[1]		HiZ Analog Unb
GPIO [unused]	P15[0]		HiZ Analog Unb
GPIO [unused]	P0[3]		HiZ Analog Unb
GPIO [unused]	P15[2]		HiZ Analog Unb
GPIO [unused]	P15[3]		HiZ Analog Unb
GPIO [unused]	P0[0]		HiZ Analog Unb
GPIO [unused]	P15[4]		HiZ Analog Unb
GPIO [unused]	P15[5]		HiZ Analog Unb
GPIO [unused]	P15[1]		HiZ Analog Unb
GPIO [unused]	P0[5]		HiZ Analog Unb
GPIO [unused]	P0[6]		HiZ Analog Unb
GPIO [unused]	P0[7]		HiZ Analog Unb
LED_Measurement_-running	P2[7]	Software In/Out	HiZ Analog Unb
LED_slider_val_-received	P2[6]	Software In/Out	HiZ Analog Unb
LED_slider_val_sent	P2[5]	Software In/Out	HiZ Analog Unb
Pin_ArdControl	P12[2]	Software In/Out	HiZ Analog Unb
Pin_IRLaserEN	P1[5]	Software In/Out	HiZ Analog Unb
Pin_LaserEN1	P12[0]	Software In/Out	HiZ Analog Unb
Pin_LaserEN2	P12[1]	Software In/Out	HiZ Analog Unb
Pin_LED	P2[4]	Software In/Out	HiZ Analog Unb
Pin_Output1	P1[4]	Software In/Out	HiZ Analog Unb
Pin_Output2	P1[2]	Software In/Out	HiZ Analog Unb
Pin_PhotoDiode	P0[4]	Analog	HiZ Analog Unb
Pin_StepperCLK	P3[1]	Software In/Out	HiZ Analog Unb
Pin_StepperDIR	P3[0]	Software In/Out	HiZ Analog Unb

Name	Port	Type	Reset State
Pin_StepperEN	P3[7]	Software In/Out	HiZ Analog Unb
Pin_StepperMS1	P3[6]	Software In/Out	HiZ Analog Unb
Pin_StepperMS2	P3[5]	Software In/Out	HiZ Analog Unb
Pin_StepperMS3	P3[4]	Software In/Out	HiZ Analog Unb
Pin_StepperRES	P3[3]	Software In/Out	HiZ Analog Unb
Pin_StepperSLEEP	P3[2]	Software In/Out	HiZ Analog Unb
Rx_PC	P1[7]	Dgtl In	HiZ Analog Unb
RX_TFT	P12[4]	Dgtl In	HiZ Analog Unb
SIO [unused]	P12[6]		HiZ Analog Unb
SIO [unused]	P12[7]		HiZ Analog Unb
SIO [unused]	P12[3]		HiZ Analog Unb
Tx_PC	P1[6]	Dgtl Out	HiZ Analog Unb
TX_TFT	P12[5]	Dgtl Out	HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x200
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

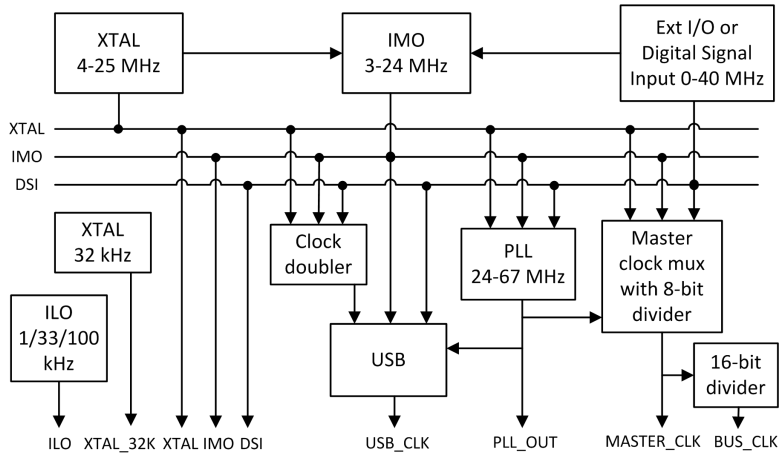
Name	Value
VDDA (V)	5.0
VDDD (V)	5.0
VDDIO0 (V)	5.0
VDDIO1 (V)	5.0
VDDIO2 (V)	5.0
VDDIO3 (V)	5.0
Variable VDDA	False
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	64 MHz	±0.25	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	64 MHz	±0.25	True	True
PLL_OUT	DIGITAL	IMO	64 MHz	64 MHz	±0.25	True	True
USB_CLK	DIGITAL	IMO	48 MHz	48 MHz	±0.25	False	True
IMO	DIGITAL		24 MHz	24 MHz	±0.25	True	True
ILO	DIGITAL		? MHz	100 kHz	-55,+100	True	True
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False
XTAL	DIGITAL		24 MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

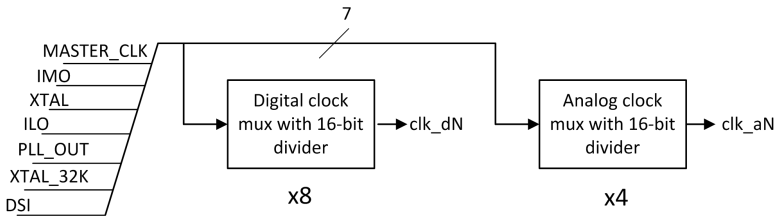


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
emFile_Clock_1	DIGITAL	MASTER_CLK	? MHz	64 MHz	±0.25	True	True
timer_clock	DIGITAL	IMO	24 MHz	24 MHz	±0.25	True	True
Analog_-Digital_-Converter_-theACLK	ANALOG	MASTER_CLK	11.368 MHz	10.667 MHz	±0.25	True	True
UART_PC_-IntClock	DIGITAL	MASTER_CLK	921.6 kHz	927.536 kHz	±0.25	True	True
UART_TFT_-IntClock	DIGITAL	MASTER_CLK	76.8 kHz	76.831 kHz	±0.25	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide

- CyPLL API routines
- CyIMO API routines
- CyILO API routines
- CyMaster API routines
- CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
Interr_PC	0	0	5
Interr_TFT	1	1	6
Timer1_Function	2	2	6
Analog_Digital_-Converter_IRQ	3	3	6
UART_TFT_-RXInternalInterrupt	4	4	6
UART_TFT_-TXInternalInterrupt	5	5	6

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

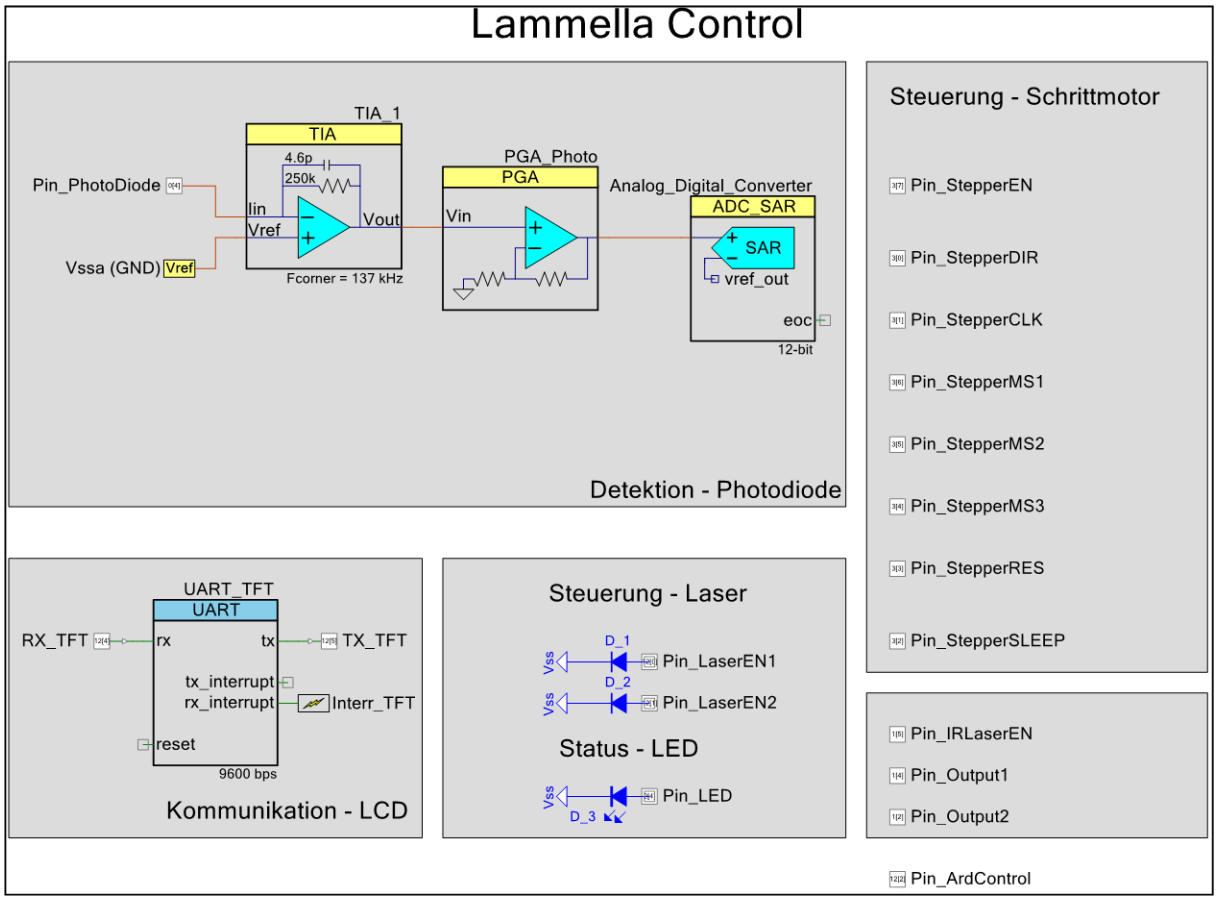
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following 6 schematic sheets:

7.1 Schematic Sheet: Start

Figure 5. Schematic Sheet: Start

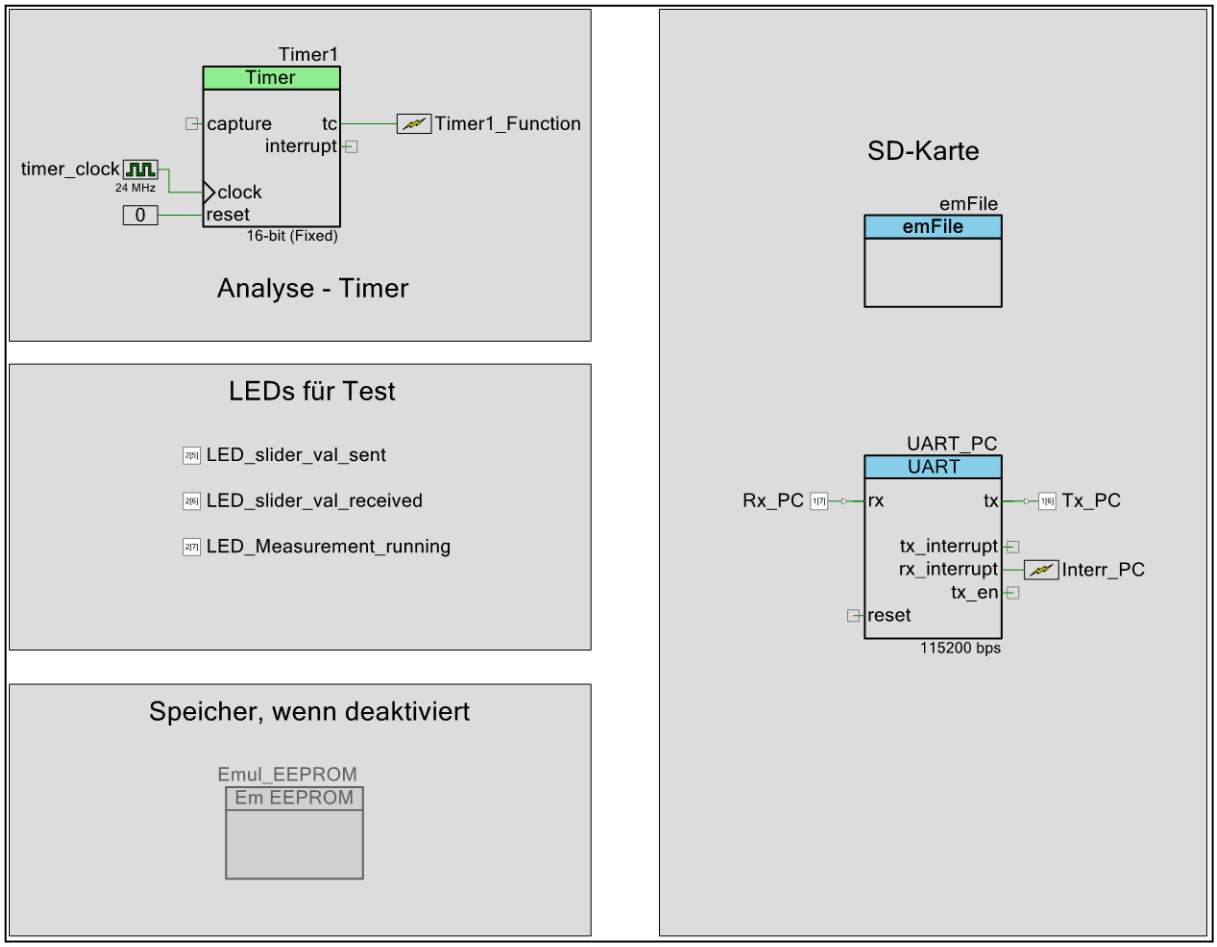


This schematic sheet contains the following component instances:

- Instance Analog_Digital_Converter (type: ADC_SAR_v3_10)
- Instance PGA_Photo (type: PGA_v2_0)
- Instance TIA_1 (type: TIA_v2_0)
- Instance UART_TFT (type: UART_v2_50)

7.2 Schematic Sheet: TimerLED_EEPROM

Figure 6. Schematic Sheet: TimerLED_EEPROM

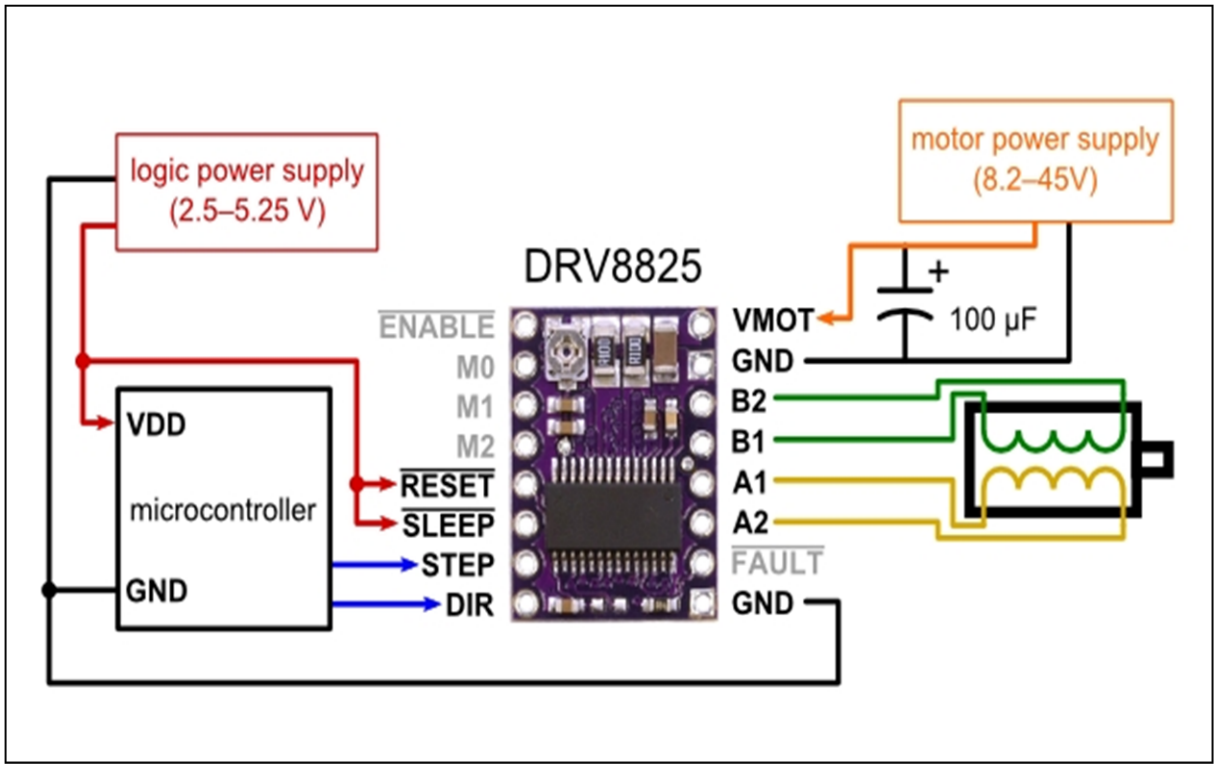


This schematic sheet contains the following component instances:

- Instance emFile (type: emFile_v1_20)
- Instance Timer1 (type: Timer_v2_80)
- Instance UART_PC (type: UART_v2_50)

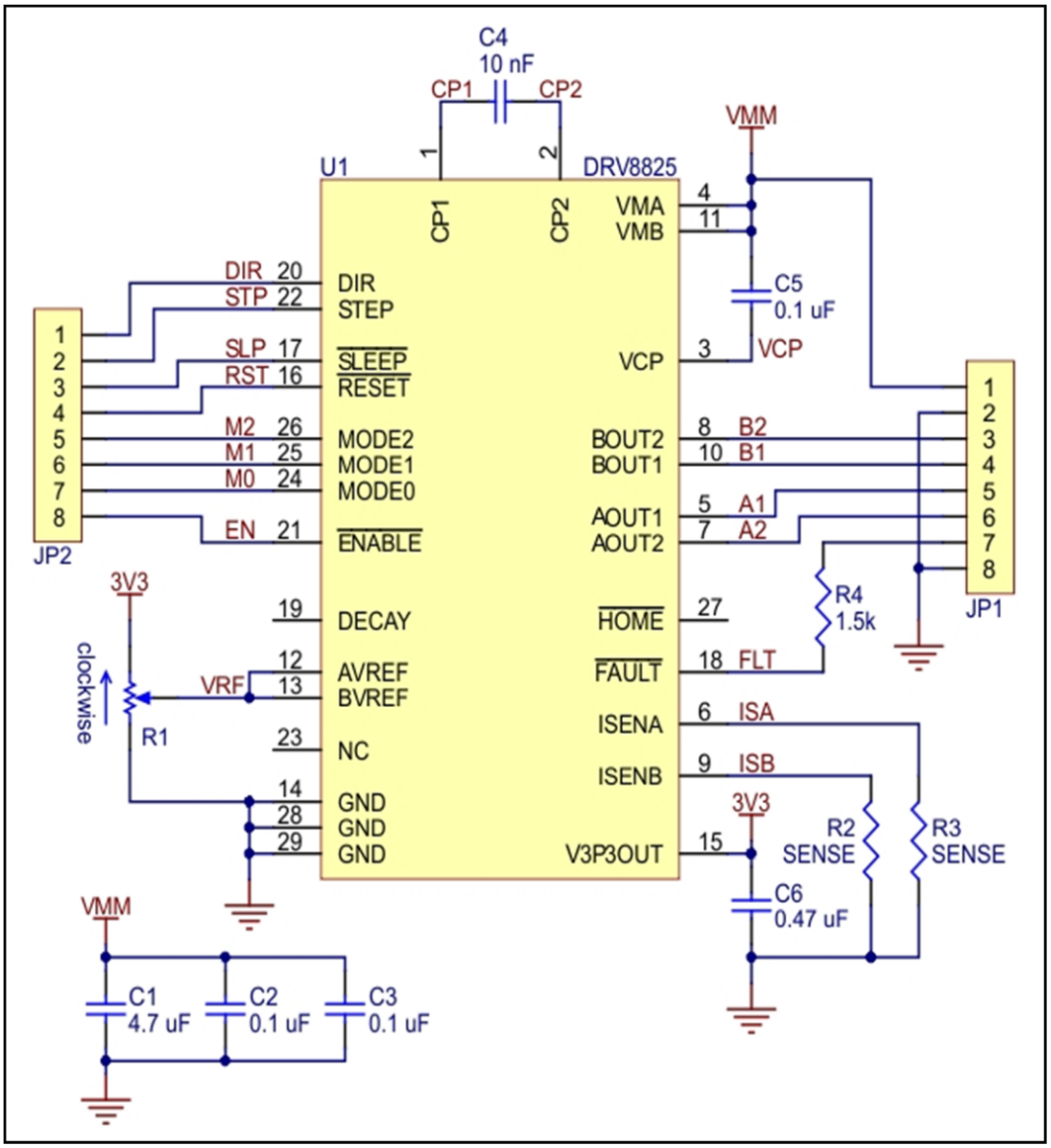
7.3 Schematic Sheet: Anschlussplan

Figure 7. Schematic Sheet: Anschlussplan



7.4 Schematic Sheet: Schaltung

Figure 8. Schematic Sheet: Schaltung

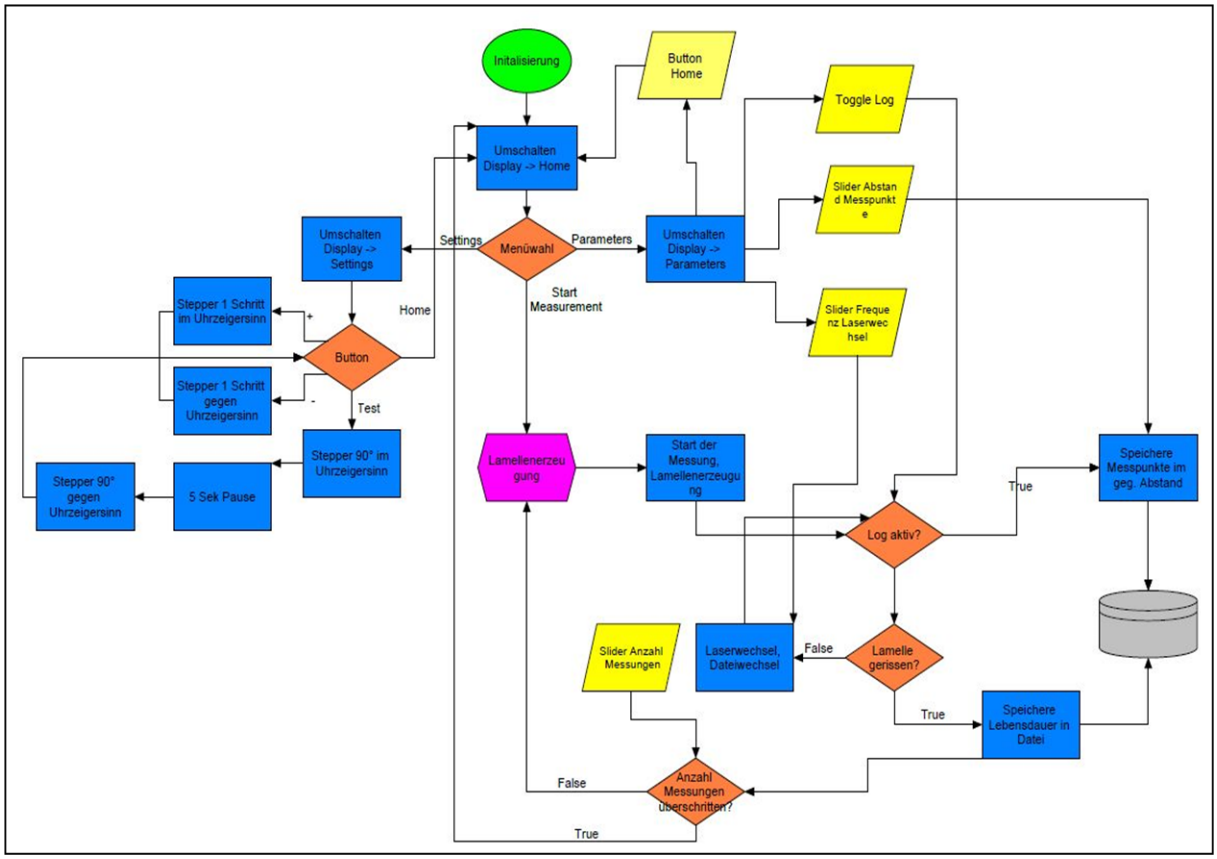


7.5 Schematic Sheet: StepperData

Figure 9. Schematic Sheet: StepperData

7.6 Schematic Sheet: FlussDiagramm

Figure 10. Schematic Sheet: FlussDiagramm



8 Components

8.1 Component type: ADC_SAR [v3.10]

8.1.1 Instance Analog_Digital_Converter

Description: Successive approximation ADC
Instance type: ADC_SAR [v3.10]
Datasheet: online component datasheet for ADC_SAR

Table 13. Component Parameters for Analog_Digital_Converter

Parameter Name	Value	Description
ADC_Clock	Internal	Selects either the internal or external clock source.
ADC_Input_Range	0.0 to 2.048V (Single Ended) 0 to Vref*2	Parameter used to choose the input operating mode that best supports the range of the signals being measured.
ADC_Power	High Power	This parameter sets the power level of the ADC.
ADC_Reference	Internal Vref, bypassed	Selects the voltage reference source and configuration.
ADC_Resolution	12	Sets the resolution of the ADC in bits.
ADC_SampleMode	Free Running	Selects the mode that the ADC operates in. This can be either free-running or triggered mode.
Enable_next_out	false	This parameter enables the End Of Sampling (eos) output terminal.
Ref_Voltage	1.024	Sets the reference voltage in volts.
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	631579	Specifies the sample rate in Hz.
User Comments		Instance-specific comments.

8.2 Component type: emFile [v1.20]

8.2.1 Instance emFile

Description: emFile file system for SD card in SPI mode
Instance type: emFile [v1.20]
Datasheet: online component datasheet for emFile

Table 14. Component Parameters for emFile

Parameter Name	Value	Description
Max_SPI_Frequency	1000	Maximum frequency (in kHz) of the SPI Master serial clock (sclk). See the SPI Master data sheet for details.
NumberSDCards	1	The number of SD cards in the system. The maximum is four (4).
User Comments		Instance-specific comments.

Parameter Name	Value	Description
WP0_En	false	Enable write protect signal for SD card #1. If disabled the SD card isn't write protected.
WP1_En	false	Enable write protect signal for SD card #2. If disabled the SD card is not write protected.
WP2_En	false	Enable write protect signal for SD card #3. If disabled the SD card is not write protected.
WP3_En	false	Enable write protect signal for SD card #4. If disabled the SD card is not write protected.

8.3 Component type: PGA [v2.0]

8.3.1 Instance PGA_Photo

Description: Programmable Gain Amplifier
Instance type: PGA [v2.0]
Datasheet: online component datasheet for PGA

Table 15. Component Parameters for PGA_Photo

Parameter Name	Value	Description
Gain	2	Selects supported gain value.
Power	Low Power	Selects the device power.
User Comments		Instance-specific comments.
Vref_Input	Internal Vss	Enables direct connection from the Analog ground (Agnd) to the inverting input.

8.4 Component type: TIA [v2.0]

8.4.1 Instance TIA_1

Description: Trans-Impedance Amplifier
Instance type: TIA [v2.0]
Datasheet: online component datasheet for TIA

Table 16. Component Parameters for TIA_1

Parameter Name	Value	Description
Capacitive_Feedback	4.6 pF	Capacitive feedback for the TIA
Fcorner	137 kHz	Calculated -3dB frequency for the given feedback settings.
Power	High Power	Power setting for TIA
Resistive_Feedback	250k ohms	Nominal resistive feedback for the TIA
User Comments		Instance-specific comments.

8.5 Component type: Timer [v2.80]

8.5.1 Instance Timer1

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.80]
Datasheet: online component datasheet for Timer

Table 17. Component Parameters for Timer1

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	Rising Edge	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	true	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	false	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	23999	Defines the timer period (This is also the reload value when terminal count is reached)
Resolution	16	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.

Parameter Name	Value	Description
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	None	Defines the required trigger input signal to cause a valid trigger enable of the timer
User Comments		Instance-specific comments.

8.6 Component type: UART [v2.50]

8.6.1 Instance UART_PC

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 18. Component Parameters for UART_PC

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	115200	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	true	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.

Parameter Name	Value	Description
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.
User Comments		Instance-specific comments.

8.6.2 Instance UART_TFT

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 19. Component Parameters for UART_TFT

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	9600	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	true	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	true	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	false	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	true	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default

Parameter Name	Value	Description
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	20	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	20	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine