QB Unit-1 LA9

Assignment-I

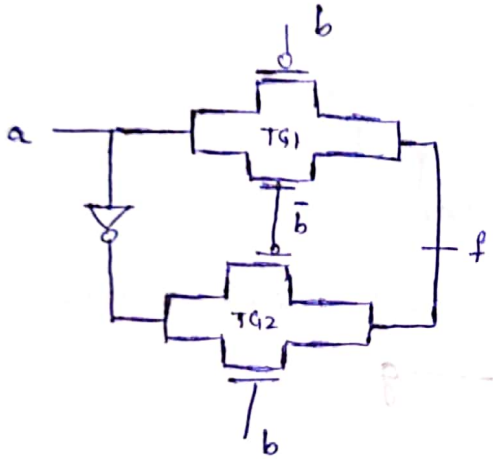
(1) (a) Identify the name of a 2 input logic gate which produce an output '1' only when the inputs are different.

Ans: XOR

(b) logical expression

Ans: $f = \bar{a}b + a\bar{b}$

(c) Draw the transmission gate

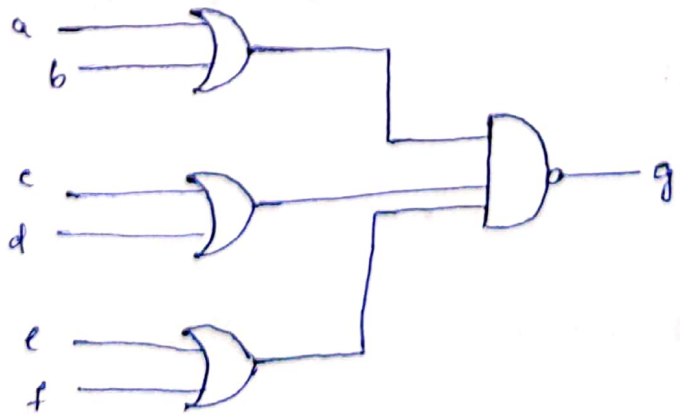


QB

(3) Use concept of bubble pushing - Draw cmos structure of

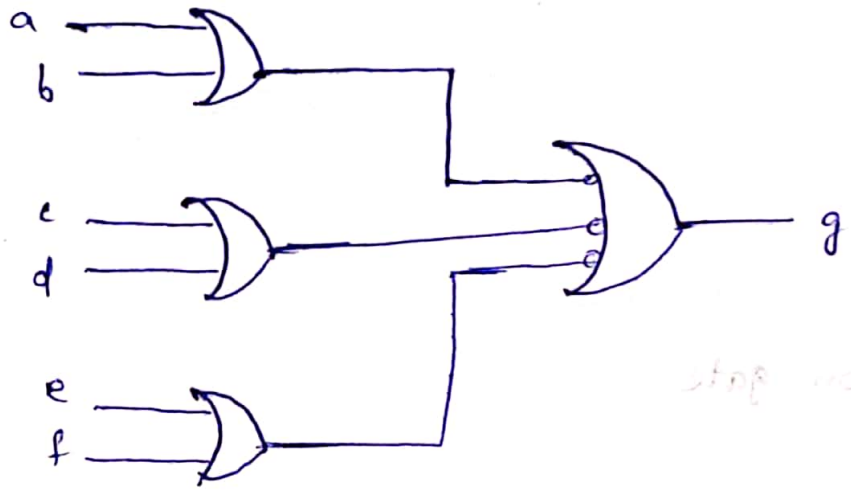
$$q = \overline{(a+b)(c+d)(e+f)}$$

Ans: Step-1 : Draw logic diagram

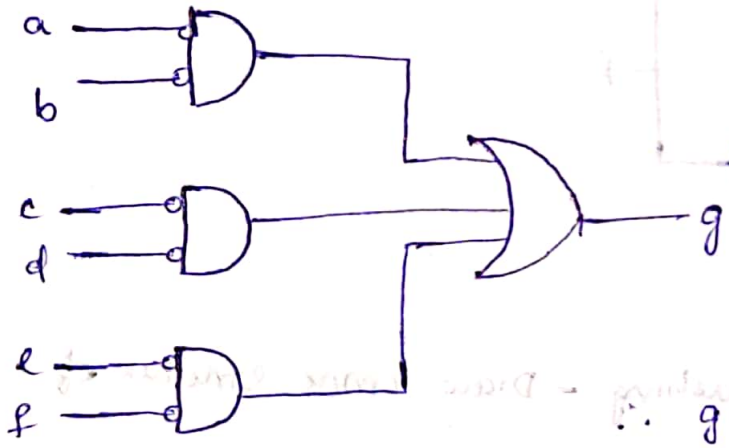


Bubble at the output is pushed to corresponding inputs.

First transformation:



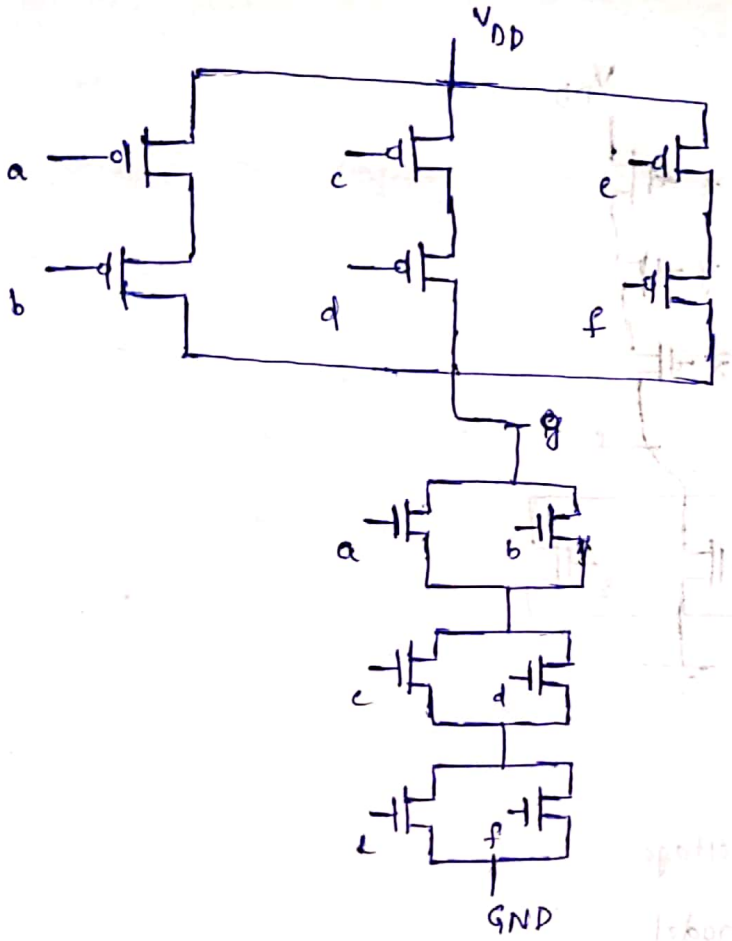
Second Transformation:



$\therefore g = \bar{a}\bar{b} + \bar{c}\bar{d} + \bar{e}\bar{f}$

- PFET path of the CMOS circuit can be obtained directly from the equation.

CMOS circuit:



QB

④ (a) Logic gate 3 input – Produce output 0 when of the input is 1.

Ans: NOR 3

(b) logical expression.

Ans: $f = \overline{x+y+z}$

(c) No. of transistors for CMOS

Ans: 6

3 → nFETs

3 → pFETs

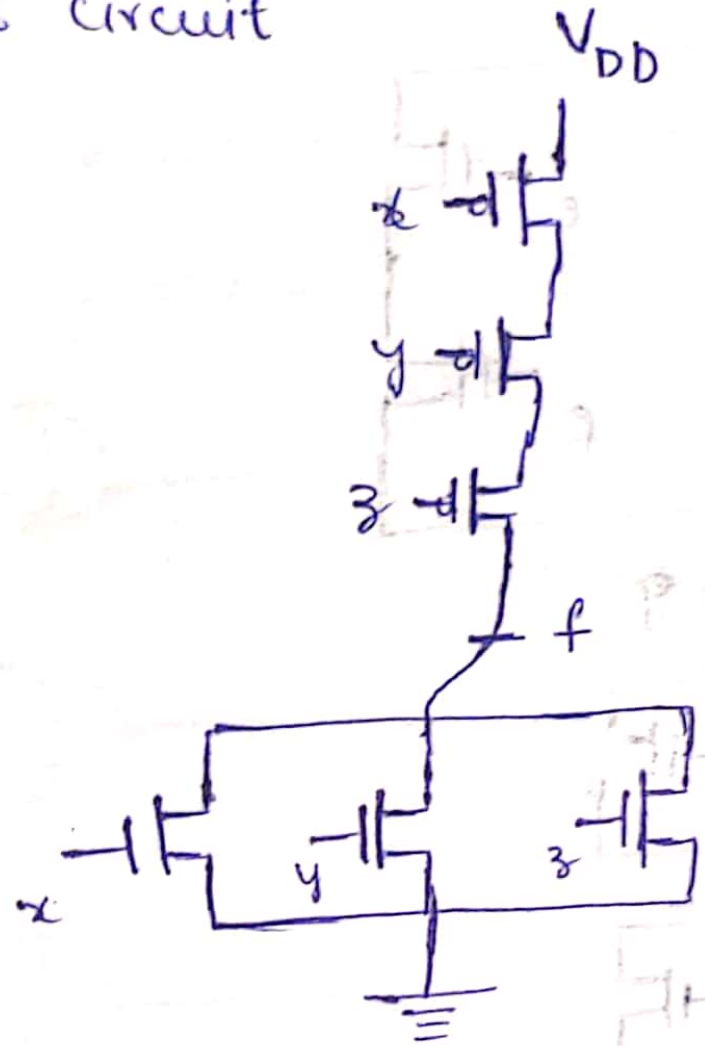
$f = \overline{x+y+z}$ ← complement

$= (\overline{x+y+z}) \cdot 1 + (x+y+z)\, 0$

$= (\bar{x}\,\bar{y}\,\bar{z}) \cdot 1 + (x+y+z)\, 0$

pFET nFET

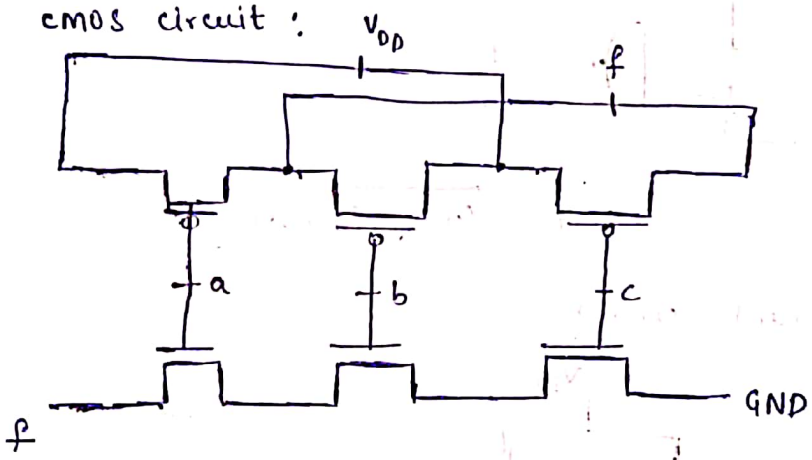
(d) CMOS Circuit



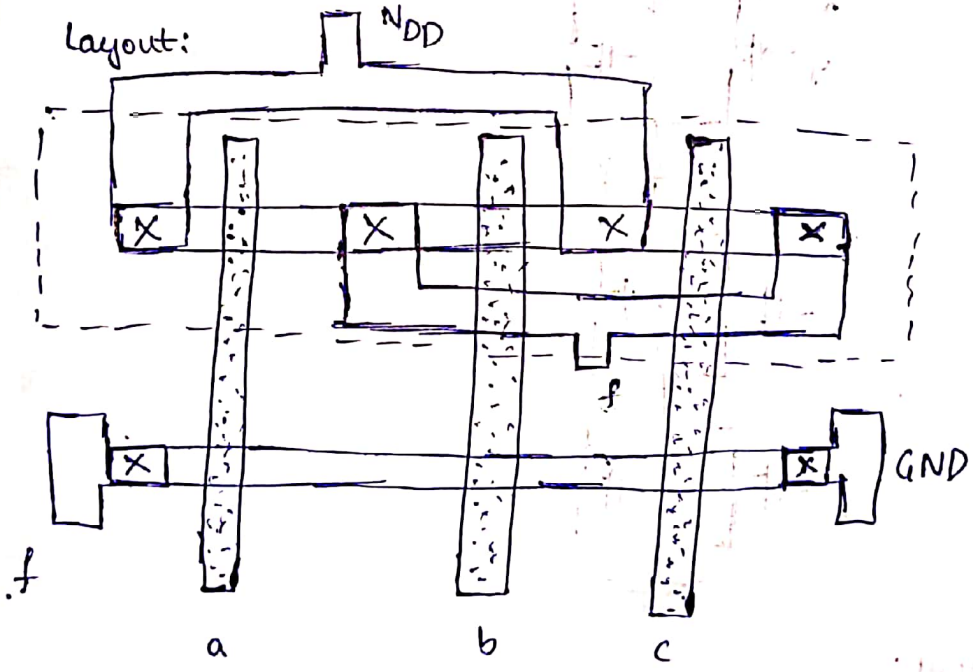
③ Layout and Stick diagram of NAND3.

Ans: $f = \overline{abc}$

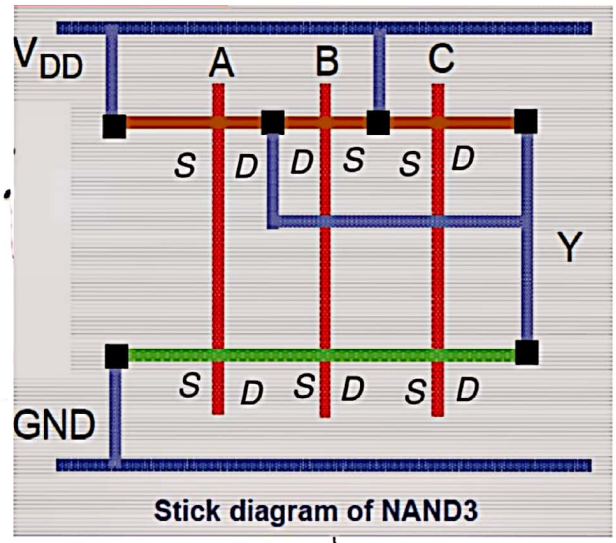
cmos circuit :



Layout:



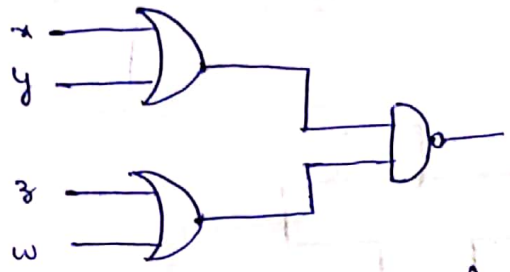
Stick Diagram:



(4)

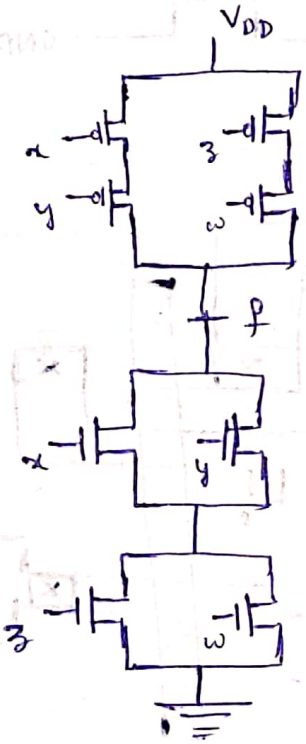
(a) Draw the logic diagram of logic circuit.

Ans:



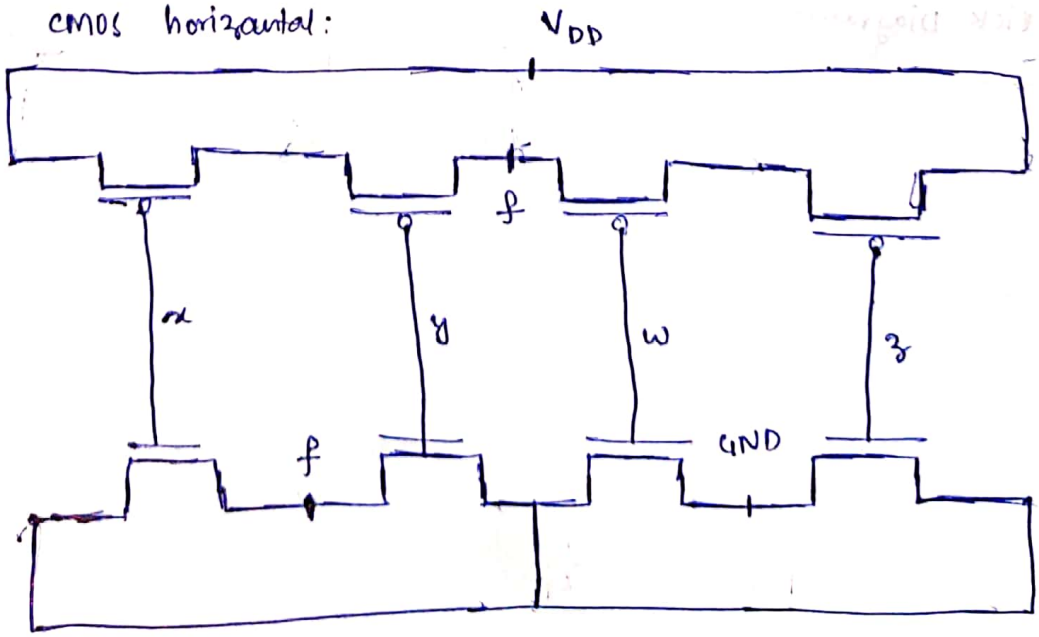
$$f = \overline{(x+y)(z+w)}$$

(b) CMOS Equivalent circuit

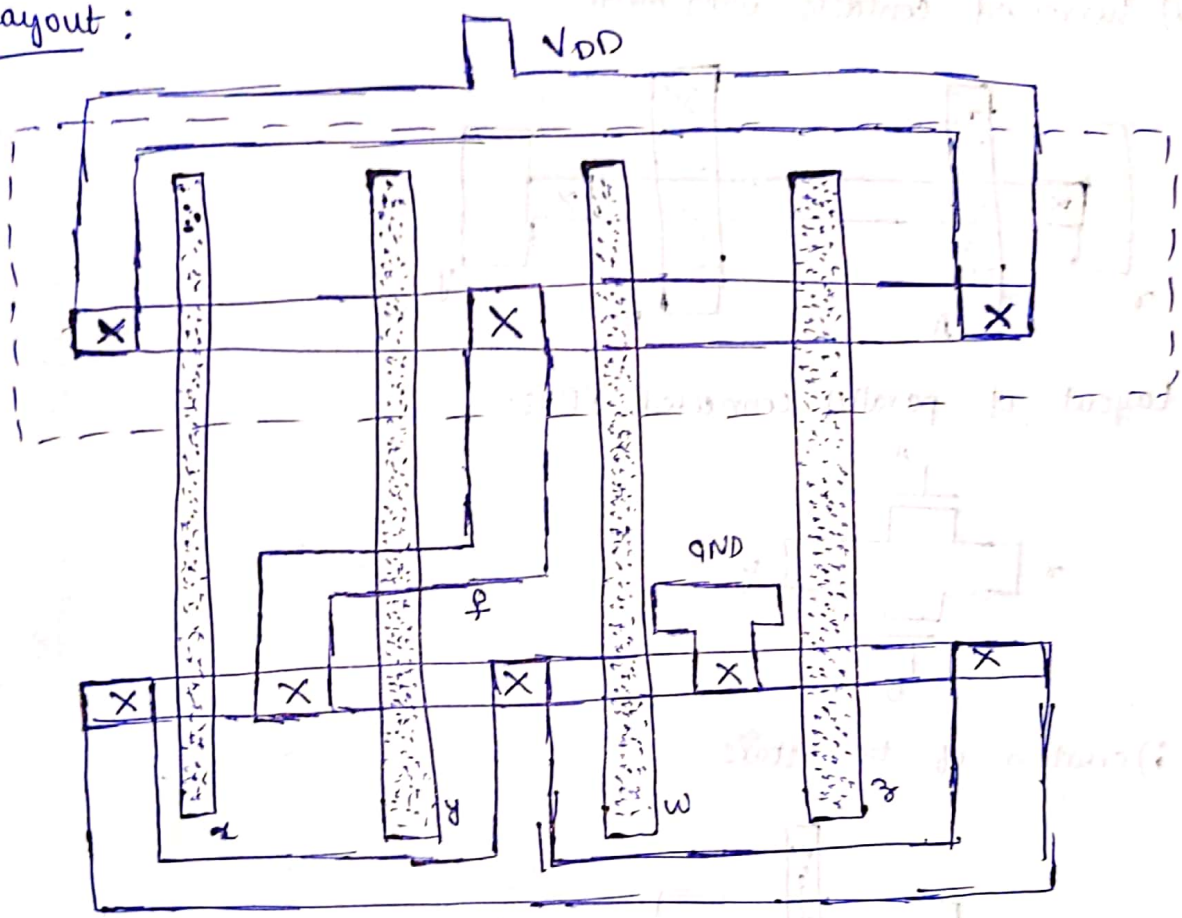


(c) Layout:

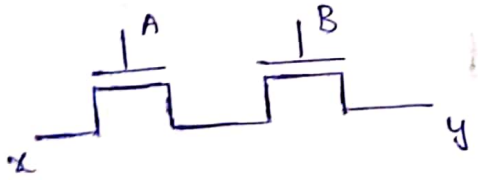
CMOS horizontal:



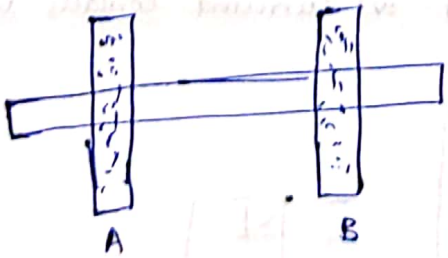
Layout :



① (a) Layout of Series connected FET;

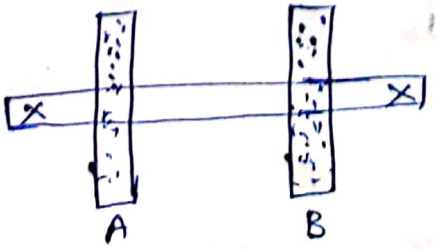


i) creation of transistor

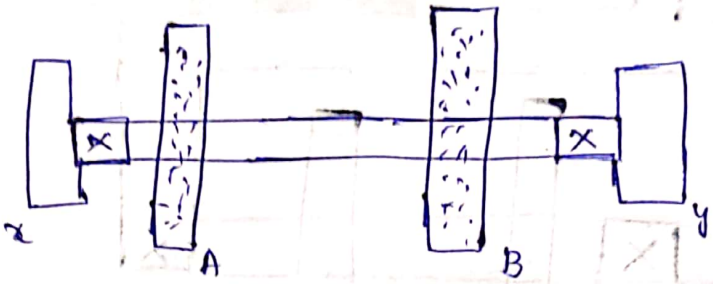


ii) Define PFET location ⇒ Here, no PFET.

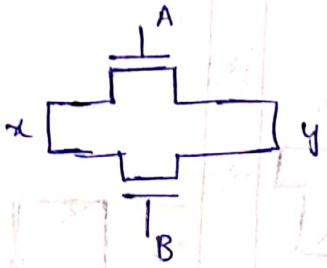
iii) create contacts



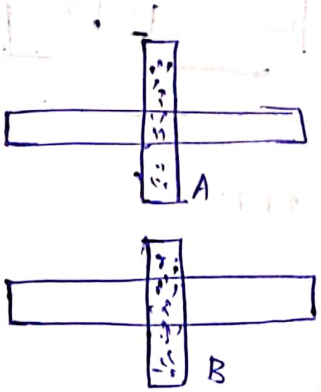
iv) Surround contacts with metal



Layout of parallel connected FETs:

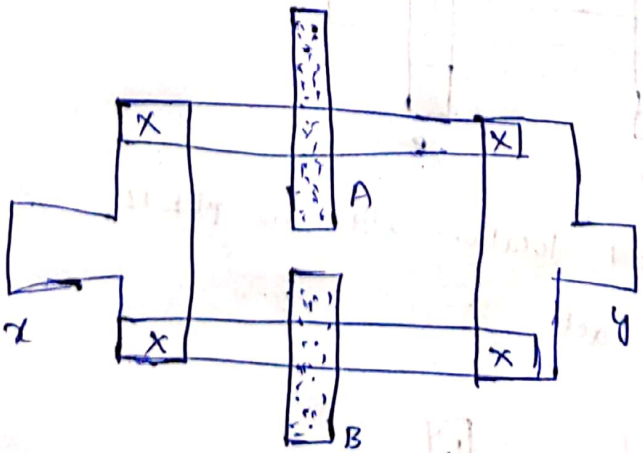


i) Creation of transistors



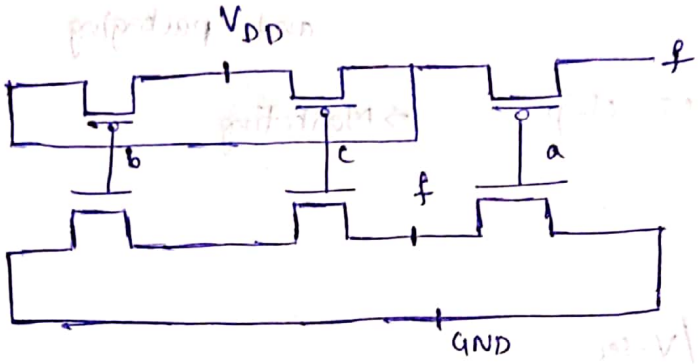
ii) Define pFET location ⇒ Here, no pFET.

iii) create contacts and iv) Surround contacts with metal

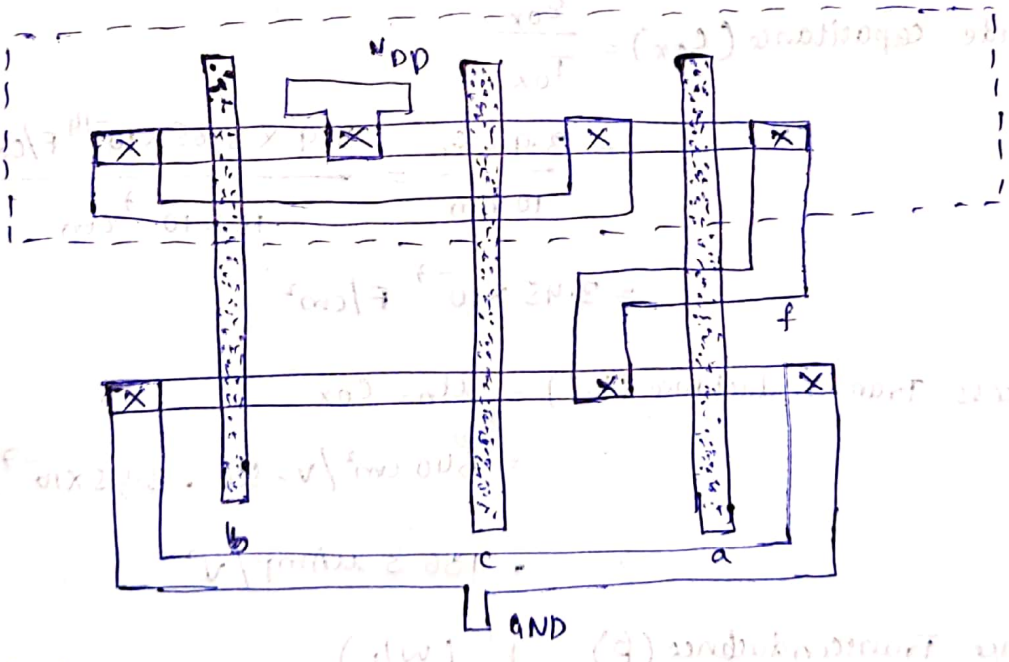


(b) Layout of $f = \overline{a + bc}$

Ans: Horizantal CMOS:



Layout:



Short Answer Questions:

Unit-1 QB

(1) Draw VLSI design Hierarchy.

Ans:

System Specifications ⇒ Initial concept

↓

Abstract - high level model ⇒ System design and verification
VHDL, Verilog HDL

↓

Logic Synthesis ⇒ Logic design and verification

↓

circuit design ⇒ CMOS design and verification

↓

Physical design ⇒ Silicon logic design and verification

↓

Manufacturing ⇒ Mass production, testing and packaging

↓

Finished VLSI chip ⇒ Marketing

(4) Ans: Given

$T_{ox} = 10nm$

$\mu_n = 540 cm^2/V\text{-}sec$

$W/L = 4$

oxide capacitance $(C_{ox}) = \frac{\varepsilon_{ox}}{T_{ox}}$

$= \frac{3.9 \times \varepsilon_0}{10\ nm} = \frac{3.9 \times 8.85 \times 10^{-14}\ F/cm^2}{10 \times 10^{-7}\ cm}$

$= 3.45 \times 10^{-7}\ F/cm^2$

Process Transconductance $(K_n') = \mu_n \cdot C_{ox}$

$= 540\ cm^2/V\text{-}sec \cdot 3.45 \times 10^{-7}\ F/cm^2$

$= 186.3\ \mu Amp/V^2$

Device Transconductance $(\beta) = k_n' (W/L)$

$= 186.3 \times 4$

$= 745.2\ \mu Amp/V^2$

Unit-2

(5) Rules for Stick diagram:

i) A red line crossing a green line creates a transistor

ii) Red over green inside a yellow border creates a pFET

iii) Red may cross blue

iv) Blue may cross red or green

v) Transistor contacts must be placed from blue to green

(4) Layout of non-inverting buffer: