QB Unit-1 LA9

Assignment-I

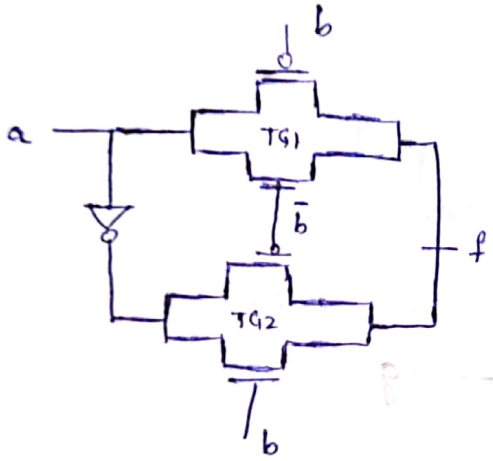
(1) (a) Identify the name of a 2 input logic gate which produce an output '1' only when the inputs are different.

Ans: XOR

(b) logical expression

Ans: $f = \bar{a}b + a\bar{b}$

(c) Draw the transmission gate

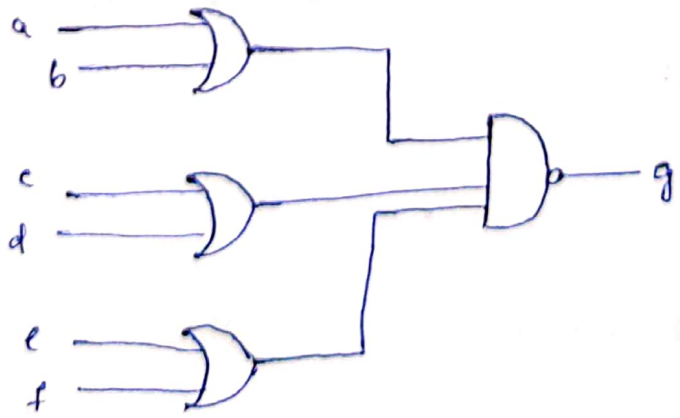


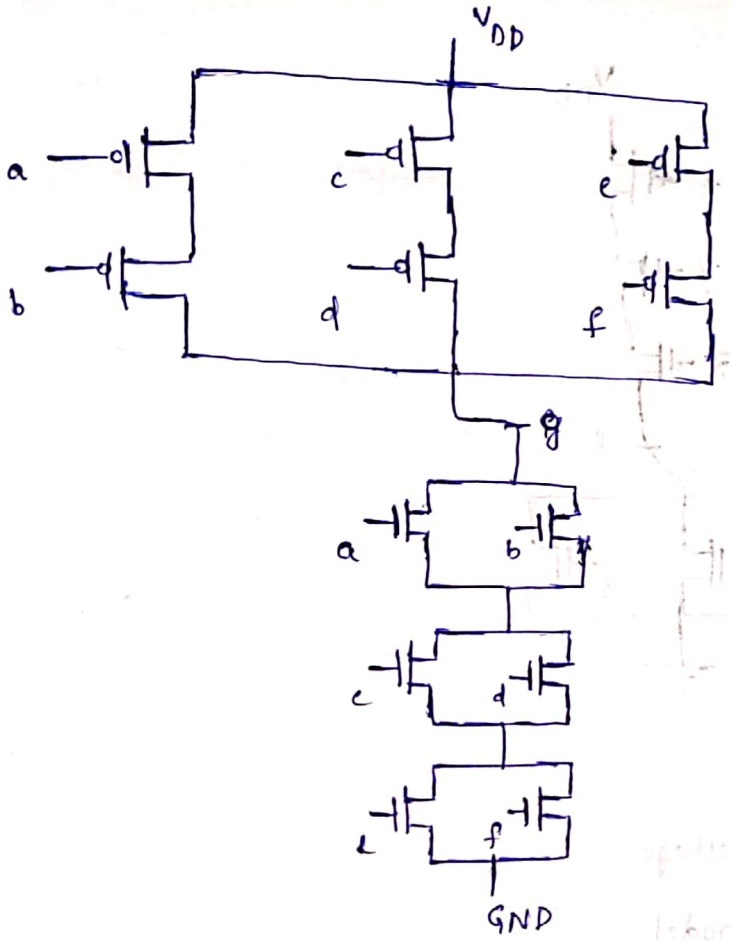
QB

(3) Use concept of bubble pushing - Draw cmos structure of

$$q = \overline{(a+b)(c+d)(e+f)}$$

Ans: Step-1 : Draw logic diagram





QB

④ (a) Logic gate 3 input – Produce output 0 when of the input is 1.

Ans: NOR 3

(b) logical expression.

Ans: $f = \overline{x+y+z}$

(c) No. of transistors for CMOS

Ans: 6

3 → nFETs

3 → pFETs

$f = \overline{x+y+z}$ ← complement

$= (\overline{x+y+z}) \cdot 1 + (x+y+z)\, 0$

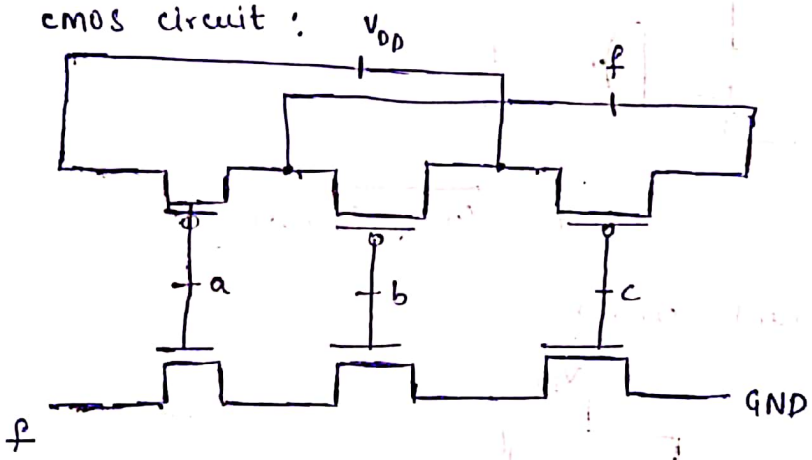
$= (\bar{x}\,\bar{y}\,\bar{z}) \cdot 1 + (x+y+z)\, 0$

pFET nFET

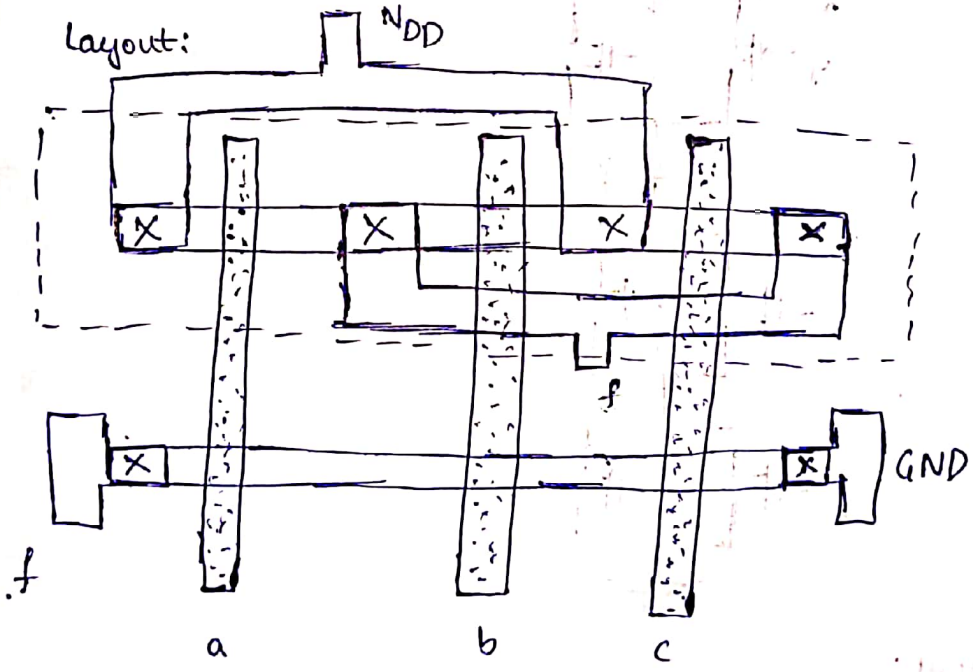
③ Layout and Stick diagram of NAND3.

Ans: $f = \overline{abc}$

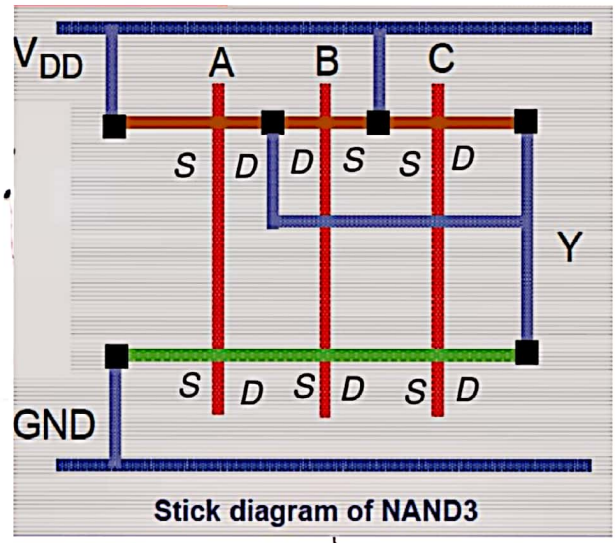
cmos circuit :



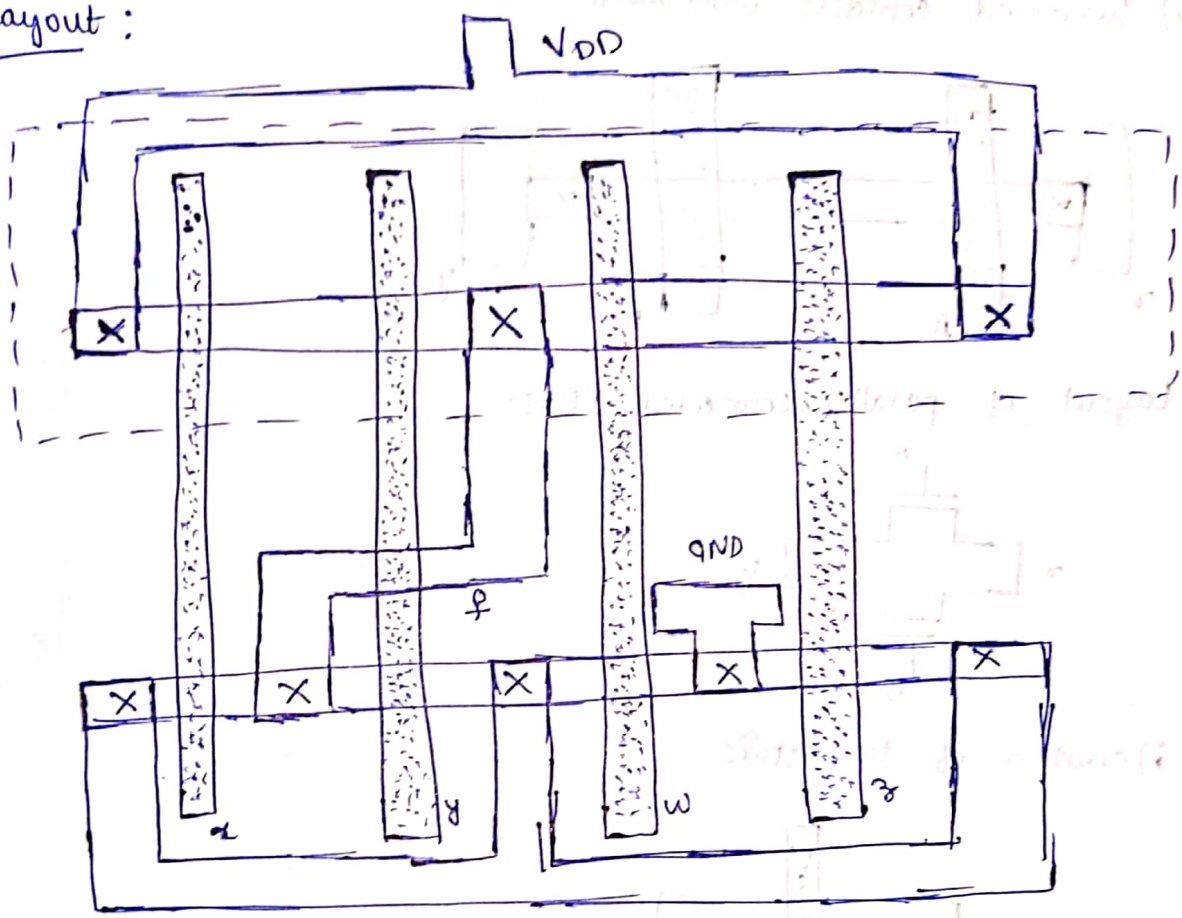
Layout:



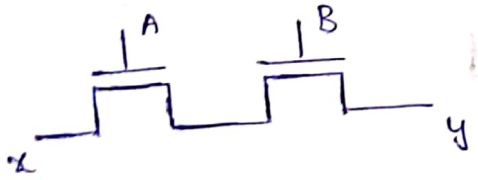
Stick Diagram:



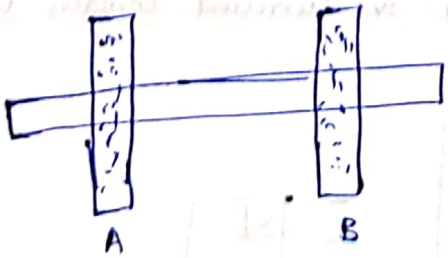
Layout :



① (a) Layout of Series connected FET;

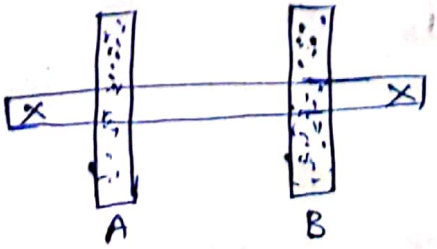


i) creation of transistor



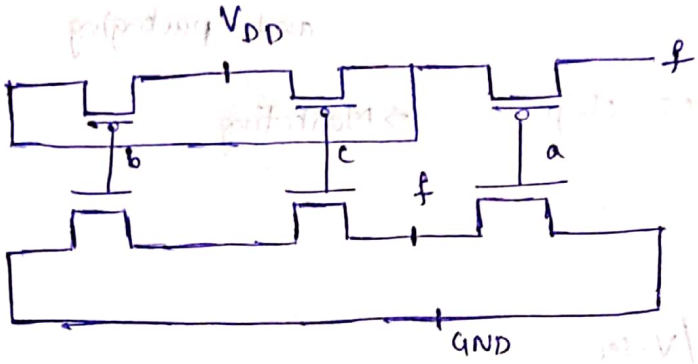
ii) Define PFET location ⇒ Here, no PFET.

iii) create contacts

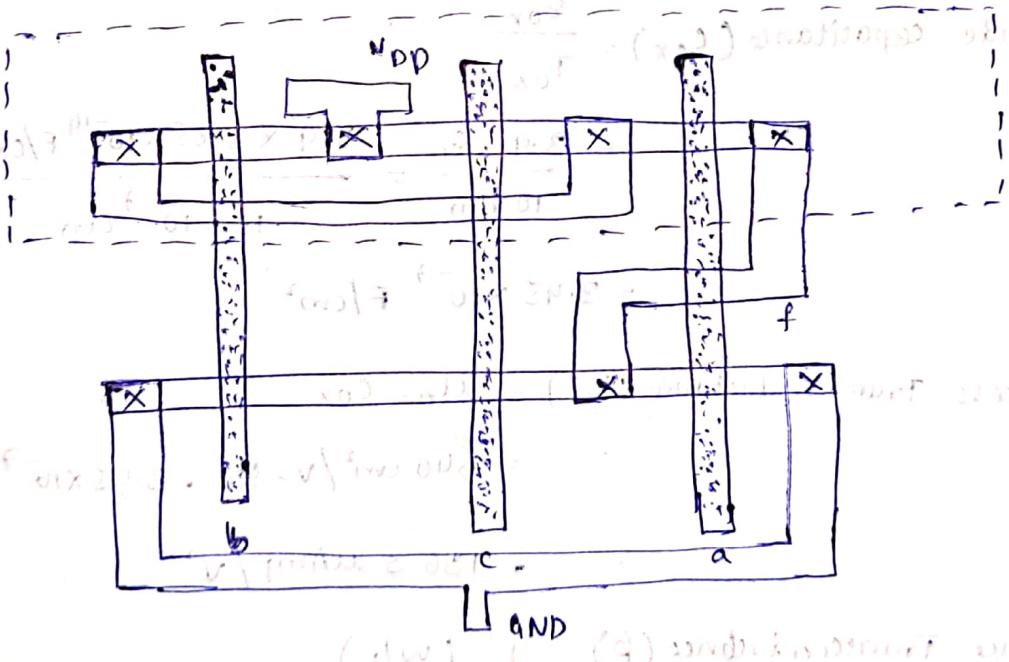


(b) Layout of $f = \overline{a + bc}$

Ans: Horizantal CMOS:



Layout:



Short Answer Questions:

Unit-1 QB

(1) Draw VLSI design Hierarchy.

Ans:

System Specifications ⇒ Initial concept

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Abstract - high level model ⇒ System design and verification
VHDL, Verilog HDL

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Logic Synthesis ⇒ Logic design and verification

↓

circuit design ⇒ CMOS design and verification

(4) Layout of non-inverting buffer: