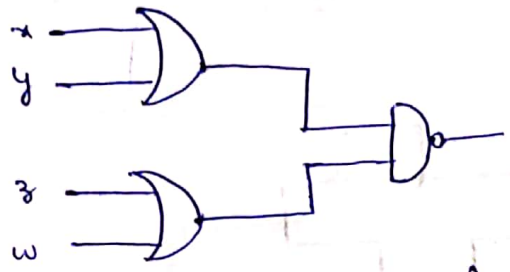
(4)

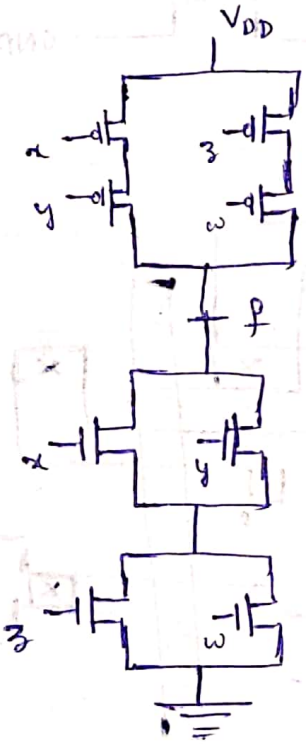
(a) Draw the logic diagram of logic circuit.

Ans:



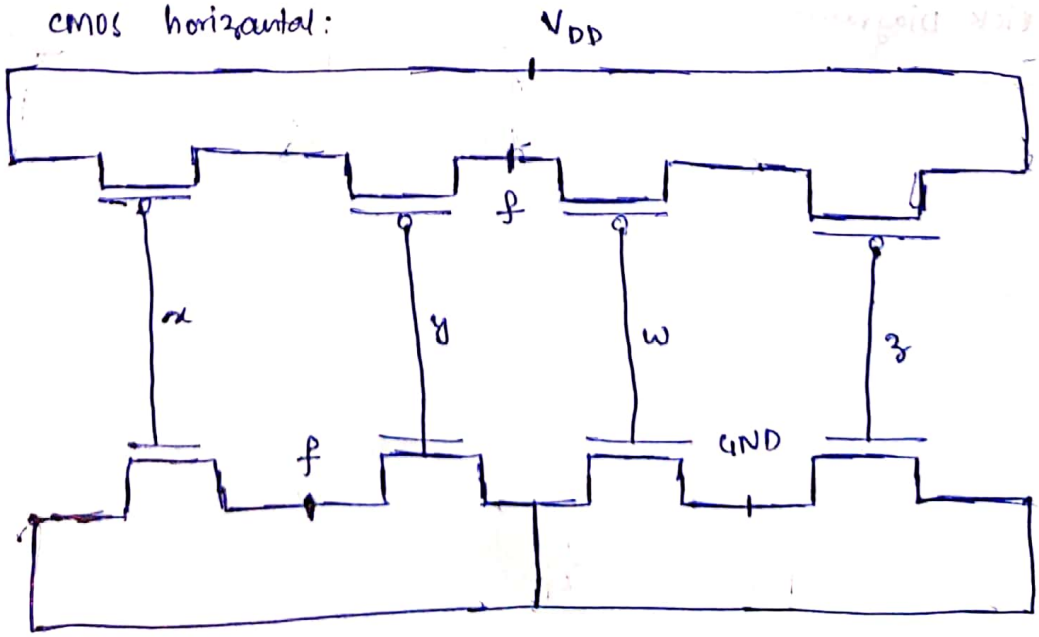
$$f = \overline{(x+y)(z+w)}$$

(b) CMOS Equivalent circuit



(c) Layout:

CMOS horizontal:



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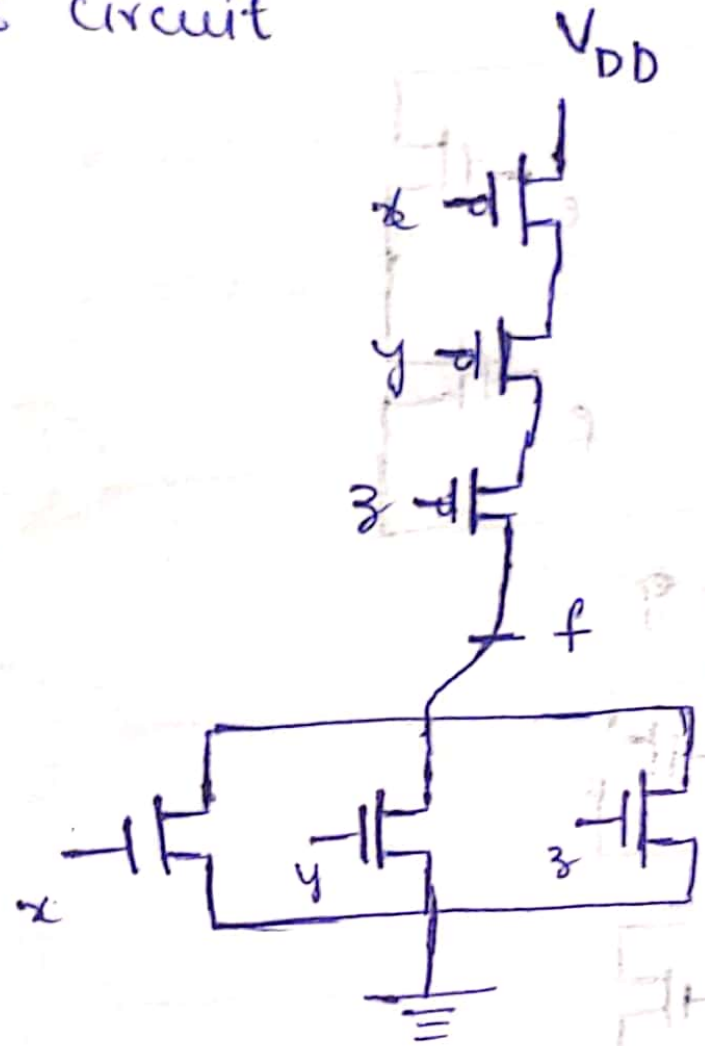
(d) CMOS Circuit



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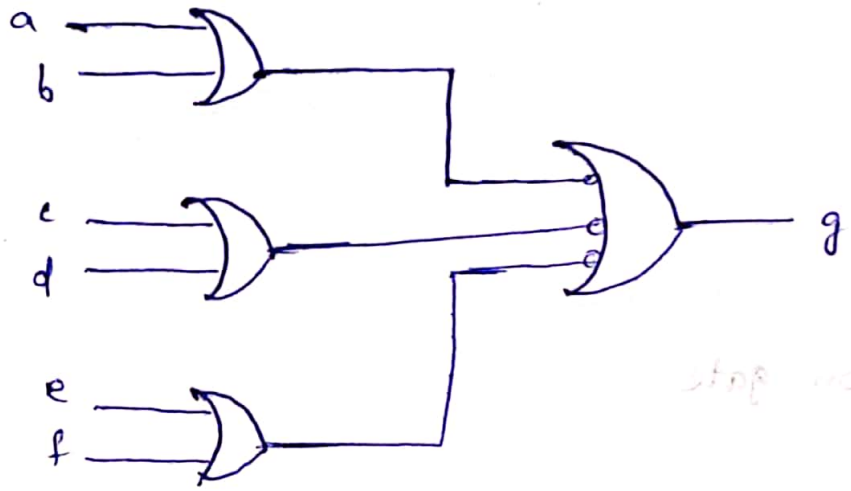
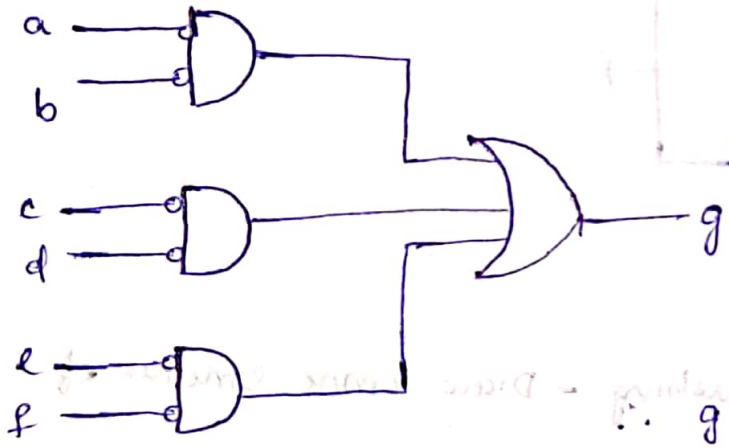
Bubble at the output is pushed to corresponding inputs.

First transformation:



Second Transformation:



$\therefore g = \bar{a}\bar{b} + \bar{c}\bar{d} + \bar{e}\bar{f}$

- PFET path of the CMOS circuit can be obtained directly from the equation.

CMOS circuit:

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↓

Physical design ⇒ Silicon logic design and verification

↓

Manufacturing ⇒ Mass production, testing and packaging

↓

Finished VLSI chip ⇒ Marketing

(4) Ans: Given

$T_{ox} = 10nm$

$\mu_n = 540 cm^2/V\text{-}sec$

$W/L = 4$

oxide capacitance $(C_{ox}) = \frac{\varepsilon_{ox}}{T_{ox}}$

$= \frac{3.9 \times \varepsilon_0}{10\ nm} = \frac{3.9 \times 8.85 \times 10^{-14}\ F/cm^2}{10 \times 10^{-7}\ cm}$

$= 3.45 \times 10^{-7}\ F/cm^2$

Process Transconductance $(K_n') = \mu_n \cdot C_{ox}$

$= 540\ cm^2/V\text{-}sec \cdot 3.45 \times 10^{-7}\ F/cm^2$

$= 186.3\ \mu Amp/V^2$

Device Transconductance $(\beta) = k_n' (W/L)$

$= 186.3 \times 4$

$= 745.2\ \mu Amp/V^2$

Unit-2

(5) Rules for Stick diagram:

i) A red line crossing a green line creates a transistor

ii) Red over green inside a yellow border creates a pFET

iii) Red may cross blue

iv) Blue may cross red or green

v) Transistor contacts must be placed from blue to green

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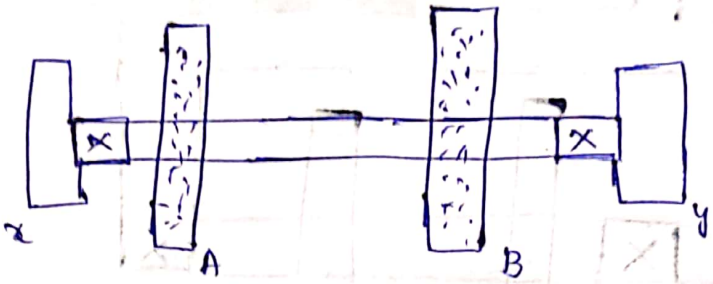
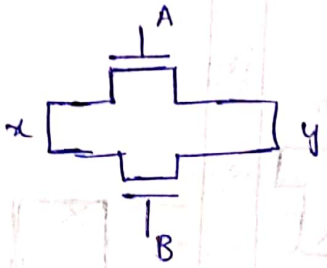
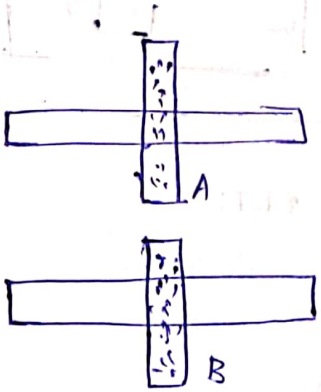
iv) Surround contacts with metal



Layout of parallel connected FETs:

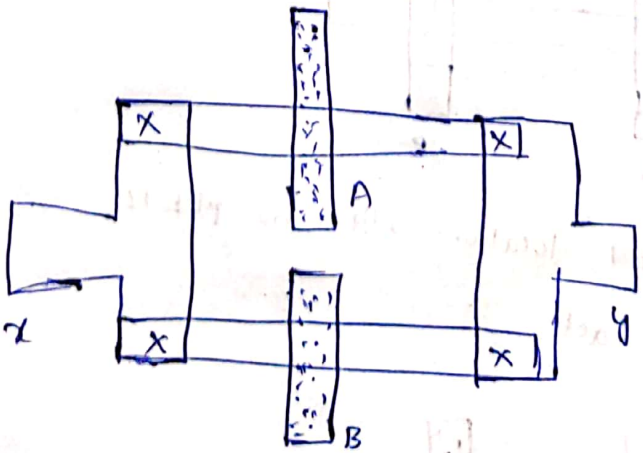


i) Creation of transistors



ii) Define pFET location ⇒ Here, no pFET.

iii) create contacts and iv) Surround contacts with metal



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