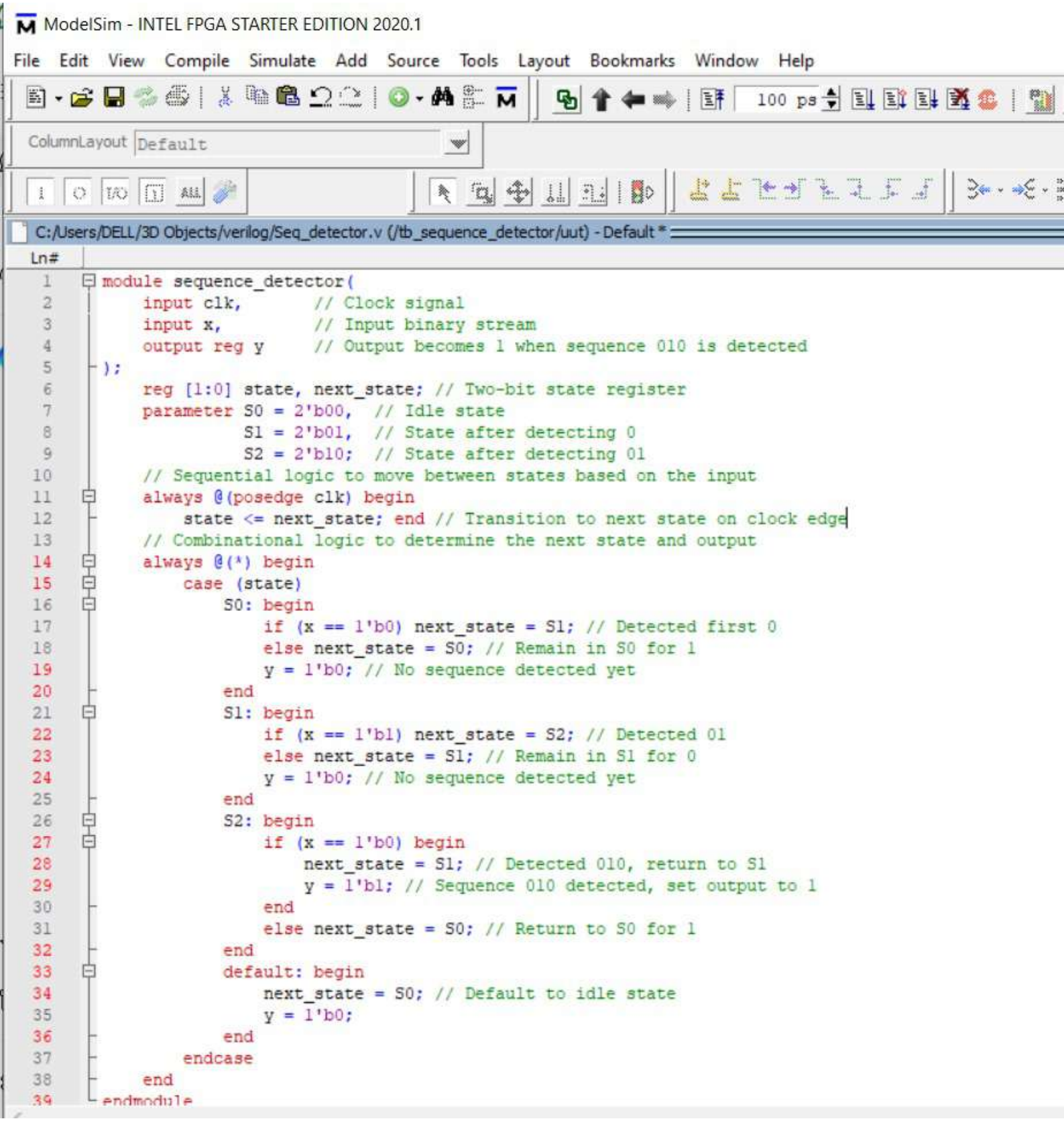
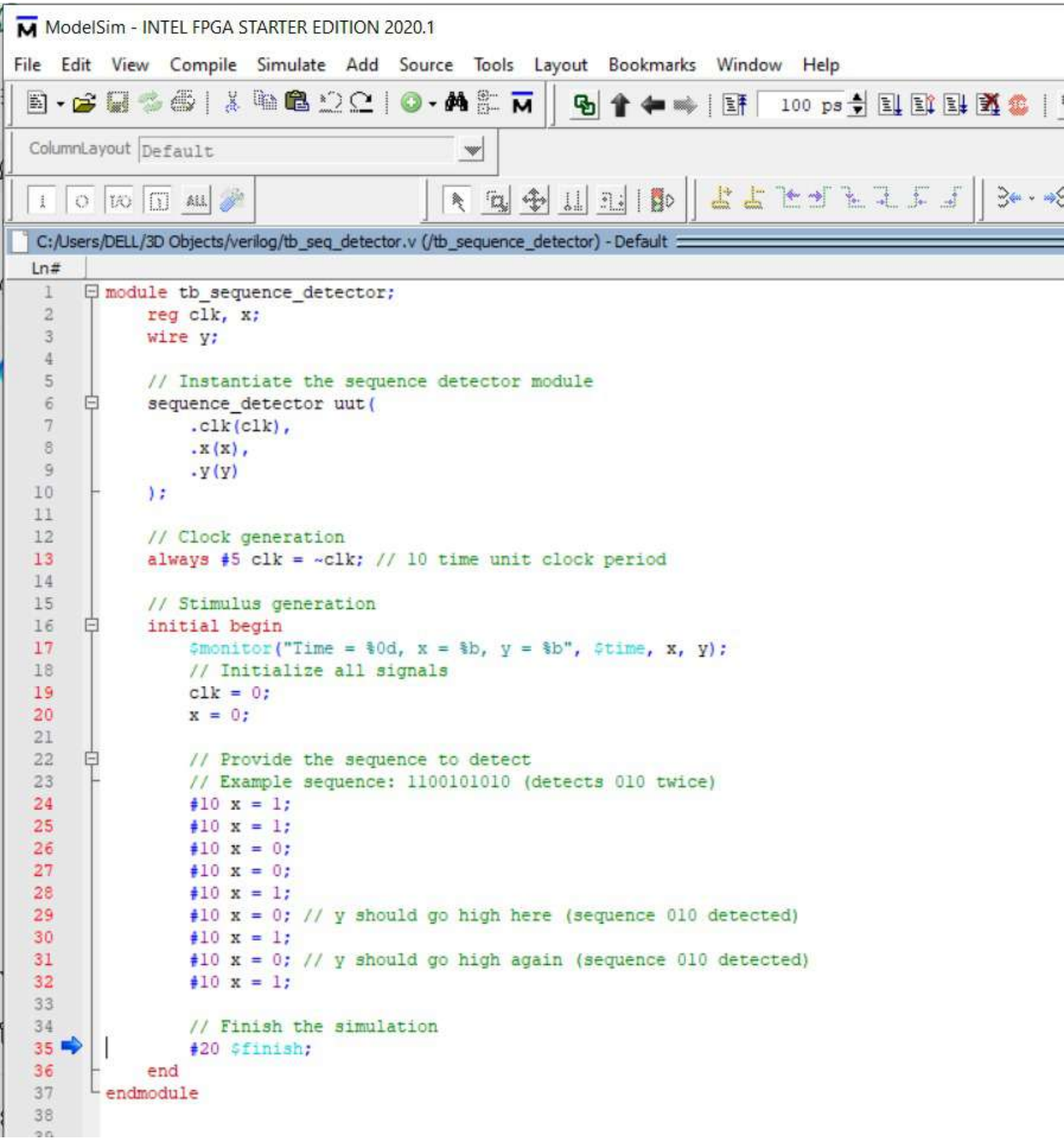
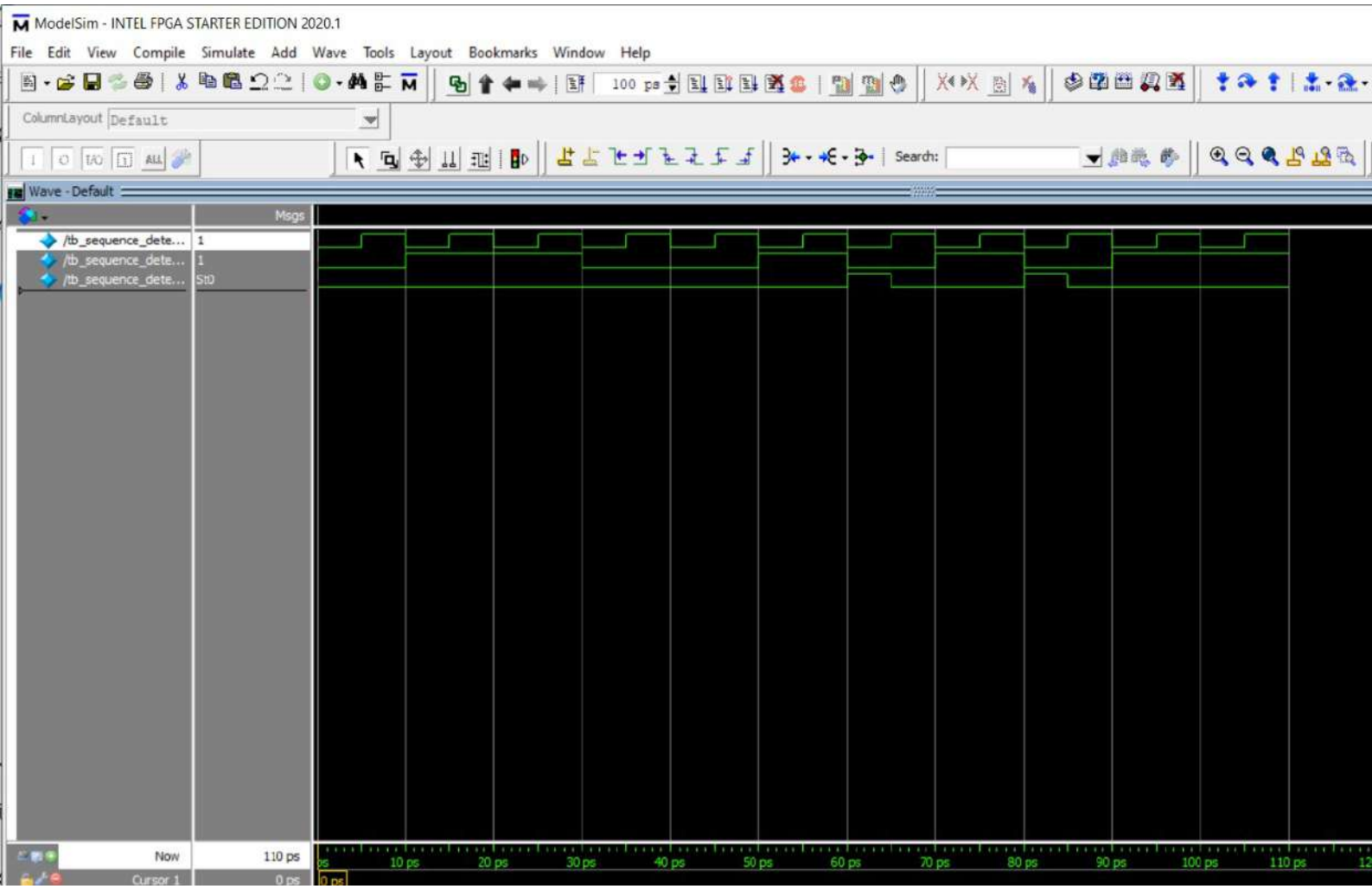

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/Seq_detector.v (/tb_sequence_detector/uut) - Default *
Ln#
1 module sequence_detector(
2 input clk, // Clock signal
3 input x, // Input binary stream
4 output reg y // Output becomes 1 when sequence 010 is detected
5);
6 reg [1:0] state, next_state; // Two-bit state register
7 parameter S0 = 2'b00, // Idle state
8 S1 = 2'b01, // State after detecting 0
9 S2 = 2'b10; // State after detecting 01
10 // Sequential logic to move between states based on the input
11 always @(posedge clk) begin
12 state <= next_state; end // Transition to next state on clock edge
13 // Combinational logic to determine the next state and output
14 always @(*) begin
15 case (state)
16 S0: begin
17 if (x == 1'b0) next_state = S1; // Detected first 0
18 else next_state = S0; // Remain in S0 for 1
19 y = 1'b0; // No sequence detected yet
20 end
21 S1: begin
22 if (x == 1'b1) next_state = S2; // Detected 01
23 else next_state = S1; // Remain in S1 for 0
24 y = 1'b0; // No sequence detected yet
25 end
26 S2: begin
27 if (x == 1'b0) begin
28 next_state = S1; // Detected 010, return to S1
29 y = 1'b1; // Sequence 010 detected, set output to 1
30 end
31 else next_state = S0; // Return to S0 for 1
32 end
33 default: begin
34 next_state = S0; // Default to idle state
35 y = 1'b0;
36 end
37 endcase
38 end
39 endmodule


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/tb_seq_detector.v (/tb_sequence_detector) - Default
Ln#
1 module tb_sequence_detector;
2 reg clk, x;
3 wire y;
4
5 // Instantiate the sequence detector module
6 sequence_detector uut(
7 .clk(clk),
8 .x(x),
9 .y(y)
10);
11
12 // Clock generation
13 always #5 clk = ~clk; // 10 time unit clock period
14
15 // Stimulus generation
16 initial begin
17 $monitor("Time = %0d, x = %b, y = %b", $time, x, y);
18 // Initialize all signals
19 clk = 0;
20 x = 0;
21
22 // Provide the sequence to detect
23 // Example sequence: 1100101010 (detects 010 twice)
24 #10 x = 1;
25 #10 x = 1;
26 #10 x = 0;
27 #10 x = 0;
28 #10 x = 1;
29 #10 x = 0; // y should go high here (sequence 010 detected)
30 #10 x = 1;
31 #10 x = 0; // y should go high again (sequence 010 detected)
32 #10 x = 1;
33
34 // Finish the simulation
35 #20 $finish;
36 end
37 endmodule
38


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
ColumnLayout Default
Search:
Wave - Default
Msgs
/tb_sequence_dete... 1
/tb_sequence_dete... 1
/tb_sequence_dete... St0
Now 110 ps
Cursor 1 0 ps
10 ps 20 ps 30 ps 40 ps 50 ps 60 ps 70 ps 80 ps 90 ps 100 ps 110 ps