ModelSim - INTEL FPGA STARTER EDITION 2020.1

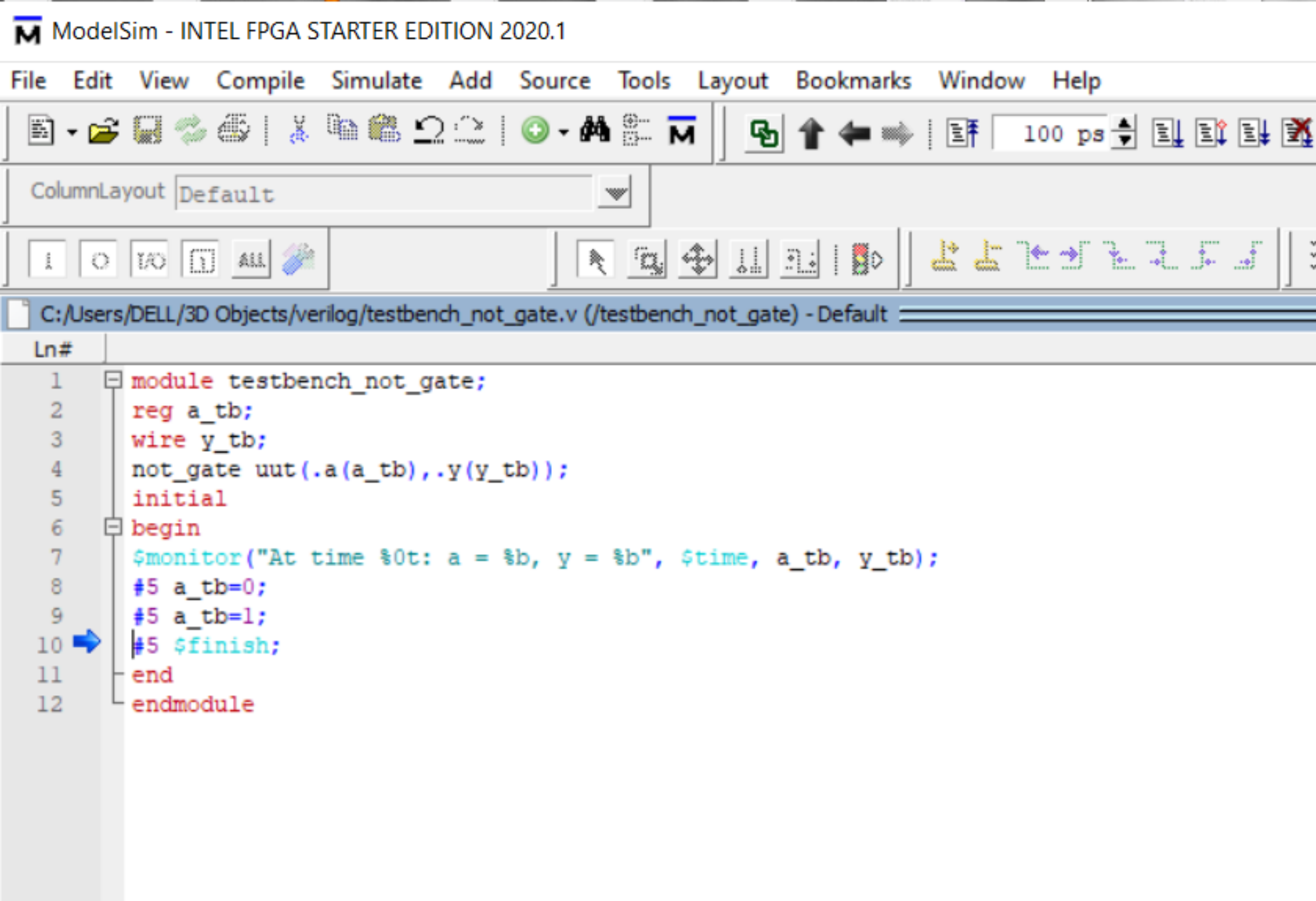
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

100 ps

ColumnLayout Default

C:/Users/DELL/3D Objects/verilog/not_gate.v (/testbench_not_gate/uut) - Default

```
Ln#
 1  module not_gate(a,y);
 2  input a;
 3  output reg y;
 4  always@(a)
 5  y=~a;
 6  endmodule
 7
```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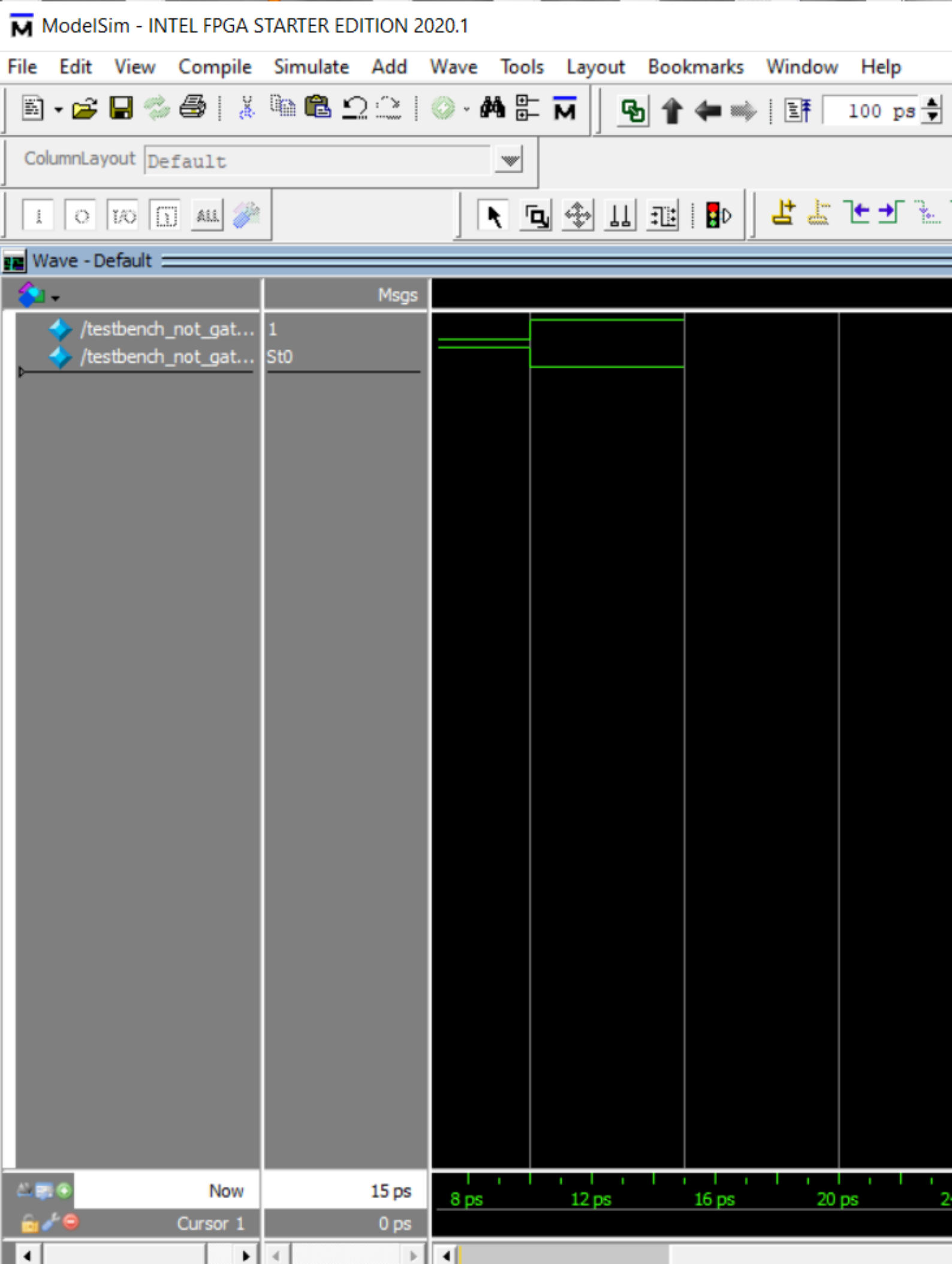
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/testbench_not_gate.v (/testbench_not_gate) - Default
Ln#
1 module testbench_not_gate;
2 reg a_tb;
3 wire y_tb;
4 not_gate uut(.a(a_tb),.y(y_tb));
5 initial
6 begin
7 $monitor("At time %0t: a = %b, y = %b", $time, a_tb, y_tb);
8 #5 a_tb=0;
9 #5 a_tb=1;
10 #5 $finish;
11 end
12 endmodule


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
Wave - Default
Msgs
/testbench_not_gat...
/testbench_not_gat...
1
St0
Now
15 ps
Cursor 1
0 ps
8 ps
12 ps
16 ps
20 ps