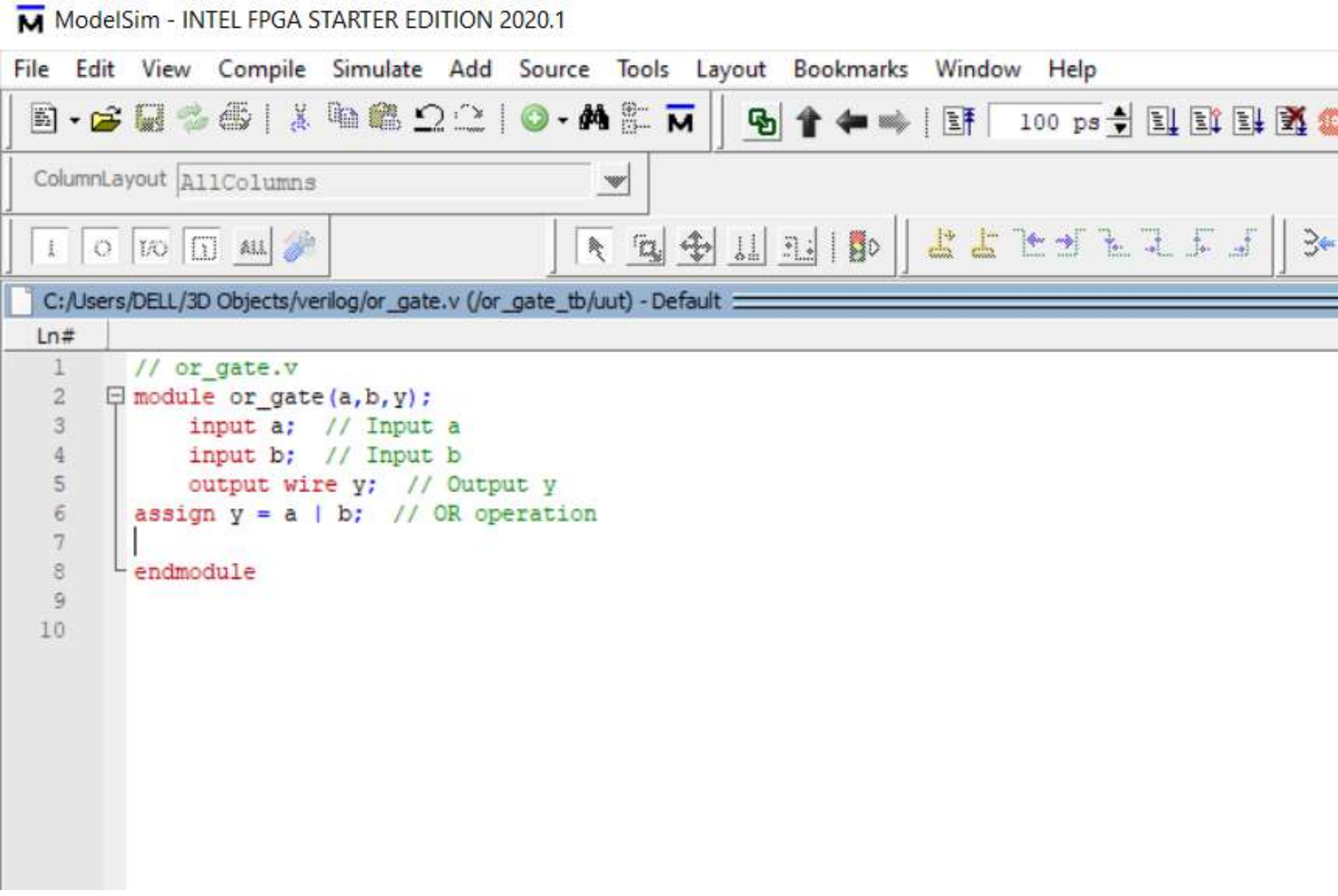
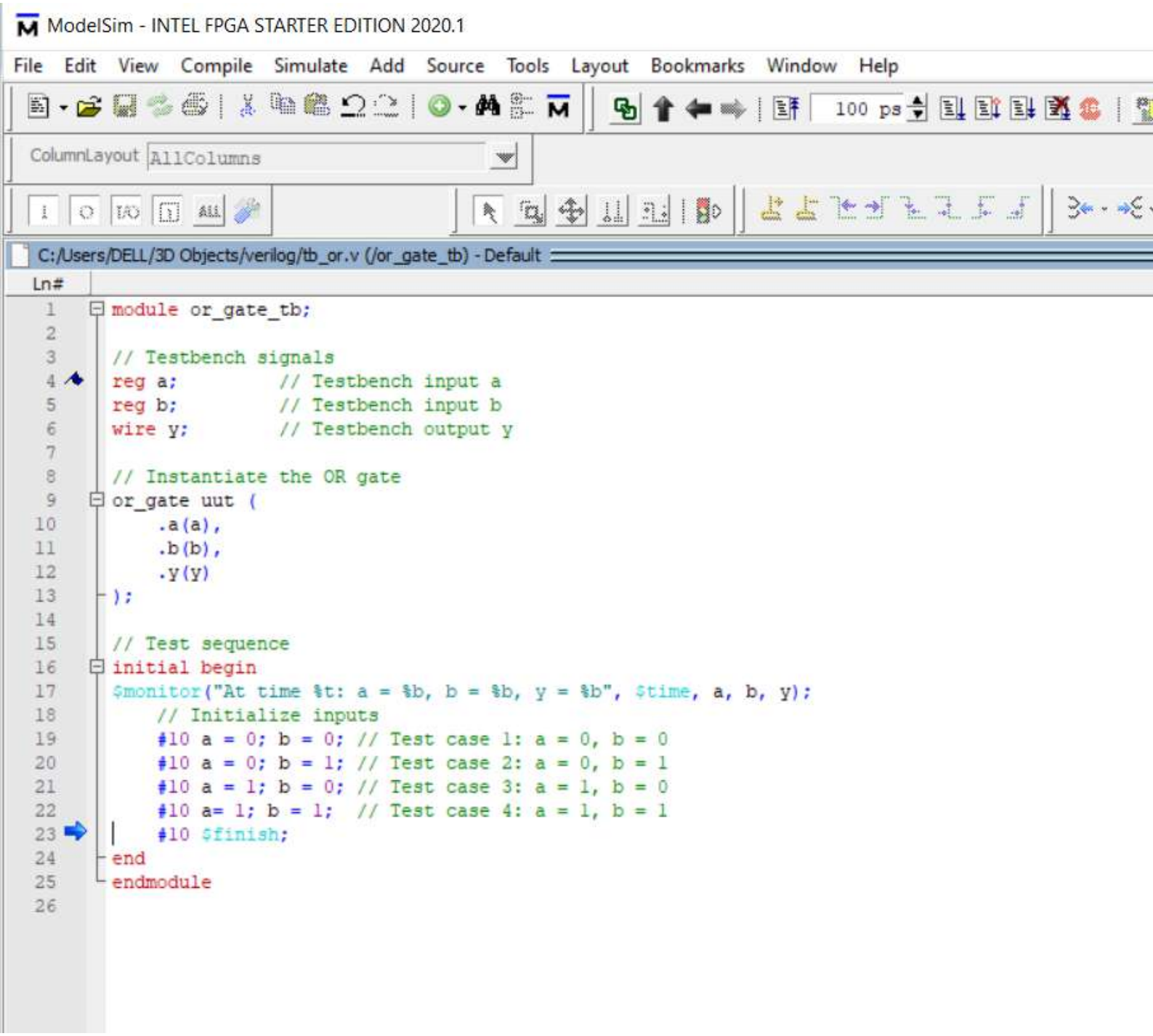
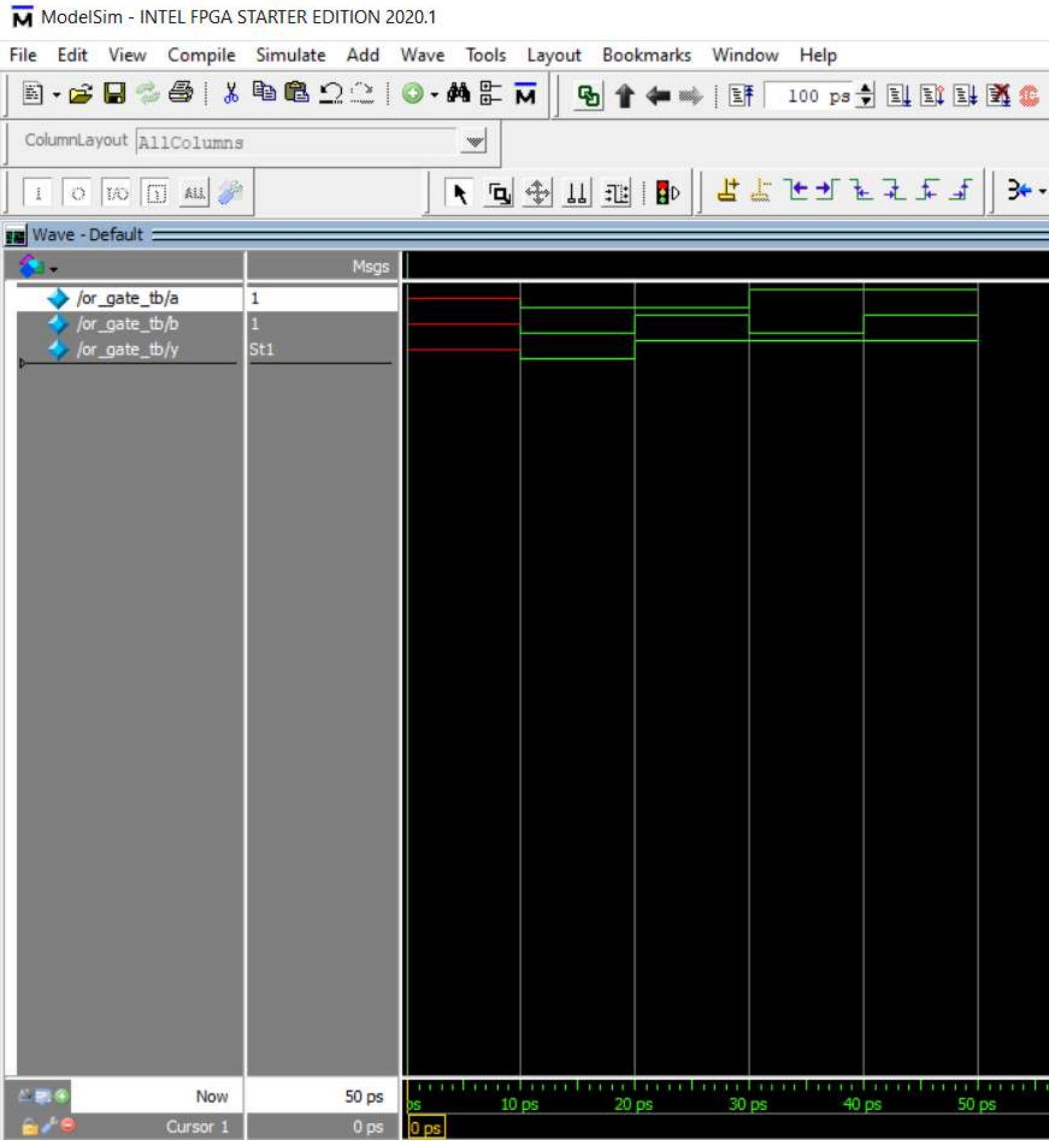

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout AllColumns
C:/Users/DELL/3D Objects/verilog/or_gate.v (/or_gate_tb/uut) - Default
Ln#
1 // or_gate.v
2 module or_gate(a,b,y);
3 input a; // Input a
4 input b; // Input b
5 output wire y; // Output y
6 assign y = a | b; // OR operation
7
8 endmodule
9
10


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout AllColumns
C:/Users/DELL/3D Objects/verilog/tb_or.v (/or_gate_tb) - Default
Ln#
1 module or_gate_tb;
2
3 // Testbench signals
4 reg a; // Testbench input a
5 reg b; // Testbench input b
6 wire y; // Testbench output y
7
8 // Instantiate the OR gate
9 or_gate uut (
10 .a(a),
11 .b(b),
12 .y(y)
13);
14
15 // Test sequence
16 initial begin
17 $monitor("At time %t: a = %b, b = %b, y = %b", $time, a, b, y);
18 // Initialize inputs
19 #10 a = 0; b = 0; // Test case 1: a = 0, b = 0
20 #10 a = 0; b = 1; // Test case 2: a = 0, b = 1
21 #10 a = 1; b = 0; // Test case 3: a = 1, b = 0
22 #10 a= 1; b = 1; // Test case 4: a = 1, b = 1
23 #10 $finish;
24 end
25 endmodule
26


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
100 ps
ColumnLayout AllColumns
Wave - Default
Msgs
/or_gate_tb/a
/or_gate_tb/b
/or_gate_tb/y
1
1
St1
Now
50 ps
Cursor 1
0 ps
10 ps
20 ps
30 ps
40 ps
50 ps
0 ps