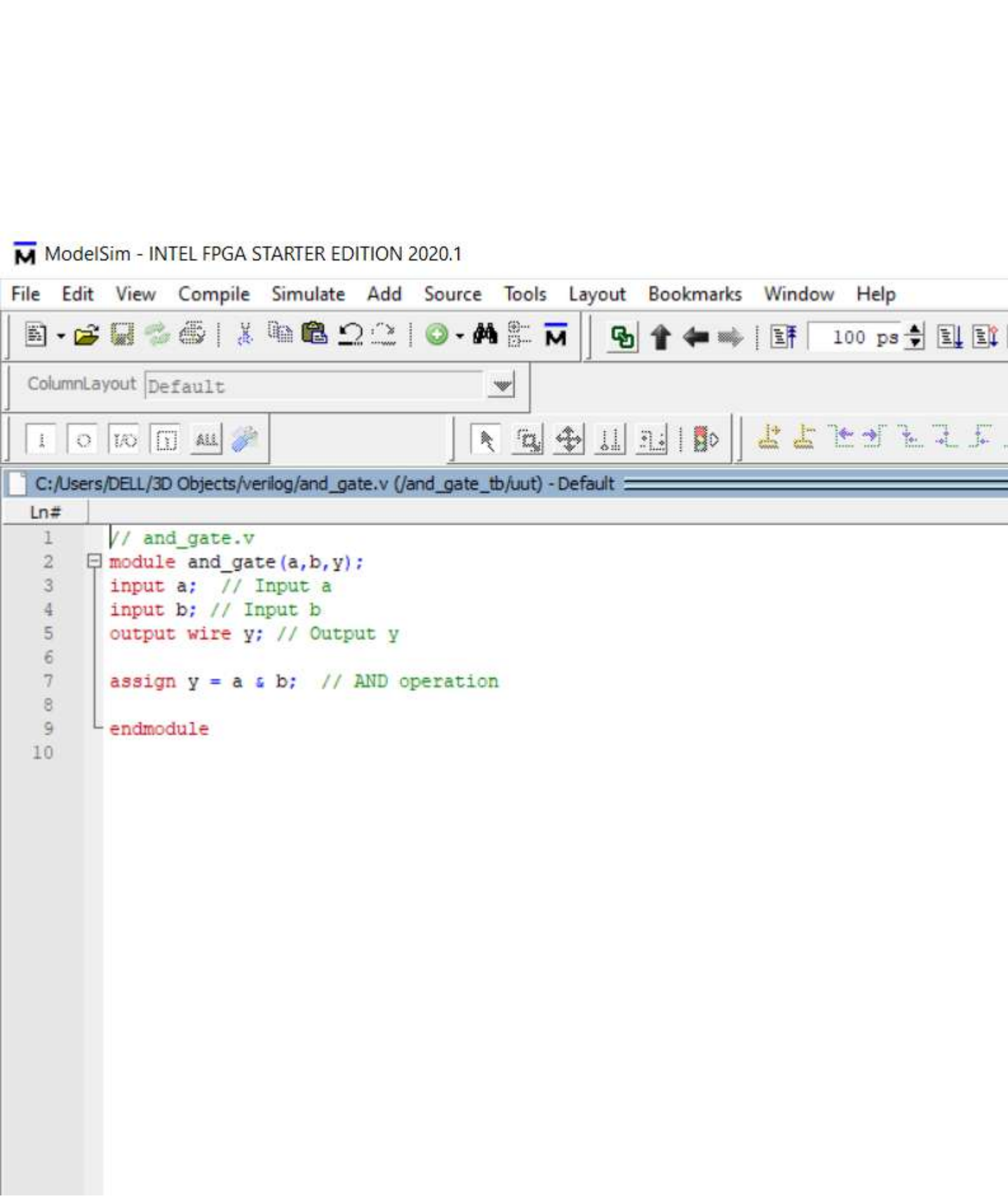
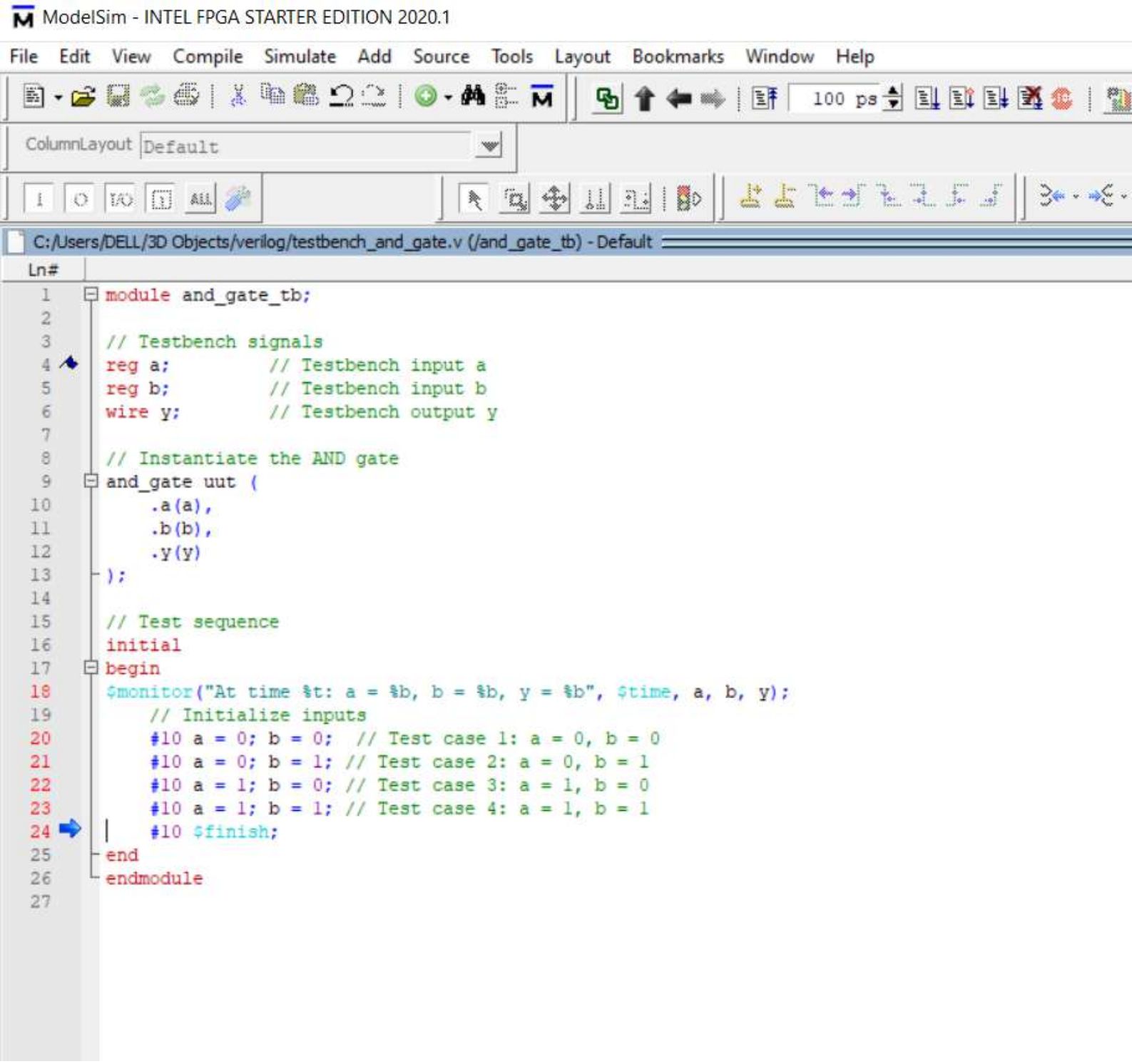
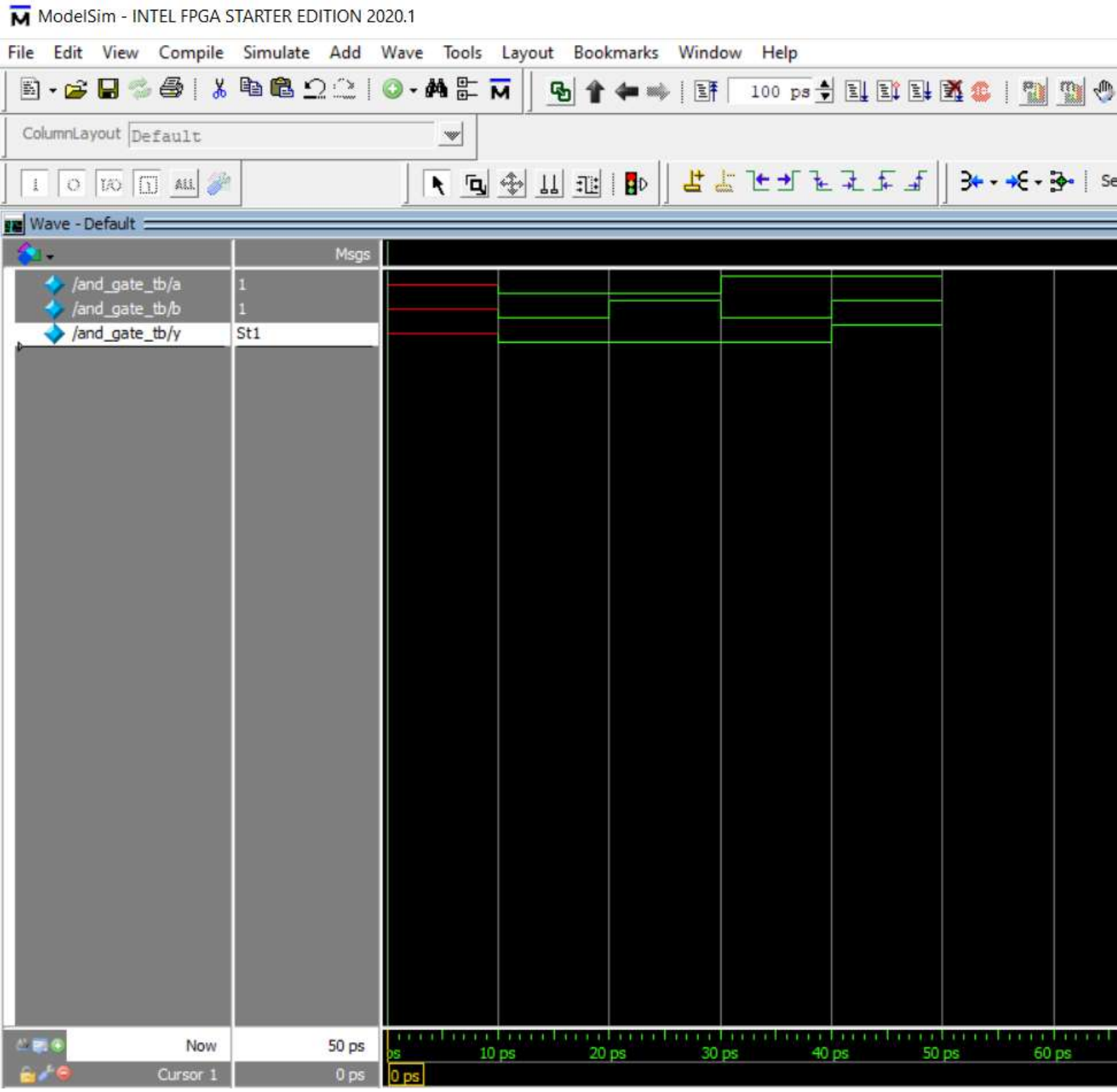

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/and_gate.v (/and_gate_tb/uut) - Default
Ln#
1 // and_gate.v
2 module and_gate(a,b,y);
3 input a; // Input a
4 input b; // Input b
5 output wire y; // Output y
6
7 assign y = a & b; // AND operation
8
9 endmodule
10


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/testbench_and_gate.v (/and_gate_tb) - Default
Ln#
1 module and_gate_tb;
2
3 // Testbench signals
4 reg a; // Testbench input a
5 reg b; // Testbench input b
6 wire y; // Testbench output y
7
8 // Instantiate the AND gate
9 and_gate uut (
10 .a(a),
11 .b(b),
12 .y(y)
13);
14
15 // Test sequence
16 initial
17 begin
18 $monitor("At time %t: a = %b, b = %b, y = %b", $time, a, b, y);
19 // Initialize inputs
20 #10 a = 0; b = 0; // Test case 1: a = 0, b = 0
21 #10 a = 0; b = 1; // Test case 2: a = 0, b = 1
22 #10 a = 1; b = 0; // Test case 3: a = 1, b = 0
23 #10 a = 1; b = 1; // Test case 4: a = 1, b = 1
24 #10 $finish;
25 end
26 endmodule
27


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
Wave - Default
Msgs
/and_gate_tb/a
/and_gate_tb/b
/and_gate_tb/y
1
1
St1
Now
50 ps
Cursor 1
0 ps
10 ps
20 ps
30 ps
40 ps
50 ps
60 ps
0 ps