

ModelSim - INTEL FPGA STARTER EDITION 2020.1

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C:/Users/DELL/3D Objects/verilog/full\_adder.v (/full\_adder\_tb/uut) - Default

```
Ln#
1 module full_adder(a,b,cin,sum,cout);
2   input a;      // Input a
3   input b;      // Input b
4   input cin;    // Carry-in
5   output sum;   // Sum
6   output cout;  // Carry-out
7
8   assign sum = a ^ b ^ cin; // Sum calculation
9   assign cout = (a & b) | (b & cin) | (a & cin); // Carry-out calculation
10
11 endmodule
12
```



C:/Users/DELL/3D Objects/verilog/tb\_FA.v (/full\_adder\_tb) - Default

```
Ln#
1  module full_adder_tb;
2
3  // Testbench signals
4  reg a;           // Testbench input a
5  reg b;           // Testbench input b
6  reg cin;         // Testbench carry-in
7  wire sum;        // Testbench sum output
8  wire cout;       // Testbench carry-out output
9
10 // Instantiate the full adder
11 full_adder uut (
12     .a(a),
13     .b(b),
14     .cin(cin),
15     .sum(sum),
16     .cout(cout)
17 );
18
19 // Test sequence
20 initial
21 begin
22     $monitor("At time %t: a = %b, b = %b, cin = %b, sum = %b, cout = %b", $time, a, b, cin, sum, cout);
23     // Initialize inputs and apply test cases
24     #10 a = 0; b = 0; cin = 0; // Test case 1: a = 0, b = 0, cin = 0
25     #10 a = 0; b = 0; cin = 1; // Test case 2: a = 0, b = 0, cin = 1
26     #10 a = 0; b = 1; cin = 0; // Test case 3: a = 0, b = 1, cin = 0
27     #10 a = 0; b = 1; cin = 1; // Test case 4: a = 0, b = 1, cin = 1
28     #10 a = 1; b = 0; cin = 0; // Test case 5: a = 1, b = 0, cin = 0
29     #10 a = 1; b = 0; cin = 1; // Test case 6: a = 1, b = 0, cin = 1
30     #10 a = 1; b = 1; cin = 0; // Test case 7: a = 1, b = 1, cin = 0
31     #10 a = 1; b = 1; cin = 1; // Test case 8: a = 1, b = 1, cin = 1
32     #10 $finish;
33 end
34 endmodule
35
```

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Wave - Default

