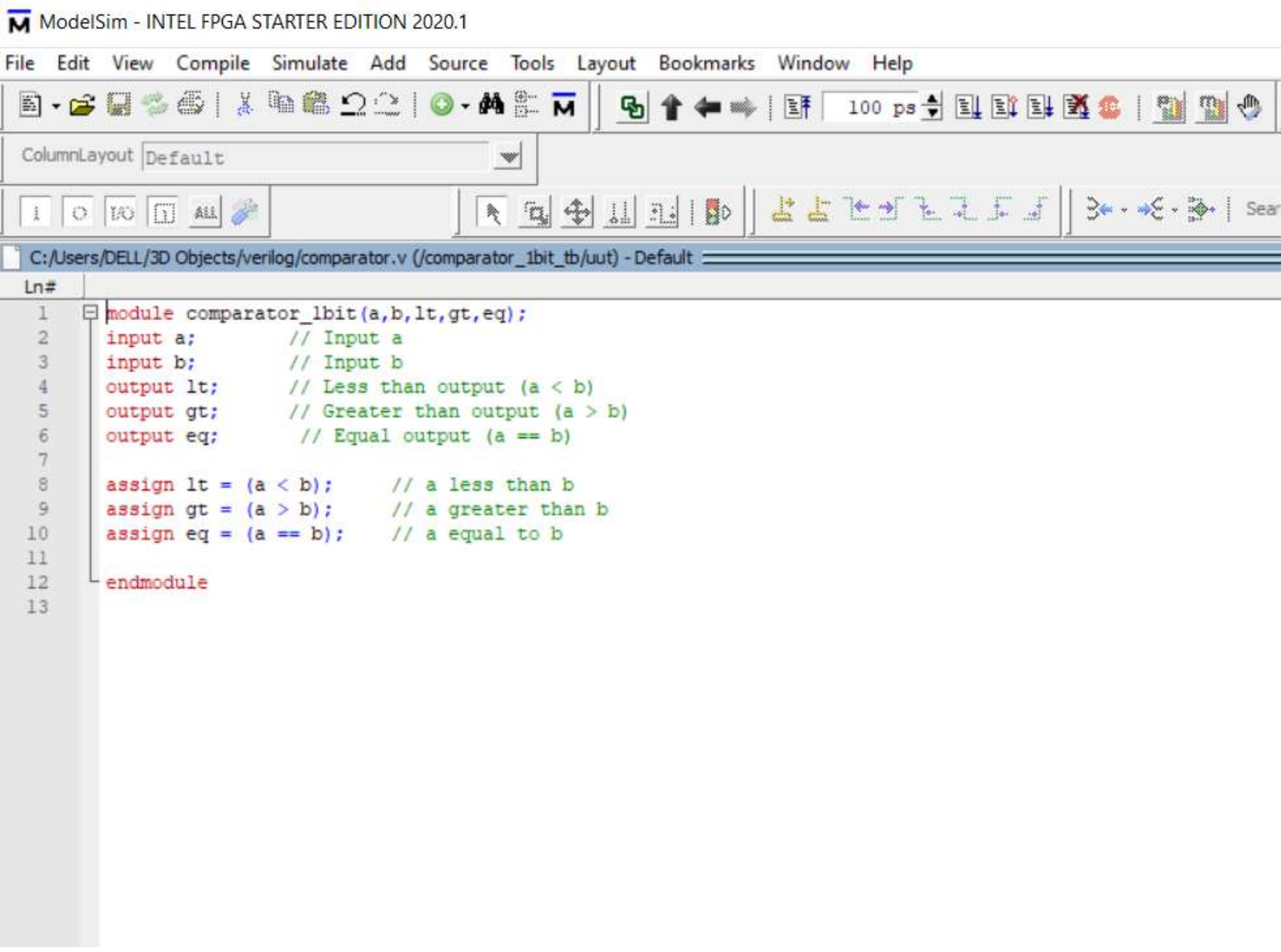
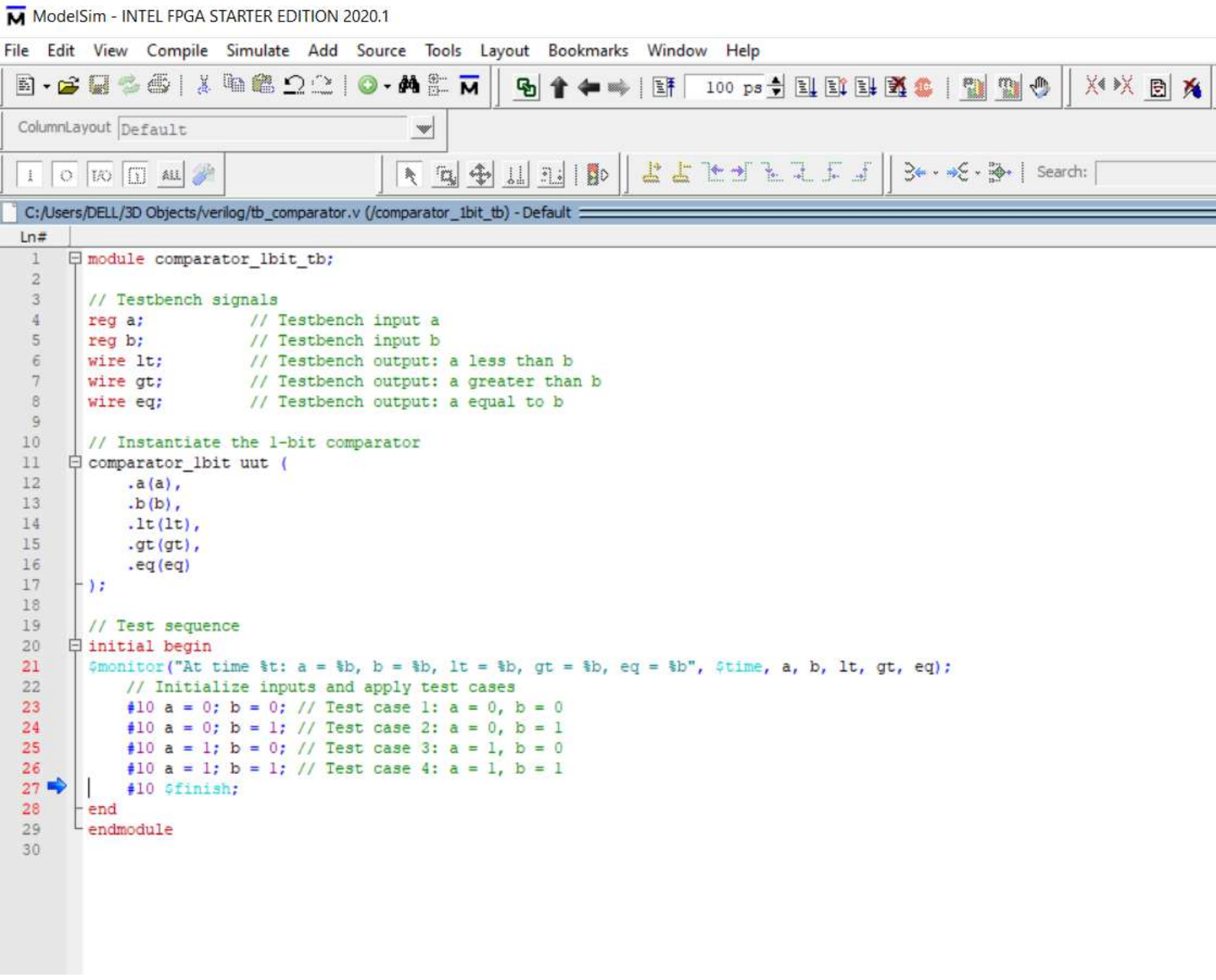

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/comparator.v (/comparator_1bit_tb/uut) - Default
Ln#
1 module comparator_1bit(a,b,lt,gt,eq);
2 input a; // Input a
3 input b; // Input b
4 output lt; // Less than output (a < b)
5 output gt; // Greater than output (a > b)
6 output eq; // Equal output (a == b)
7
8 assign lt = (a < b); // a less than b
9 assign gt = (a > b); // a greater than b
10 assign eq = (a == b); // a equal to b
11
12 endmodule
13


ModelSim - INTEL FPGA STARTER EDITION 2020.1
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100 ps
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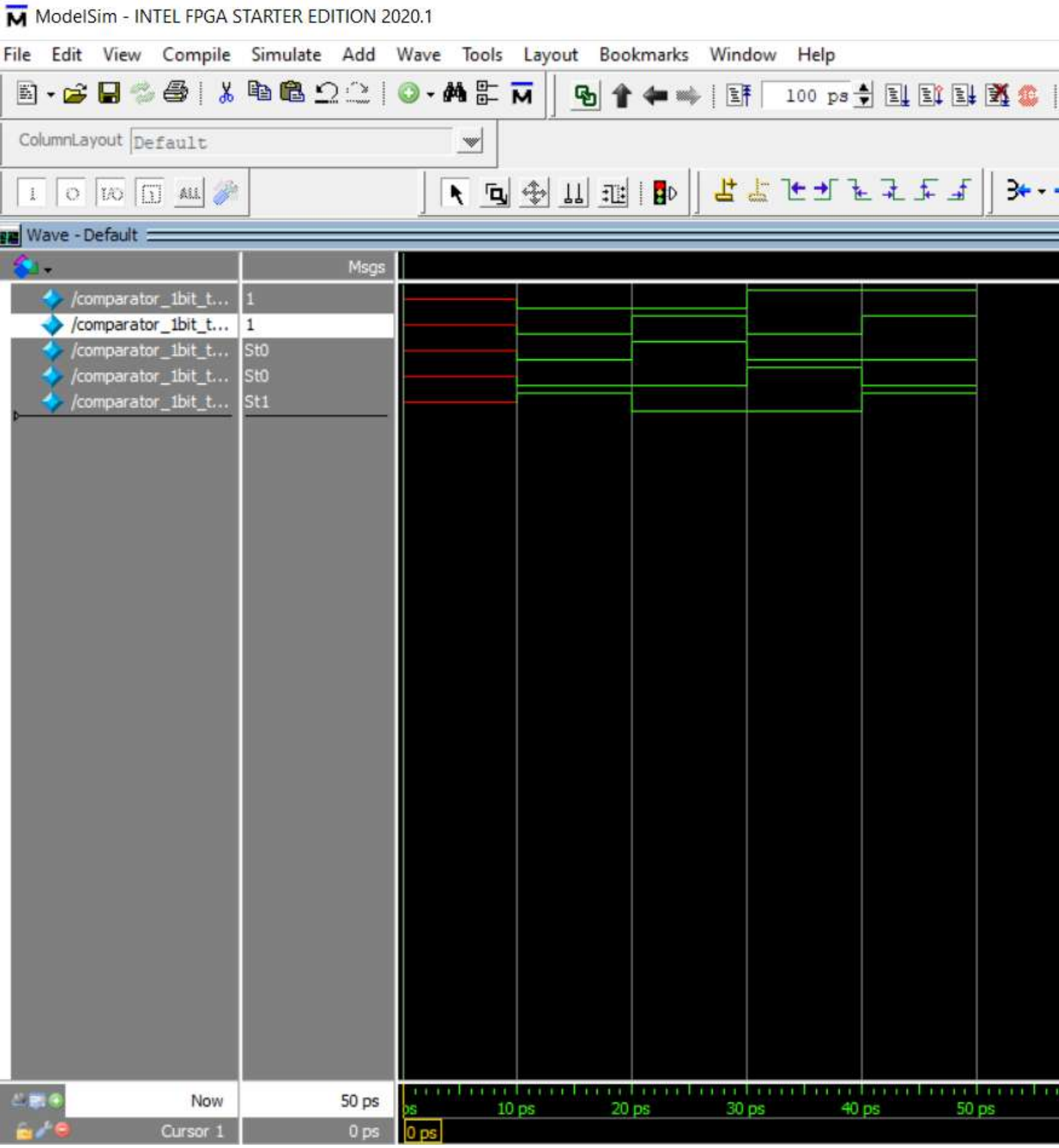
C:/Users/DELL/3D Objects/verilog/tb_comparator.v (/comparator_1bit_tb) - Default
Ln#
1 module comparator_1bit_tb;
2
3 // Testbench signals
4 reg a; // Testbench input a
5 reg b; // Testbench input b
6 wire lt; // Testbench output: a less than b
7 wire gt; // Testbench output: a greater than b
8 wire eq; // Testbench output: a equal to b
9
10 // Instantiate the 1-bit comparator
11 comparator_1bit uut (
12 .a(a),
13 .b(b),
14 .lt(lt),
15 .gt(gt),
16 .eq(eq)
17 );
18
19 // Test sequence
20 initial begin
21 $monitor("At time %t: a = %b, b = %b, lt = %b, gt = %b, eq = %b", $time, a, b, lt, gt, eq);
22 // Initialize inputs and apply test cases
23 #10 a = 0; b = 0; // Test case 1: a = 0, b = 0
24 #10 a = 0; b = 1; // Test case 2: a = 0, b = 1
25 #10 a = 1; b = 0; // Test case 3: a = 1, b = 0
26 #10 a = 1; b = 1; // Test case 4: a = 1, b = 1
27 #10 $finish;
28 end
29 endmodule
30


ModelSim - INTEL FPGA STARTER EDITION 2020.1
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100 ps
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Wave - Default
Msgs
/comparator_1bit_t...
/comparator_1bit_t...
/comparator_1bit_t...
/comparator_1bit_t...
/comparator_1bit_t...
1
1
St0
St0
St1
Now
50 ps
Cursor 1
0 ps
10 ps
20 ps
30 ps
40 ps
50 ps
0 ps