ModelSim - INTEL FPGA STARTER EDITION 2020.1

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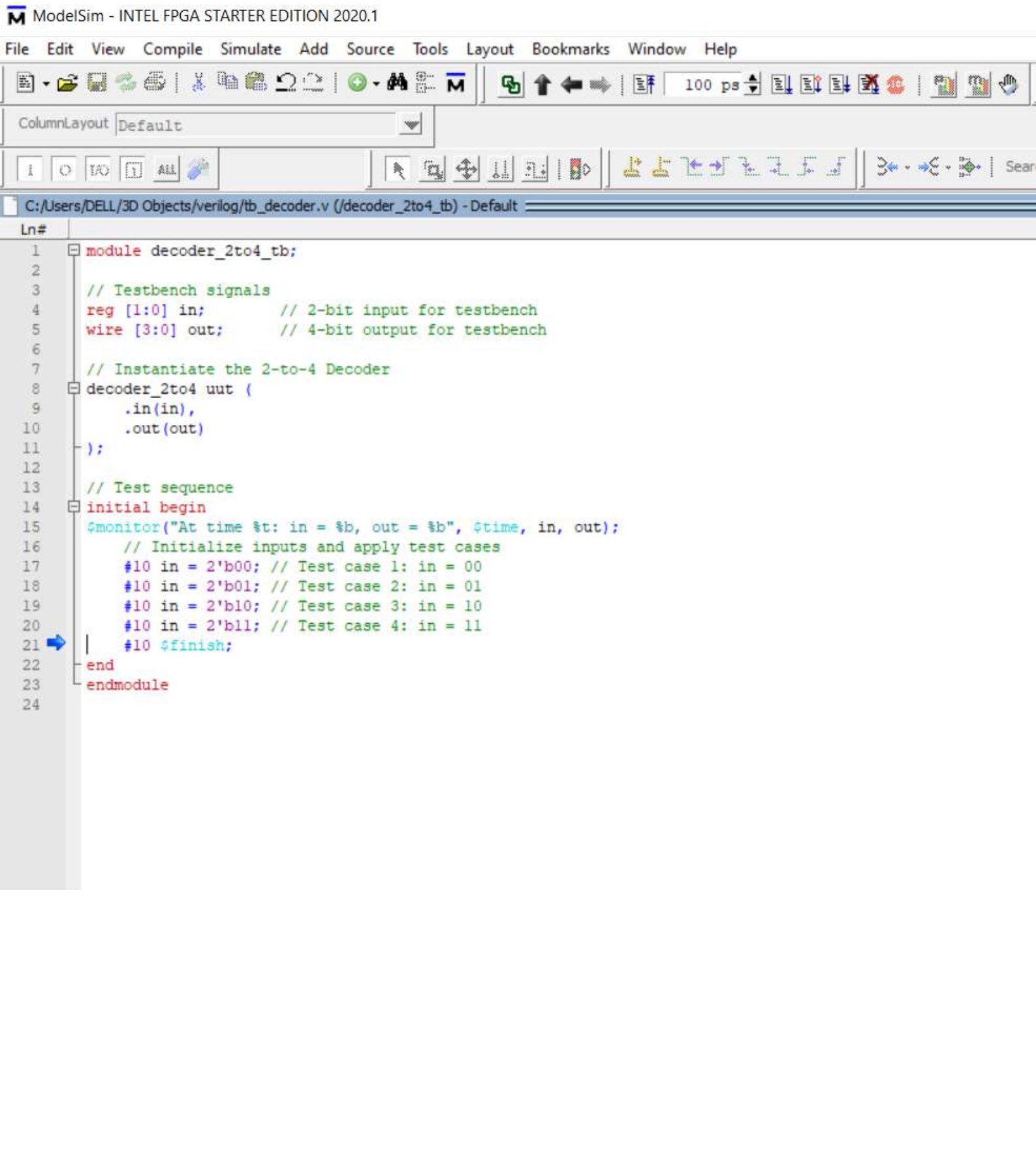
C:/Users/DELL/3D Objects/verilog/decoder2_4.v (/decoder_2to4_tb/uut) - Default

Ln#

```
1  module decoder_2to4(in,out);
2  input [1:0] in;   // 2-bit input
3  output wire [3:0] out;  // 4-bit output
4
5  assign out = (in == 2'b00) ? 4'b0001 :  // When in = 00, out = 0001
6               (in == 2'b01) ? 4'b0010 :  // When in = 01, out = 0010
7               (in == 2'b10) ? 4'b0100 :  // When in = 10, out = 0100
8               (in == 2'b11) ? 4'b1000 :  // When in = 11, out = 1000
9               4'b0000;                  // Default value
10
11 endmodule
12
```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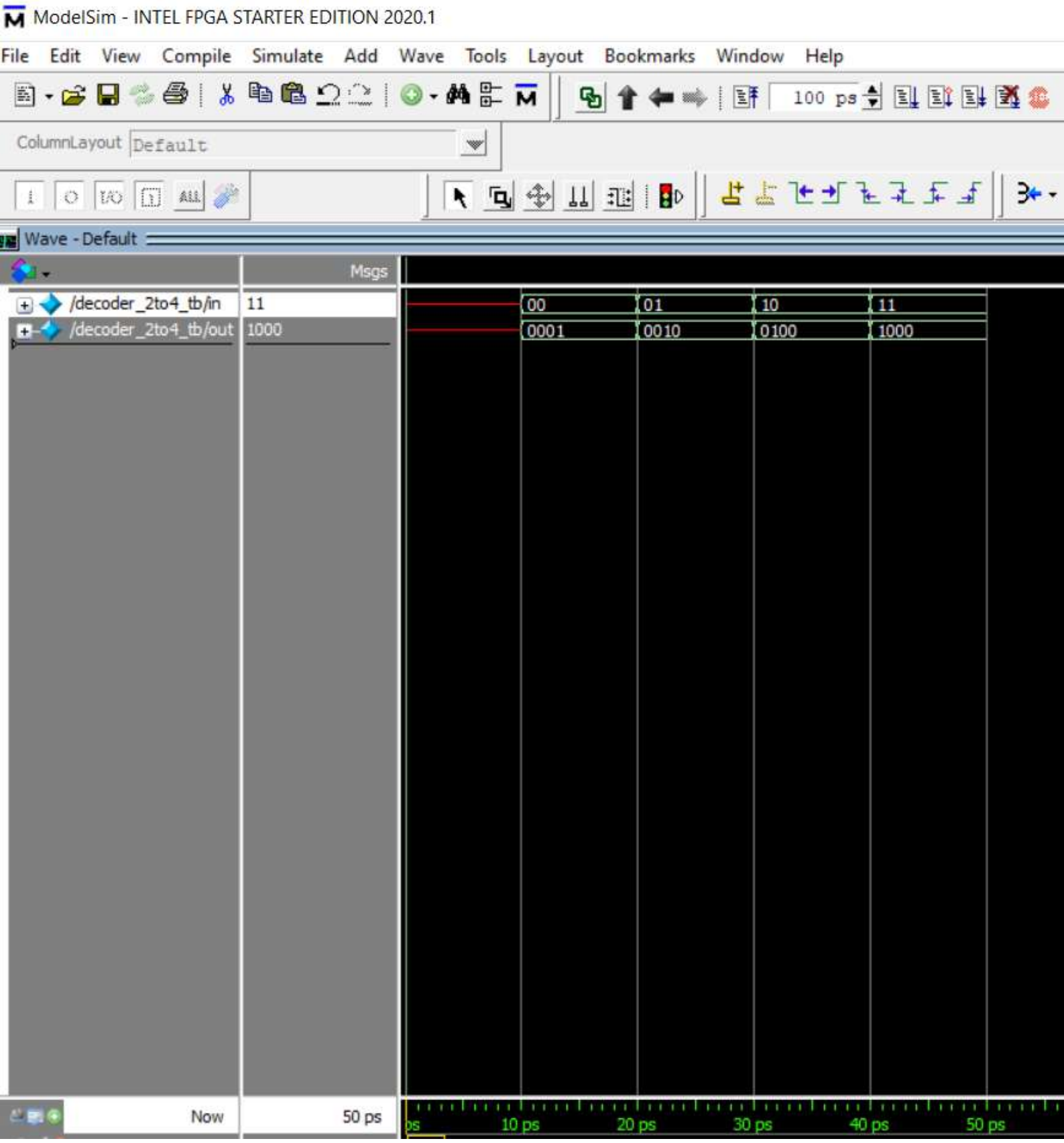
100 ps
ColumnLayout Default
C:/Users/DELL/3D Objects/verilog/tb_decoder.v (/decoder_2to4_tb) - Default
Ln#
1 module decoder_2to4_tb;
2
3 // Testbench signals
4 reg [1:0] in; // 2-bit input for testbench
5 wire [3:0] out; // 4-bit output for testbench
6
7 // Instantiate the 2-to-4 Decoder
8 decoder_2to4 uut (
9 .in(in),
10 .out(out)
11);
12
13 // Test sequence
14 initial begin
15 $monitor("At time %t: in = %b, out = %b", $time, in, out);
16 // Initialize inputs and apply test cases
17 #10 in = 2'b00; // Test case 1: in = 00
18 #10 in = 2'b01; // Test case 2: in = 01
19 #10 in = 2'b10; // Test case 3: in = 10
20 #10 in = 2'b11; // Test case 4: in = 11
21 #10 $finish;
22 end
23 endmodule
24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100 ps
ColumnLayout Default
Wave - Default
Msgs
/decoder_2to4_tb/in
/decoder_2to4_tb/out
11
1000
00 01 10 11
0001 0010 0100 1000
Now
50 ps
10 ps 20 ps 30 ps 40 ps 50 ps