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ModelSim - INTEL FPGA STARTER EDITION 2020.1
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 C:/Users/DELL/3D Objects/verilog/tb_FS.v (/full_subtractor_tb) - Default
 Ln#
  1
      module full_subtractor_tb;
        // Testbench signals
  4 1
        red a:
                     // Testbench minuend input
  5
        reg b;
                     // Testbench subtrahend input
                     // Testbench borrow-in input
  6
        reg bin;
        wire diff;
                     // Testbench difference output
                     // Testbench borrow-out output
  8
        wire bout;
  9
 10
        // Instantiate the full subtractor
 11
      full_subtractor uut (
 12
            .a(a),
 13
            .b(b),
 14
            .bin(bin),
 15
            .diff (diff) ,
 16
            .bout (bout)
 17
       -);
 18
 19
        // Test sequence
 20
        initial
 21
      = begin
        $monitor("At time %t: a = %b, b = %b, bin = %b, diff = %b, bout = %b", $time, a, b, bin, diff, bout);
 22
 23
            // Initialize inputs and apply test cases
 24
            #10 a = 0; b = 0; bin = 0; // Test case 1: a = 0, b = 0, bin = 0
 25
            #10 a = 0; b = 0; bin = 1; // Test case 2: a = 0, b = 0, bin = 1
            #10 a = 0; b = 1; bin = 0; // Test case 3: a = 0, b = 1, bin = 0
 26
 27
            #10 a = 0; b = 1; bin = 1; // Test case 4; a = 0, b = 1, bin = 1
            #10 a = 1; b = 0; bin = 0; // Test case 5: a = 1, b = 0, bin = 0
 28
 29
            #10 a = 1; b = 0; bin = 1; // Test case 6: a = 1, b = 0, bin = 1
            #10 a = 1; b = 1; bin = 0; // Test case 7: a = 1, b = 1, bin = 0
 30
            #10 a = 1; b = 1; bin = 1; // Test case 8: a = 1, b = 1, bin = 1
 31
 32
            #10 Sfinish;
 33
        end
       endmodule
 34
 35
```

