

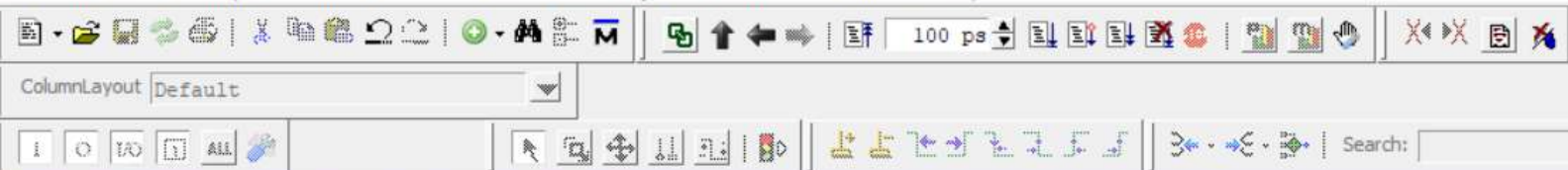


ColumnLayout Default



C:/Users/DELL/3D Objects/verilog/mux2\_1.v (/mux\_2x1\_tb/uut) - Default

Ln#	
1	module mux_2x1(a,b,sel,y);
2	input a; // Input 0
3	input b; // Input 1
4	input sel; // Select signal
5	output y; // Output
6	
7	assign y = sel ? b : a; // If sel is 1, choose b; otherwise, choose a
8	
9	endmodule
10	



C:/Users/DELL/3D Objects/verilog/tb\_mux2\_1.v (/mux\_2x1\_tb) - Default

```
Ln#
1  module mux_2x1_tb;
2
3      // Testbench signals
4      reg a;           // Testbench input 0
5      reg b;           // Testbench input 1
6      reg sel;         // Testbench select signal
7      wire y;          // Testbench output
8
9      // Instantiate the 2x1 MUX
10     mux_2x1 uut (
11         .a(a),
12         .b(b),
13         .sel(sel),
14         .y(y)
15     );
16
17     // Test sequence
18     initial begin
19         $monitor("At time %t: a = %b, b = %b, sel = %b, y = %b", $time, a, b, sel, y);
20         // Initialize inputs and apply test cases
21         #10 a = 0; b = 0; sel = 0; // Test case 1: sel = 0, choose a = 0
22         #10 a = 0; b = 1; sel = 0; // Test case 2: sel = 0, choose a = 0
23         #10 a = 1; b = 0; sel = 0; // Test case 3: sel = 0, choose a = 1
24         #10 a = 1; b = 1; sel = 0; // Test case 4: sel = 0, choose a = 1
25         #10 a = 0; b = 0; sel = 1; // Test case 5: sel = 1, choose b = 0
26         #10 a = 0; b = 1; sel = 1; // Test case 6: sel = 1, choose b = 1
27         #10 a = 1; b = 0; sel = 1; // Test case 7: sel = 1, choose b = 0
28         #10 a = 1; b = 1; sel = 1; // Test case 8: sel = 1, choose b = 1
29         #10 $finish;
30     end
31 endmodule
32
```

