SCHOOL OF ELECTRONICS ENGINEERING

KALINGA INSTITUTE OF INDUSTRIAL TECHNOLOGY (KIIT)

VLSI LABORATORY REPORT

(EC-3095)

Submitted By

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Section: ETC-06

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Experiment: 4th

Design of 1Kx8 RAM cell and its READ, WRITE operation.

Experiment No-04

Aim of the Experiment :

Design a 1K x 8 RAM using behavioral modelling.

Software used :

EDA playground

Theory :-

In computing, memory refers to a device that is used to store information. For immediate use in a computer or related to semiconductor memory. It is typically refferd to as semiconductor memory, specially MOS memory, where data is stored within MOS memory cells on a silicon integrated circuit chip. Most semiconductor memory is organized into memory cell or bistable flip-flops, each storing one bit.

Random access memory (RAM) is a form of computer memory that can be read and changed in any order, typically used to store working data and machine code.

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A random access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of Data inside the memory.

Design 1 KB RAM

data line = 8 bits

Memory space = 8 X 1024

address lines = 10 bits.

Codes:-

Design.sv

```
// Code your design here
module ram(output [7:0]dout, input [7:0]din, input [9:0]addr, input clk,en,rw);
  reg [7:0]dout;
  reg [7:0]raw[1023:0];
  always@(negedge clk) begin
    if(en == 1'b1) begin
      if(rw == 1'b1) begin
        raw[addr] = din;
            dout <= 8'bx;
      end
      else
        dout <= raw[addr];
      end
    else
      dout <= 8'bz;
  end
endmodule
```

Testbench.sv

```
// Code your testbench here
// or browse Examples
module ram_tb;
  reg en,rw,clk;
  reg [7:0]din;
  reg [9:0]addr;
  wire [7:0]dout;
  ram r1(dout,din,addr,clk,en,rw);
  initial begin
    $dumpfile("dump.vcd"); $dumpvars;
    clk=0;en=1;rw=1;
    addr=8'ha;din=8'h14;#20;
    addr=8'hff;din=8'h32;#20;
    rw=0;
    addr=8'ha;#20;
    addr=8'hff;#20;
    addr=8'h5;#20;
    en=0;#20;
  end
  always #5 clk=!clk;
endmodule
```

Observations

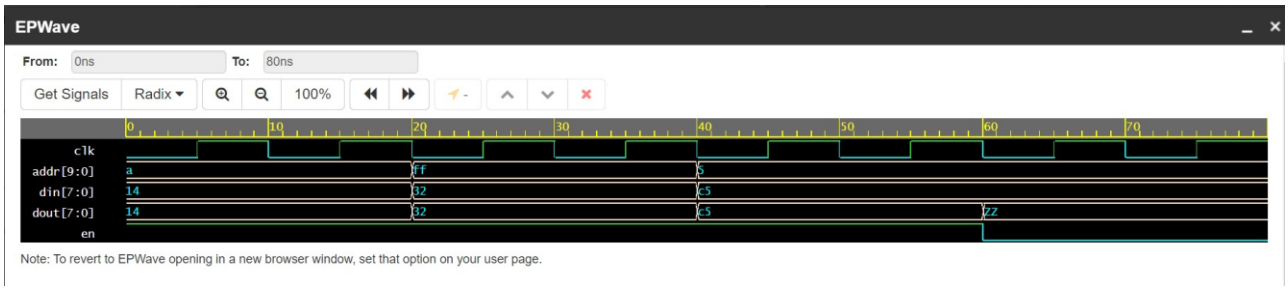

Fig 4.1: EPWAVE diagram of 8kB RAM

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Conclusion: In this experiment we learned about computer memory, ~~and~~ specially about RAM. We successfully designed a 1KB RAM in EDA playground by ~~so~~ writing a code and we also simulated output waveform of 1KB RAM by writing testbench code in EDA playground.