SCHOOL OF ELECTRONICS ENGINEERING

KALINGA INSTITUTE OF INDUSTRIAL TECHNOLOGY (KIIT)

VLSI LABORATORY REPORT

(EC-3095)

Submitted By

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Section: ETC - 06

Semester: 6 TH SEM

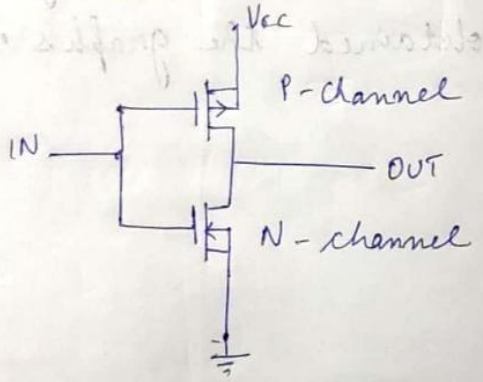
Experiment No-8

Aim:- Simulation of CMOS Inverter and Design & Simulation of CMOS NAND, NOR and XOR gates in TINA-TI Software.

Software used :- TINA-TI

Theory :-

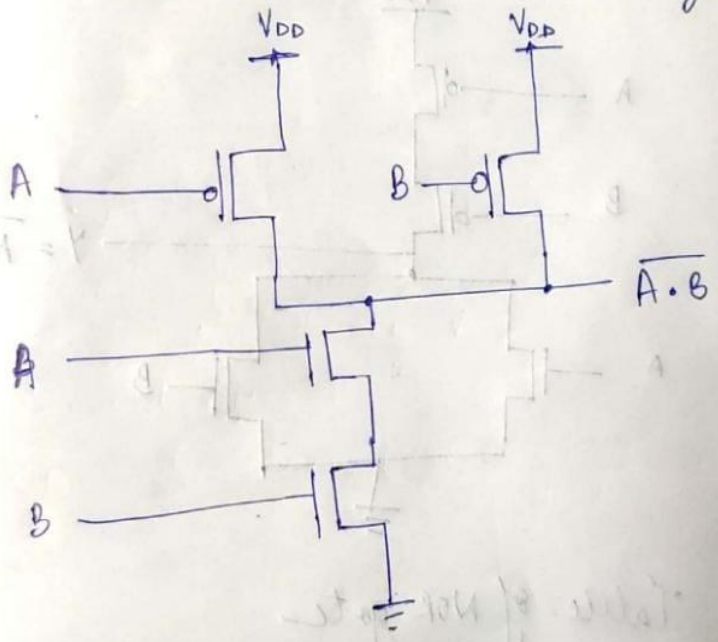
* CMOS inverter contains a PMOS and a NMOS transistor connected at the drain and gate terminals, a supply voltage VDD at the PMOS source terminal & a ground connected at the NMOS source terminal, where Vin is connected to the gate terminal & Vout is connected to the drain terminals.



CMOS inverter configuration is called complementary MOS. For high input, the NMOS

transistor pulls down the output node while the PMOS transistor acts as the load, and for low input the PMOS transistor pulls up the output node while the NMOS transistor acts as the load.

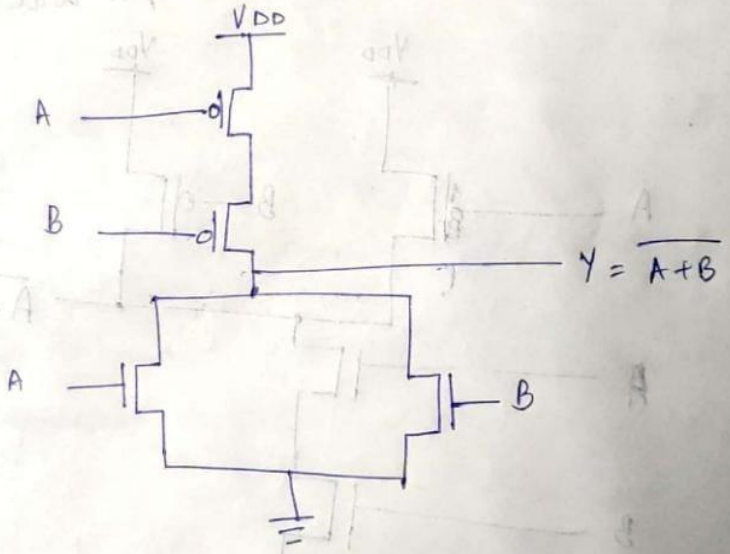
CMOS NAND gate consists of two series NMOS transistors between Y and ground and two parallel PMOS transistors between Y & VDD. If either of the top transistors saturate output will go high (1). If both lower transistors saturate output will go low (0).



Truth table of NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NOR gate circuit also uses 4 MOSFETS. where 2 are connected in series and source & 2 parallel - connected sinking transistors.
Only when Both inputs are low (0) will both lower transistors be in cutoff mode & both upper in saturated so the output goes to (1) high otherwise for rest input cases output is always (0) low.



Truth Table of NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

* CMOS XOR gate

$$Y = \bar{A}B + A\bar{B}$$

Can also be written as

$$Y = \overline{\bar{A}B + A\bar{B}}$$

$$= \overline{\bar{A}B} \cdot \overline{A\bar{B}}$$

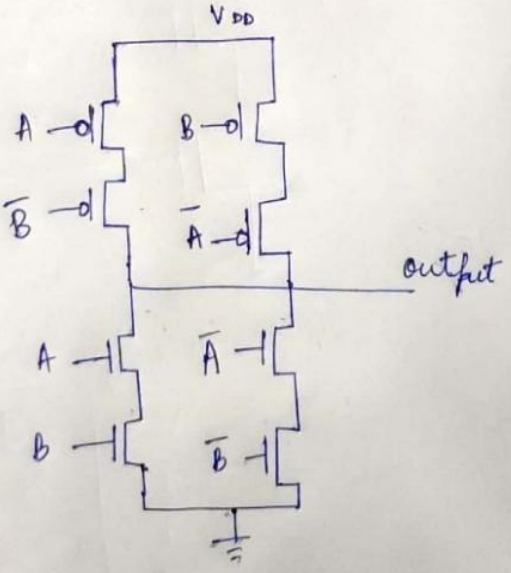
$$= (A + \bar{B}) \cdot (\bar{A} + B)$$

$$= A\bar{A} + AB + B\bar{B} + \bar{A}\bar{B}$$

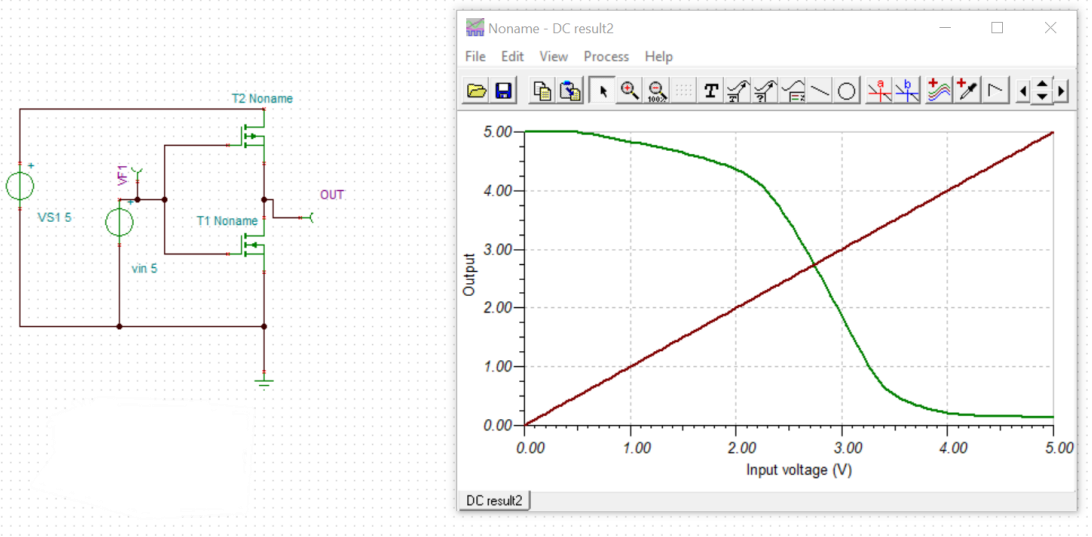
$$= \overline{AB + \bar{A}\bar{B}}$$

Truth table of XOR gate.

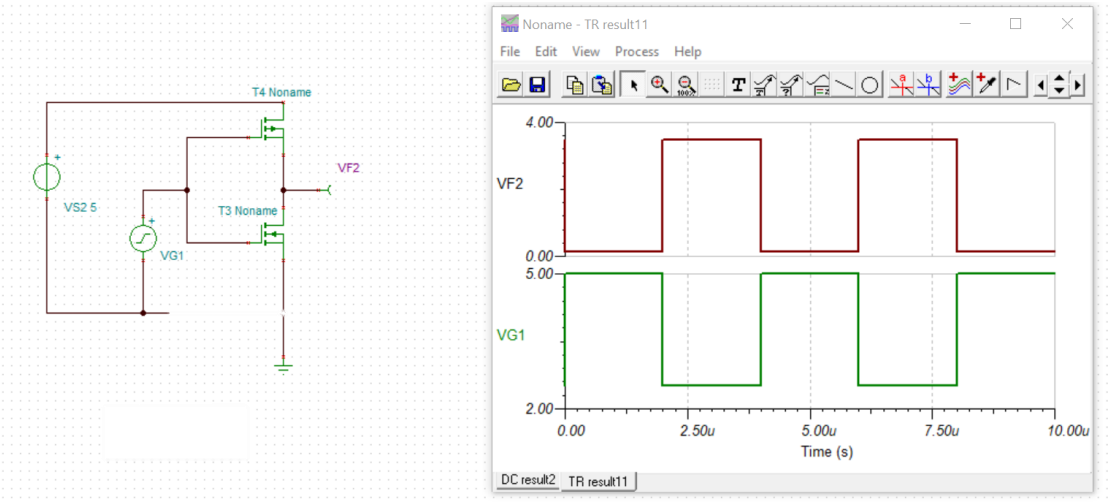
A	B	y
0	0	0
0	1	1
1	0	1
1	1	0



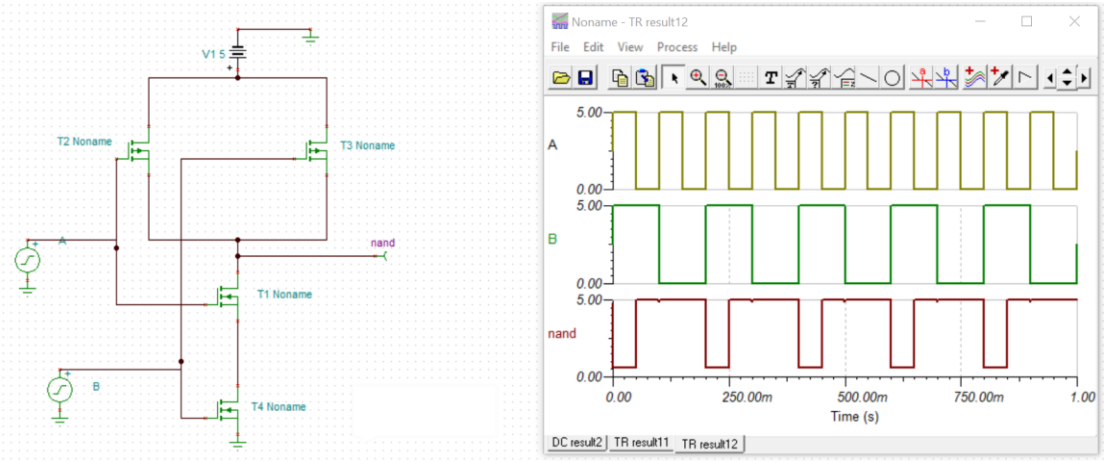
OUTPUTS :-



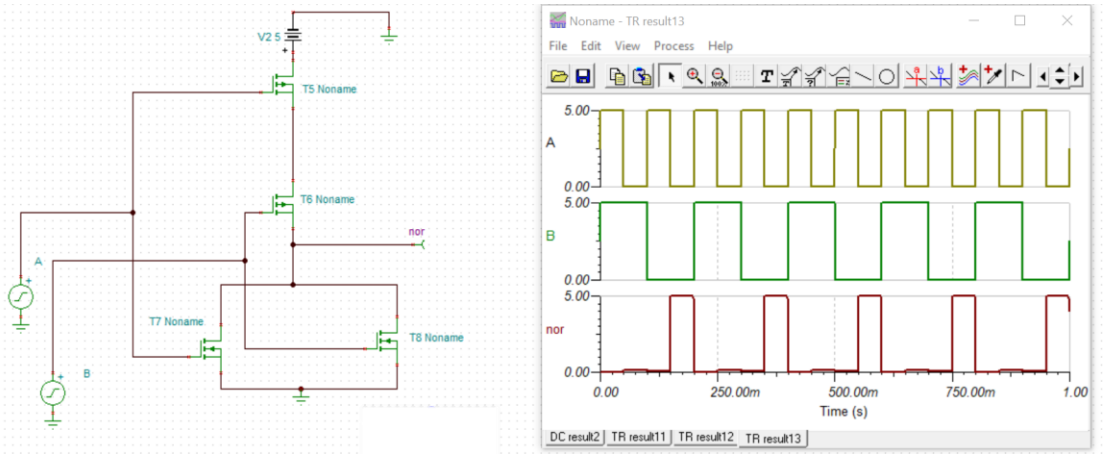
Circuit diagram of CMOS INVERTER and its transfer characteristics



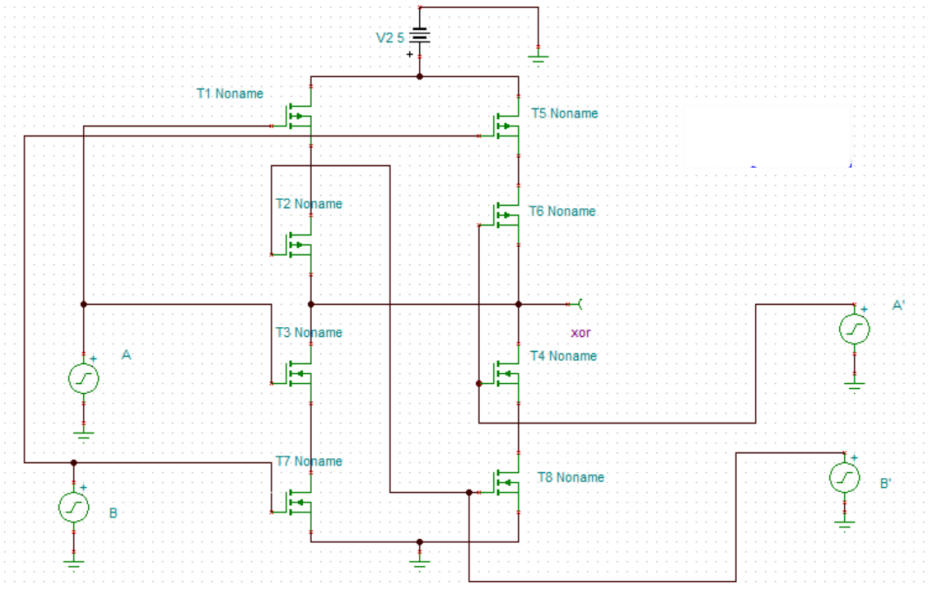
Circuit diagram of CMOS INVERTER and its output waveform



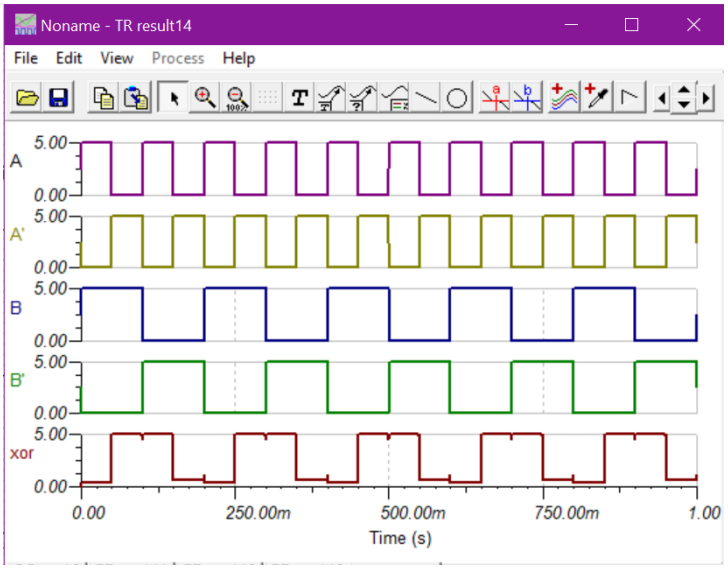
Circuit diagram of CMOS NAND GATE and its output waveform



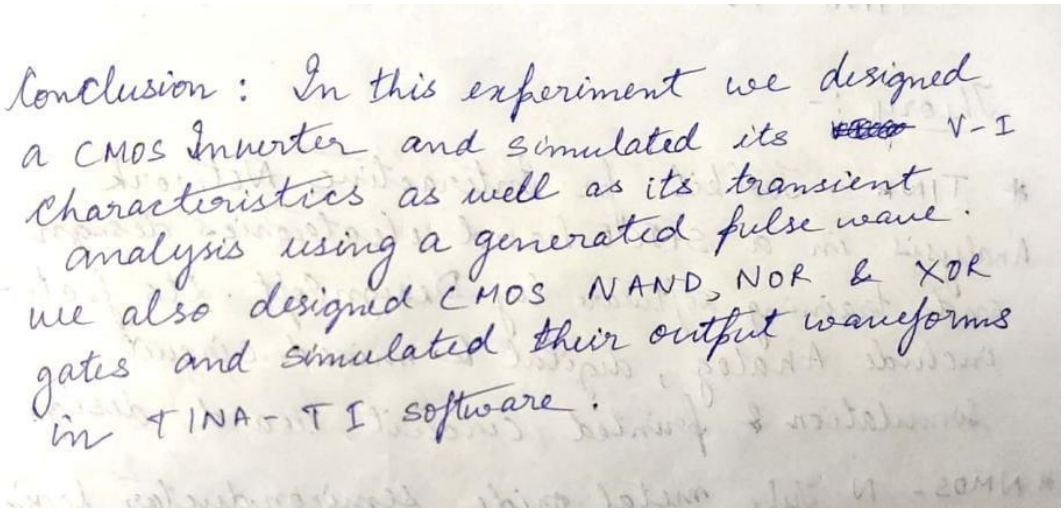
Circuit diagram of CMOS NOR GATE and its output waveform



Circuit diagram of CMOS XOR GATE



Output waveform of CMOS XOR GATE


Conclusion : In this experiment we designed a CMOS Inverter and simulated its ~~VTC~~ V-I characteristics as well as its transient analysis using a generated pulse wave. We also designed CMOS NAND, NOR & XOR gates and simulated their output waveforms in TINA-TI software.