Experiment no. 01

Aim of the Experiment - Design of full adder in gate level ~~and data flow modeling~~, 4 bit full adder using single bit adder. 4 bit full substractor.

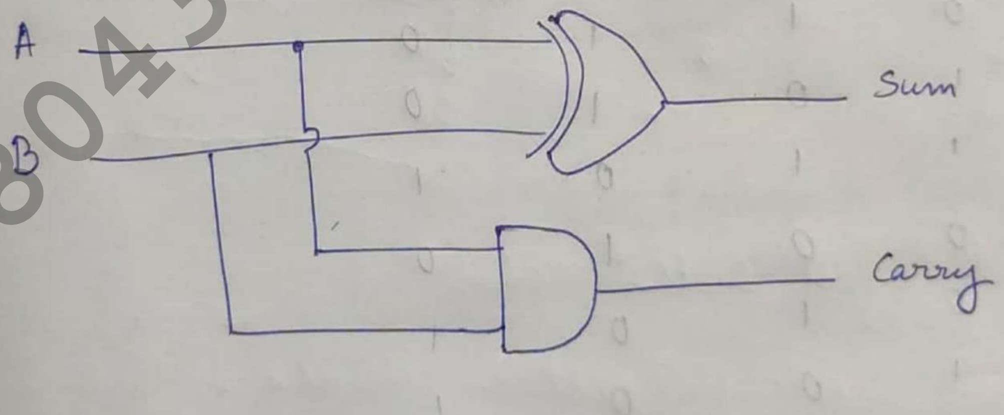
Software used

- www. edaplayground . com.

Theory

1 Half adder is a combinational logical circuit which is designed by connecting an XOR gate & an AND gate. Its circuit has 2 inputs A & B which adds 2 bits & generates a carry & a sum.

$$Sum = A \oplus B \quad ; \quad Carry = A \cdot B$$



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Truth Table

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2) Full Adder is the circuit which adds 3 bits and consists of 2 XOR gates, 2 AND gates and 1 OR gate. The inputs are A B & Cin whereas outputs are Sum & Carry.

$$\text{Sum} = A \oplus B \oplus C_{in}$$

$$\text{carry} = A \cdot B + C_{in} \cdot (A \oplus B)$$

Truth Table

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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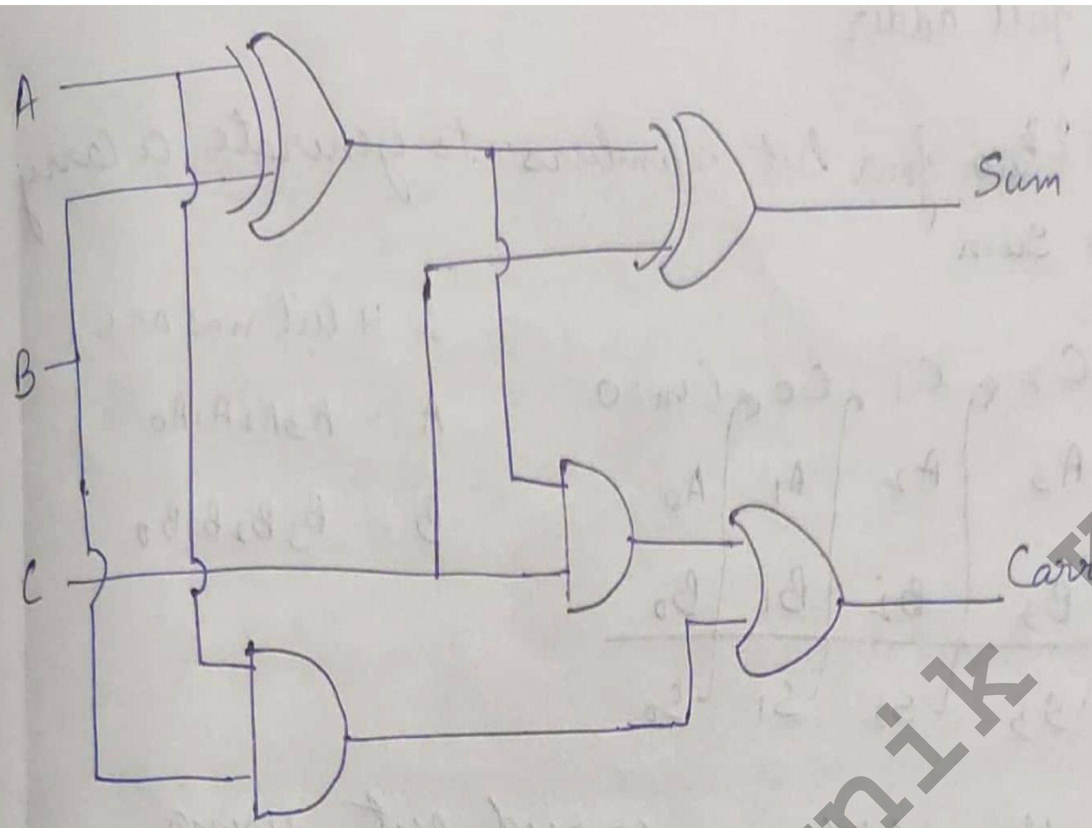
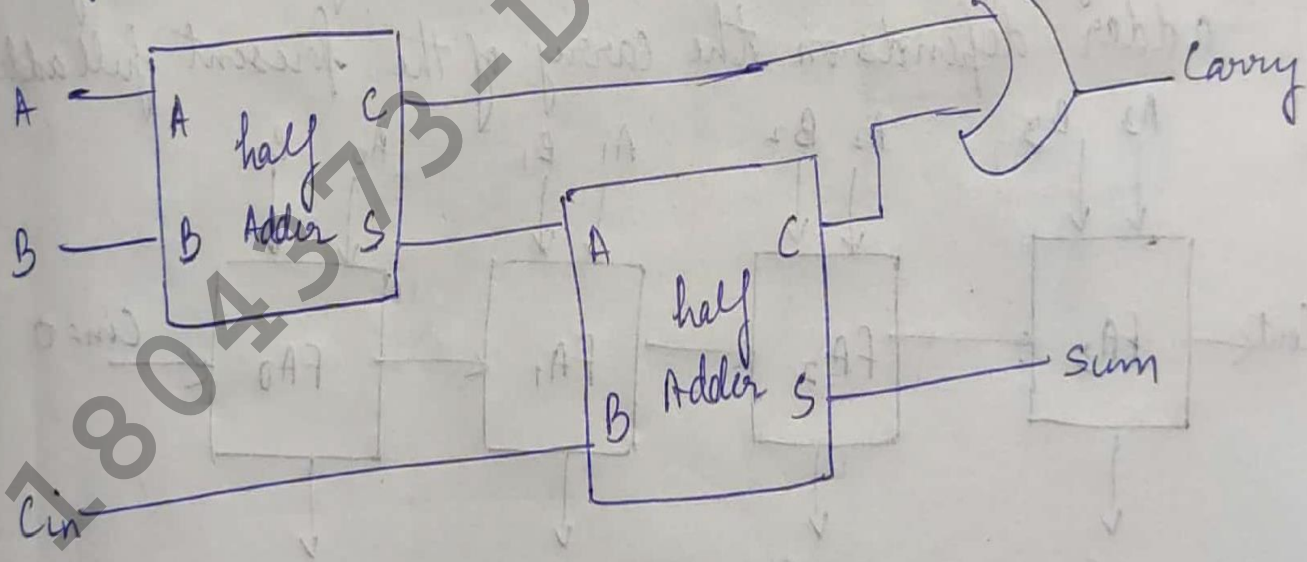


A full adder can also be constructed using 2 half adders and an OR gate in the following manner



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3) 4 bit full adder

It adds 2 ~~two~~ four bit numbers to generate a carry and a sum

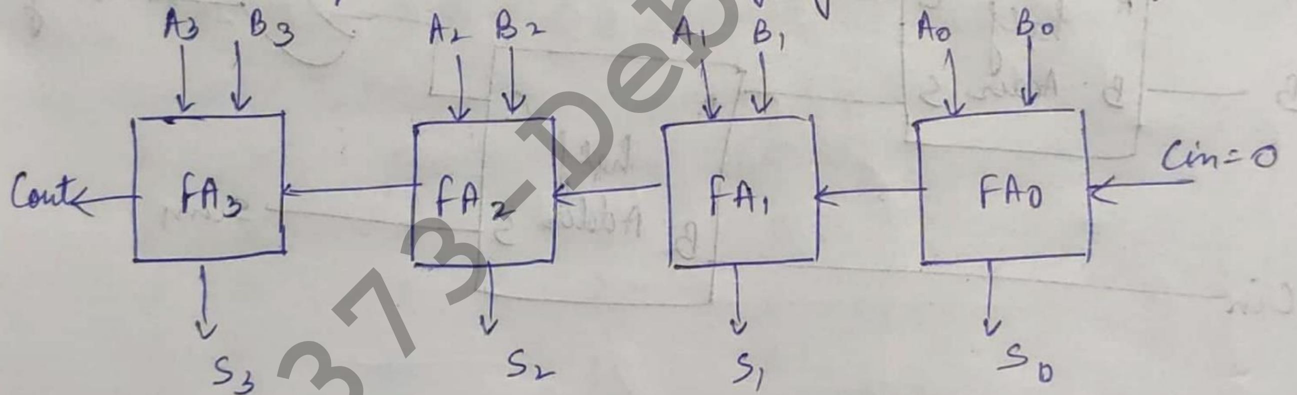
$$\begin{array}{ccccc} C_{out} & C_2 & C_1 & C_0 & C_{in}=0 \\ & A_3 & A_2 & A_1 & A_0 \\ + & B_3 & B_2 & B_1 & B_0 \\ \hline & S_3 & S_2 & S_1 & S_0 \end{array}$$

2 4 bit nos. are

$A = A_3A_2A_1A_0$

$B = B_3B_2B_1B_0$

Thus this addition is carried out using ripple carry adder where $C_{in} = 0$. It used 4 singlebitfull adders. The output of the next full adder depends on the carry of the present full adder.



4) 4 bit full substractor

It performs substraction between 2 four bit nos. to generate difference & borrow.

The two 4 bit nos are

$A = A_3A_2A_1A_0$

$B = B_3\ B_2B_1B_0$

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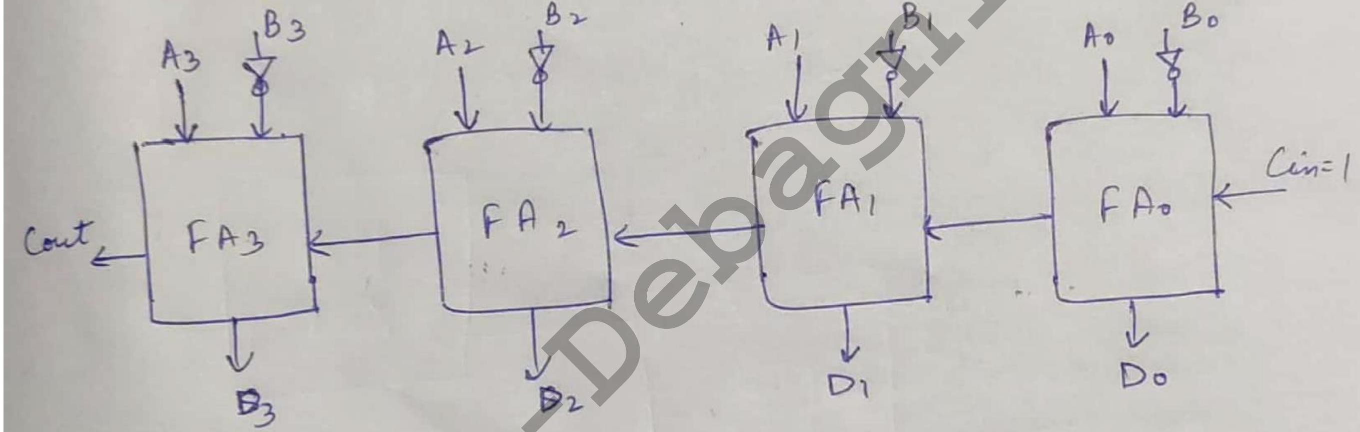
$$
\begin{array}{cccccc}
C_{out} & C_2 & C_1 & C_0 & C_{in}=1 \\
 & A_3 & A_2 & A_1 & A_0 \\
+ & \overline{B}_3 & \overline{B}_2 & \overline{B}_1 & \overline{B}_0 \\
\hline
 & D_3 & D_2 & D_1 & D_0
\end{array}
$$

Substraction is done by 2's complement method where one of the 4 bit nos. are inverted and added to the other 4 bit no. while Cin = 1.



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Code:-

```
//File: Halfadder.sv
module halfadder(output sum,carry, input A,B);
  xor summer(sum,A,B);
  and car(carry,A,B);
endmodule

//File design.sv for Full adder
`include "halfadder.sv"
module fulladder(output s1,cout, input cin,P,Q);
  wire s2,c2,c1;
  halfadder ha1(s2,c1,P,Q);
  halfadder ha2(s1,c2,cin,s2);
  or or1(cout,c1,c2);
endmodule

// File Testbench.sv for full adder
module test_fulladder;
  wire sum,carry;
  reg in1,in2,cin;
  fulladder a1(sum,carry,cin,in1,in2);
  //halfaddef ha2(.carry(car),.sum(s),.A(in2),.B(in2))

  initial begin
    $dumpfile("dump.vcd"); $dumpvars;
    // t=0
    in1=0; in2=0; cin=0;
    // t=10ns
    #10 in1=0; in2=1; cin=0;
    // t=20ns
            #10 in1=1; in2=0; cin=0;
    // t=30ns
    #10 in1=1; in2=1; cin=0;
    // t=40ns
    #10 in1=0; in2=0; cin=1;
    // t=50ns
    #10 in1=0; in2=1; cin=1;
    // t=60ns
    #10 in1=1; in2=0; cin=1;
    // t=70
    #10 in1=1; in2=1; cin=1;
  end
endmodule
```

Click here to access the code at edaplayground.com for Full Adder

```
// Design.sv for 4-bit adder
`include "fulladder.sv"
module fourbitadder(output [3:0]s,output cout,input [3:0]A,B, input cin);
  wire c1,c2,c3;
  fulladder fa0(s[0],c1,cin,A[0],B[0]);
  fulladder fa1(s[1],c2,c1,A[1],B[1]);
  fulladder fa2(s[2],c3,c2,A[2],B[2]);
  fulladder fa3(s[3],cout,c3,A[3],B[3]);
endmodule
```

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```
// testbench.sv for 4-bit adder
module test_fourbitadder;
  wire cout;
  wire [3:0]s;
  reg [3:0]a,b;
  reg cin;
  fourbitadder fba(s,cout,a,b,cin);
  reg [8:0]i;
  initial begin
    $dumpfile("dump.vcd"); $dumpvars;
    for(i=0;i<512;i=i+1) begin
      a=i;b=i+1;cin=0;
      #10;
    end
  end
endmodule
```

Click here to access the code at edaplayground.com for 4-bit Adder

```
// File halfsubtractor.sv
module halfsub(output diff,bor, input A,B);
  wire a;
  xor x1(diff,A,B);
  not g(a,A);
  and a1(bor,a,B);
endmodule

//File: fullsubtractor.sv
`include "halfsubtractor.sv"
module fullsub(output diff,bout, input P,Q,bin);
  wire d1,b1,b2;
  halfsub hs1(d1,b1,P,Q);
  halfsub hs2(diff,b2,d1,bin);
  or o(bout,b2,b1);
endmodule

//File design.sv for 4-bit substractor
`include "fullsubtractor.sv"
module fourbitsub(output [3:0]D,output bout,input [3:0]A,B, input bin);
  wire b1,b2,b3;
  fullsub fs0(D[0],b1,A[0],B[0],bin);
  fullsub fs1(D[1],b2,A[1],B[1],b1);
  fullsub fs2(D[2],b3,A[2],B[2],b2);
  fullsub fs3(D[3],bout,A[3],B[3],b3);
endmodule

// file: testbence.sv for 4-bit substructor
module test_fourbitadder;
  wire [3:0]d;
  wire bout;
  reg [3:0]a,b;
  reg bin;
  fourbitsub fbs(d,bout,a,b,bin);
  reg [8:0]i;
  initial begin
```

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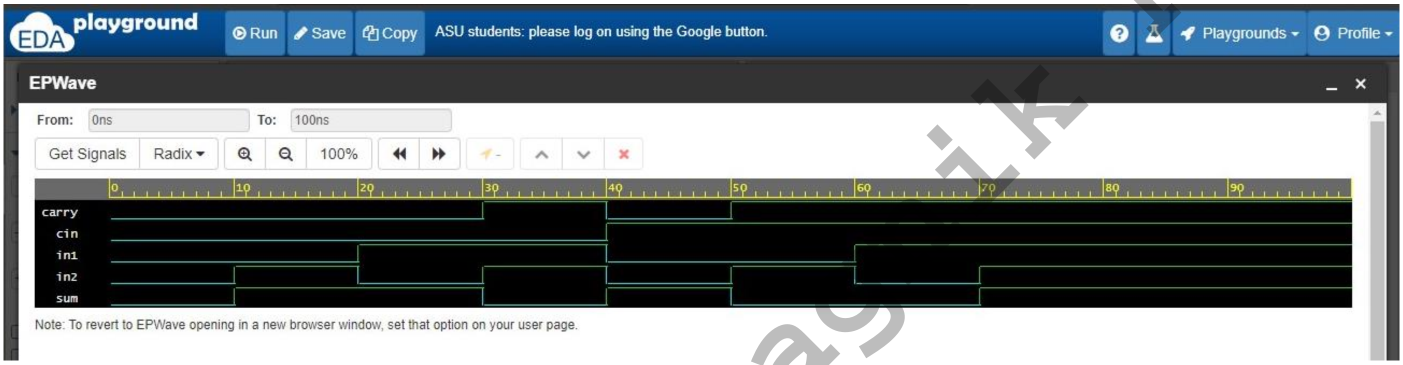
```
    $dumpfile("dump.vcd"); $dumpvars;
    for(i=0;i<256;i=i+1) begin
      a = 1;
      b = i+1;
      bin = 1;
      #10;
    end
  end
endmodule
```

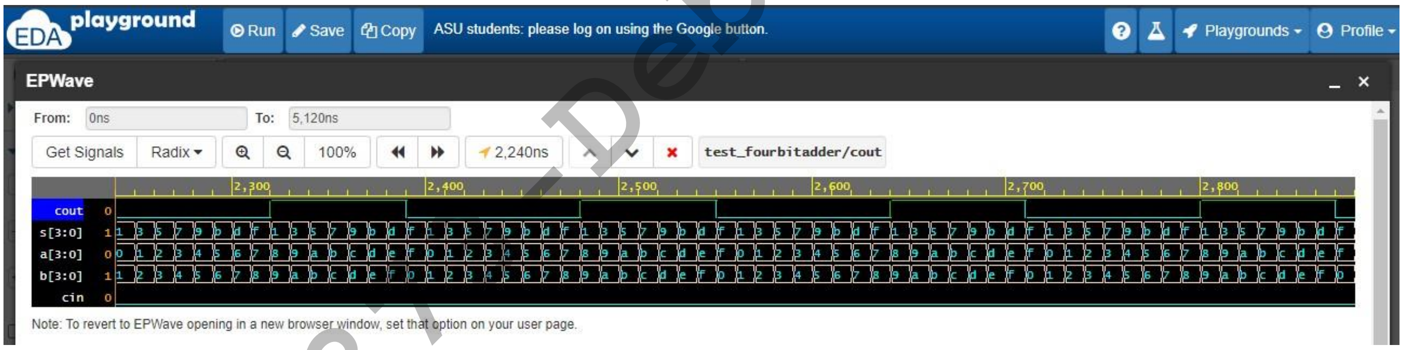
[Click here to access the code at edaplayground.com]() for 4-bit Subtractor

Observations:-


ASU students: please log on using the Google button.

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Fig 1.1: EPWave table of a full adder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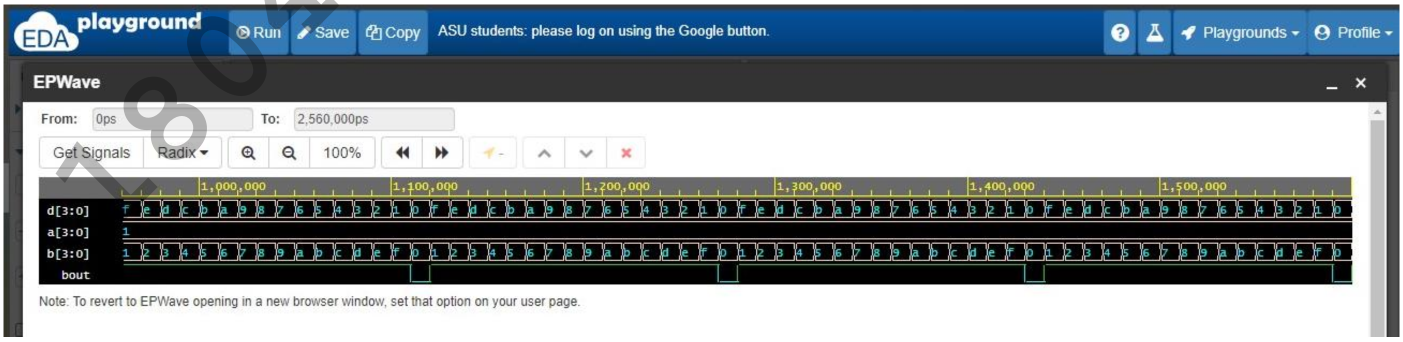
Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Fig 1.2: EPWave table of a 4-bit substractor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Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Fig 1.3: EPWave table of 4-bit substractor

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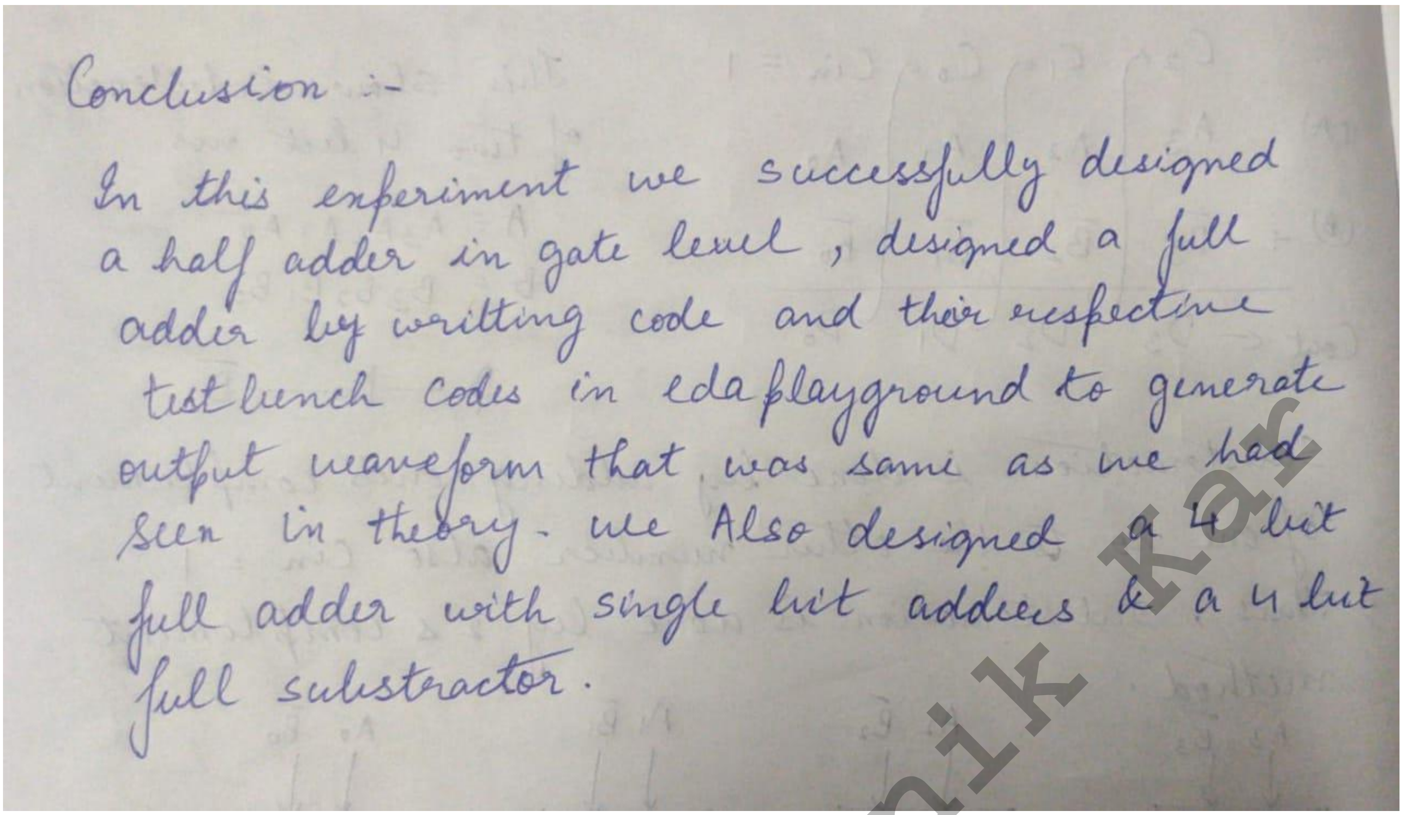

Conclusion :-

In this experiment we successfully designed a half adder in gate level, designed a full adder by writting code and their respective test bench codes in edaplayground to generate output waveform that was same as we had seen in theory. we Also designed a 4 bit full adder with single bit adders & a 4 bit full substractor.

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