Novel Design of A 4:1 Multiplexer Circuit Using Reversible Logic

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ABSTRACT:
Area of reversible logic is attracting much attention of researchers nowadays. Reversible logic concept of digital circuit designing is gaining wide scope in the area of nanotechnology, quantum computing, signal processing, optical computing etc due to its ability to design low power loss digital circuits. This paper presents an optimized multiplexer circuit based on reversible logic using various available basic reversible gates. Optimization of the multiplexer circuit is achieved on the basis of total number of gates used in the circuit and total number of outputs generated. These circuits are useful for further circuit designing with low power loss.

KEYWORDS: Reversible circuit design, Basic reversible gates, Multiplexer circuit.

I. INTRODUCTION

An integrated circuit containing many identical cells which can be electrically programmed to become almost any kind of digital circuit or system is called as Field Programmable Gate Arrays (FPGAs) [1]. Multiplexers play the key role in the functionalities of FPGAs, so to design a multiplexer with reversible logic will generate the concept of designing low power loss circuits for FPGAs.Earlier digital circuits were made up of conventional logic gates. These gates were irreversible in nature. Reversible circuit designing is the way of today's digital circuit designing. In 1961, R. Landauer has shown that these conventional irreversible circuits dissipate some energy due to the information loss during the operation of the circuit [2]. After that in 1973, Benette has shown that this energy loss can be minimized or even removed if the circuits are designed using reversible gates [3].

II. REVERSIBLE LOGIC CIRCUIT DESIGN

[2.1] Reversible Logic- conventional logic gates were generally (n:1) in nature. Where n represents the number of input signals applied and 1 indicated the single output generated from the gate. Whereas reversible logic gates are (n,n) logic gates. Here both, the number of input signals and the number of output signal are equal to n. In conventional logic gates output signals are less in number as compared to the number of input signals. But in reversible gates input and output signals are equal in number. The combination of output signal at any instance can provide the exact status of input combination. This is the main reason to name these (n,n) gates, reversible logic gates[4,5,6].

[2.2] Basic Reversible Gates- There are various basic reversible (n,n) gates[7,8,9,10,11,12,13]. For designing multiplexer TKS gate[14] is the optimum choice. TKS gate is a (3,3) reversible gate. Its block diagram is shown in figure 1 and output equations are given below the diagram.

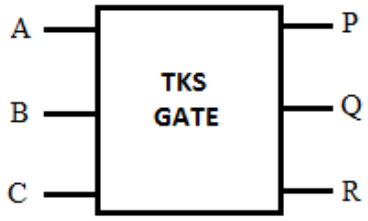

Figure 1: TKS Gate

Where -

$P = A.\bar{C} + B.C$
$Q = A \oplus B \oplus C$
$R = A.C + B.\bar{C}$

In any reversible gate if we know the status of output signals (P, Q, R in case of TKS Gate) we can deduct the instance combination of input stage (A, B, C in case of TKS Gate).

[2.3] Proposed Reversible Gate (VSMT Gate)- VSMT is a new proposed (6,6) reversible gate. This gate conforms to the necessary characteristics of the reversible logic gates. These characteristics are as follows-
(a) Number of inputs = Number of outputs.
(b) One to one mapping between input and output.
(c) Zero feedback.
(d) Individual output bits are high for a total of half the number of total input combinations.
The block diagram of VSMT gate is shown in figure 2. Here input signals are A, B, C, D, E and F, whereas output signals are P, Q, R, S, T and U.

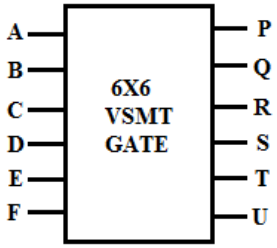

Figure 2: Block diagram of VSMT gate

Output equations of above gate is given as below-
$P = \bar{E}.(A.\bar{F} + B.F) + E.(C.\bar{F} + D.F)$
$Q = A \oplus B \oplus C$
$R = E \oplus F$
$S = C \oplus D$
$T = D \oplus E \oplus F$
$U = E$

The truth table of this gate has a total of 64 input combinations. Here in this gate each input combination produce unique output combination. This VSMT gate is a reversible gate for 6 input signals. This paper shows the application of VSMT gate to design multiplexer circuit. Apart from proposed multiplexer circuit there can be various other applications of DSM gates to design other digital circuits in optimized manner.

[2.4] Multiplexer Circuit- A multiplexer (MUX) is a device which selects any one of the several input signals applied and provide it to the single output line according to the combination of selection lines applied. Multiplexers are generally used for the conversion of parallel data lines into serial one. These are also called as Data Selectors, as multiplexer selects one of the given input for the output according to the condition [15]. Figure 3 gives the block diagram of a 2^n:1 multiplexer. Here 2^n refers to the total number of input signal lines and 1 refers to the single output signal line. Total number of selection lines required is n as shown in the figure.

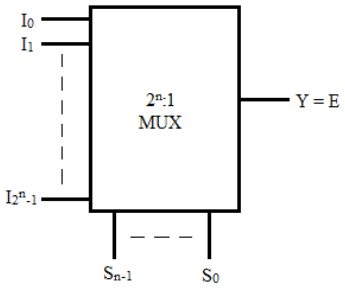

Figure 3: Block Diagram of a 2^n:1 Multiplexer

Where output equation is-

$$Y = E = I_0(\overline{S_{n-1}} \dots \dots \overline{S_1}.\overline{S_0}) + I_1((\overline{S_{n-1}} \dots \dots \overline{S_1}.S_0) + \dots \dots + I_{2^n-1}(S_{n-1} \dots \dots S_1.S_0)$$

If we name input signals of the multiplexer as I_0, I_1, I_2, ... I_{2^n-1}, selection lines as S_0,S_1, ... S_{n-1} and output as Y then truth table of a 2^n:1 multiplexer can be shown as in Table 1.

Table 1: Truth Table of a 2^n:1 multiplexer

S. No.	Input Section Lines	Output
	S_{n-1} ..... S_1 S_0	Y
1	0 ..... 0 0	I_0
2	0 ..... 0 1	I_1
-	----------	-
-	----------	-
2^n	1 ..... 1 1	I_{2^n-1}

As shown in the table 1 input selection lines combination decide the signal to be forwarded at the output lines [16]. Multiplexers of different sizes can be designed by varying the number of selection lines i.e. n. Examples of a simple multiplexer of size 4:1 is shown below-

4:1 MUX- a 4:1 multiplexer contains 2 selection lines and 4 input lines. Figure 5 shows the block diagram and output equation of a 4:1 multiplexer.

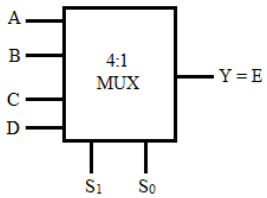

Figure 4: Block Diagram of a 4:1 Multiplexer

Output equation can be written as-

$$E = A.\overline{S_1}.\overline{S_0} + B.\overline{S_1}.S_0 + D.S_1.\overline{S_0} + D.S_1.S_0$$

III. MULTIPLEXER DESIGN USING REVERSIBLE LOGIC GATES

Multiplexers are data selector circuits. To design a multiplexer circuit using reversible logic gates there are few conditions of reversible circuit designing to be followed-

(a) There should be no feedback.
(b) There should be no fan-out.
(c) Garbage outputs should be minimum.
(d) Total number of gates should be minimum.

According to above conditions any digital circuit to be designed by reversible logic requires the optimum selection of basic reversible gate for minimizing the said variants[17, 18, 19].

Earlier researchers have proposed to use TKS gates to design the multiplexer circuit. TKS gate is a (3,3) reversible gate as explained in the subsection 2.2. Here we propose the designing of multiplexer circuit using the combination of TKS and VSMT gates to achieve better circuits. Following subsection explain the designing of 4:1 multiplexers in detail-

Design of 4:1 MUX using reversible gates- As explained in the earlier subsection, a 4:1 MUX has 2 selection lines and 4 input lines. The design of this multiplexer in reversible logic requires 3 TKS gates. Input signals are A, B, C, D and selection lines used are S_1 and S_0. The output variable is denoted by Y. The design approach 1 of the same using TKS gates only is shown in the figure 5 below.

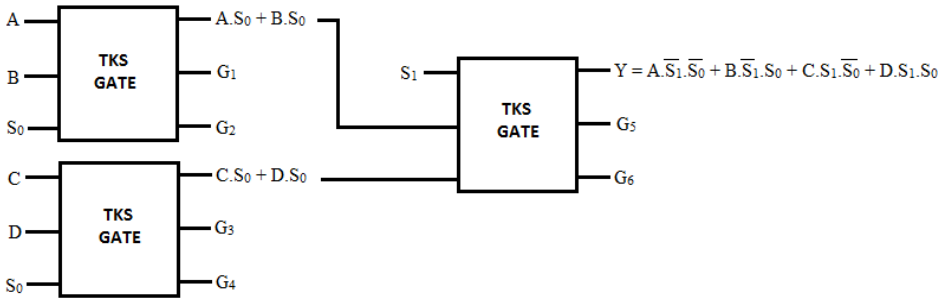

Figure 5: Approach 1 to design a 4:1 MUX using reversible gates

Where various output equations are given below-

$$E_1 = A.\bar{S}_0 + B.S_0$$
$$E_2 = C.\bar{S}_0 + D.S_0$$
$$Y = A.\bar{S}_1.\bar{S}_0 + B.\bar{S}_1.S_0 + C.S_1.\bar{S}_0 + D.S_1.S_0$$

Where E_1 and E_2 are intermediate results of the circuit. Above design produces 6 garbage outputs using a total of 3 reversible gates. Now we will design the same 4:1 MUX circuit using the proposed 6X6 reversible gate i.e. VSMT gate. This circuit design approach 2 is shown in the figure 6 below.

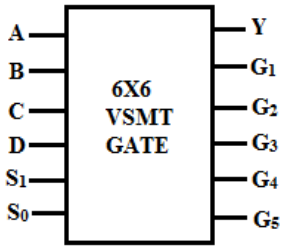

Figure 6: Approach 2 to design a 4:1 MUX using VSMT gate

Here various output equations are as shown below-

$$Y = A.\bar{S}_1.\bar{S}_0 \oplus B.\bar{S}_1.S_0 \oplus C.S_1.\bar{S}_0 \oplus D.S_1.S_0$$

In the approach 2 only one VSMT gate is used to design the 4:1 multiplexer. Input combinations applied to VSMT gate are by connecting A, B, C, D, S_1, S_0 i.e. input and selection line signals to the (A, B, C, D, E and F) input lines of the reversible gate. Output Y is taken from the P output line of the gate. Other outputs of the VSMT gate produce the garbage outputs (G_1, G_2, G_3, G_4, G_5). Here a total of 5 garbage output signals are produced by using single reversible gate. Comparison of these design approaches for 4:1 multiplexer is shown in the table 4 below.

Table 2: Comparison of various approaches to design a 4:1 MUX using reversible gates

S. No.	Variable	Approach 1	Approach 2
1	Total Number of Reversible Gates used	3	1
2	Total Number of Garbage Outputs	6	5
3	1-Bit XORs	3	1

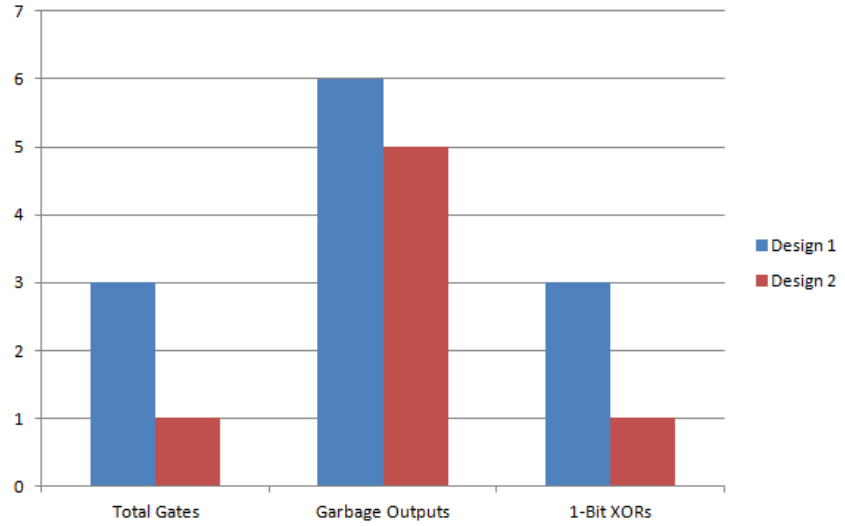

Figure 7: Comparison Chart for mux designs

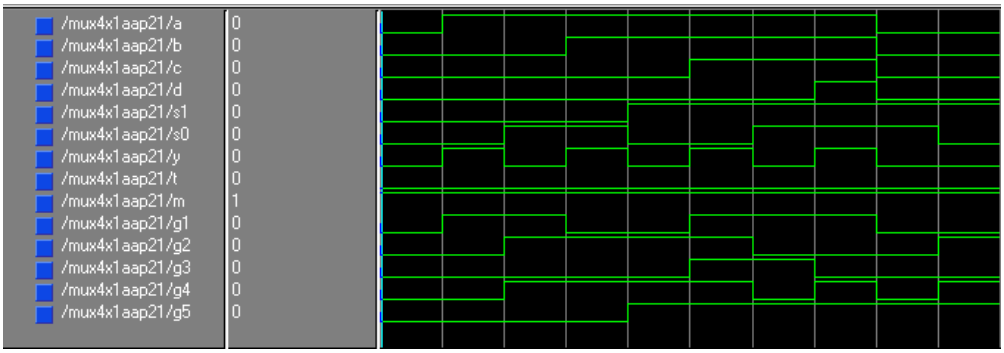

Figure 8: Simulated waveform

IV. RESULT AND ANALYSIS

As shown above in the table 2, the value of various variants to be considered in the process of reversible circuit designing reduces when the circuit for 4:1 multiplexer using reversible gate is designed with the help of the proposed VSMT gate. Here only one reversible gate is required to design the circuit of 4:1 multiplexer and the total number of garbage outputs produced are reduced to 5 as compared to 6 in the earlier designs proposed.

V. CONCLUSION AND FUTURE SCOPE

Reversible logic is becoming the modern way of digital logic circuit designing. Here in this paper we have designed reversible circuits for 4:1 multiplexer. The optimized circuits are achieved with help of a proposed reversible gate i.e. VSMT Gate, which is a (6,6) reversible gate. These designs can be further expanded to achieve the reversible circuits for various other functions and devices. As multiplexers are the basic building blocks of FPGA boards. These proposed multiplexers with reversible gates will help the researchers to employ these FPGAs with reversible gates in low power logical design applications.

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