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Design of a Multiplexer Using Reversible Logic

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Abstract. In the past few decades, the Reversible logic has emerged as one of the promising research areas find its applications in various emerging technologies such as Bioinformatics, Cryptography, Optical computing, Nanotechnology, DNA computing, and Quantum computing etc. This paper presents the implementation of multiplexers using reversible logic gates and evaluates their Gate count, Quantum cost and Garbage outputs.

Keywords: Reversible logic, Nanotechnology, Multiplexer.

1 Introduction

In the early 1960's researcher, R. Landauer proved that irreversible computation results in KTln2 joules of energy dissipation due to the each bit of information loss where K = Boltzmann's constant, T = Temperature at which computation is performed [1]. Later in 1973, C.H. Bennett showed that KTln2 joules of energy dissipation can be eliminated, if the computation is performed in a reversible manner [2].

A Multiplexer (MUX) is a combinational logic circuit. It consists of more than one input line, only one output line and one or more select line. A multiplexer with 2^N inputs has N select lines which are used to selects data or binary information available on any one of the input lines and steers it to the output line, therefore the multiplexer is named as a 2^N x 1 multiplexer or 2^N – to –1or 2^N : 1 multiplexer and it is known as a Data selector [3, 4].

The paper is structured as follows: Section II: briefly explains the fundamentals of Reversible logic, Section III: deals with the design of Reversible Multiplexers. Section IV: shows the simulation results. Comparisons between existing reversible multiplexer designs with the proposed reversible multiplexer designs are given in Section V. Section VI: gives the conclusion.

2 Reversible Logic

A Reversible logic gate is an m-input, m-output logic circuit which consists of an equal number of outputs and inputs. It produces a unique output vector from each input vector and vice versa.

The main goal in reversible logic synthesis is optimization of the number of reversible logic gates (Gate Count), quantum cost, constant inputs and garbage outputs [5, 6]. Gate count refers to number of reversible logic gates that are used for the implementation of the given reversible logic circuit [7]. Quantum cost is defined as the number of 1x1 and 2x2 reversible gates that are essential to realize the circuit [5]. The outputs of a reversible logic gate, which are needed to maintain the reversibility of a gate but not required for the further computation is known as Garbage outputs [5, 6]. Constant inputs relate to the inputs of a reversible gate to retain at constant value either '0' or '1' to produce a given logical expression [7].

Several reversible logic gates have existed in the literature. Among them, Fredkin gate and RMUX1 gate has been discussed below.

2.1 Fredkin gate

It is a three inputs and three outputs (3x3) reversible logic gate. Fig. 1 shows its logic circuit and the output equations of this gate are given as P=A, Q= A'B+AC, R= AB+A'C. The Fredkin gate has a quantum cost of Five [8].

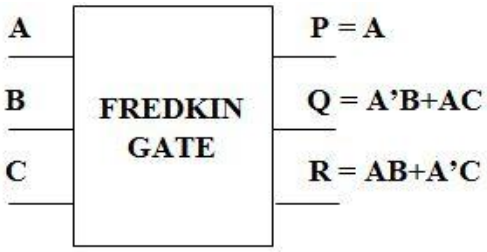

Fig. 1. Fredkin gate

2.2 RMUX 1 gate

It is a three inputs and three outputs (3x3) reversible logic gate. Fig. 2 shows its logic circuit and the output equations of this gate are given as P=A, Q= A'B+AC, R= A'C+AB'. The RMUX 1 gate has a quantum cost of Four [9].

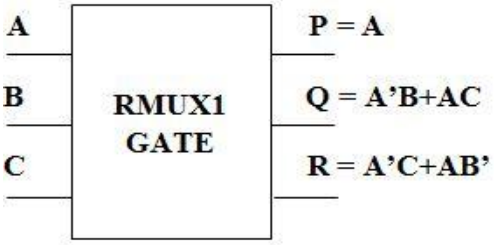

Fig. 2. RMUX1 gate

3 Designing of Reversible Multiplexers

In [7] the Reversible Multiplexers was proposed, with Fredkin Gates. In this design, the gate count, quantum cost and garbage outputs are calculated for different types of multiplexers.

In this presented design, the reversible multiplexers are implemented with a RMUX1 reversible logic gate which can be used as Multiplexer. A single RMUX1 Gate can be used as a 2 to1 Multiplexer as shown in Fig. 3. The output expression Y of Reversible 2x1 Multiplexer is given by $Y = S'I_0 + SI_1$.

Where S = select line,
I_0 , I_1 = Inputs,
Y = output

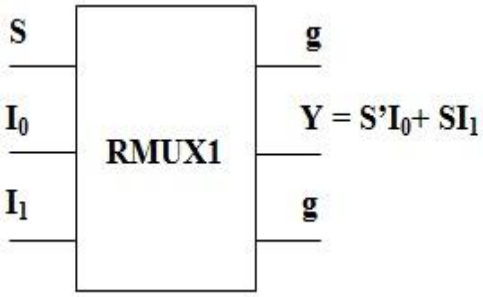

Fig. 3. RMUX1 Gate as a Reversible 2x1 Multiplexer

For designing a 4x1 Reversible Multiplexer three 2x1 Reversible Multiplexers are needed, which is as shown in Fig. 4. This design quantum cost is twelve and generates five garbage outputs. The Reversible 4x1 Multiplexer is implemented by using the following equation [4].

$$Y = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$$

For implementing an 8x1 Reversible Multiplexer, two 4x1 Reversible Multiplexer and one 2x1 Reversible Multiplexer are required which is as shown in Fig. 5. This design quantum cost is twenty eight and produces ten garbage outputs. The Reversible 8x1 Multiplexer is implemented based on the following equation [4].

$$Y = S_2'S_1'S_0'I_0 + S_2'S_1'S_0I_1 + S_2'S_1S_0'I_2 + S_2' S_1S_0I_3 +$$

$$S_2S_1'S_0'I_4 + S_2S_1'S_0I_5 + S_2S_1S_0'I_6 + S_2S_1S_0I_7$$

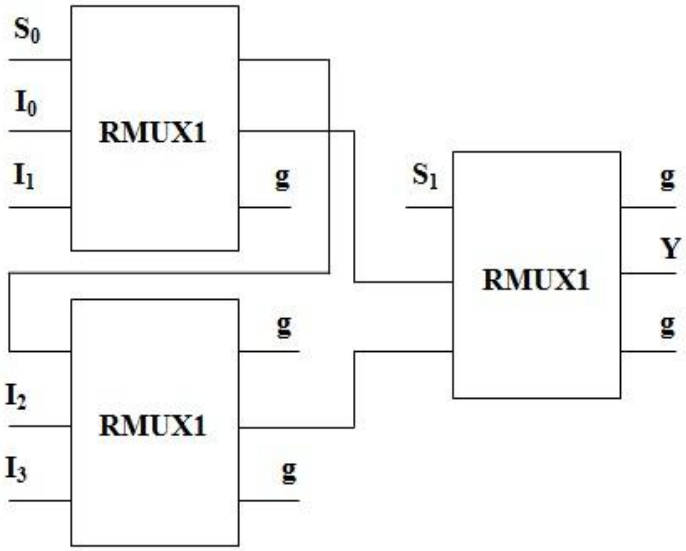

Fig. 4. Reversible 4x1 Multiplexer Using RMUX1 Gates

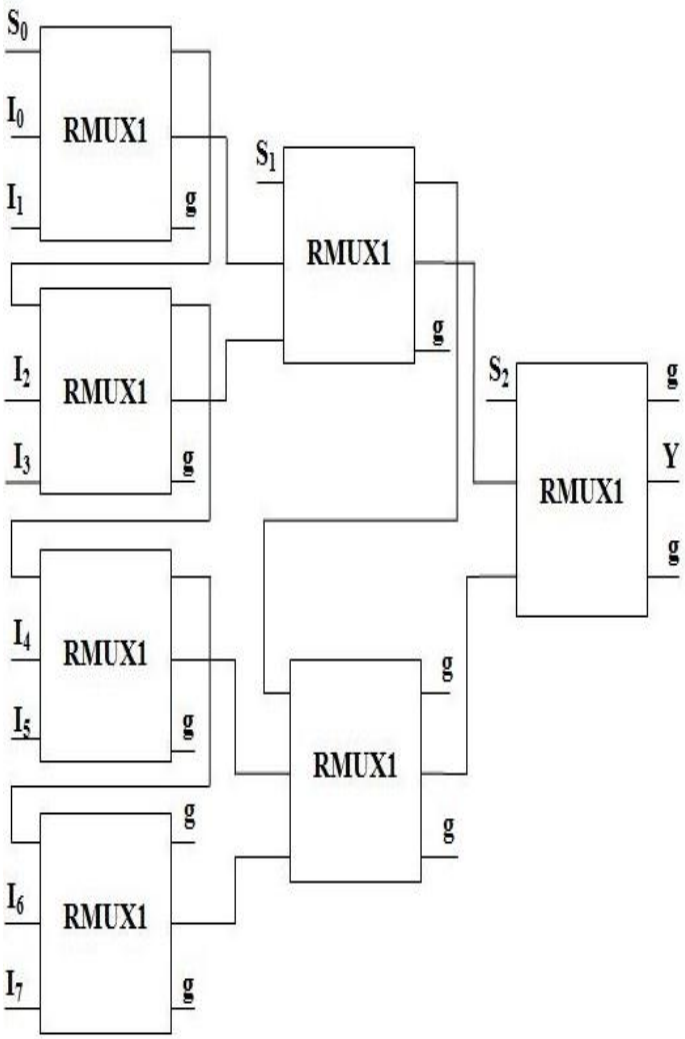

Fig. 5. Reversible 8x1 Multiplexer Using RMUX1 Gates

Higher bit Multiplexers can be implemented by cascading smaller multiplexers together. To design 2^N x 1 Reversible multiplexer (2^N-1) RMUX1 gates are needed where N is 1, 2, 3 …N with 4 (2N-1) quantum cost and produces (2^N+N-1) garbage outputs.

4 Simulation Results

The proposed reversible multiplexer designs are verified through a simulation process, for this test benches are written and simulations are performed to verify the logical correctness of the reversible multiplexer designs by using the Verilog Hardware Description Language in Xilinx ISE 14.3. The simulation waveforms for proposed reversible multiplexer designs are shown from Fig. 6 to Fig. 8.

Fig. 6. Simulation waveforms for Reversible 2x1 Multiplexer Using RMUX1 Gate

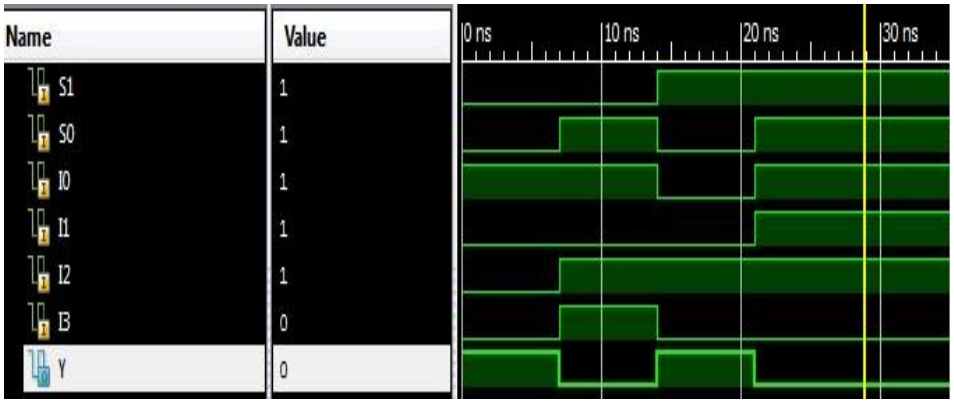

Fig. 7. Simulation waveforms for Reversible 4x1 Multiplexer Using RMUX1 Gates

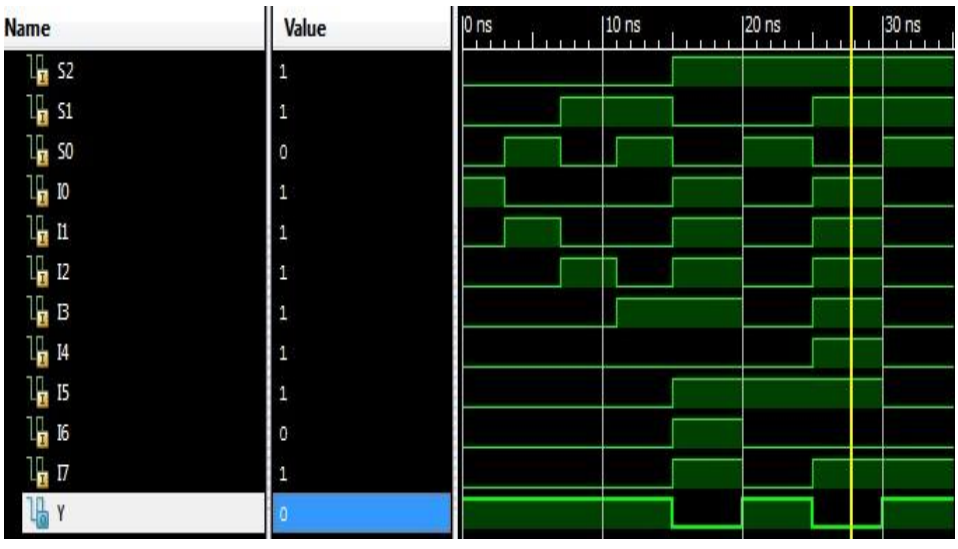

Fig. 8. Simulation waveforms for Reversible 8x1 Multiplexer Using RMUX1 Gates

5 Comparison

The Gate count, Garbage outputs and Quantum cost for proposed and existing reversible multiplexer designs comparison is given in Table. 1.

Table 1. Comparison of Cost Metrics of different proposed reversible multiplexer designs with existing reversible multiplexer designs.

MULTIPLEXER	COST METRICS		
	Gate Count	**Garbage Output**	**Quantum Cost**
2x1	1	2	4
2:1 [7]	1	2	5
4x1	3	5	12
4:1 [7]	3	5	15
8x1	7	10	28
8:1 [7]	7	10	35
16x1	15	19	60
16:1 [7]	15	19	75
2^Nx1	2^N-1	2^N+N-1	$4(2^N-1)$
2^N:1 [7]	2^N-1	2^N+N-1	$5(2^N-1)$

6 Conclusion

In this work, multiplexers are implemented by using reversible logic gates. The obtained results from proposed reversible multiplexer designs are compared to the existing reversible multiplexer designs which show the reduction in the quantum cost.

References

1. R. Landauer.: Irreversibility and Heat Generation in the Computing Process, IBM Journal of Research and Development. vol. 5, pp. 183-191 (1961)
2. C.H. Bennett.: Logical reversibility of Computation, IBM Journal of Research and Development. vol. 17, pp. 525-532 (1973)
3. M.Morris Mano.: Digital Design. Prentice Hall Publisher (2001)
4. Anil k. Maini.: Digital Electronics. Principles, Devices and Applications, John Wiley & Sons (2007)
5. Mozhgan Shiri and Majid Haghparast.: Design of the Efficient Nanometric Reversible Subtractor Circuit. Research Journal of Applied Sciences, Engineering and Technology, vol. 4, pp 4561-4564 (2012)
6. Himanshu Thapliyal and Nagarajan Ranganathan.: Design of Efficient Reversible Binary Subtractors Based on a New Reversible Gate. IEEE Computer Society Annual Symposium on VLSI, pp. 229-234 (2009)
7. Rakshith Saligram, Shrihari Shridhar Hegde, Shashidhar A Kulkarni, H.R. Bhagyalakshmi, M K Venkatesha.: Design of Fault Tolerant Reversible Multiplexer based Multi-Boolean Function Generator using Parity Preserving Gates. International Journal of Computer Applications, Vol. 66, pp 20-24 (2013)
8. Fredkin.E And Toffoli. T.: Conservative Logic. International Journal of Theoretical Physics, vol. 21, pp 219-253 (1982)
9. M Morrison , M Lewandowski and N Ranganthan.: Design of a Tree based Comparator and Memory Unit based on a Novel Reversible Logic Structure. IEEE Computer Society Annual Symposium on VLSI, pp. 331-336 (2012)