Efficient Implementation of Fault-tolerant $4:1$ Quantum Multiplexer(QMUX) using Clifford+T-group

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***Abstract*—Since last couple of years quantum computing has made tremendous advancement towards developing the next generation computing paradigm and much to this cause several investigations already have started to make efficient implementation for quantum logic circuit. By considering several design constraints especially from noisy sources, new design models (like Nearest Neighbor design, Fault-tolerant architecture, single $T-depth$ design) are evolving on daily basis. Focusing on this need, here in this work we show an efficient implementation of Quantum Multiplexer circuit towards realizing the quantum ALU. Two different design models are shown here, where in the first model, we have proposed the ancilla free garbage based implementation of MUX circuit and in the second model, we improve the previous design to make it garbage free. In our design phase, initially we have derived smaller modules and then they are integrated to make the generalized representation. For, ensuring fault-tolerant property in our made designs, we have used the functional power of Clifford +T group. All the made circuits are tested over input vectors and the logical correctness of the designs have been verified individually.**

Keywords:- QMUX, QECC, Clifford+T, $T-depth$, $T-count$.

I. INTRODUCTION

Revolutionary Quantum Computer (QC) has evolved as a game-changer in the field of computational world with promise to solve classically intractable problem(s) [1], [2] which seems to be impossible for today's technologies. However, the quantum computer is still now in infancy and long way off to achieve so-called quantum supremacy due to catastrophic obstacles from noisy sources. Basically, quantum computer works on the principle of quantum mechanical phenomena and relies on quantum bit (Qubit) in lieu of classical bits [3]. The formal definition, and properties on qubit is presented in section II.

Literally, quantum states are highly fragile. On the other hand, quantum hardware are highly susceptible towards noise which affects the coherent superposition of the quantum basis states and may collapse into classical states prior to termination of computational process called as Decoherence [4].

In way to achieve so-called quantum supremacy in near-future, powerful quantum information processor (QIP) with low execution time is need to be realized along with ability to suppress inherent noise as well in way to retrieve the correct information from the errors [5].

Hereof, Quantum Error Correction Code (QECC) has been used in a systematic way to detect and correct the errors. In this regard, the surface code has come out as the most promising one which has high error threshold value (approximately 0.75%) [6]. So, a suitable fault-tolerant quantum circuit is to be modelled for translation of most powerful quantum algorithm into circuital form so as to limit the error rate per gate within the threshold limit [7].

The fault-tolerant property can be achieved tranversally over the operators which eventually restricts the diffusion of errors within the encoded blocks of QECC. In contrast, there does not exist any operators are available *w.r.t.* any default QECC which is transversal as well as universal for encoding of quantum algorithms. However, a universal transversal gate set is most desirable to achieve fault-tolerance in greater extent which can be accomplished in turns of huge space-time overheads. For example, distillation and state injection approaches are used in surface code [6].

Now a days, the Clifford+T-group is used as universal set of primitive transversal operators which has the ability to decompose Multi Controlled Toffoli gate (MCT) up-to size of three qubits into fault-tolerant structure without using any ancilla inputs [5]. The details about the popular Clifford+T-group is described in section II.

In fact, the non-Clifford phase gate *viz.* T -gate has high resource overheads as well as high latency in compared to Clifford-group. Basically, circuit-depth of any fault-tolerant quantum circuit is the summation of Clifford gate-cycles and non Clifford phase gate-cycles. Thus, the mapping of any Boolean function into fault-tolerant circuital form without using any ancilla input(s) in low circuit-depth especially in low $T-depth$ is still now an open problem. Further, it is necessary to minimize $T-count$ and $T-cycle$ to elude inevitable issues with respect to noise.

In this conjecture, Clifford+T-based fault-tolerant circuit for Quantum Multiplexer (QMUX) has been proposed. This MUX is an integral part of the most crucial Arithmetic Logical Unit (ALU) and is always embedded with QIP. In addition to

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this, our proposed methodology ensures cost optimized designs *w.r.t.* $T-depth$ and $T-count$. Now, here we are highlighting our key contribution as follows:

- we have designed fault-tolerant 2:1 QMUX with two different features *viz.* with no-ancilla input and other one is garbage-free.
- We have used the approach stated in [8], [5], [9] in the realization of fault-tolerant $4:1$ QMUX.

The reminder of this paper is organized as follows: Section II provides a detail Background for better apprehension of this paper. In Section III, our method is presented. In Section IV, experimental result and comparative analysis are summarized. Finally, the work is concluded in Section V.

II. BACKGROUND

In this section, we briefly discuss about some basic fundamentals related to quantum circuit, circuit performance parameter and Multiplexer models.

A. Quantum Circuits

Definition 2.1 (Qubit): It is abbreviated from the term "**Qu**antum" "**bit**" and used to represent quantum information states. Mathematically, it is defined as the coherent superposition of basis ortho-normal states with complex probability. It is denoted by *Ket*-function as $|\psi\rangle$.

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \tag{1}$$

where $\alpha, \beta \in C \;\; and \;\; |\alpha|^2 + |\beta|^2 = 1$

Definition 2.2 (Quantum circuit): It is a directed acyclic graph where vertices are primitive quantum operators known as quantum gate, of finite set and takes the input as tensor product of input states.

Basically, all elementary primitive quantum gates are either be 2x2 or 4x4 unitary transfer metrics.

Definition 2.3 (Clifford+T-group): It is a set of universal transversal primitive gates which contains CNOT-gate with 1-qubit H-gate, S-gate, Pauli(X, Y, Z)-gate and non-Clifford T-gate [5].

The T-gate represents 4^{th}-root of Pauli-Z-gate. Mathematically, the T-gate is expressed through transfer matrix by

$$T = \begin{bmatrix} 1 & 0 \\ 0 & e^{\frac{i\pi}{4}} \end{bmatrix} \tag{2}$$

Definition 2.4 (Clifford+T-based fault-tolerant representation Toffoli-gate): Fig. 1a presents reversible Toffoli gate which toggles the state of the target bit when both the control bits are to 1. The Clifford+T-based fault-tolerant implementation is presented in Fig. 1c and its unit phase-depth based design using additional ancilla input is shown in Fig. 1d.

For better apprehension, here, a list of the quantum gates and its properties are illustrated in Table I.

Definition 2.5 ($T-count$): The minimum number of logical T-gates requires to realize a Boolean function into quantum circuital form is termed as $T-count$.

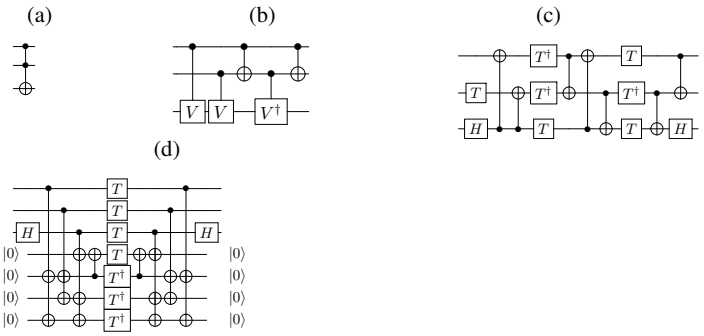

Fig. 1: (a) *Reversible Toffoli gate.* (b) *Equivalent NCV-based decomposition of Fig. 1a.* (c) *Equivalent Clifford+T-based realization of Fig. 1a as depicted in [5, Fig. 1.(c)].* (d) *Equivalent unit T-depth based realization of Fig. 1a as depicted in [9, Fig. 1].*

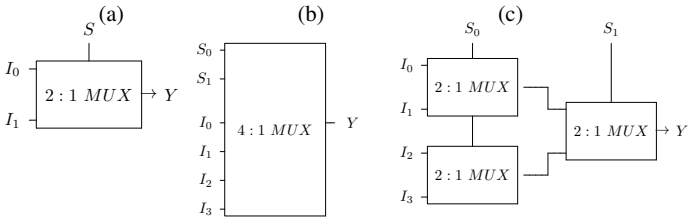

Fig. 2: (a) *Schematic diagram of 2:1 MUX.* (b) *Schematic diagram of 4:1 MUX.* (c) *Realization of 4:1-MUX using 2:1 MUX.*

Basically, T-gate flips the phase of the quantum state with no effect towards bit flip and due to this reason, T-gate is known as phase gate.

Definition 2.6 ($T-depth$): The number of $T-cycle$ requires to execute all the T-gates of quantum circuit is known as $T-depth$.

B. Multiplexer

Multiplexer (MUX) is an electronic switching network which accept multiple inputs and provides single output. Basically, MUX passes selective input signal to the output based on the condition of select lines. The MUX contains two different kind of inputs *viz.* signal lines as well as select lines. In this paper, I_i stands for input data lines, S_j stands for select lines; whereas Y stands for output. The MUX takes n-select lines to select 2^n-input data lines to output. Fig. 2a represents schematic diagram for 2:1 Multiplexer and $4:1$-MUX is shown in Fig. 2b. MUX circuits are widely used in communication system as switching network, in ALU for multi-operation.

III. PROPOSED TECHNIQUE

In this section, we present a methodology to realize Clifford+T-based fault-tolerant circuit for $2:1$-QMUX in

TABLE I: Elementary Quantum Gates and Their Properties

Name of elementary quantum gate	Block diagram	Transformation matrix	Properties
NOT (X)		$\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}$	$X\|0\rangle = \|1\rangle$ $X\|1\rangle = \|0\rangle$
CNOT(CN)		$\begin{bmatrix}1 & 0 & 0 & 0\\ 0 & 1 & 0 & 0\\ 0 & 0 & 0 & 1\\ 0 & 0 & 1 & 0\end{bmatrix}$	$\|00\rangle \rightarrow \|00\rangle$ $\|01\rangle \rightarrow \|01\rangle$ $\|10\rangle \rightarrow \|11\rangle$ $\|11\rangle \rightarrow \|10\rangle$
Z gate	$-\boxed{Z}-$	$\begin{bmatrix}0 & 0\\ 0 & -1\end{bmatrix}$	$X\|0\rangle = \|0\rangle$ $X\|1\rangle = -\|1\rangle$
S gate	$-\boxed{S}-$	$\begin{bmatrix}1 & 0\\ 0 & i\end{bmatrix}$	$S\|0\rangle = \|0\rangle$ $S\|1\rangle = e^{\frac{i\pi}{2}}\|1\rangle$
$S^\dagger$gate	$-\boxed{S^\dagger}-$	$\begin{bmatrix}1 & 0\\ 0 & e^{\frac{-i\pi}{2}}\end{bmatrix}$	$S^\dagger\|0\rangle = \|0\rangle$ $S^\dagger\|1\rangle = e^{\frac{-i\pi}{2}}\|1\rangle$
T gate	$-\boxed{T}-$	$\begin{bmatrix}1 & 0\\ 0 & e^{\frac{i\pi}{4}}\end{bmatrix}$	$T\|0\rangle = \|0\rangle$ $T\|1\rangle = e^{\frac{i\pi}{4}}\|1\rangle$
$T^\dagger$gate	$-\boxed{T^\dagger}-$	$\begin{bmatrix}1 & 0\\ 0 & e^{\frac{-i\pi}{4}}\end{bmatrix}$	$T^\dagger\|0\rangle = \|0\rangle$ $T^\dagger\|1\rangle = e^{\frac{-i\pi}{4}}\|1\rangle$
Hadamard(H)	$-\boxed{H}-$	$\frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix}$	$H\|0\rangle = \frac{1}{\sqrt{2}}(\|0\rangle + \|1\rangle)$ $H\|1\rangle = \frac{1}{\sqrt{2}}(\|0\rangle - \|1\rangle)$

subsection III-A, $4:1$-QMUX in III-B.

A. *Fault-tolerant implementation of 2:1 QMUX*

Here, we are designing the fault-tolerant implementation of $2:1$-QMUX by invoking Clifford+T-group. In the later part, we also have investigated how to make the design efficient by optimizing $T-count$ and $T-depth$ parameters. Two different design models are shown here, where in the first model we have used the indeterminate design of [10] to build ancilla free MUX circuit. In the other model, ancilla-based implementation of fault-tolerant MUX is proposed by considering the $2:1$ MUX of [11] as indeterminate template.

1) Design1(Fault-tolerant implementation of $2:1$*-QMUX with no-ancilla):* Here Fredkin-based $2:1$-RMUX is shown in Fig. 3a which is also used as intermediary circuit. In this design, the I_0 and I_1 represents input states; whereas S represents select line. The output (Y) takes the state of input(s) in accordance to the conditional state of the select line. The Toffoli-based realization of Fig. 3a is derived in Fig. 3b.

In way to map Fig. 3b into Clifford+T-group, the said figure is scanned and found that it contains two CNOT-gates and one Toffoli-gate. During the mapping of the said design into Clifford+T-group, the CNOT-gates remained same whereas; Toffoli gate is replaced by Fig. 1c and the resulting circuit is shown in Fig.3c. Furthermore, the same Toffoli gate can be replaced by its equivalent unit $T-depth$ structure (*pl. see* Fig. 1d) and also can be transformed to more desirable unit $T-depth$ based design. However, this transformation will cost additional 4 ancilla overhead in the subsequent design. The resulting unit $T-depth$ based fault-tolerant $2:1$ QMUX is formed in Fig. 3d. Both the out-coming figures contain garbage output which further has added design overhead in the circuit.

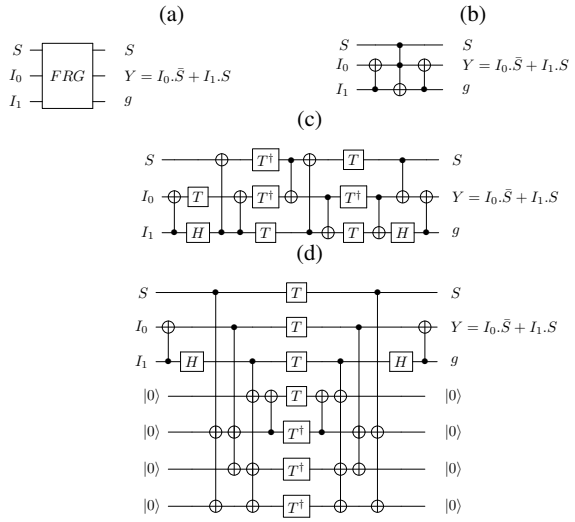

Fig. 3: *(a) Fredkin gate-based 2:1 RMUX. (b) Toffoli realization of Fig. 3a. (c) Clifford+T-based realization of Fig. 3a. (d) Unit $T-depth$ based Clifford+T realization of Fig. 3a*

2) Design2 (Garbage free Realization of Fault-tolerant $2:1$*-QMUX with one ancilla input):* Fig. 5a presents the schematic diagram of $2:1$-RMUX which has one ancilla input and the subsequent implementation of Toffoli-gate based design of Fig. 5a is derived in Fig. 5b.

Fig. 5b contains two Toffoli-gates, and one CNOT-gate. So, we replace both the Toffoli-gates with its equivalent

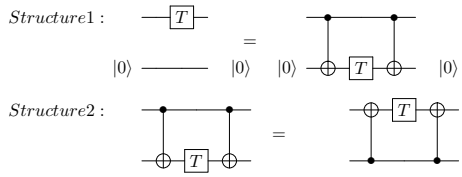

Fig. 4: Equivalent fault-tolerant circuit identities as depicted in [8, Fig. 3(f)]

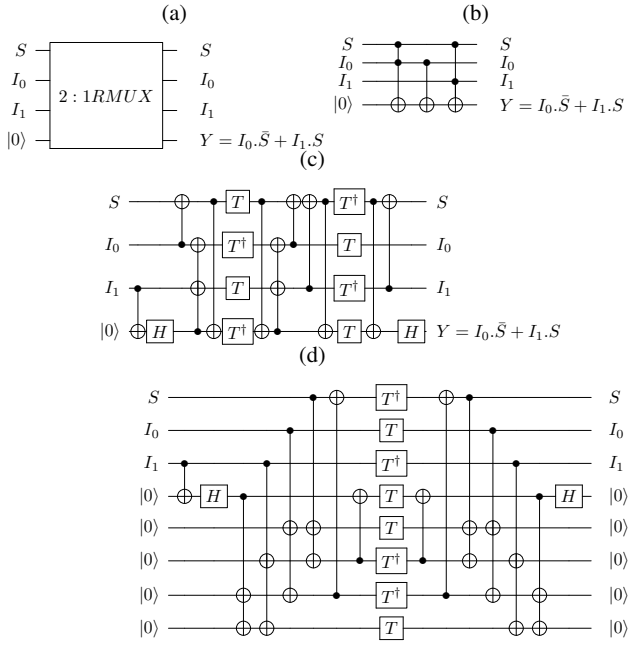

Fig. 5: (a) $2:1$ *RMUX with one ancilla.*(b) *Proposed Toffoli realization of Fig. 5a.* (c) *Clifford+*T*-based realization of Fig. 5a.* (d) *Unit* $T-depth$ *based realization of Fig. 5a.*

Clifford+T-based structure as depicted in Fig. 1c followed by optimization of primitive quantum operators; where successive gates are eliminated if their net effect is identity. For example the net effect of two successive CNOT-gates operated on same control and target bit, successive H-gate and T, $T^\dagger$-gate is identity. Besides, we use inverse polarity-based Toffoli-gate(s) to reduce error caused due to De-coherence. After the due procedure of mapping and optimization, the resultant circuit is obtained in Fig. 5c.

In way to transform the design into unit $T-depth$ based fault-tolerant QMUX circuit, we use Mathematical model of [8] Considering that circuital identities followed by multiple iterative process over Fig. 5c, the resulting circuit is reported in Fig. 5d which has unit $T-depth$. For better apprehension, we present both the structures in Fig. 4.

B. Fault-tolerant implementation of 4:1-QMUX

Here, we design fault-tolerant $4:1$-QMUX in two steps considering different designs of $2:1$-QMUX.

1) Fault-tolerant implementation of Fredkin-based $4:1$*-QMUX:* The $4:1$-QMUX can be designed by assembling of $2:1$-QMUXs as depicted in Fig. 2c; where 2^2-1 numbers of $2:1$-QMUX is placed in $\frac{\pi}{2}$ angle right-inclined pyramid structure with 2-level which is same as number of select lines. So, $4:1$-QMUX can directly be realized by replacing each $2:1$-QMUX of Fig. 2c by its equivalent Clifford+T-based structure either using the structure of Fig. 3c or Fig. 3d.

a) case-1: In Fig. 2c, all the $2:1$-QMUX in each level operates in parallel. So, replacement by Fig. 3c incurs $6\ T-depth$ for overall $4:1$-QMUX as each Fig. 3c has $3\ T-depth$.

b) Case-2: Here, we take Fig. 3d in lieu Fig. 3c as basic building block. Though Fig. 3d has unit $T-depth$ which eventually reduces overall $T-depth$ of the $4:1$-QMUX design but, four additional ancilla is needed. On the other hand, parallel operation of $2:1$-QMUX in each level restricts the reuse of that four ancilla inputs to each $2:1$-QMUX in each level which results at most 2^{2+1} *i.e.* 8 numbers of ancilla inputs. So, overall $4:1$-QMUX has $2\ T-depth$ as each $2:1$ QMUX has unit $T-depth$ and at most 2^{2+1} numbers of ancilla.

In special case, if we reuse that four additional ancilla input and place it on top of $2:1$-QMUX of level-1 by remaining $2:1$-QMUX in Fig. 2c then the overall $T-depth$ of the $4:1$-QMUX becomes $4-1$ *i.e.* 3 and number of ancillae turns to be 4.

2) Fault-tolerant implementation of $4:1$*-QMUX using Fig. 5a:* To realize the said design, we are extrapolating existing $2:1$-RMUX (*pl. see* Fig. 5a) and formulating a generalized representation of reversible $4:1$-RMUX in Fig. 7a. The output ($Y = I_0.\bar{S}_1.\bar{S}_0 + I_1.\bar{S}_1.S_0 + I_2.S_1.\bar{S}_0 + I_3.S_1.S_0$) of $4:1$-QMUX contains Boolean sum of four literals which can be translated into XOR function of literals where each literal is represented by Mixed Polarity MCT (MPMCT)-gates as shown in Fig. 7b. Further, Fig. 7b is translated into MCT-based structure (*pl. see Fig. 7c*). On finding, Fig. 7c contains four 3-MCT-gates, four Toffoli-gates along with one CNOT-gate. For ease of mapping, internal gates are rearranged within Fig. 7c and the obtained structure is presented in Fig. 7d.

For efficient mapping, Fig. 7d is mapped into NCVW-based structure followed by elimination of extraneous gates. The resulting NCVW-based circuit is reported in Fig. 7e.

Now, Fig. 7e is scanned from left to right in top-down fashion and it is found that similar kind of sub-structures (*pl. see Fig. 8a*) exist in inverse polarity which can be translated using Clifford+T-group through successive intermediate replacements. Fig. 8 presents the resultant design where each sub-structure is derived from the preceding sub-structure.

Furthermore, the CV, $CV^\dagger$, CS and $CS^\dagger$ gates are directly replaced by its equivalent Clifford+T-based structure as depicted in [5, Fig. 1(b)]. Fig. 6 represents Clifford+T-based equivalent fault-tolerant representation of CV, $CV^\dagger$, CS and $CS^\dagger$ gates. After replacing of each template-based

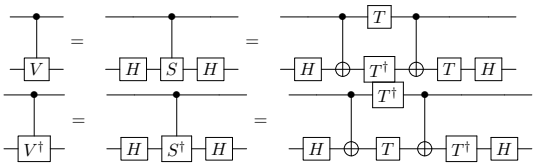

Fig. 6: Clifford+T-based fault-tolerant circuit of CS, $CS^\dagger$, CV, and $CV^\dagger$-gates as depicted in [5, Fig. 1(b)]

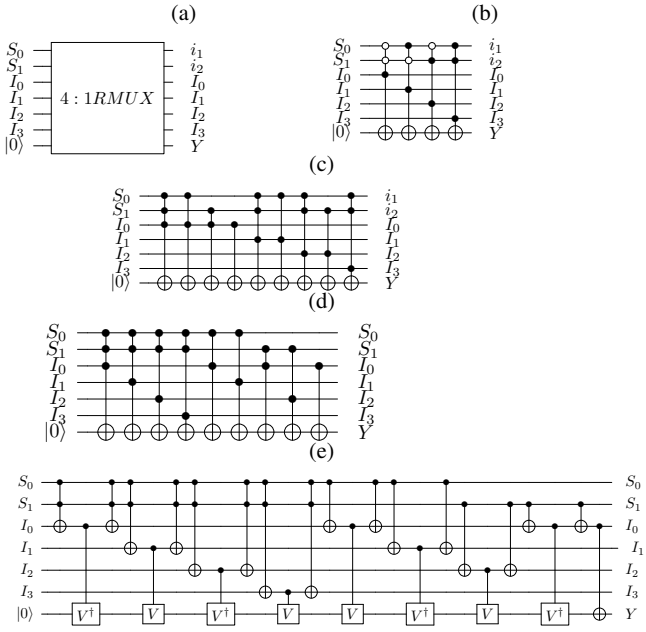

Fig. 7: (a) *Proposed* $4:1$*-RMUX with one ancilla.*(b) *MPMCT-based realization of Fig. 7a.* (c) *MCT-based realization of Fig. 7b.* (d) *Reconfiguration of Fig. 7c.* (e) *NCV-based optimized structure of Fig. 7d.*

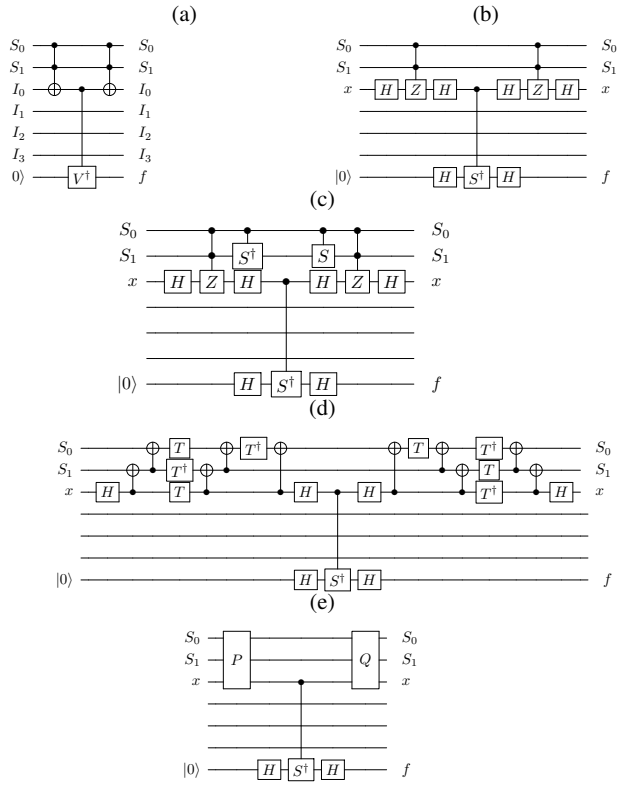

Fig. 8: (a) *Sub-structure of Fig. 7e.* (b) *Translation of Fig. 8a into Hadamard(H)-gate, CCZ, and* $CS/CS^\dagger$ *gates.* (c) *Appending of* $CS/CS^\dagger$*-gate into Fig. 8b.* (d) *Replacement of templates by Clifford+*T*-based structure as depicted in [9].* (e) *Equivalent representation of Fig. 8d in schematic diagram.*

sub-structure of Fig. 7e using equivalent Clifford+T-based structures defined in Fig. 8 and in Fig. 6 followed by elimination of redundancy gates, the resulting circuit is obtained in Fig. 9.

IV. Experimental result and comparative analysis

Here, we provide results over the performance parameters associated with each design in table- II for comparison of proposed approach with existing design approach. As, there hardly exists any fault-tolerant implementation of $4:1$-QMUX for which we remain unable to compare our results with state-of-the-art design models. However, some design approach has reported over reversible logic in [12], [13], [14], [15], [16], [17], [18], [19], [20], [21].

In III-A1, though the proposed method has realized fault-tolerant circuit for $2:1$-QMUX and $4:1$-QMUX but, the information of either of the input lines for each $2:1$-QMUX is lost during the operation of QMUX which is very essential in other operation too within the ALU. As fan-out is not allowed in quantum phenomena, so the design approach in III-A2 is more useful even though it takes an additional ancilla input, where all the input lines are reflected in output and are available for other purposes.

In our mapping approach, we have used matrix identities in the decomposition of large reversible gates into set of primitive transversal quantum operators to achieve fault-tolerance property and to satisfy no-cloning theorem. In addition to these, opposite polarity-based templates are used to minimize the effect of Decoherence.

V. Conclusion

In this work, we have shown Clifford+T-based implementation of $4:1$ Quantum Multiplexer Circuit (QMUX). The functional power of Clifford+T library is extensively used to achieve fault-tolerance. During the design, multiple strategies have been adopted to make the design more efficient like low $T-depth$-based templates are used to contain the coherence

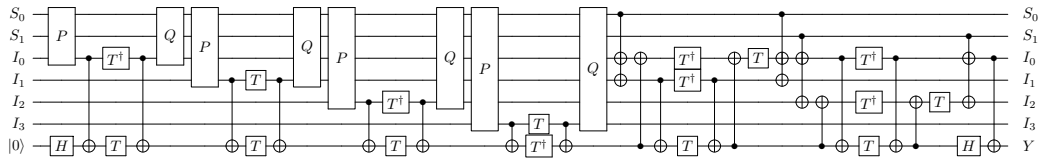

Fig. 9: Garbage free fault-tolerant implementation of $4:1$-QMUX using Clifford+T-group

TABLE II: Incurred Cost Values of Our Proposed Designs

Name of the QMUX	Design Methodology		Performance parameter(s)			
	Design1(with Garbage	Design2(Garbage free	$T-count$	$T-depth$	**Number of garbage output)**	**No. of ancila lines**
2:1-QMUX	Regular deign	-	7	3	1	0
	Unit T-depth deign	-	7	1	1	4
	-	Regular deign	8	2	0	1
	-	Unit T-depth deign	8	1	0	5
4:1-QMUX	Regular deign	-	21	9	4	0
	low T-depth deign	-	21	3	3	6
	-	Regular deign	48	24	0	1
	-	Unit T-depth deign	-	-	-	-

time of entanglement of quantum basis states. In this work, we are unable to design unit Phase-depth based fault-tolerant $4:1$-QMUX due to the limiting power of Clifford+T-group which can not decompose n qubit MCT-gate for $n \geq 4$ into fault-tolerant structure without the help of ancilla input [5].

In future, we are focusing to realize unit $phase-depth$ based fault-tolerant circuit for $N:1$ QMUX using newly reported Clifford+Z_N-group [22].

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