REPORT LAB-1

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Table 1: Implementation results for the 3 different implementations of the studied circuit.

	Baseline Circuit	**Pipelined Circuit**	**Shared HW Circuit**
Resources for one circuit	36 ALMs + 6 DSPs	92 ALMs + 4 DSPs	30 ALMs + 1 DSPs
Operating frequency	45.45 MHz	215.05 MHz	1GHz
Critical path	ALM-based multiplier and adder + 2x DSP mult + ALM-based adder + 6x DSP mult + ALM-based adder	mult2+addr2+mult3+ addr2_pipelined	Getting Error
Cycles per valid output	1	1	5
Max. # of copies/device	1518 DSPs/6 DSPs = 253 copies per device	1518 DSPs /4 DSPs = 380	1518 DSPs/1 DSP =1518 copies/device
Max. Throughput for a full device (computations/s)	45.45 * 10^6 *253 = 11.5 *10^9 computations/s	215.05 *10^6 * 380 = 81.7 *10^9 computations/s	1GHz * 1518 computations/s
Dynamic power of one circuit	0.98 mW	4.02mW	Getting vcd error, unable to change settings.
Max. throughput/Watt for a full device	3.55 *10^9 computations/watt	18*10^9 computations/watt	Getting vcd error, unable to change settings.

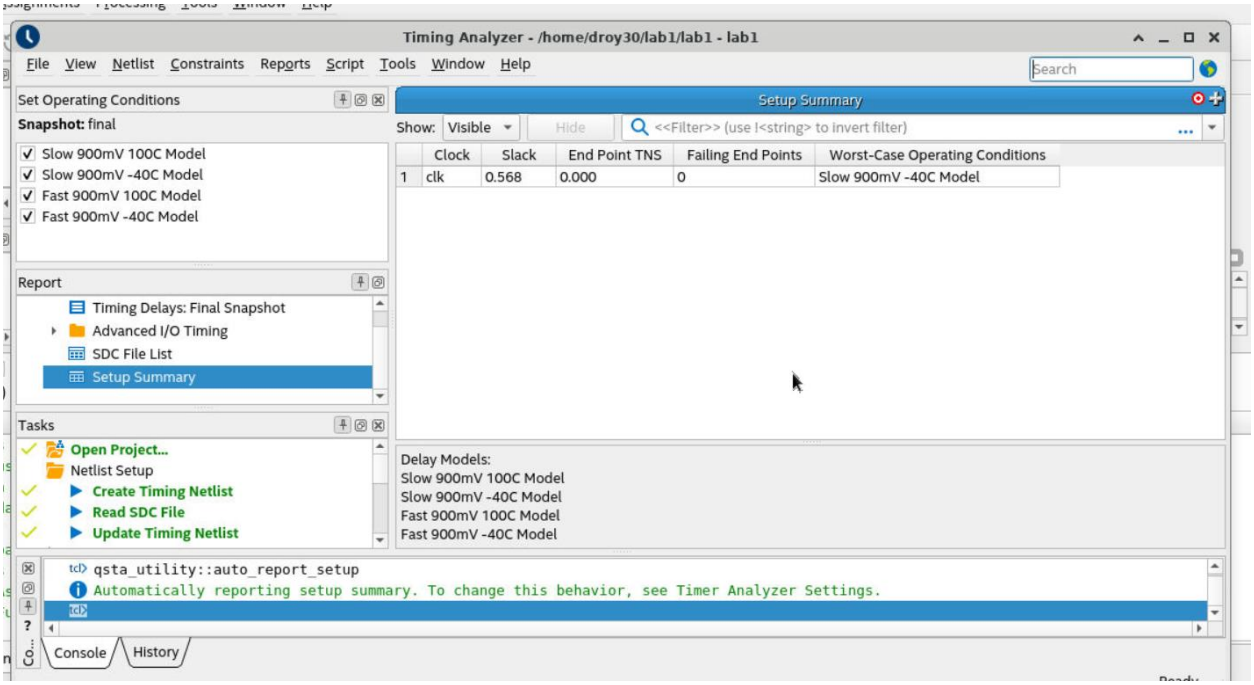
Baseline Implementation:

At frequency 45.45MHz (22ns)

Dynamic power of one circuit: 0.98 mW from the picture provided below at frequency of 45.45 MHz

Max. throughput/Watt for a full device: Power used = 0.98 * 253 + 2992.23 = 3240.17 mW

Therefore, max throughput/watt = 11.5 *10^9 /3240.17*10^(-3) = 3.55 *10^9 computations/watt


Timing Analyzer - /home/droy30/lab1/lab1 - lab1
File View Netlist Constraints Reports Script Tools Window Help
Search
Set Operating Conditions
Snapshot: final
Slow 900mV 100C Model
Slow 900mV -40C Model
Fast 900mV 100C Model
Fast 900mV -40C Model
Setup Summary
Show: Visible
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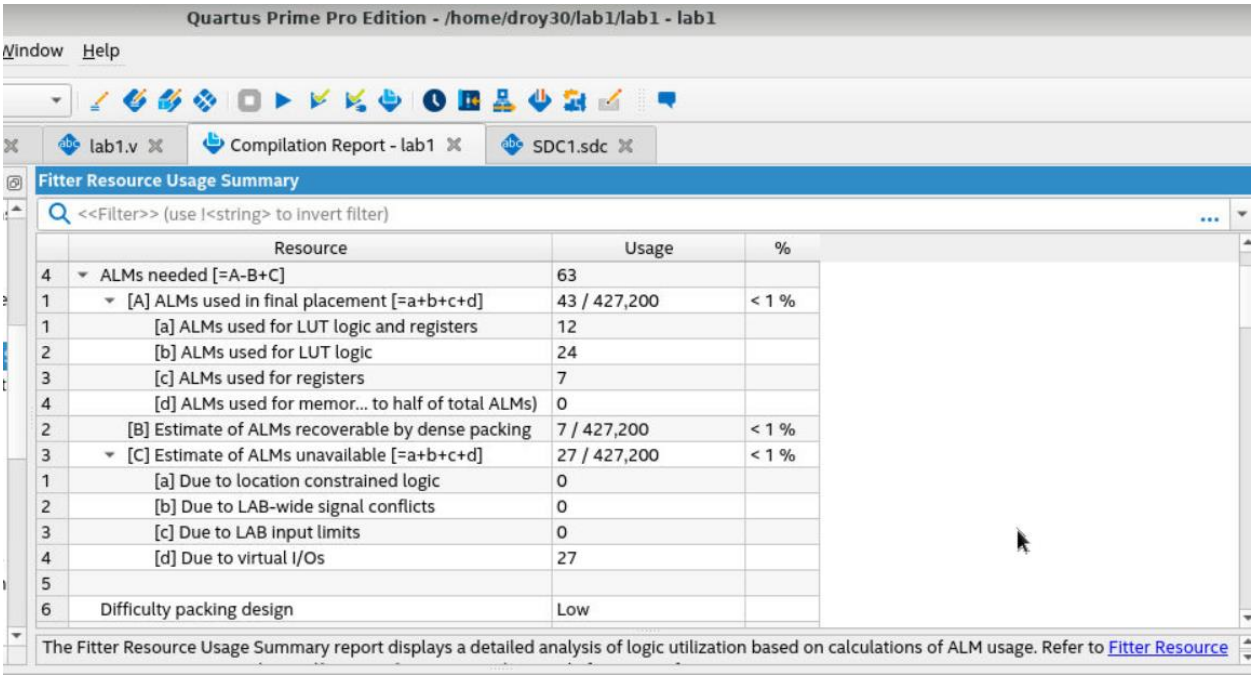
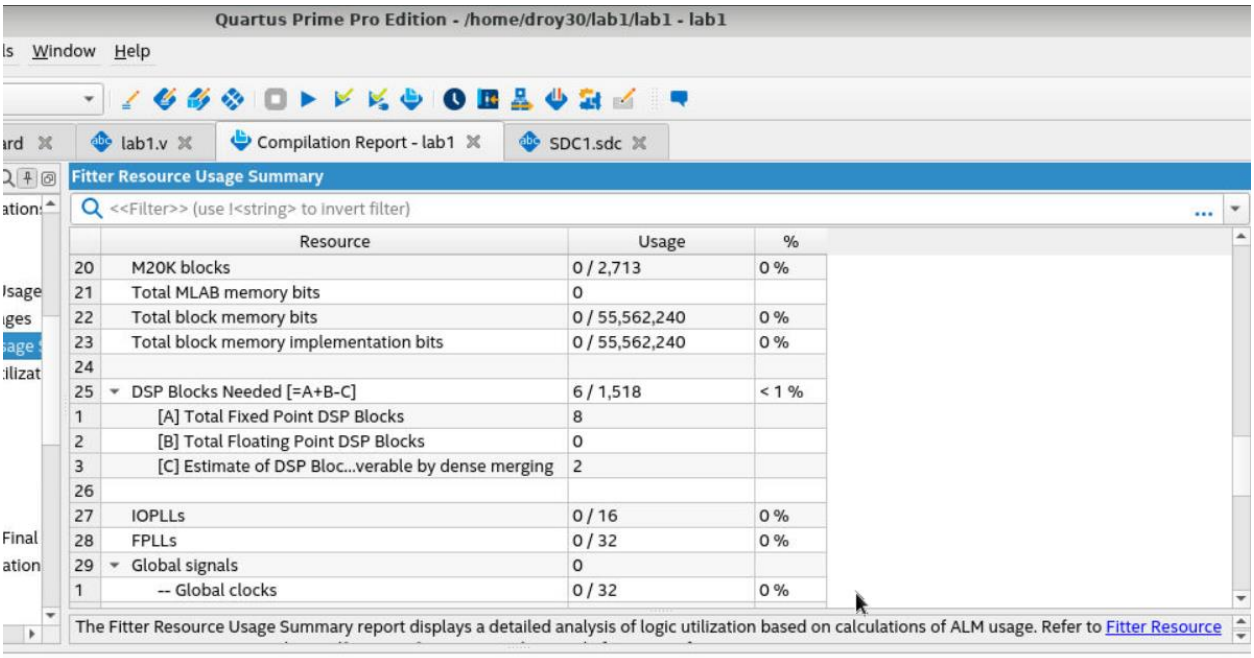
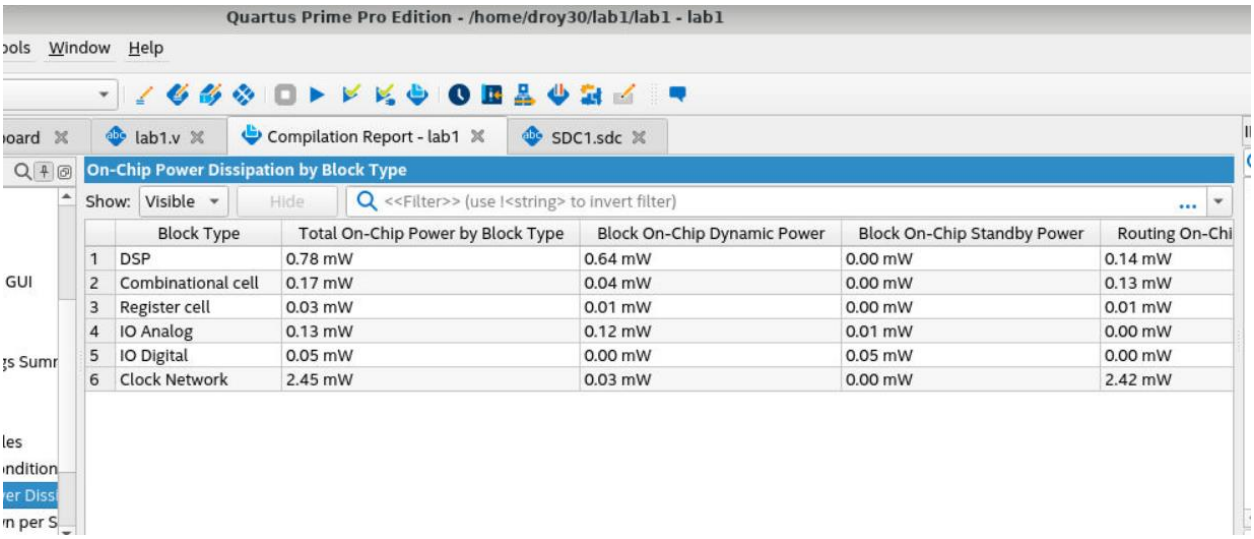
Clock Slack End Point TNS Failing End Points Worst-Case Operating Conditions
1 clk 0.568 0.000 0 Slow 900mV -40C Model
Report
Timing Delays: Final Snapshot
Advanced I/O Timing
SDC File List
Setup Summary
Tasks
Open Project...
Netlist Setup
Create Timing Netlist
Read SDC File
Update Timing Netlist
Delay Models:
Slow 900mV 100C Model
Slow 900mV -40C Model
Fast 900mV 100C Model
Fast 900mV -40C Model
qsta_utility::auto_report_setup
Automatically reporting setup summary. To change this behavior, see Timer Analyzer Settings.
Console
History

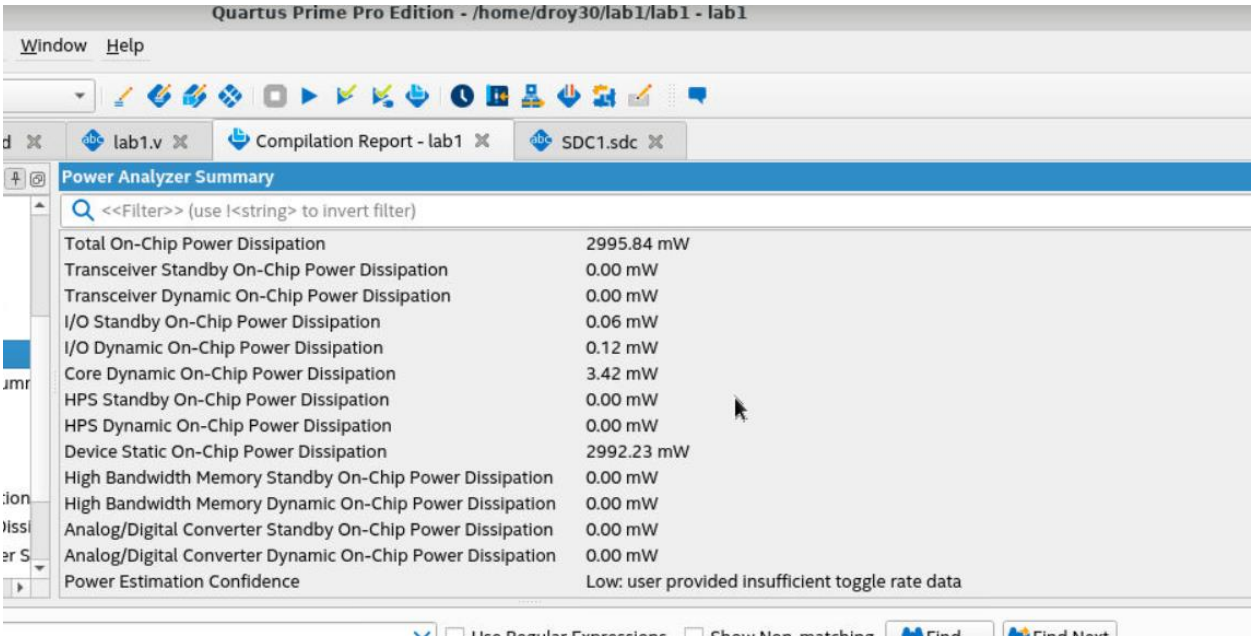

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1
Window Help
lab1.v
Compilation Report - lab1
SDC1.sdc
Fitter Resource Usage Summary
<<Filter>> (use !<string> to invert filter)
Resource Usage %
4 ALMs needed [=A-B+C] 63
1 [A] ALMs used in final placement [=a+b+c+d] 43 / 427,200 < 1 %
1 [a] ALMs used for LUT logic and registers 12
2 [b] ALMs used for LUT logic 24
3 [c] ALMs used for registers 7
4 [d] ALMs used for memor... to half of total ALMs) 0
2 [B] Estimate of ALMs recoverable by dense packing 7 / 427,200 < 1 %
3 [C] Estimate of ALMs unavailable [=a+b+c+d] 27 / 427,200 < 1 %
1 [a] Due to location constrained logic 0
2 [b] Due to LAB-wide signal conflicts 0
3 [c] Due to LAB input limits 0
4 [d] Due to virtual I/Os 27
5
6 Difficulty packing design Low
The Fitter Resource Usage Summary report displays a detailed analysis of logic utilization based on calculations of ALM usage. Refer to Fitter Resource



Here, ALMs used i.e logic utilization is 63 – 27 = 36 ALMs.



The total power for these block types, including the routing between them is 0.78 + 0.17 + 0.03 = 0.98 mW @ 45.45 MHz

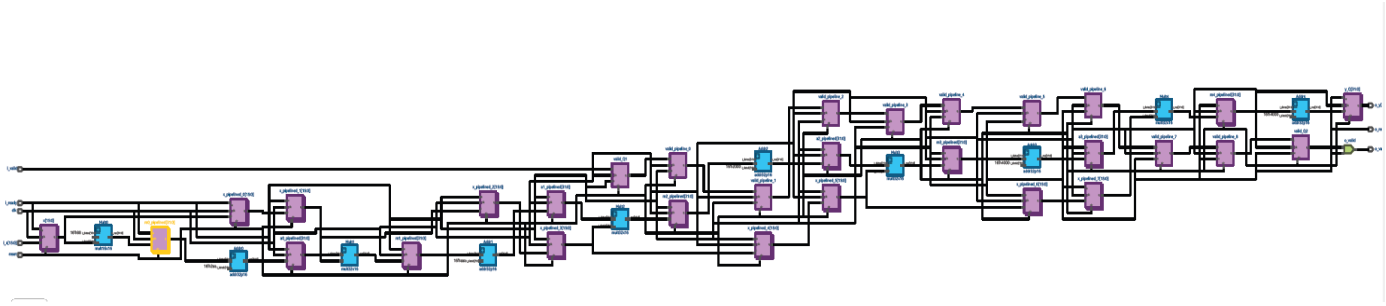


'Total On-Chip Power Dissipation' = 2995mW or about 3W.

'Core Dynamic On-Chip Power Dissipation'= 3.42mW

'Device Static On-Chip Power Dissipation' = 2992.23

PIPELINE IMPLEMENTATION



Basic Operation of Pipeline Implementation:

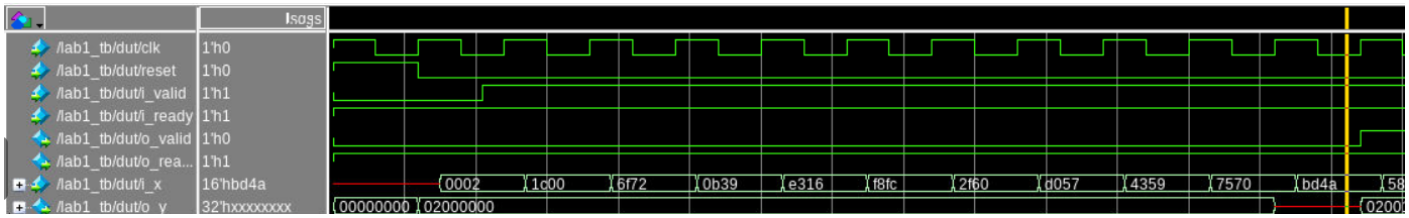


Fig : Basic Operation

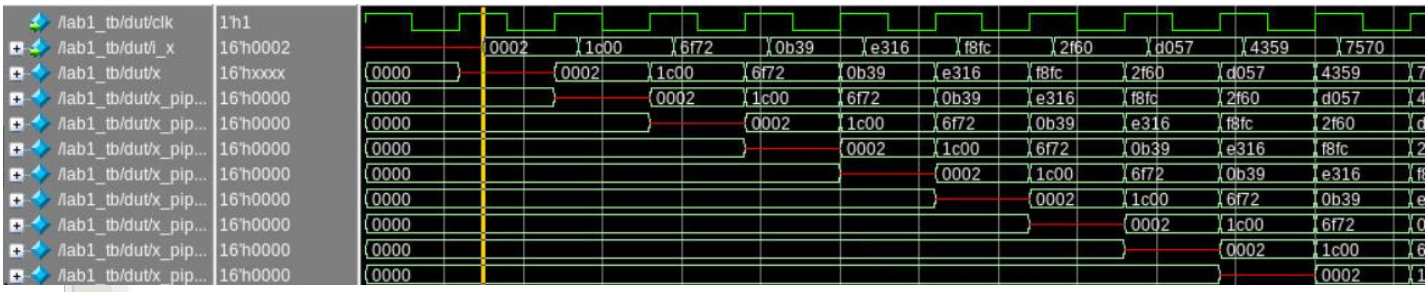


Fig : X pipeline (8 Stages)

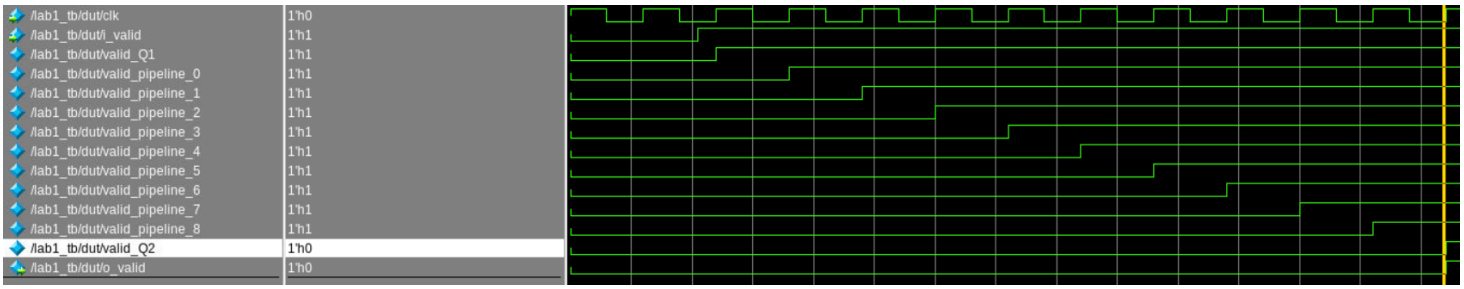


Fig : Valid_pipeline (9 stages : 5 Mult + 4 Adders)

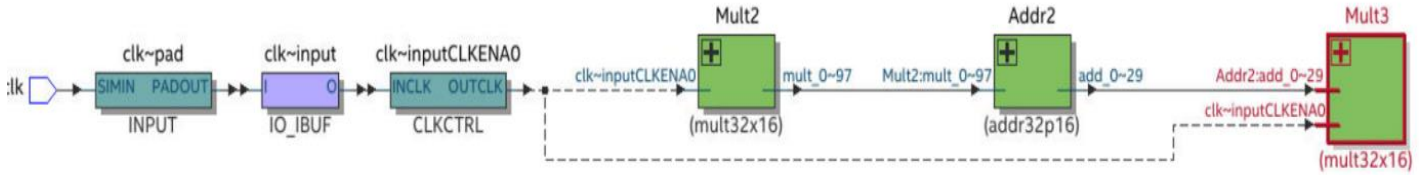
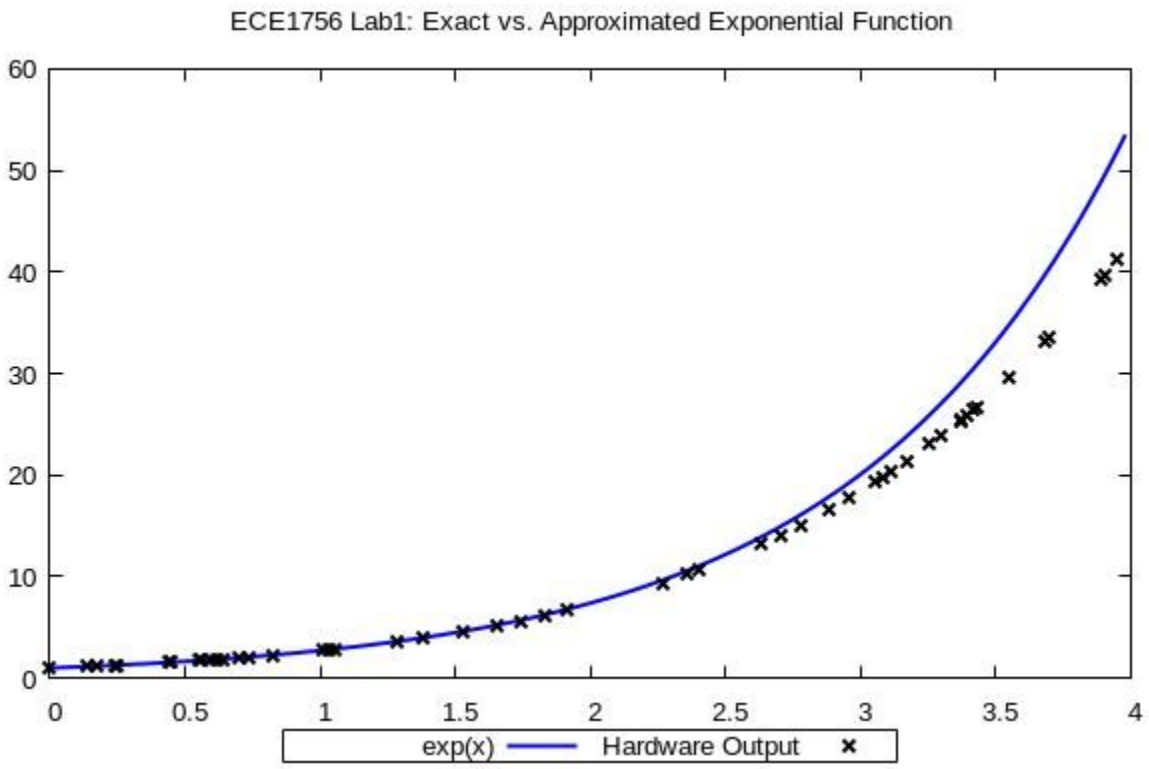


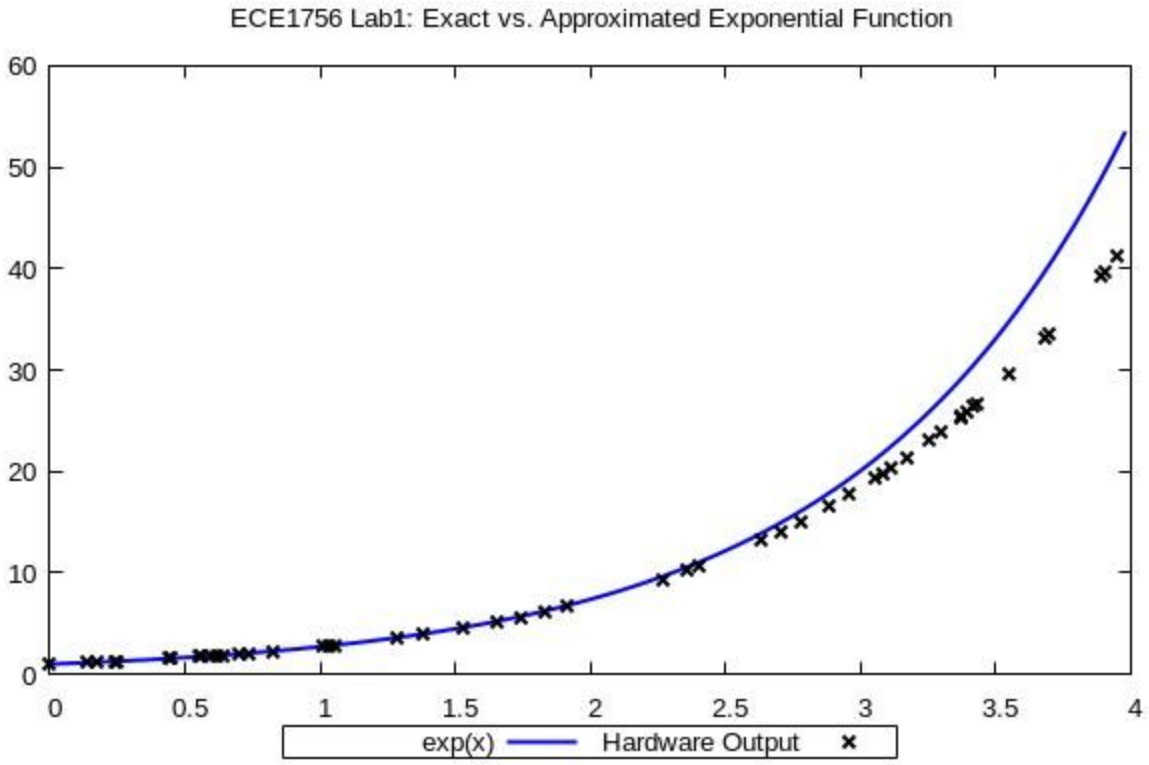
Fig: Critical Path Delay

Explanation:

Baseline error



Pipelined Error



(a) What are the different sources of error (i.e. difference between exp(x) and Hardware Output in the graph you plotted for the testbench output)? Include the graph in the report. What changes could you make to the circuit to reduce this error?

The errors of pipeline and baseline are similar as there are no major changes in the design. The only changes that are taking place are in additions to pipelining stages using flip flops. However, as the shared operator is using mult32 and add32 for all the 5 alu (mult + add) operations, the error rates of the shared operator are higher. [Baseline and pipelining using a 16-bit Multiplier for their first input]. In our case, we have truncated the precision to match the data size between the inputs and outputs. A 32-bit Multiplier will truncate more bits than the 16-bit multiplier, which might lead to higher error rates.

(b) Which of the 3 hardware circuits (baseline, pipelined, and shared) achieves the highest throughput/device? Explain the reasons for the efficiency differences between them.

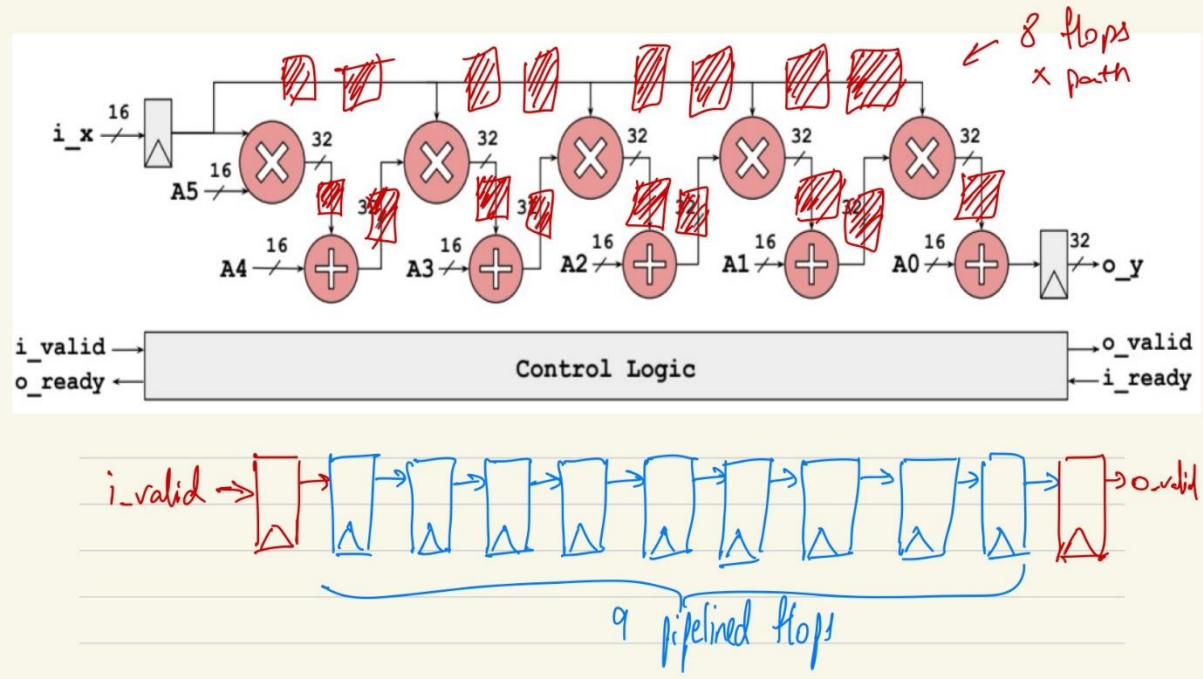
We believe that the pipelined stage gives the highest throughput. At maximum pipelining, there's just one combinational block (adder/multiplier) between two flops, leading in a higher frequency. However, in quartus, we observed that the pipelining added after the adder, was a part of the multiplier DSP input flop, and

the pipelining after the multiplier was not realized. In that case, the frequencies of the pipelined design and the shared operator should be similar. But as a shared operator takes more cycles to produce the output, the throughput is lowered.

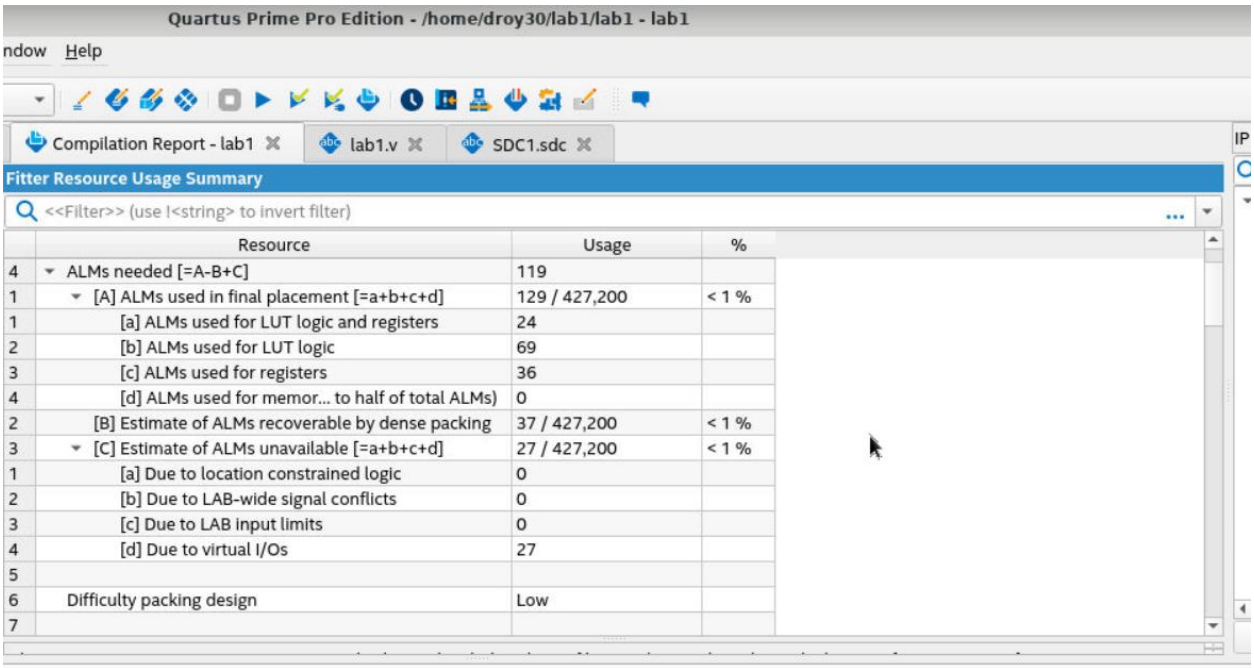
(c) Look at the average toggle rates (how often the average signal changes) for the 3 circuits (this information is in the messages section of the PowerAnalyzer report). Comment on the relative efficiency of the 3 circuits in terms of computations/J and explain why each style is more or less efficient in computations/J than the others.

In a fully pipelined scenario, a total of 26 flops (8 x, 5 multipliers, 4 adders and 9 valid) were added. This leads to more toggling and a higher dynamic power. However, the static power is constant, high, and similar in all 3 cases. Hence, as pipelined has a higher throughput, it has the best efficiency.

Pipelined design:

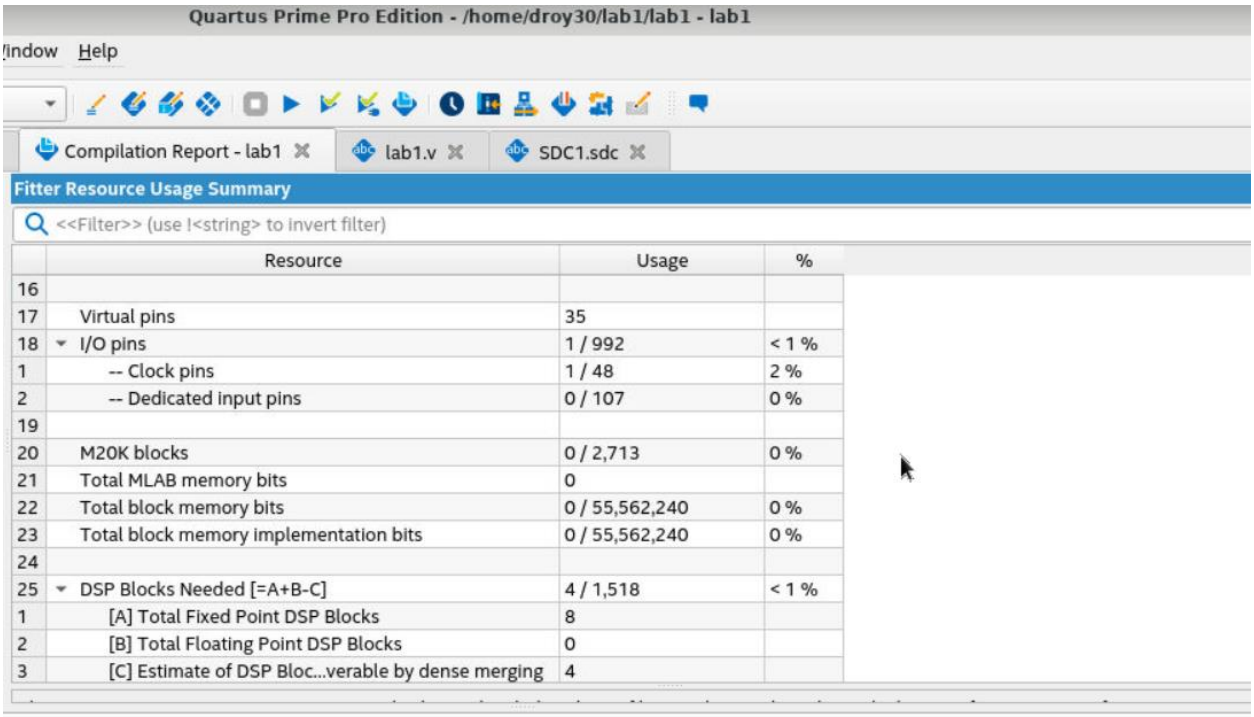


1. Adding flops after each intermediate multiplier / adder. Hence each intermediate multiplier needs to have x pushed behind by two cycles. We've added 2 flops per multiplier on the x path.
2. The first output is valid after 11 cycles of the i_x being sent. (2 flops for i_x and o_y and 9 flops to match the multiplier + adder pipelined flops)



	Resource	Usage	%
4	ALMs needed [=A-B+C]	119	
1	[A] ALMs used in final placement [=a+b+c+d]	129 / 427,200	< 1 %
1	[a] ALMs used for LUT logic and registers	24	
2	[b] ALMs used for LUT logic	69	
3	[c] ALMs used for registers	36	
4	[d] ALMs used for memor... to half of total ALMs)	0	
2	[B] Estimate of ALMs recoverable by dense packing	37 / 427,200	< 1 %
3	[C] Estimate of ALMs unavailable [=a+b+c+d]	27 / 427,200	< 1 %
1	[a] Due to location constrained logic	0	
2	[b] Due to LAB-wide signal conflicts	0	
3	[c] Due to LAB input limits	0	
4	[d] Due to virtual I/Os	27	
5			
6	Difficulty packing design	Low	
7			

Fig: Resource Utilization for Pipeline



	Resource	Usage	%
16			
17	Virtual pins	35	
18	I/O pins	1 / 992	< 1 %
1	-- Clock pins	1 / 48	2 %
2	-- Dedicated input pins	0 / 107	0 %
19			
20	M20K blocks	0 / 2,713	0 %
21	Total MLAB memory bits	0	
22	Total block memory bits	0 / 55,562,240	0 %
23	Total block memory implementation bits	0 / 55,562,240	0 %
24			
25	DSP Blocks Needed [=A+B-C]	4 / 1,518	< 1 %
1	[A] Total Fixed Point DSP Blocks	8	
2	[B] Total Floating Point DSP Blocks	0	
3	[C] Estimate of DSP Bloc...verable by dense merging	4	

Fig : DSP Blocks utilization in Resource Utilization

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

Window Help

Compilation Report - lab1 | lab1.v | SDC1.sdc

Fitter Resource Utilization by Entity

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	Compilation Hierarchy Node	ALMs needed [=A-B+C]	[A] ALMs used in final placement	[B] Estimate of ALMs recoverable by dense packing
1	|	118.5 (38.2)	127.5 (47.7)	35.5 (36.0)
1	|Addr0|	5.0 (5.0)	5.0 (5.0)	0.0 (0.0)
2	|Addr1|	10.0 (10.0)	10.0 (10.0)	0.0 (0.0)
3	|Addr2|	4.0 (4.0)	4.0 (4.0)	0.0 (0.0)
4	|Addr3|	4.0 (4.0)	4.0 (4.0)	0.0 (0.0)
5	|Addr4|	2.2 (2.2)	2.2 (2.2)	0.0 (0.0)
6	|Mult0|	4.5 (4.5)	4.5 (4.5)	0.0 (0.0)
7	|Mult1|	14.0 (14.0)	14.0 (14.0)	0.0 (0.0)
8	|Mult2|	13.7 (13.7)	13.7 (13.7)	0.0 (0.0)
9	|Mult3|	14.0 (14.0)	14.0 (14.0)	0.0 (0.0)
10	|Mult4|	8.5 (8.5)	8.5 (8.5)	0.0 (0.0)

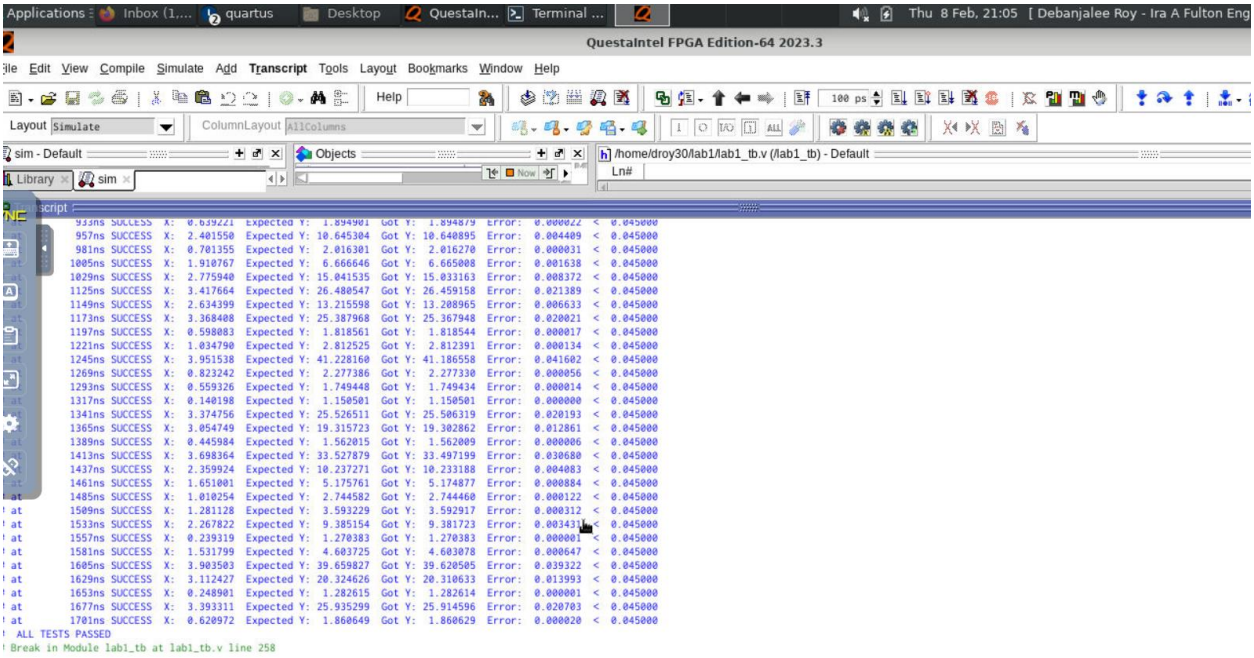
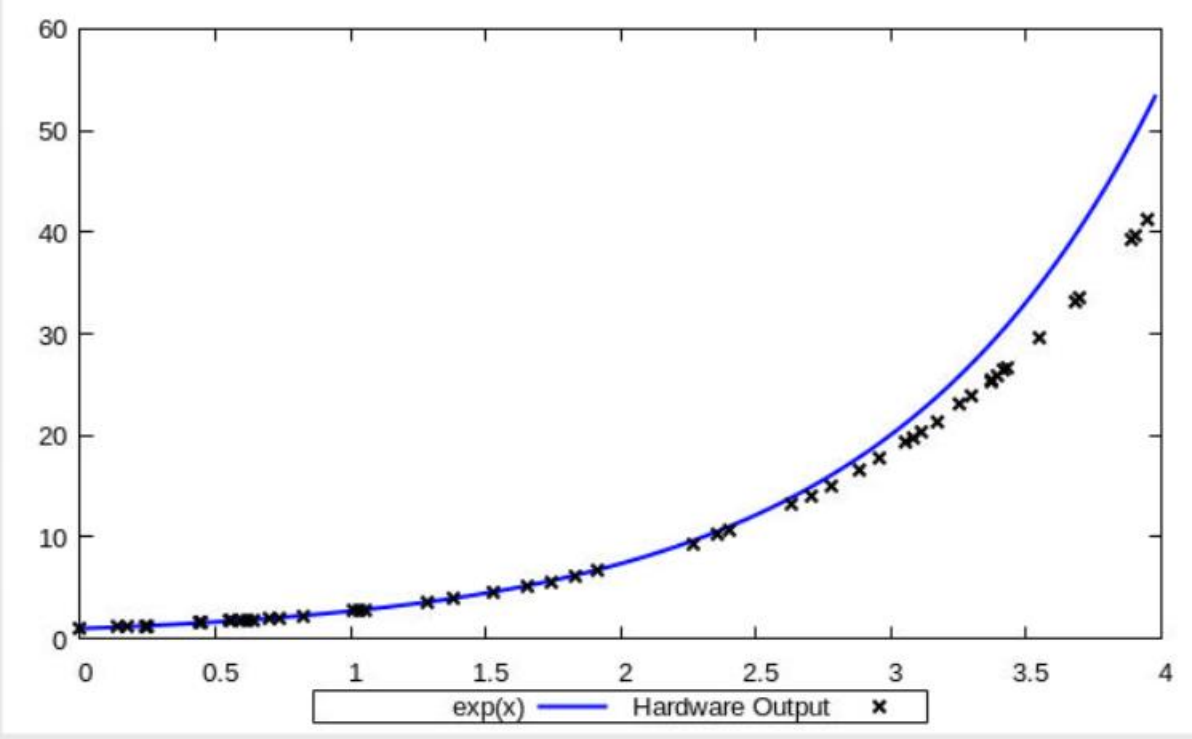
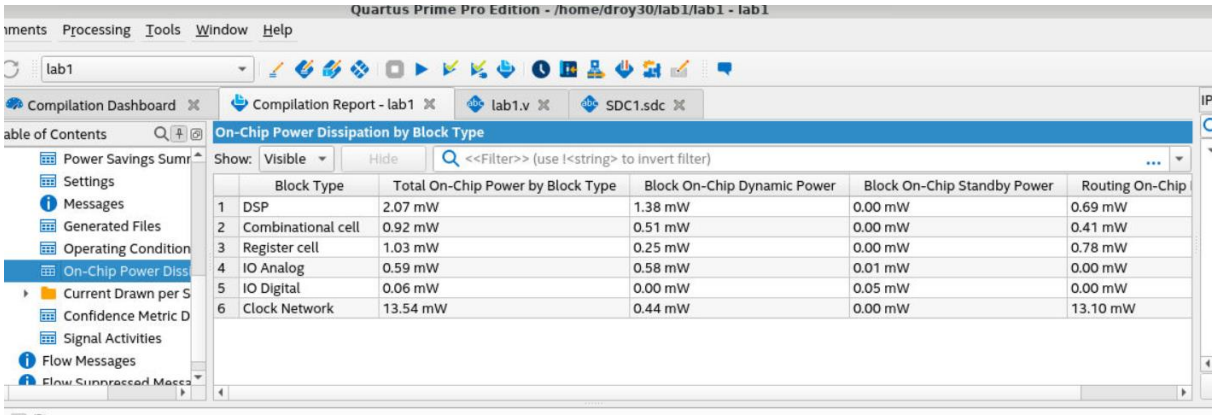


Fig: Questa Testbench Results: Pipeline





	Block Type	Total On-Chip Power by Block Type	Block On-Chip Dynamic Power	Block On-Chip Standby Power	Routing On-Chip
1	DSP	2.07 mW	1.38 mW	0.00 mW	0.69 mW
2	Combinational cell	0.92 mW	0.51 mW	0.00 mW	0.41 mW
3	Register cell	1.03 mW	0.25 mW	0.00 mW	0.78 mW
4	IO Analog	0.59 mW	0.58 mW	0.01 mW	0.00 mW
5	IO Digital	0.06 mW	0.00 mW	0.05 mW	0.00 mW
6	Clock Network	13.54 mW	0.44 mW	0.00 mW	13.10 mW

Fig: On-chip Power Dissipation by block type

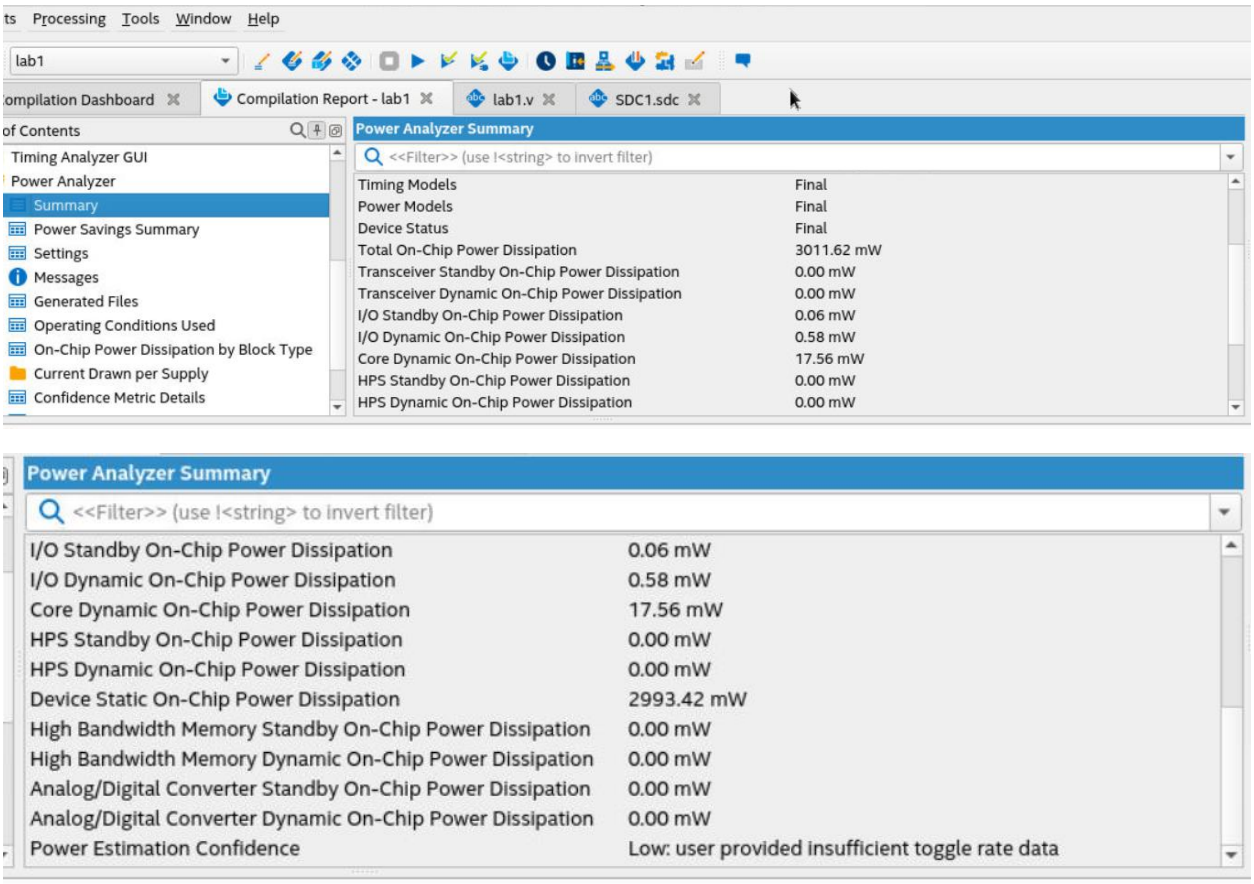


Fig: Power Analyzer Summary

Pipeline Implementation Tasks:

1. Resources for one circuit = Here, ALMs used i.e logic utilization is **119 – 27 = 92 ALMs.**

Max. # of copies/device is restricted by the number of DSPs needed = 1518 DSPs/6 DSPs = 253 copies per device.

2. Operating frequency: Time in SDC1.sdc is set to 4.65ns corresponding to 215.05 MHz.

3. Critical path:

4. Cycles per valid output: In the pipeline, after saturation is 1 cycle per valid output.

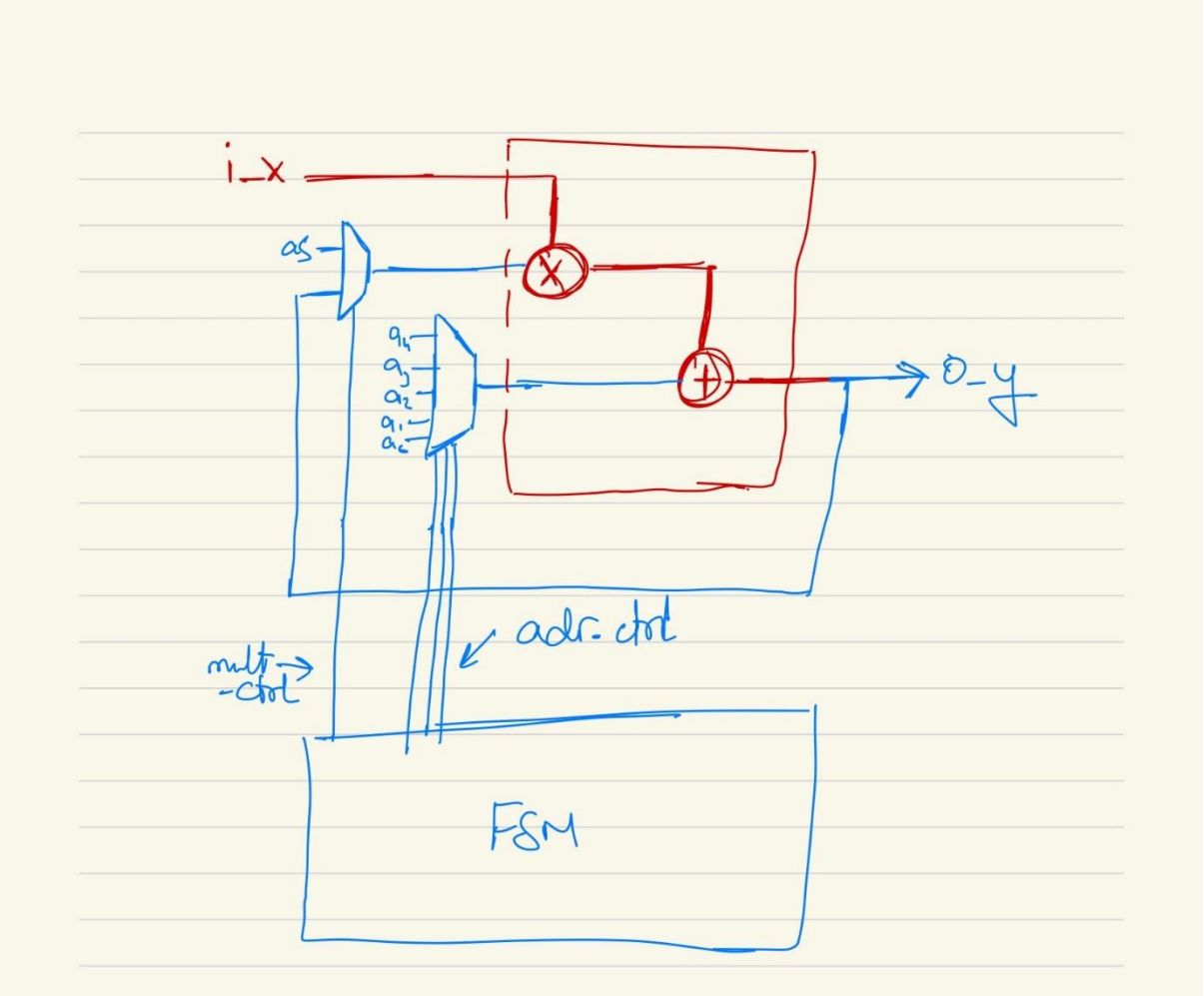
5. Max. Throughput for a full device (computations/s): 215.05 *10^6 * 380 = 81.7 *10^9 computations/s

6. Dynamic power of one circuit: 2.07+0.92+1.03 mW = 4.02mW

7. Max. throughput/Watt for a full device: power consumed = 4.02mW * 380 + 2993.42 = 4521.02mW

Therefore, throughput/ Watt = 81.7 *10^9 /4521.02 * 10^(-3) W = 18*10^9 computations/watt

Shared Operator



Frequency: 1 GHz

No of cycles: 5

<u>Shared Implementation Tasks:</u>

1. Resources for one circuit = Here, ALMs used i.e. logic utilization **= 30 ALMs.**

Max. # of copies/device is restricted by the number of DSPs needed = 1518 /1 = 1518 copies per device.

2. Operating frequency: Time in SDC1.sdc is set to 1 ns corresponding to 1GHz.

3. Critical path:

4. Cycles per valid output: In the shared, 5 cycles per valid output are designed.

5. Max. Throughput for a full device (computations/s): 215.05 *10^6 * 380 = 81.7 *10^9 computations/s

6. Dynamic power of one circuit: 2.07+0.92+1.03 mW = 4.02mW

7. Max. throughput/Watt for a full device: power consumed = 4.02mW * 1518 + 2993.42 = 4521.02mW

Therefore, throughput/ Watt = 81.7 *10^9 /4521.02 * 10^(-3) W = 18*10^9 computations/watt