

## REPORT LAB-1

**Submitted by Deepesh Sahoo(ASU ID: 1230089330) and Debanjalee Roy (ASU ID: 1225660787)**

Table 1: Implementation results for the 3 different implementations of the studied circuit.

	<b>Baseline Circuit</b>	<b>Pipelined Circuit</b>	<b>Shared HW Circuit</b>
<b>Resources for one circuit</b>	36 ALMs + 6 DSPs	92 ALMs + 4 DSPs	30 ALMs + 1 DSPs
<b>Operating frequency</b>	45.45 MHz	215.05 MHz	1GHz
<b>Critical path</b>	ALM-based multiplier and adder + 2x DSP mult + ALM-based adder + 6x DSP mult + ALM-based adder	mult2+addr2+mult3+ addr2_pipelined	Getting Error
<b>Cycles per valid output</b>	1	1	5
<b>Max. # of copies/device</b>	1518 DSPs/6 DSPs = 253 copies per device	1518 DSPs /4 DSPs = 380	1518 DSPs/1 DSP =1518 copies/device
<b>Max. Throughput for a full device (computations/s)</b>	$45.45 * 10^6 * 253 = 11.5 * 10^9$ computations/s	$215.05 * 10^6 * 380 = 81.7 * 10^9$ computations/s	$1\text{GHz} * 1518$ computations/s
<b>Dynamic power of one circuit</b>	0.98 mW	4.02mW	Getting vcd error, unable to change settings.
<b>Max. throughput/Watt for a full device</b>	$3.55 * 10^9$ computations/watt	$18 * 10^9$ computations/watt	Getting vcd error, unable to change settings.

### **Baseline Implementation:**

At frequency 45.45MHz (22ns)

**Dynamic power of one circuit:** 0.98 mW from the picture provided below at frequency of 45.45 MHz

**Max. throughput/Watt for a full device:** Power used =  $0.98 * 253 + 2992.23 = 3240.17$  mW

Therefore, max throughput/watt =  $11.5 * 10^9 / 3240.17 * 10^{-3} = 3.55 * 10^9$  computations/watt

Timing Analyzer - /home/droy30/lab1/lab1 - lab1

File View Netlist Constraints Reports Script Tools Window Help

Search

Set Operating Conditions

Snapshot: final

- ✓ Slow 900mV 100C Model
- ✓ Slow 900mV -40C Model
- ✓ Fast 900mV 100C Model
- ✓ Fast 900mV -40C Model

Report

- Timing Delays: Final Snapshot
- Advanced I/O Timing
- SDC File List
- Setup Summary

Tasks

- ✓ Open Project...
- Netlist Setup
- ✓ Create Timing Netlist
- ✓ Read SDC File
- ✓ Update Timing Netlist

Delay Models:

- Slow 900mV 100C Model
- Slow 900mV -40C Model
- Fast 900mV 100C Model
- Fast 900mV -40C Model

	Clock	Slack	End Point TNS	Failing End Points	Worst-Case Operating Conditions
1	clk	0.568	0.000	0	Slow 900mV -40C Model

qsta\_utility::auto\_report\_setup

Automatically reporting setup summary. To change this behavior, see Timer Analyzer Settings.

Console History

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

Window Help

lab1.v Compilation Report - lab1 SDC1.sdc

Fitter Resource Usage Summary

Search <<Filter>> (use !<string> to invert filter)

	Resource	Usage	%
4	ALMs needed [=A-B+C]	63	
1	[A] ALMs used in final placement [=a+b+c+d]	43 / 427,200	< 1 %
1	[a] ALMs used for LUT logic and registers	12	
2	[b] ALMs used for LUT logic	24	
3	[c] ALMs used for registers	7	
4	[d] ALMs used for memor... to half of total ALMs)	0	
2	[B] Estimate of ALMs recoverable by dense packing	7 / 427,200	< 1 %
3	[C] Estimate of ALMs unavailable [=a+b+c+d]	27 / 427,200	< 1 %
1	[a] Due to location constrained logic	0	
2	[b] Due to LAB-wide signal conflicts	0	
3	[c] Due to LAB input limits	0	
4	[d] Due to virtual I/Os	27	
5			
6	Difficulty packing design	Low	

The Fitter Resource Usage Summary report displays a detailed analysis of logic utilization based on calculations of ALM usage. Refer to [Fitter Resource](#)

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

File Window Help

lab1.v Compilation Report - lab1 SDC1.sdc

### Fitter Resource Usage Summary

Search: <<Filter>> (use !<string> to invert filter)

Resource	Usage	%
20 M20K blocks	0 / 2,713	0 %
21 Total MLAB memory bits	0	
22 Total block memory bits	0 / 55,562,240	0 %
23 Total block memory implementation bits	0 / 55,562,240	0 %
24		
25 DSP Blocks Needed [=A+B-C]	6 / 1,518	< 1 %
1 [A] Total Fixed Point DSP Blocks	8	
2 [B] Total Floating Point DSP Blocks	0	
3 [C] Estimate of DSP Block...verable by dense merging	2	
26		
27 IOPLLs	0 / 16	0 %
28 FPLLs	0 / 32	0 %
29 Global signals	0	
1 -- Global clocks	0 / 32	0 %

The Fitter Resource Usage Summary report displays a detailed analysis of logic utilization based on calculations of ALM usage. Refer to [Fitter Resource](#)

Here, ALMs used i.e logic utilization is  $63 - 27 = 36$  ALMs.

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

Tools Window Help

lab1.v Compilation Report - lab1 SDC1.sdc

### On-Chip Power Dissipation by Block Type

Show: Visible Hide Search: <<Filter>> (use !<string> to invert filter)

Block Type	Total On-Chip Power by Block Type	Block On-Chip Dynamic Power	Block On-Chip Standby Power	Routing On-Chip
1 DSP	0.78 mW	0.64 mW	0.00 mW	0.14 mW
2 Combinational cell	0.17 mW	0.04 mW	0.00 mW	0.13 mW
3 Register cell	0.03 mW	0.01 mW	0.00 mW	0.01 mW
4 IO Analog	0.13 mW	0.12 mW	0.01 mW	0.00 mW
5 IO Digital	0.05 mW	0.00 mW	0.05 mW	0.00 mW
6 Clock Network	2.45 mW	0.03 mW	0.00 mW	2.42 mW

The total power for these block types, including the routing between them is  $0.78 + 0.17 + 0.03 = 0.98$  mW @ 45.45 MHz

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

Window Help

lab1.v x Compilation Report - lab1 x SDC1.sdc x

### Power Analyzer Summary

Q <<Filter>> (use !<string> to invert filter)

Total On-Chip Power Dissipation	2995.84 mW
Transceiver Standby On-Chip Power Dissipation	0.00 mW
Transceiver Dynamic On-Chip Power Dissipation	0.00 mW
I/O Standby On-Chip Power Dissipation	0.06 mW
I/O Dynamic On-Chip Power Dissipation	0.12 mW
Core Dynamic On-Chip Power Dissipation	3.42 mW
HPS Standby On-Chip Power Dissipation	0.00 mW
HPS Dynamic On-Chip Power Dissipation	0.00 mW
Device Static On-Chip Power Dissipation	2992.23 mW
High Bandwidth Memory Standby On-Chip Power Dissipation	0.00 mW
High Bandwidth Memory Dynamic On-Chip Power Dissipation	0.00 mW
Analog/Digital Converter Standby On-Chip Power Dissipation	0.00 mW
Analog/Digital Converter Dynamic On-Chip Power Dissipation	0.00 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

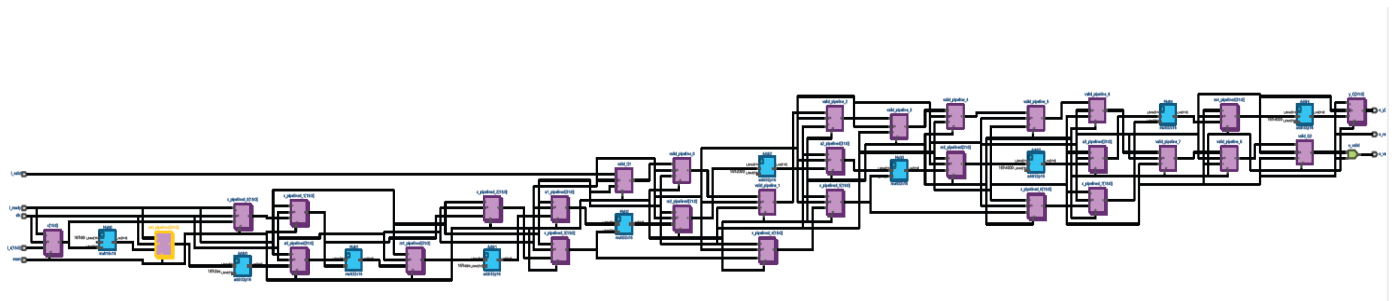
Use Reader Suppression Show Non-estimates Find Find Next

**'Total On-Chip Power Dissipation' = 2995mW or about 3W.**

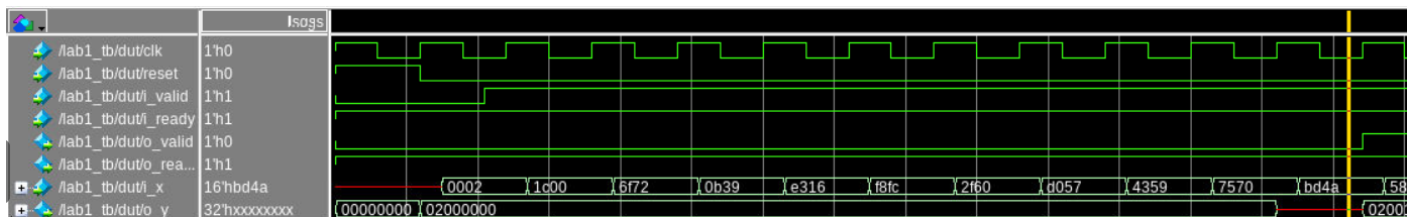
**'Core Dynamic On-Chip Power Dissipation' = 3.42mW**

**'Device Static On-Chip Power Dissipation' = 2992.23**

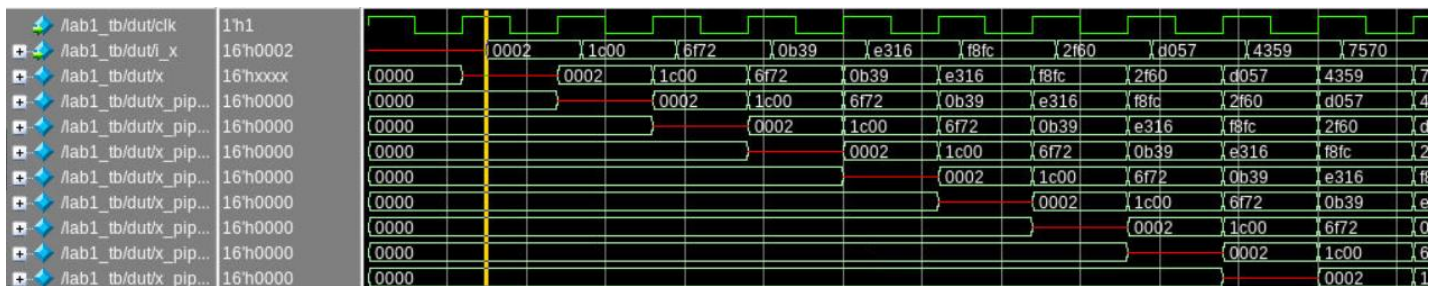
## PIPELINE IMPLEMENTATION



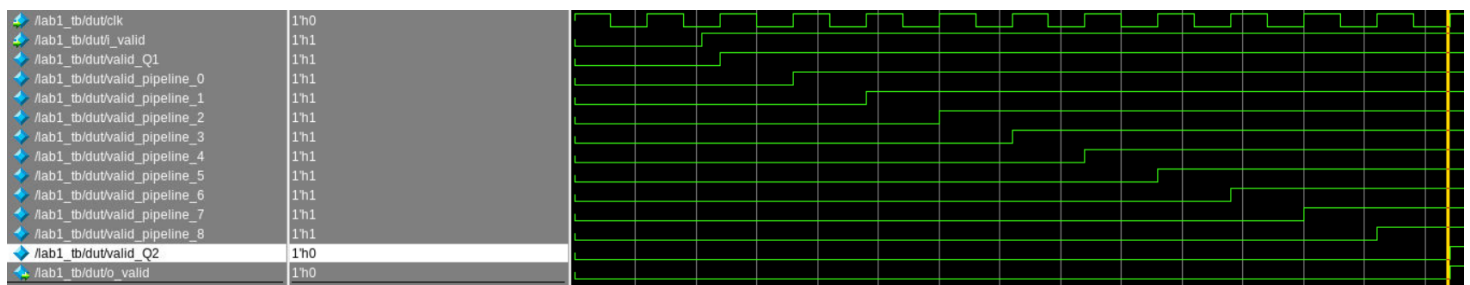
### Basic Operation of Pipeline Implementation:



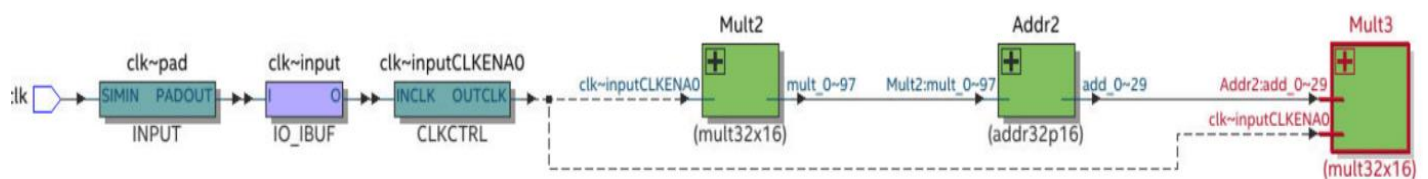
### Fig : Basic Operation



**Fig : X pipeline ( 8 Stages )**



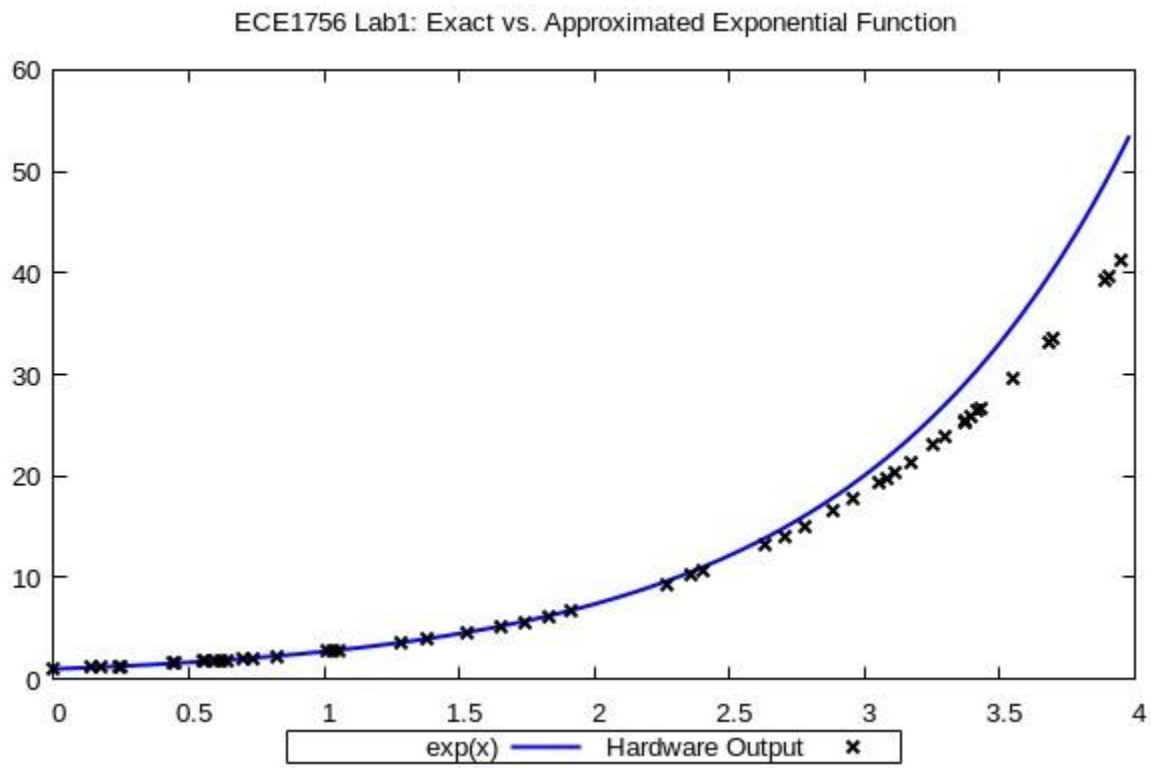
**Fig : Valid\_pipeline (9 stages : 5 Mult + 4 Adders)**



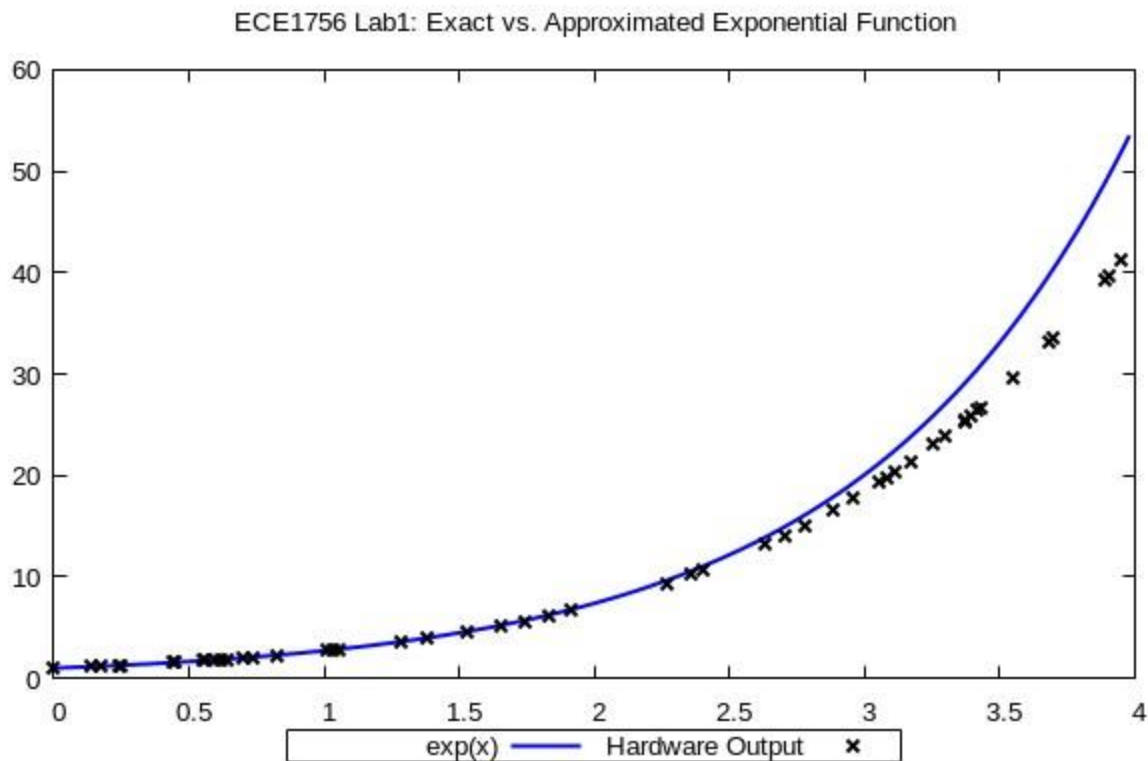
**Fig: Critical Path Delay**

**Explanation:**

## Baseline error



## Pipelined Error



**(a) What are the different sources of error (i.e. difference between  $\exp(x)$  and Hardware Output in the graph you plotted for the testbench output)? Include the graph in the report. What changes could you make to the circuit to reduce this error?**

The errors of pipeline and baseline are similar as there are no major changes in the design. The only changes that are taking place are in additions to pipelining stages using flip flops. However, as the shared operator is using mult32 and add32 for all the 5 alu (mult + add) operations, the error rates of the shared operator are higher. [Baseline and pipelining using a 16-bit Multiplier for their first input]. In our case, we have truncated the precision to match the data size between the inputs and outputs. A 32-bit Multiplier will truncate more bits than the 16-bit multiplier, which might lead to higher error rates.

**(b) Which of the 3 hardware circuits (baseline, pipelined, and shared) achieves the highest throughput/device? Explain the reasons for the efficiency differences between them.**

We believe that the pipelined stage gives the highest throughput. At maximum pipelining, there's just one combinational block (adder/multiplier) between two flops, leading in a higher frequency. However, in quartus, we observed that the pipelining added after the adder, was a part of the multiplier DSP input flop, and

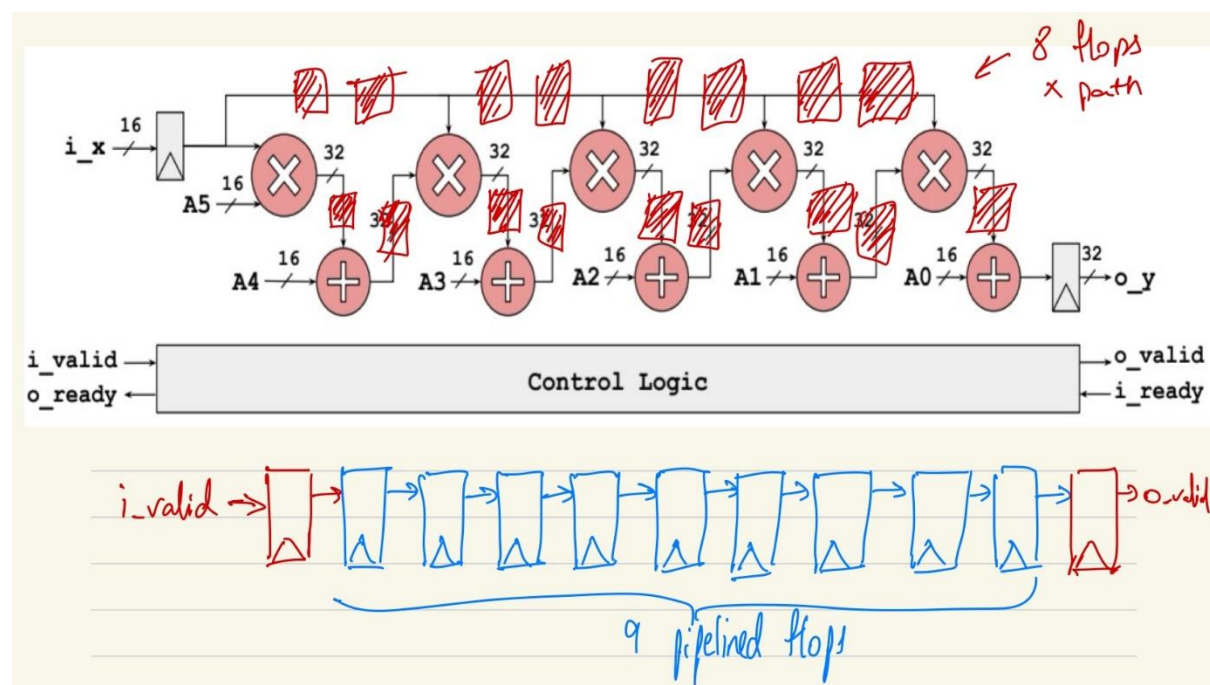


the pipelining after the multiplier was not realized. In that case, the frequencies of the pipelined design and the shared operator should be similar. But as a shared operator takes more cycles to produce the output, the throughput is lowered.

(c) Look at the average toggle rates (how often the average signal changes) for the 3 circuits (this information is in the messages section of the PowerAnalyzer report). Comment on the relative efficiency of the 3 circuits in terms of computations/J and explain why each style is more or less efficient in computations/J than the others.

In a fully pipelined scenario, a total of 26 flops (8 x, 5 multipliers, 4 adders and 9 valid) were added. This leads to more toggling and a higher dynamic power. However, the static power is constant, high, and similar in all 3 cases. Hence, as pipelined has a higher throughput, it has the best efficiency.

### Pipelined design:



1. Adding flops after each intermediate multiplier / adder. Hence each intermediate multiplier needs to have  $x$  pushed behind by two cycles. We've added 2 flops per multiplier on the  $x$  path.
2. The first output is valid after 11 cycles of the  $i_x$  being sent. (2 flops for  $i_x$  and  $o_y$  and 9 flops to match the multiplier + adder pipelined flops)



Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

ndow Help

Compilation Report - lab1 lab1.v SDC1.sdc

**Fitter Resource Usage Summary**

Q <<Filter>> (use !<string> to invert filter)

	Resource	Usage	%
4	ALMs needed [=A-B+C]	119	
1	[A] ALMs used in final placement [=a+b+c+d]	129 / 427,200	< 1 %
1	[a] ALMs used for LUT logic and registers	24	
2	[b] ALMs used for LUT logic	69	
3	[c] ALMs used for registers	36	
4	[d] ALMs used for memor... to half of total ALMs)	0	
2	[B] Estimate of ALMs recoverable by dense packing	37 / 427,200	< 1 %
3	[C] Estimate of ALMs unavailable [=a+b+c+d]	27 / 427,200	< 1 %
1	[a] Due to location constrained logic	0	
2	[b] Due to LAB-wide signal conflicts	0	
3	[c] Due to LAB input limits	0	
4	[d] Due to virtual I/Os	27	
5			
6	Difficulty packing design	Low	
7			

Fig: Resource Utilization for Pipeline

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

ndow Help

Compilation Report - lab1 lab1.v SDC1.sdc

**Fitter Resource Usage Summary**

Q <<Filter>> (use !<string> to invert filter)

	Resource	Usage	%
16			
17	Virtual pins	35	
18	I/O pins	1 / 992	< 1 %
1	-- Clock pins	1 / 48	2 %
2	-- Dedicated input pins	0 / 107	0 %
19			
20	M20K blocks	0 / 2,713	0 %
21	Total MLAB memory bits	0	
22	Total block memory bits	0 / 55,562,240	0 %
23	Total block memory implementation bits	0 / 55,562,240	0 %
24			
25	DSP Blocks Needed [=A+B-C]	4 / 1,518	< 1 %
1	[A] Total Fixed Point DSP Blocks	8	
2	[B] Total Floating Point DSP Blocks	0	
3	[C] Estimate of DSP Bloc...verable by dense merging	4	

Fig : DSP Blocks utilization in Resource Utilization

Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

Window Help

Compilation Report - lab1 lab1.v SDC1.sdc

Filter Resource Utilization by Entity

<<Filter>> (use !<string> to invert filter)

Compilation Hierarchy Node	ALMs needed [=A-B+C]	[A] ALMs used in final placement	[B] Estimate of ALMs recoverable by dense packing
1	118.5 (38.2)	127.5 (47.7)	35.5 (36.0)
1   [Addr0]	5.0 (5.0)	5.0 (5.0)	0.0 (0.0)
2   [Addr1]	10.0 (10.0)	10.0 (10.0)	0.0 (0.0)
3   [Addr2]	4.0 (4.0)	4.0 (4.0)	0.0 (0.0)
4   [Addr3]	4.0 (4.0)	4.0 (4.0)	0.0 (0.0)
5   [Addr4]	2.2 (2.2)	2.2 (2.2)	0.0 (0.0)
6   [Mult0]	4.5 (4.5)	4.5 (4.5)	0.0 (0.0)
7   [Mult1]	14.0 (14.0)	14.0 (14.0)	0.0 (0.0)
8   [Mult2]	13.7 (13.7)	13.7 (13.7)	0.0 (0.0)
9   [Mult3]	14.0 (14.0)	14.0 (14.0)	0.0 (0.0)
10   [Mult4]	8.5 (8.5)	8.5 (8.5)	0.0 (0.0)

Applications: Inbox (1... quartus Desktop Questal... Terminal ... Thu 8 Feb, 21:05 [Debanjalee Roy - Ira A Fulton Eng]

Questalntel FPGA Edition-64 2023.3

File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help

Layout [Simulate] ColumnLayout AllColumns

sim - Default Objects h:/home/droy30/lab1/lab1\_tb.v (lab1\_tb) - Default

Library sim

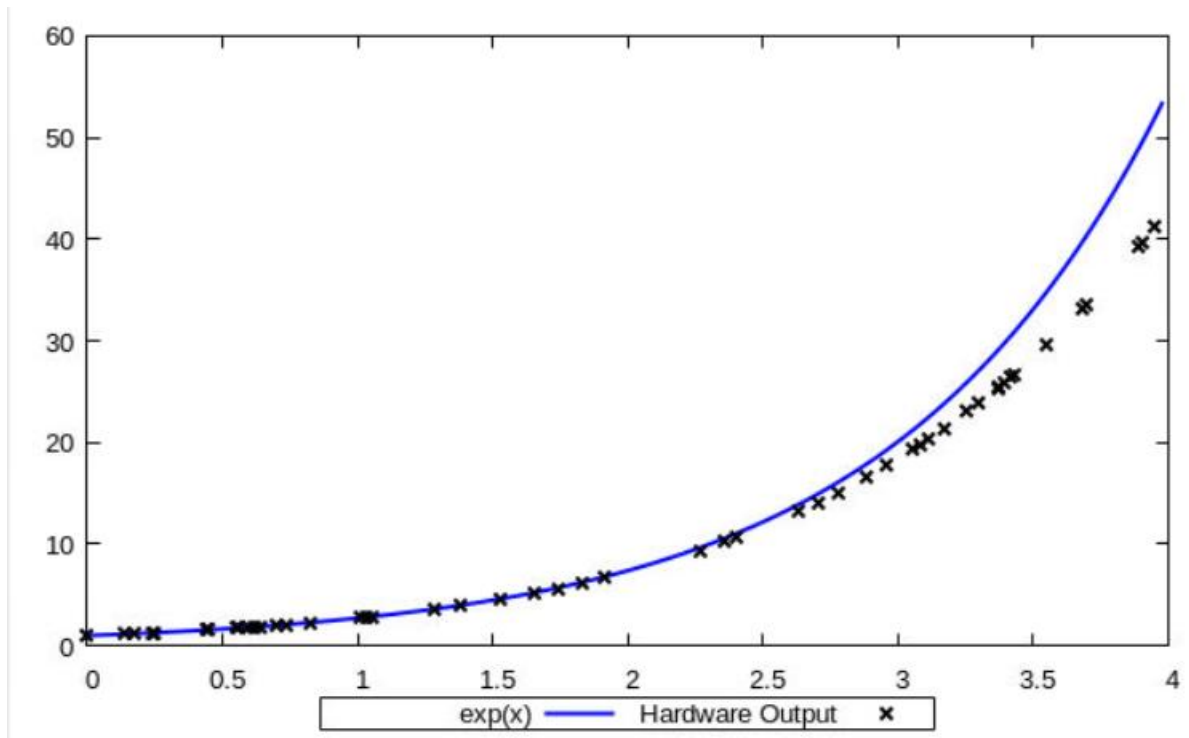
script

933ns	SUCCESS	X: 0.639421	Expected Y: 1.894901	Got Y: 1.894879	Error: 0.000022	< 0.045000
957ns	SUCCESS	X: 2.401550	Expected Y: 10.645304	Got Y: 10.640895	Error: 0.004409	< 0.045000
981ns	SUCCESS	X: 0.701355	Expected Y: 2.016301	Got Y: 2.016270	Error: 0.000031	< 0.045000
1005ns	SUCCESS	X: 1.910767	Expected Y: 6.666646	Got Y: 6.665008	Error: 0.001638	< 0.045000
1029ns	SUCCESS	X: 2.775940	Expected Y: 15.041535	Got Y: 15.033163	Error: 0.008372	< 0.045000
1125ns	SUCCESS	X: 3.417664	Expected Y: 26.480547	Got Y: 26.459158	Error: 0.021389	< 0.045000
1149ns	SUCCESS	X: 2.634399	Expected Y: 13.215598	Got Y: 13.208965	Error: 0.006633	< 0.045000
1173ns	SUCCESS	X: 3.368408	Expected Y: 25.387968	Got Y: 25.367948	Error: 0.020021	< 0.045000
1197ns	SUCCESS	X: 0.598083	Expected Y: 1.818561	Got Y: 1.818544	Error: 0.000017	< 0.045000
1221ns	SUCCESS	X: 1.034790	Expected Y: 2.812525	Got Y: 2.812391	Error: 0.000134	< 0.045000
1245ns	SUCCESS	X: 3.951538	Expected Y: 41.228160	Got Y: 41.186558	Error: 0.041602	< 0.045000
1269ns	SUCCESS	X: 0.823242	Expected Y: 2.277386	Got Y: 2.277330	Error: 0.000056	< 0.045000
1293ns	SUCCESS	X: 0.559326	Expected Y: 1.749448	Got Y: 1.749434	Error: 0.000014	< 0.045000
1317ns	SUCCESS	X: 0.140198	Expected Y: 1.150501	Got Y: 1.150501	Error: 0.000000	< 0.045000
1341ns	SUCCESS	X: 3.374756	Expected Y: 25.526511	Got Y: 25.506319	Error: 0.020193	< 0.045000
1365ns	SUCCESS	X: 3.054749	Expected Y: 19.315723	Got Y: 19.302862	Error: 0.012861	< 0.045000
1389ns	SUCCESS	X: 0.445984	Expected Y: 1.562015	Got Y: 1.562009	Error: 0.000006	< 0.045000
1413ns	SUCCESS	X: 3.698364	Expected Y: 33.527879	Got Y: 33.497199	Error: 0.030680	< 0.045000
1437ns	SUCCESS	X: 2.359924	Expected Y: 10.237271	Got Y: 10.233188	Error: 0.004083	< 0.045000
1461ns	SUCCESS	X: 1.051001	Expected Y: 5.175761	Got Y: 5.174877	Error: 0.000884	< 0.045000
1485ns	SUCCESS	X: 1.010254	Expected Y: 2.744582	Got Y: 2.744460	Error: 0.000122	< 0.045000
1509ns	SUCCESS	X: 1.281128	Expected Y: 3.593229	Got Y: 3.592917	Error: 0.000312	< 0.045000
1533ns	SUCCESS	X: 2.267822	Expected Y: 9.385154	Got Y: 9.381723	Error: 0.003431	< 0.045000
1557ns	SUCCESS	X: 0.239319	Expected Y: 1.270383	Got Y: 1.270383	Error: 0.000001	< 0.045000
1581ns	SUCCESS	X: 1.531799	Expected Y: 4.603725	Got Y: 4.603078	Error: 0.000647	< 0.045000
1605ns	SUCCESS	X: 3.901503	Expected Y: 39.659827	Got Y: 39.620505	Error: 0.039322	< 0.045000
1629ns	SUCCESS	X: 3.112427	Expected Y: 20.324626	Got Y: 20.310633	Error: 0.013993	< 0.045000
1653ns	SUCCESS	X: 0.248901	Expected Y: 1.282615	Got Y: 1.282614	Error: 0.000001	< 0.045000
1677ns	SUCCESS	X: 3.393311	Expected Y: 25.935299	Got Y: 25.914596	Error: 0.020703	< 0.045000
1701ns	SUCCESS	X: 0.620972	Expected Y: 1.860649	Got Y: 1.860629	Error: 0.000020	< 0.045000

ALL TESTS PASSED

Break in Module lab1\_tb at lab1\_tb.v line 258

Fig: Questa Testbench Results: Pipeline



Quartus Prime Pro Edition - /home/droy30/lab1/lab1 - lab1

ments Processing Tools Window Help

lab1

Compilation Dashboard Compilation Report - lab1 lab1.v SDC1.sdc

Table of Contents

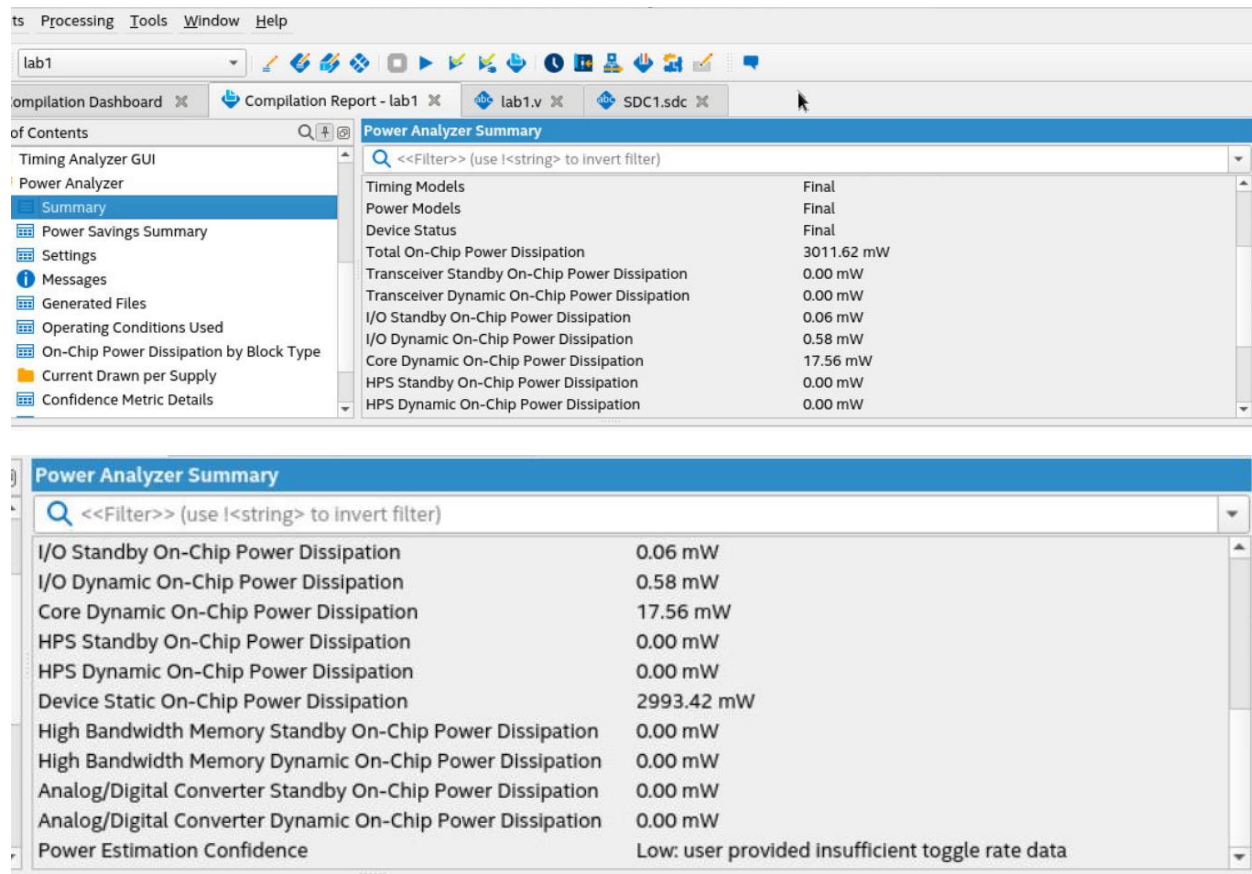
On-Chip Power Dissipation by Block Type

Show: Visible Hide <<Filter>> (use I<string> to invert filter)

	Block Type	Total On-Chip Power by Block Type	Block On-Chip Dynamic Power	Block On-Chip Standby Power	Routing On-Chip
1	DSP	2.07 mW	1.38 mW	0.00 mW	0.69 mW
2	Combinational cell	0.92 mW	0.51 mW	0.00 mW	0.41 mW
3	Register cell	1.03 mW	0.25 mW	0.00 mW	0.78 mW
4	IO Analog	0.59 mW	0.58 mW	0.01 mW	0.00 mW
5	IO Digital	0.06 mW	0.00 mW	0.05 mW	0.00 mW
6	Clock Network	13.54 mW	0.44 mW	0.00 mW	13.10 mW

Power Savings Summary  
Settings  
Messages  
Generated Files  
Operating Conditions  
On-Chip Power Dissipation  
Current Drawn per Signal  
Confidence Metric Data  
Signal Activities  
Flow Messages  
Flow Suppressed Messages

Fig: On-chip Power Dissipation by block type



**Fig: Power Analyzer Summary**

### Pipeline Implementation Tasks:

**1. Resources for one circuit =** Here, ALMs used i.e logic utilization is  $119 - 27 = 92$  ALMs.

Max. # of copies/device is restricted by the number of DSPs needed =  $1518 \text{ DSPs} / 6 \text{ DSPs} = 253$  copies per device.

**2. Operating frequency:** Time in SDC1.sdc is set to 4.65ns corresponding to 215.05 MHz.

**3. Critical path:**

**4. Cycles per valid output:** In the pipeline, after saturation is 1 cycle per valid output.

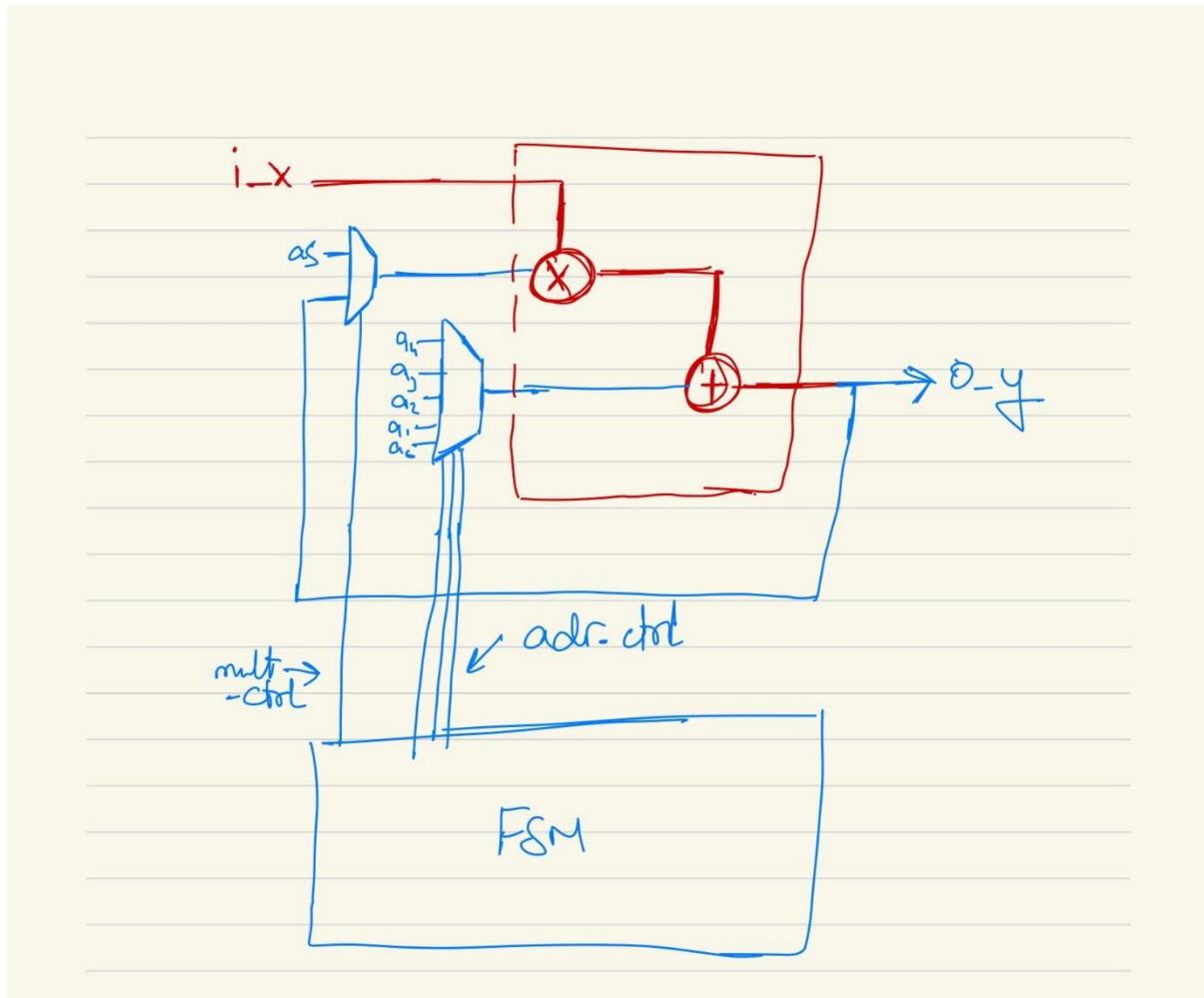
**5. Max. Throughput for a full device (computations/s):**  $215.05 * 10^6 * 380 = 81.7 * 10^9$  computations/s

**6. Dynamic power of one circuit:**  $2.07 + 0.92 + 1.03 \text{ mW} = 4.02 \text{ mW}$

**7. Max. throughput/Watt for a full device:** power consumed =  $4.02 \text{ mW} * 380 + 2993.42 = 4521.02 \text{ mW}$

Therefore, throughput/ Watt =  $81.7 * 10^9 / 4521.02 * 10^{-3} \text{ W} = 18 * 10^9$  computations/watt

## Shared Operator



Frequency: 1 GHz

No of cycles: 5

### Shared Implementation Tasks:

**1. Resources for one circuit** = Here, ALMs used i.e. logic utilization = **30 ALMs**.

Max. # of copies/device is restricted by the number of DSPs needed =  $1518 / 1 = 1518$  copies per device.

**2. Operating frequency:** Time in SDC1.sdc is set to 1 ns corresponding to 1GHz.

**3. Critical path:**

**4. Cycles per valid output:** In the shared, 5 cycles per valid output are designed.

**5. Max. Throughput for a full device (computations/s):**  $215.05 * 10^6 * 380 = 81.7 * 10^9$   
computations/s

**6. Dynamic power of one circuit:**  $2.07 + 0.92 + 1.03 \text{ mW} = 4.02 \text{ mW}$

**7. Max. throughput/Watt for a full device:** power consumed =  $4.02 \text{ mW} * 1518 + 2993.42 = 4521.02 \text{ mW}$

Therefore, throughput/ Watt =  $81.7 * 10^9 / 4521.02 * 10^{-3} \text{ W} = 18 * 10^9$  computations/watt