

Paging Limitations

- Can still have internal fragmentation
- Requires 2 or more references, which could limit performance
- ➔ **Solution:** use a hardware cache of lookups (coming next)
- The amount of memory to store the page table is significant
 - Need one PTE per page, with 32 bit address space w/ 4KB pages = 2^{20} PTEs
 - 4 bytes/PTE = 4MB/page table
 - 25 processes = 100MB just for page tables!
- ➔ **Solution :** page the page tables (coming next)

x86 Paging and Segmentation

x86 architecture supports both paging and segmentation

- Segment register base + pointer val = linear address
- Page translation happens on linear addresses
- Two levels of protection and translation check
 - Segmentation model has four privilege levels (CPL 0–3)
 - Paging only two, so 0–2 = kernel, 3 = user