Translation Lookaside Buffers (TLBs)

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special hardware to translate virtual page #s into PTEs (not physical address) in a single machine cycle

- Typically 4-way to fully associative cache (all entries looked up in parallel)
- Cache 32-128 PTE values (128-512K memory)
- → TLBs exploit locality: processes only use a handful of pages at a time TLB hit rate is a very important for performances (>99% of translations)

TLB Page Lookup Physical Memory Virtual Address offset page TLB Physical Address TLB hit frame offset PTE TLB miss Page Directory/Table(s) page frame