| **Discente:** | **RGA** |
| --- | --- |
| Débora Mateus | 202221901007 |
| Kelvin Wender Martins Pereira | 202021901031 |
| Marcos Antonio Borges | 202121901056 |
| Victor Daniel Mohr Steffens | 202221901059 |

**Relatório da aula prática do dia 22/08/2023**

1. **Objetivo**

Criar um registrador contador crescente utilizando um somador de clock, como resultado retornar um simbolo (letras e numeros), em dois display de sete segmento.

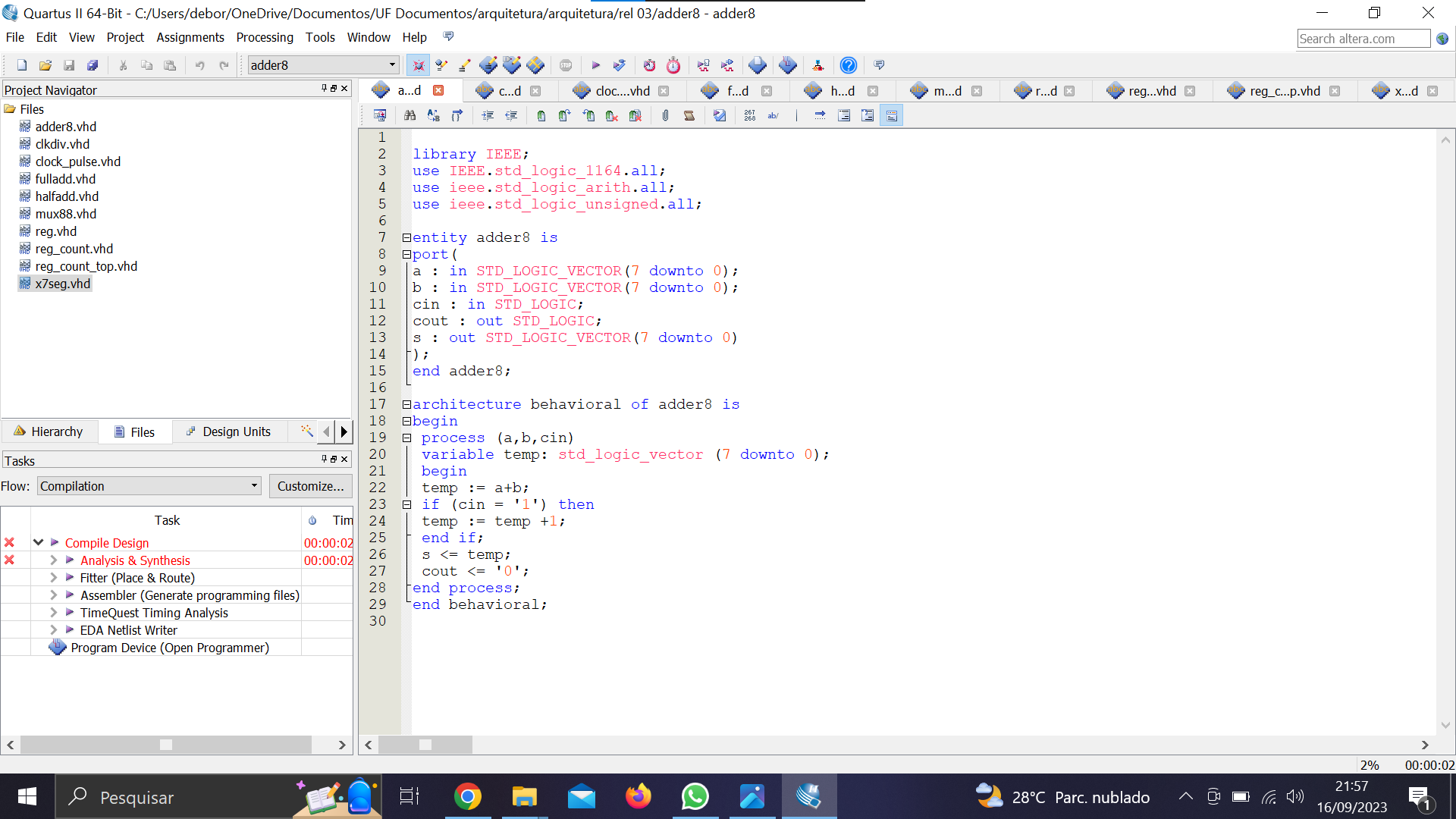
1. **Materiais e Métodos**

Para a realização da atividade foram utilizados:

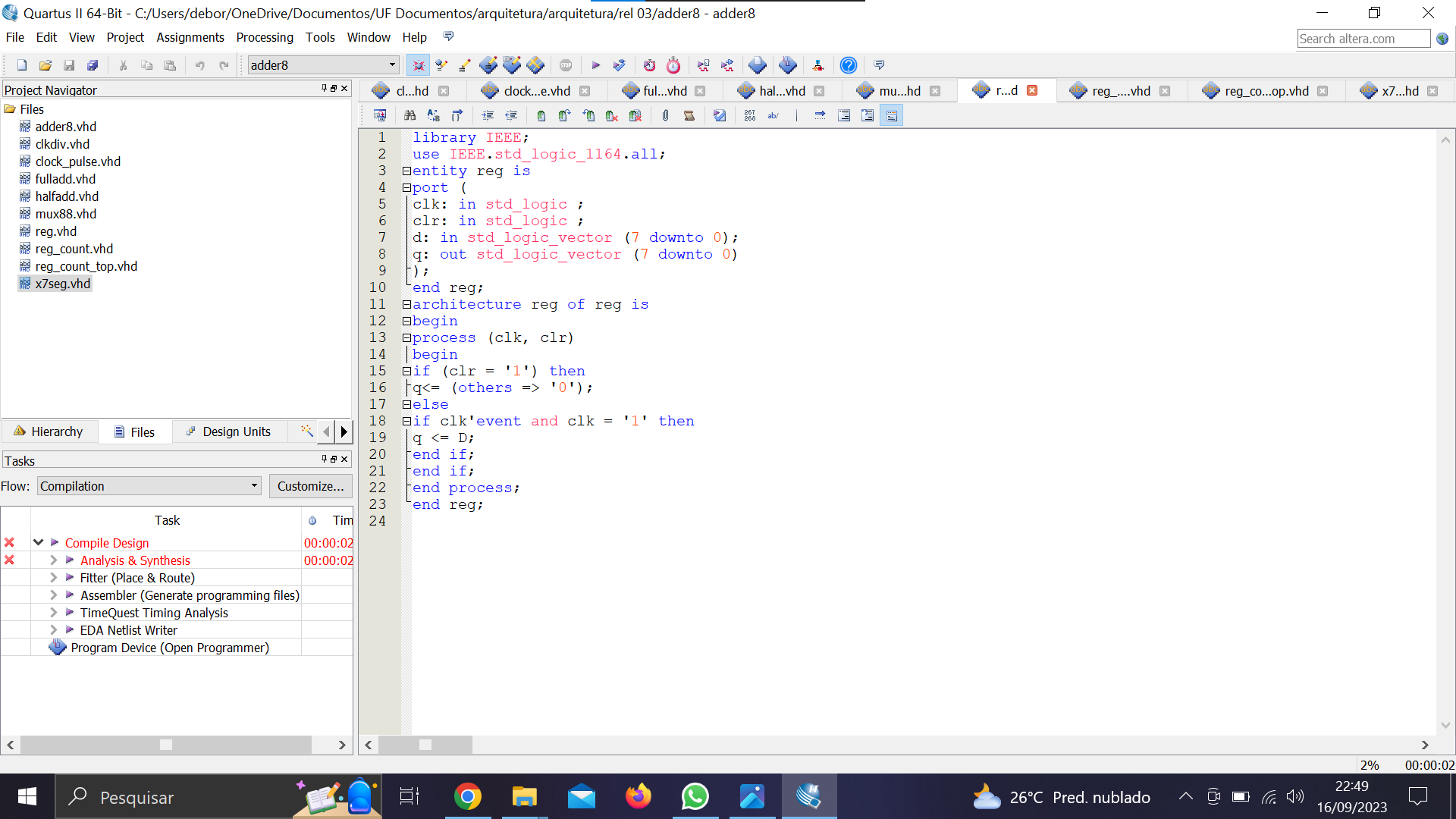
* **Software Altera**
* **Quartus II**
* **Placa OMDAZZ EP4CE6E22C8**
* **UBS Blaster**

1. **Procedimento Experimental**

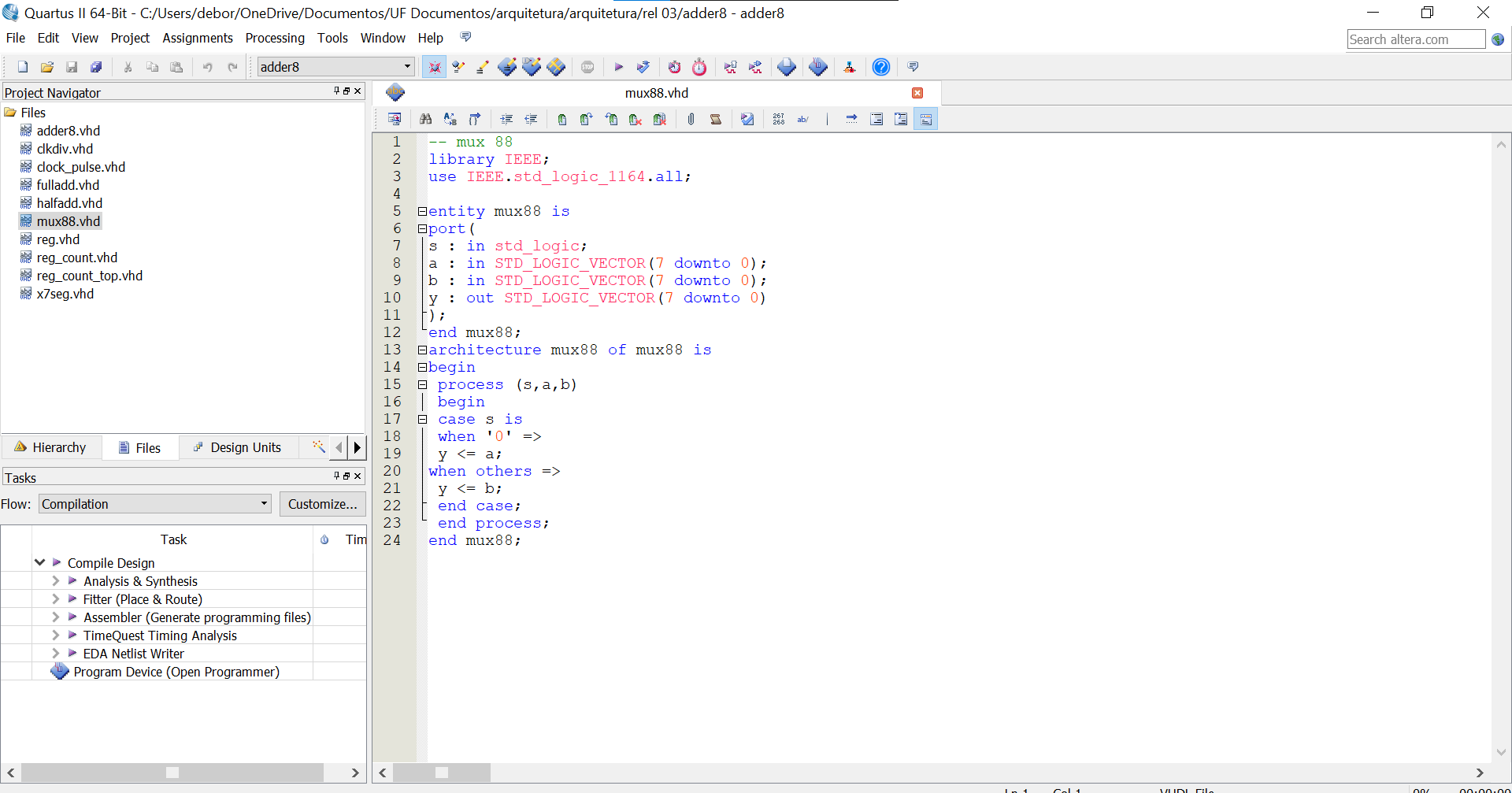
**adder8**

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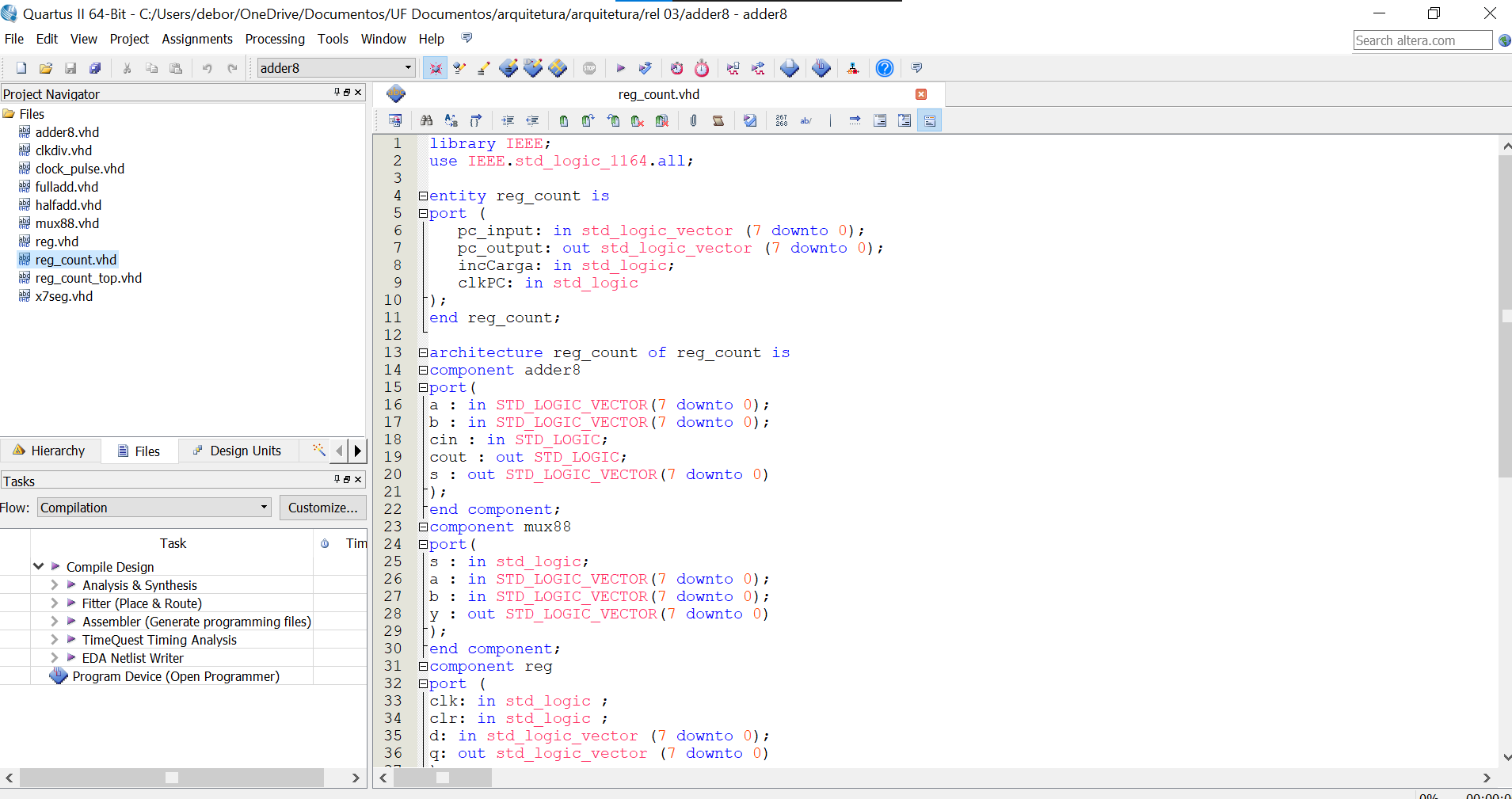
**reg**

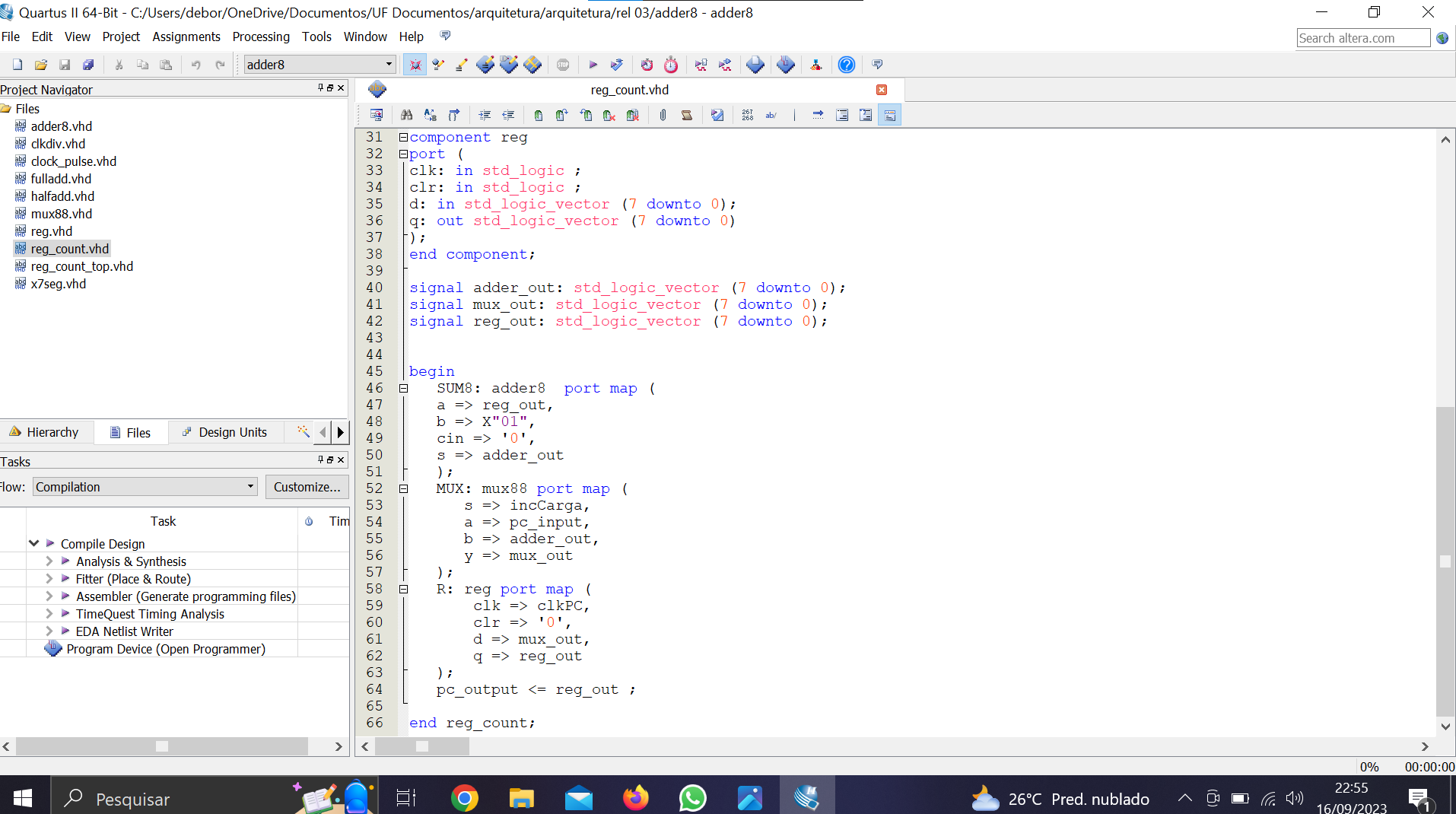
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**mux88**

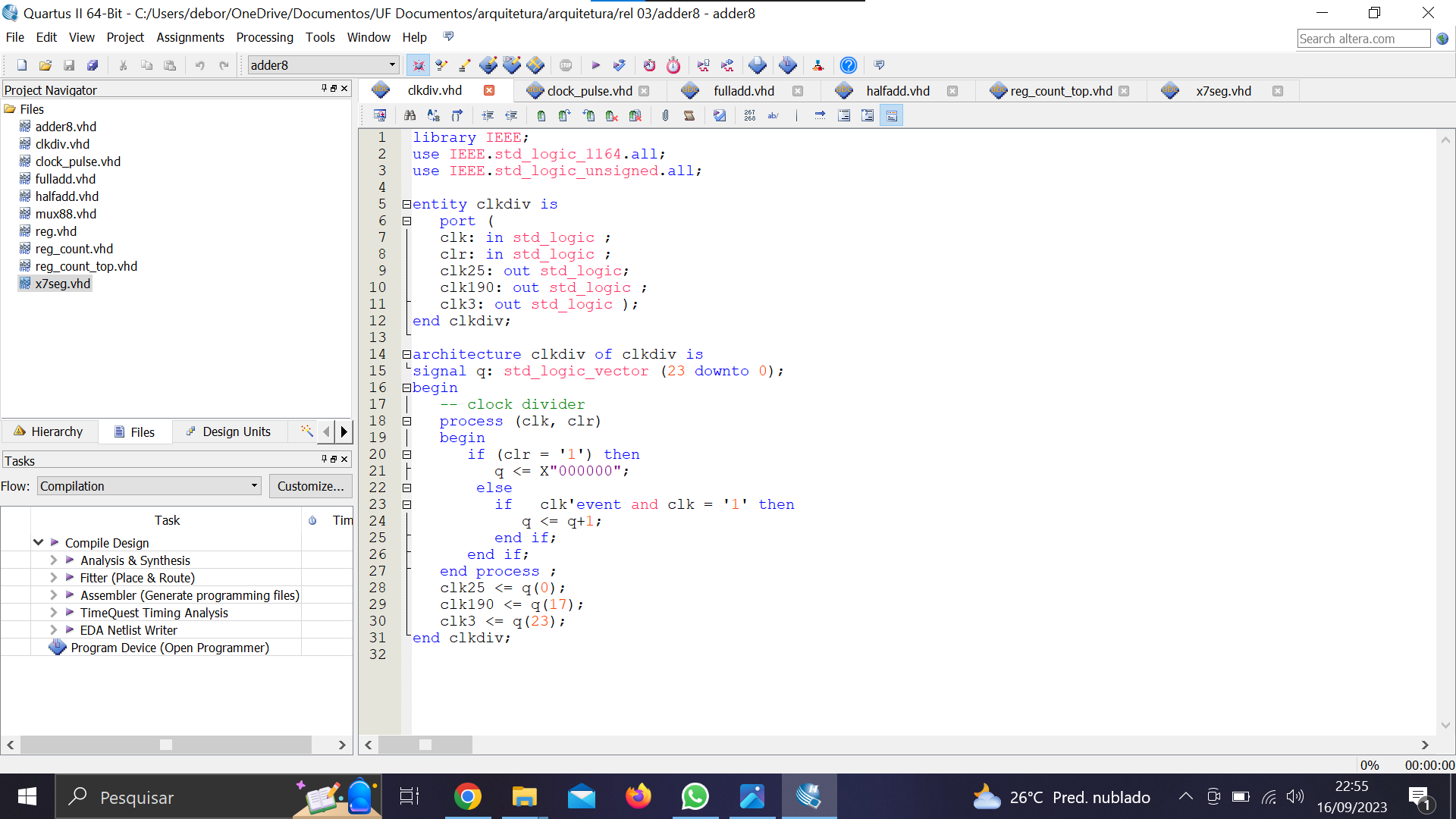
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**reg\_count**

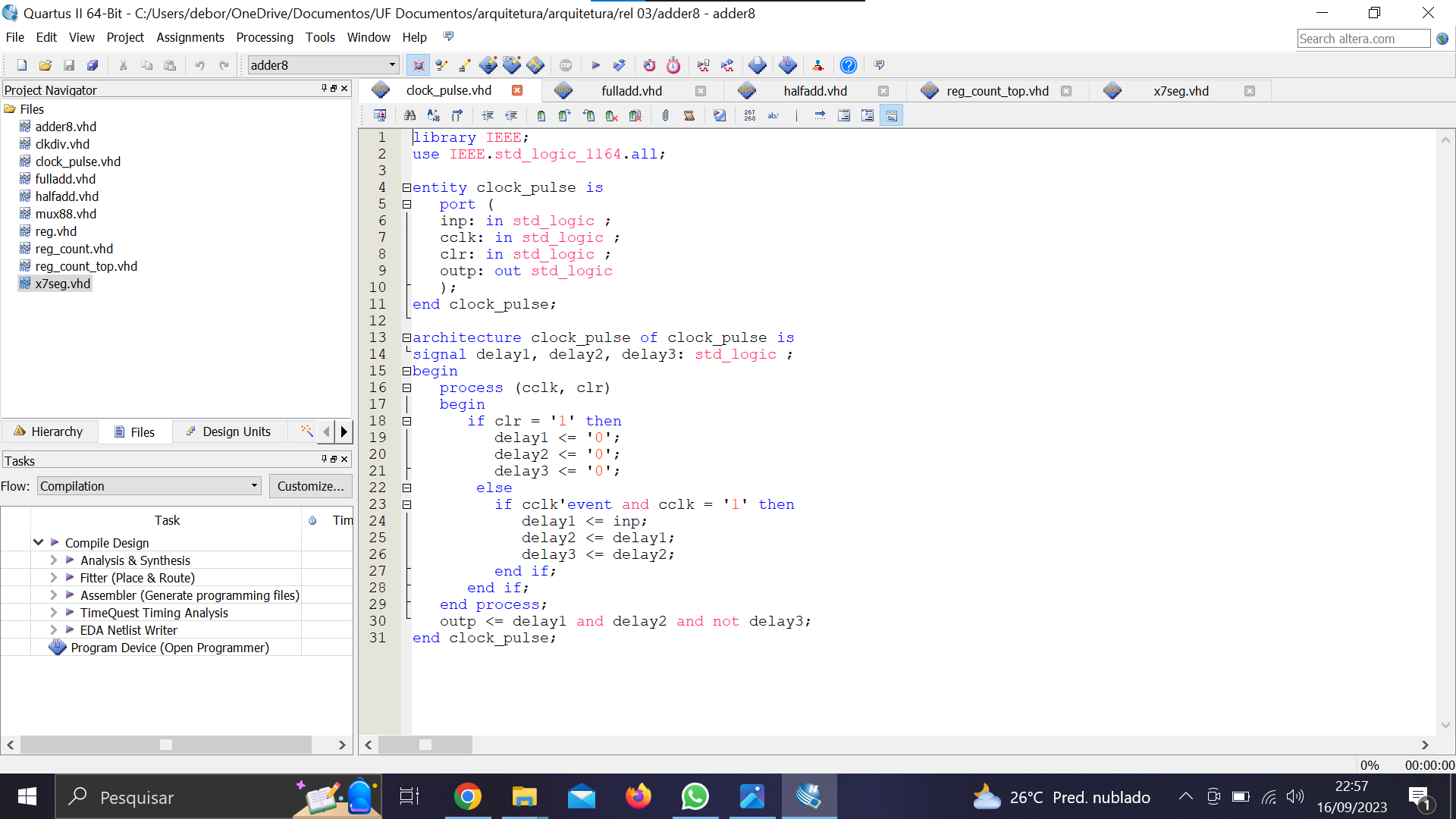
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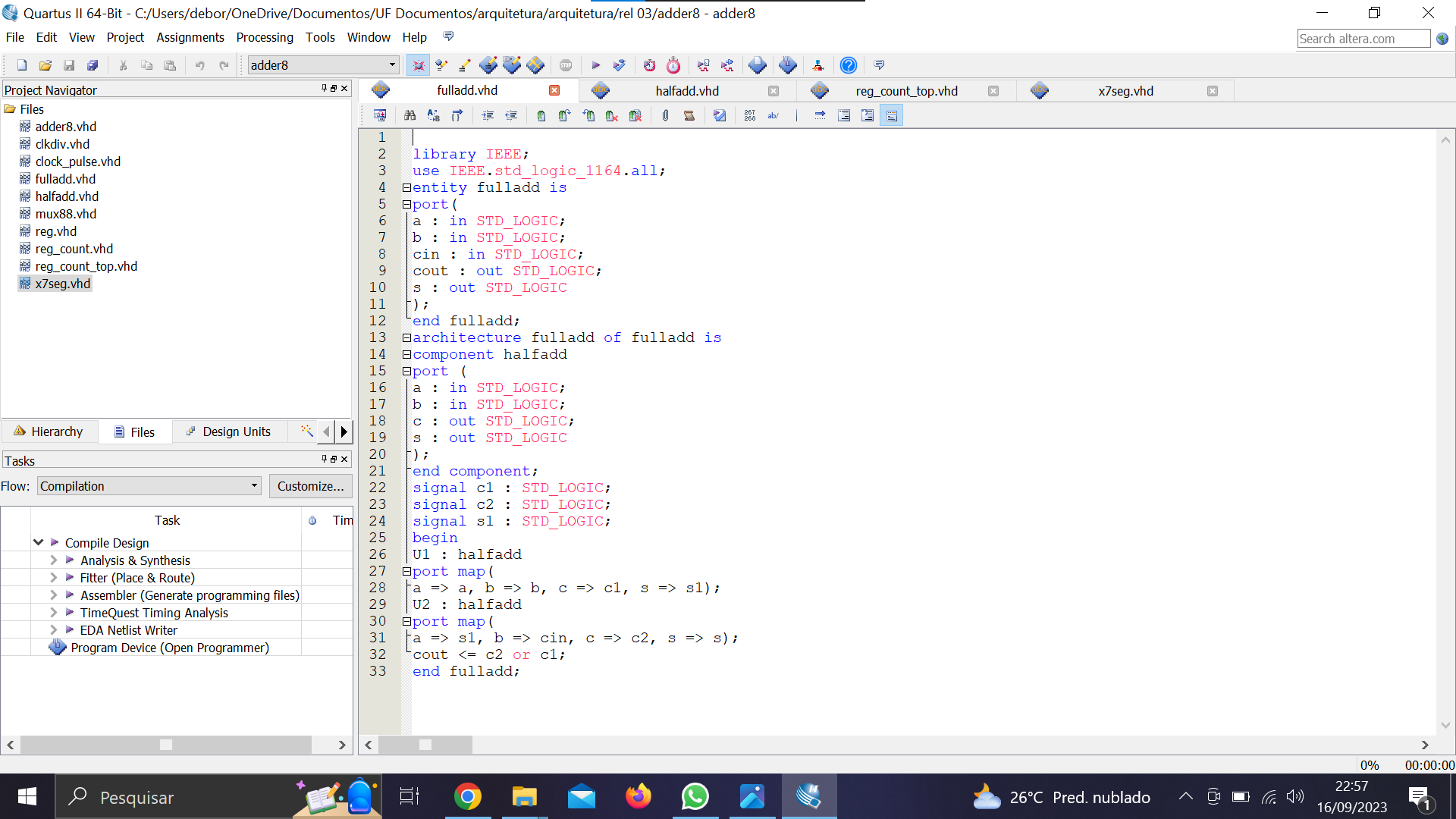
**Clkdiv**

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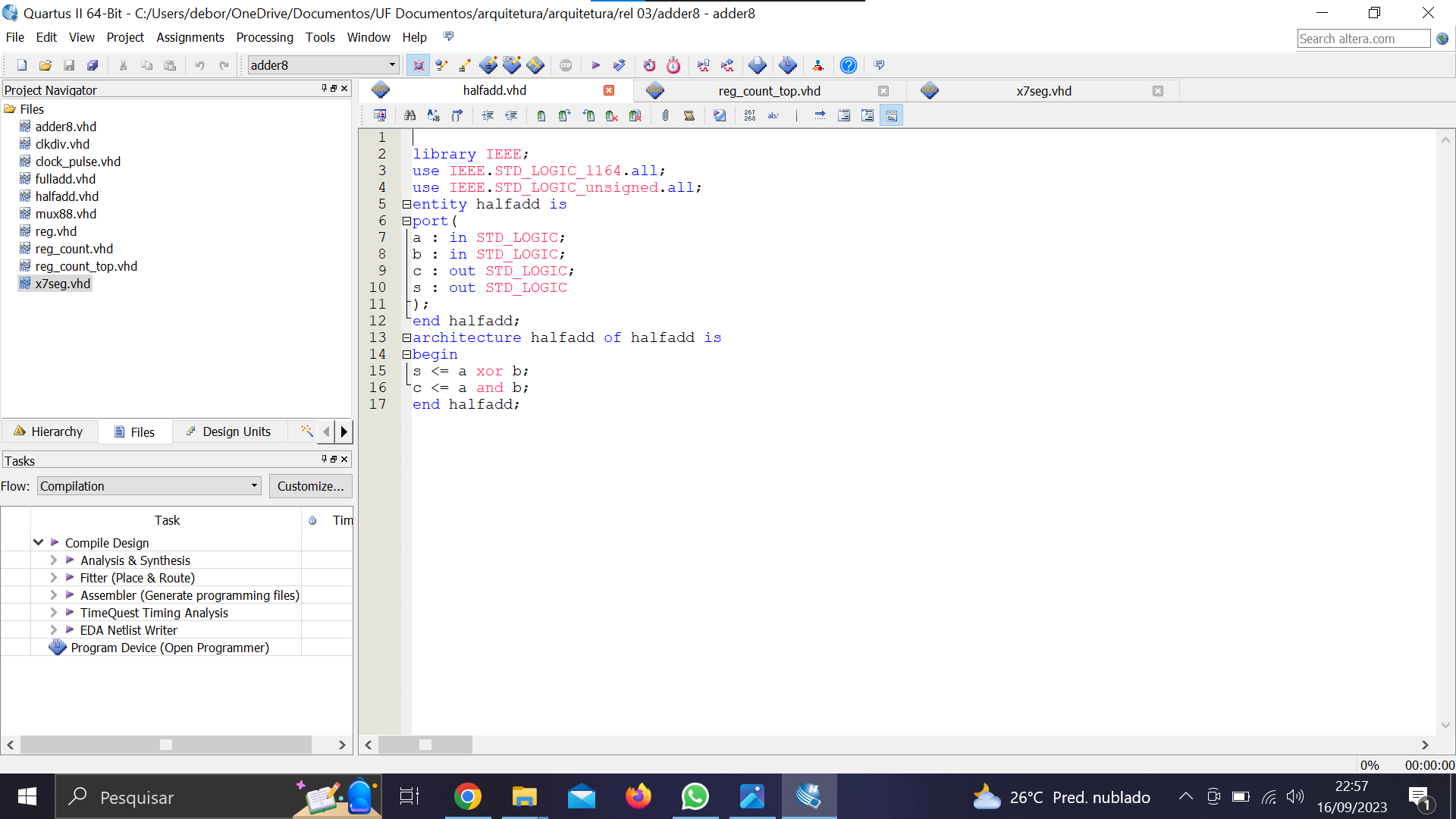
**clock\_pulse**

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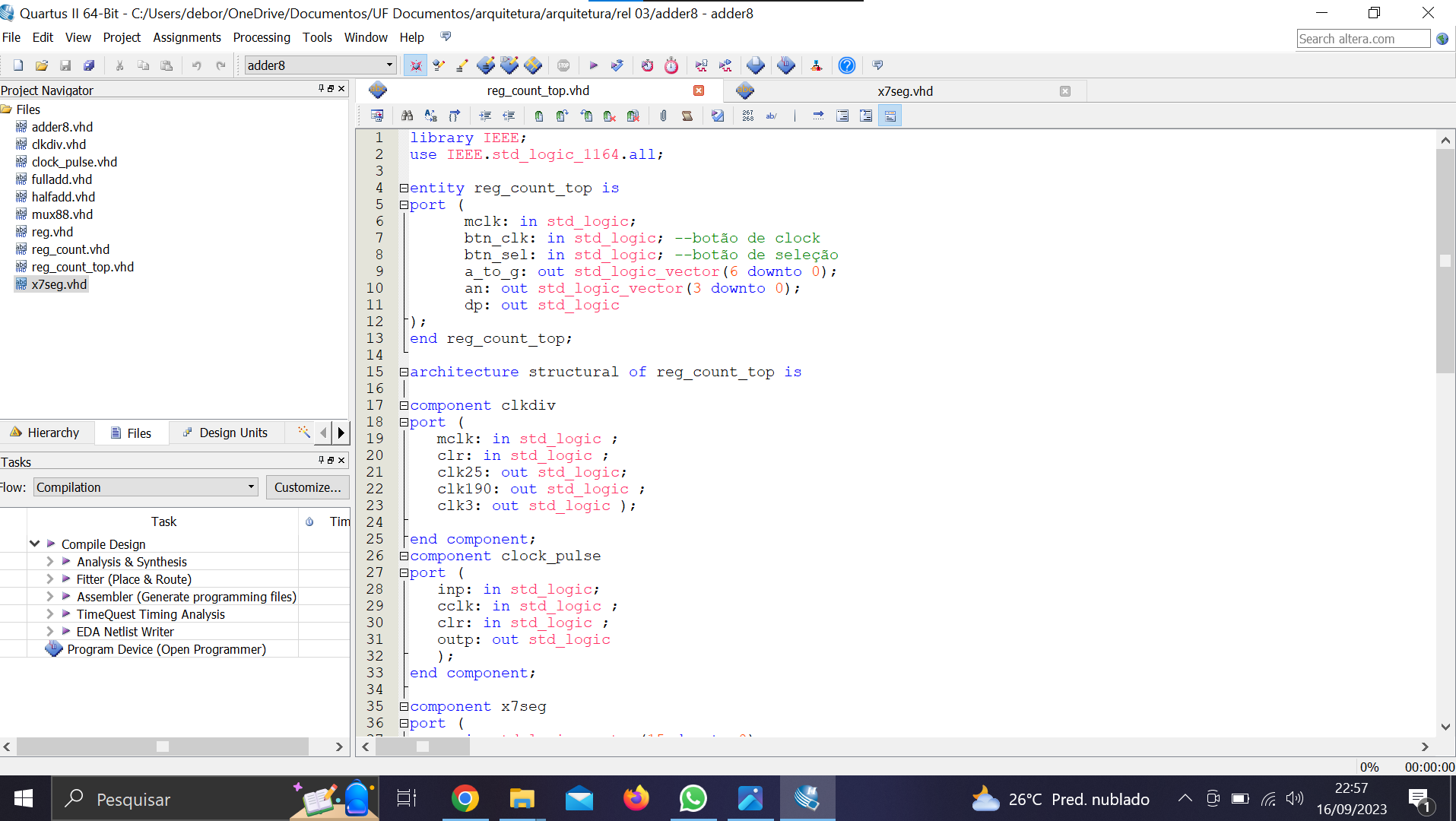
**fulladd**

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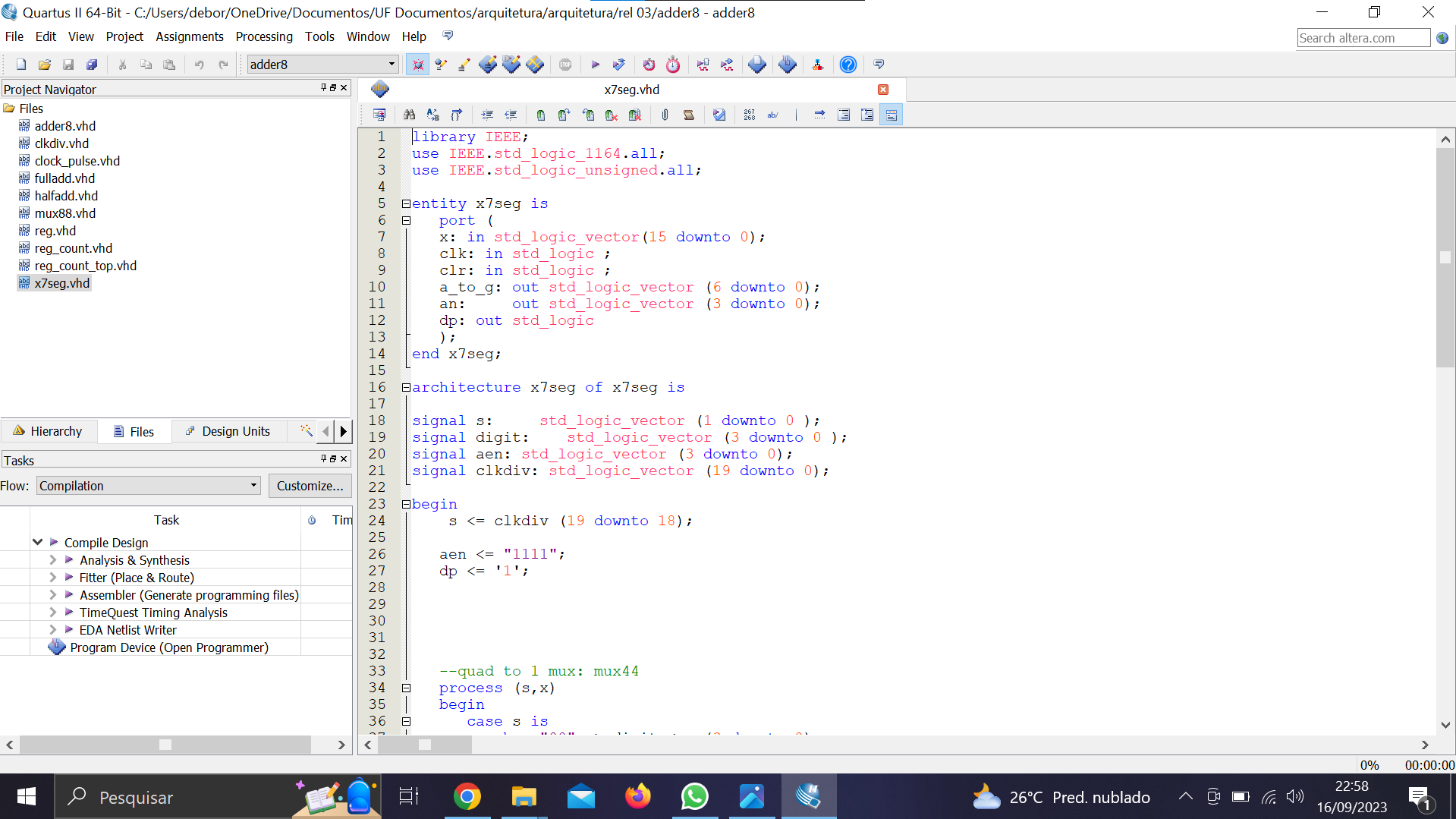
**halfadd**

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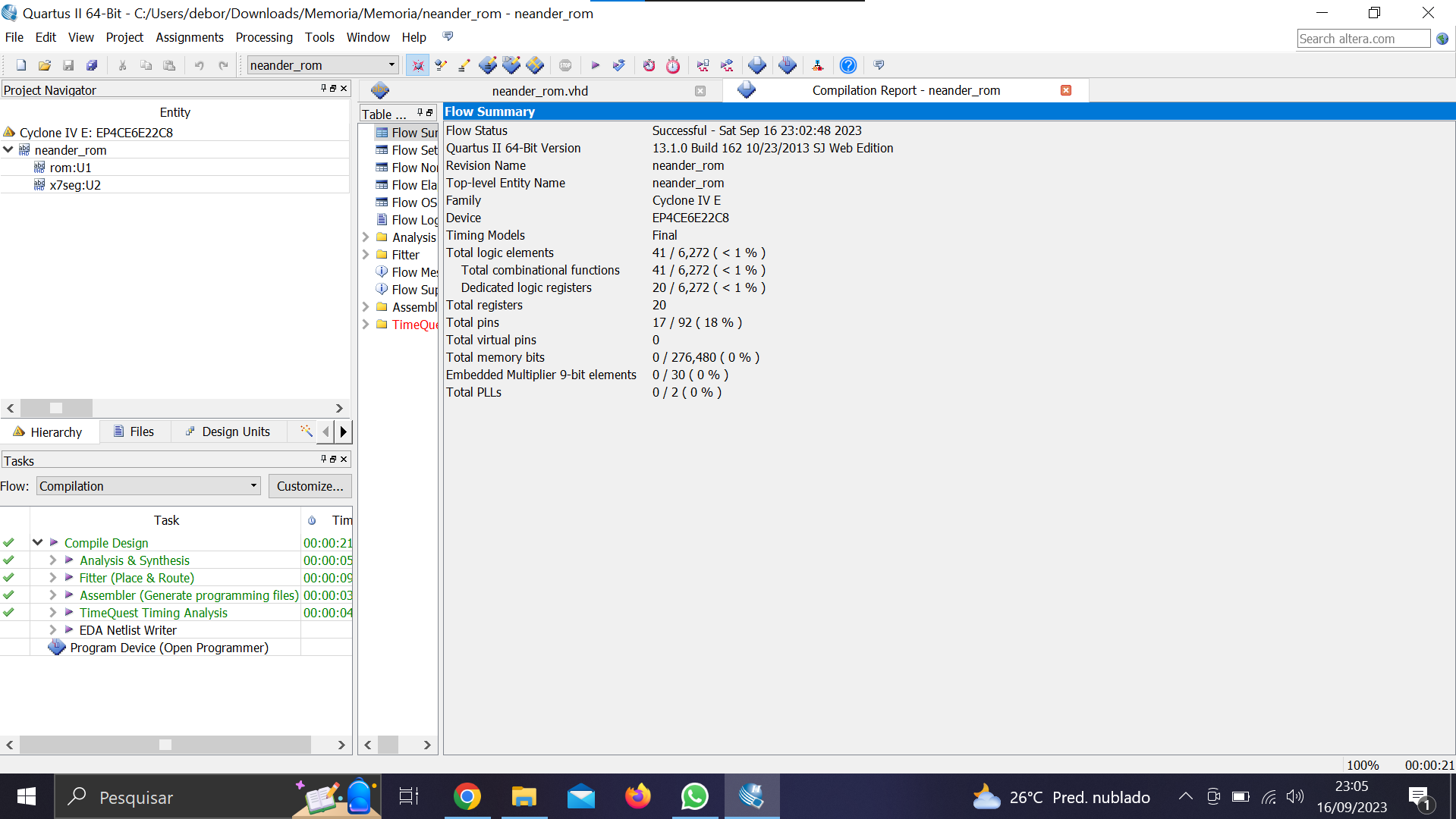
**reg\_count\_top**

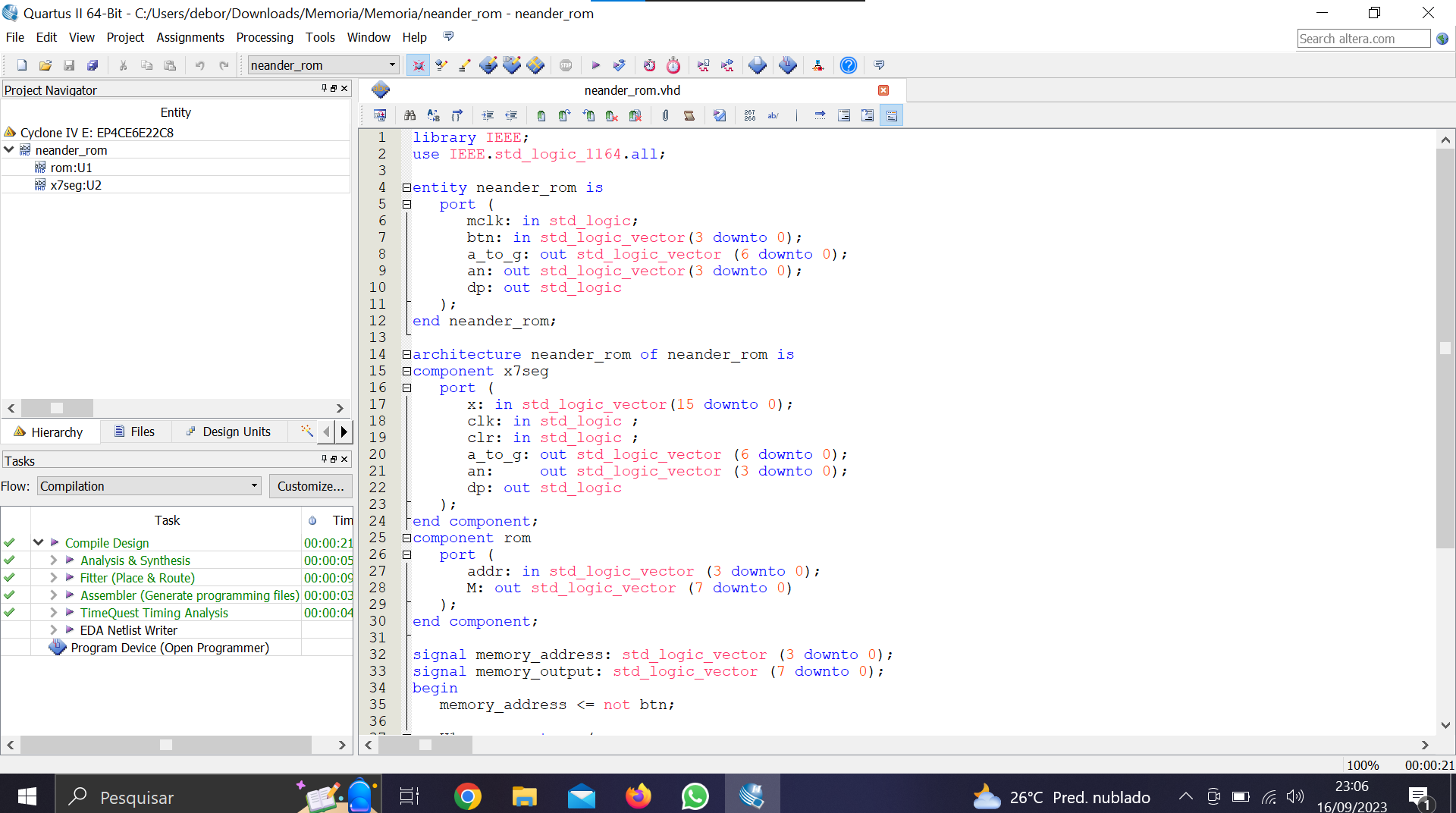
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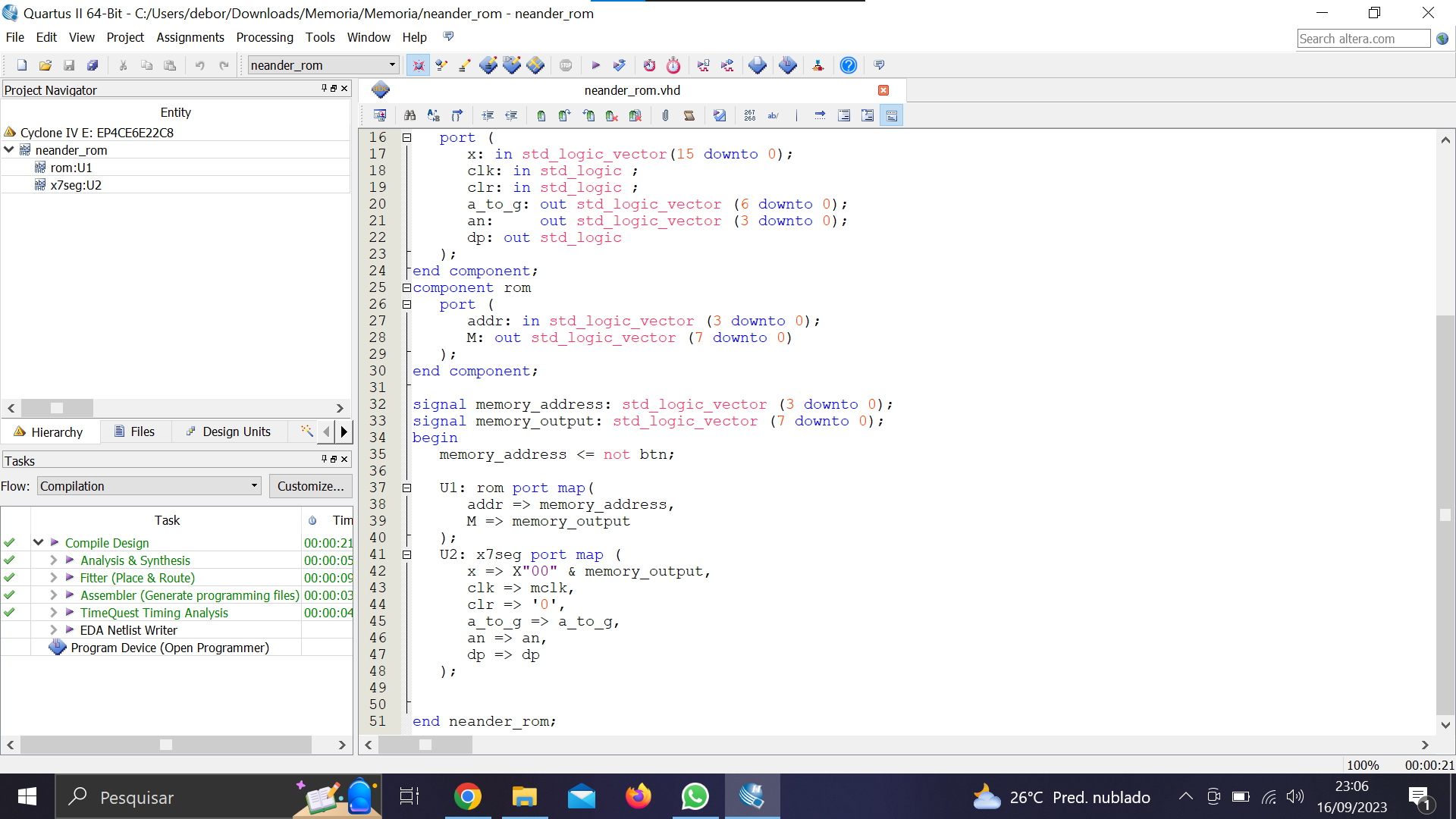
**x7seg**

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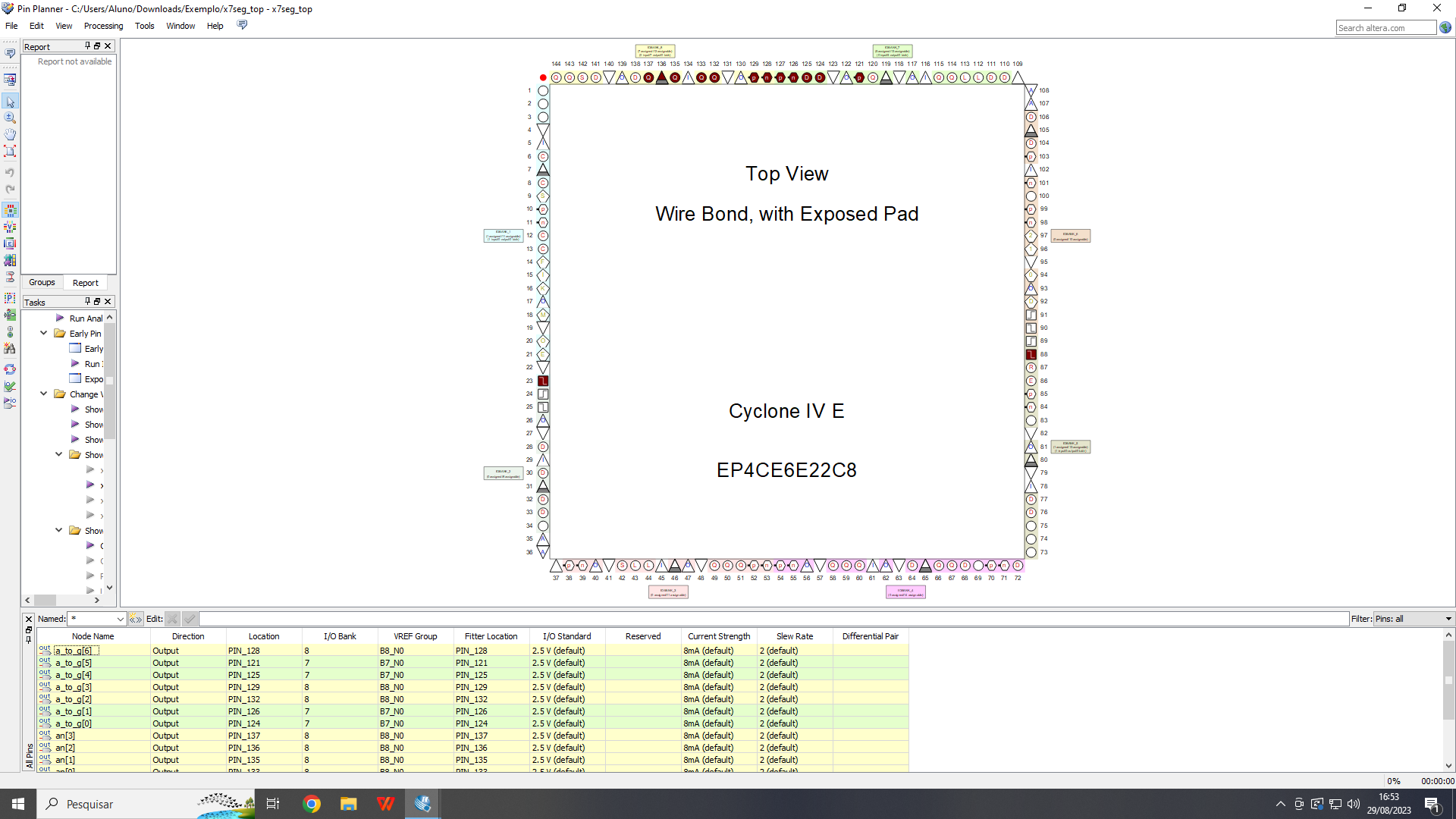
**Neander\_room**

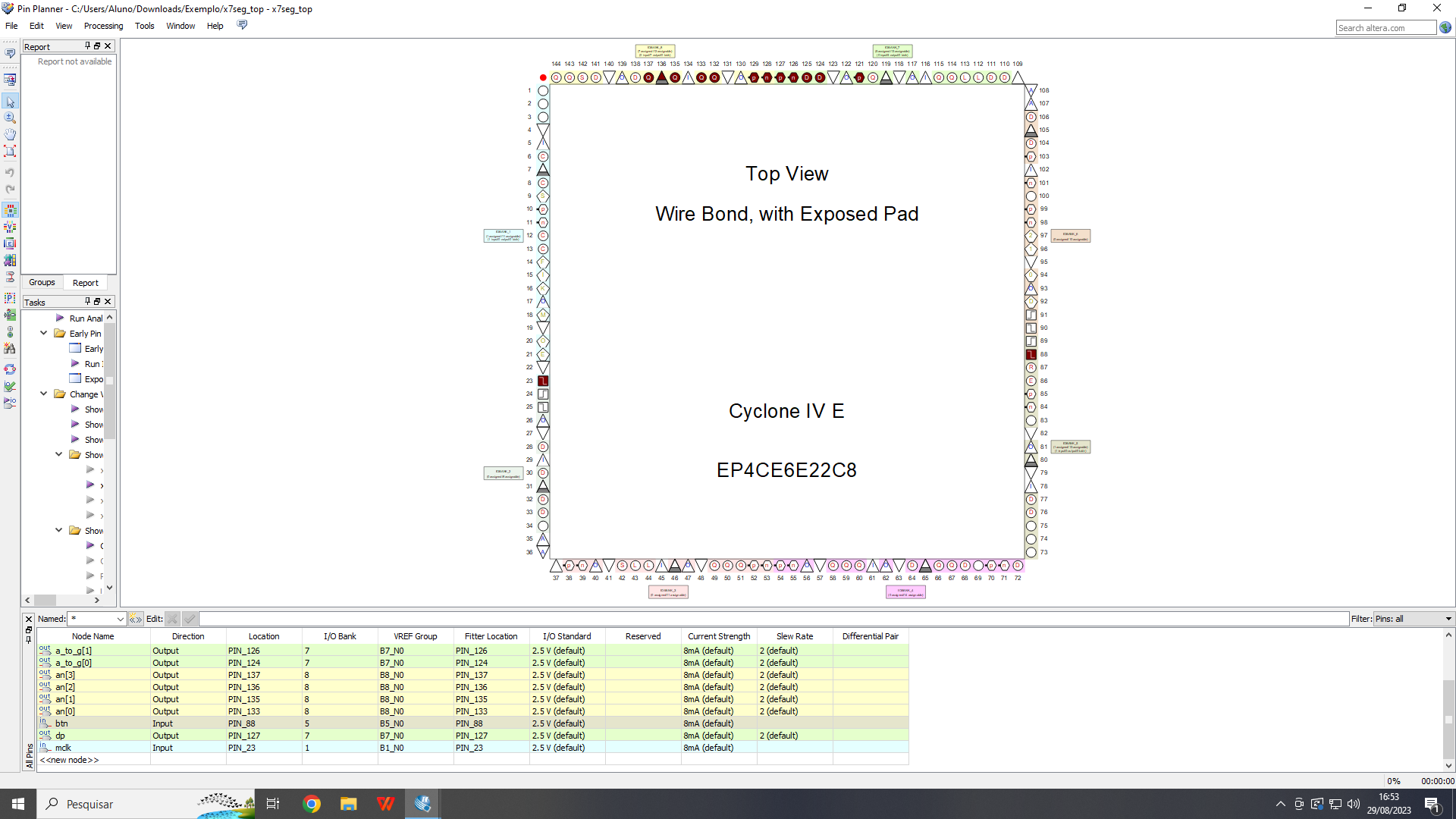
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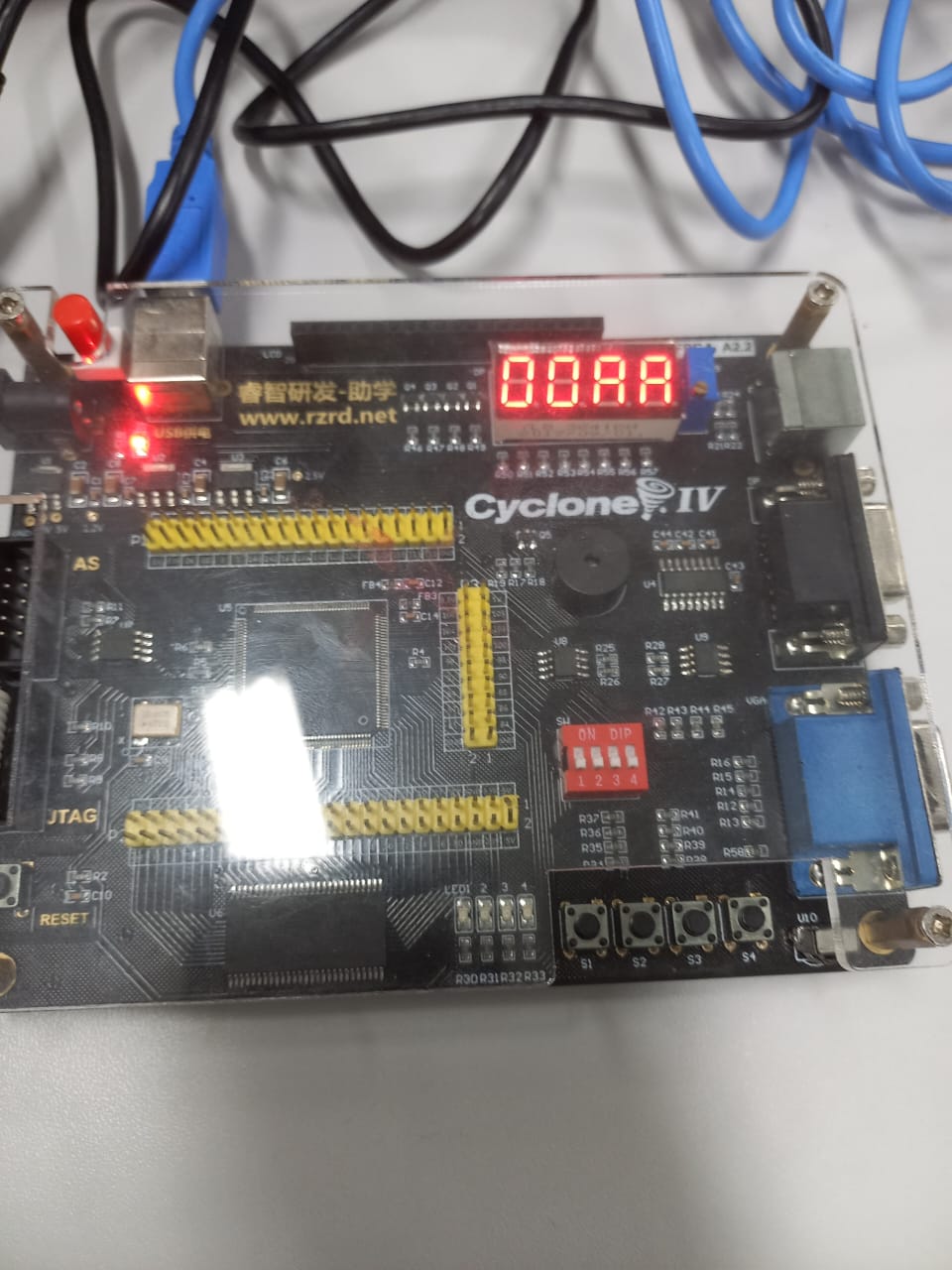
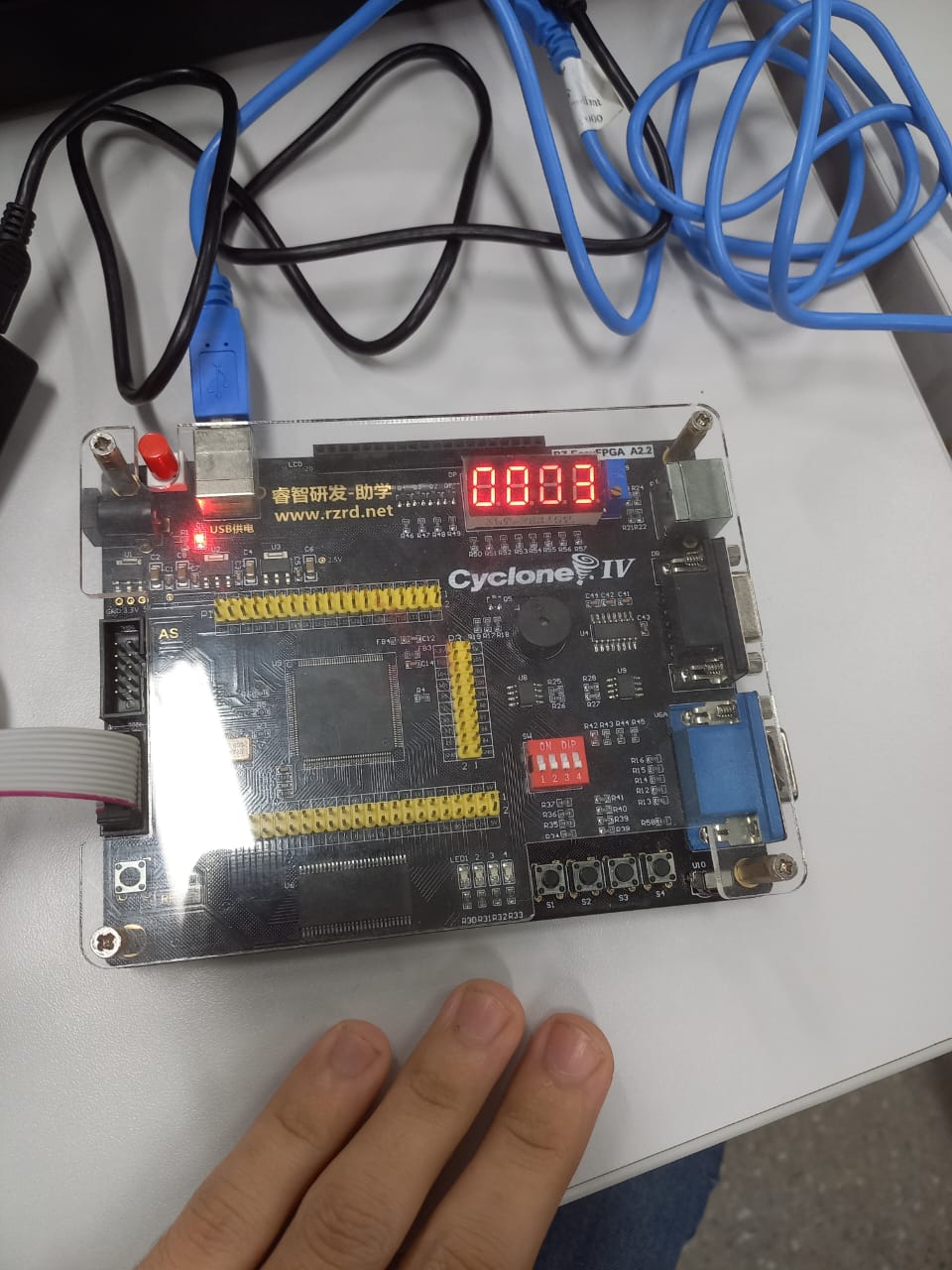
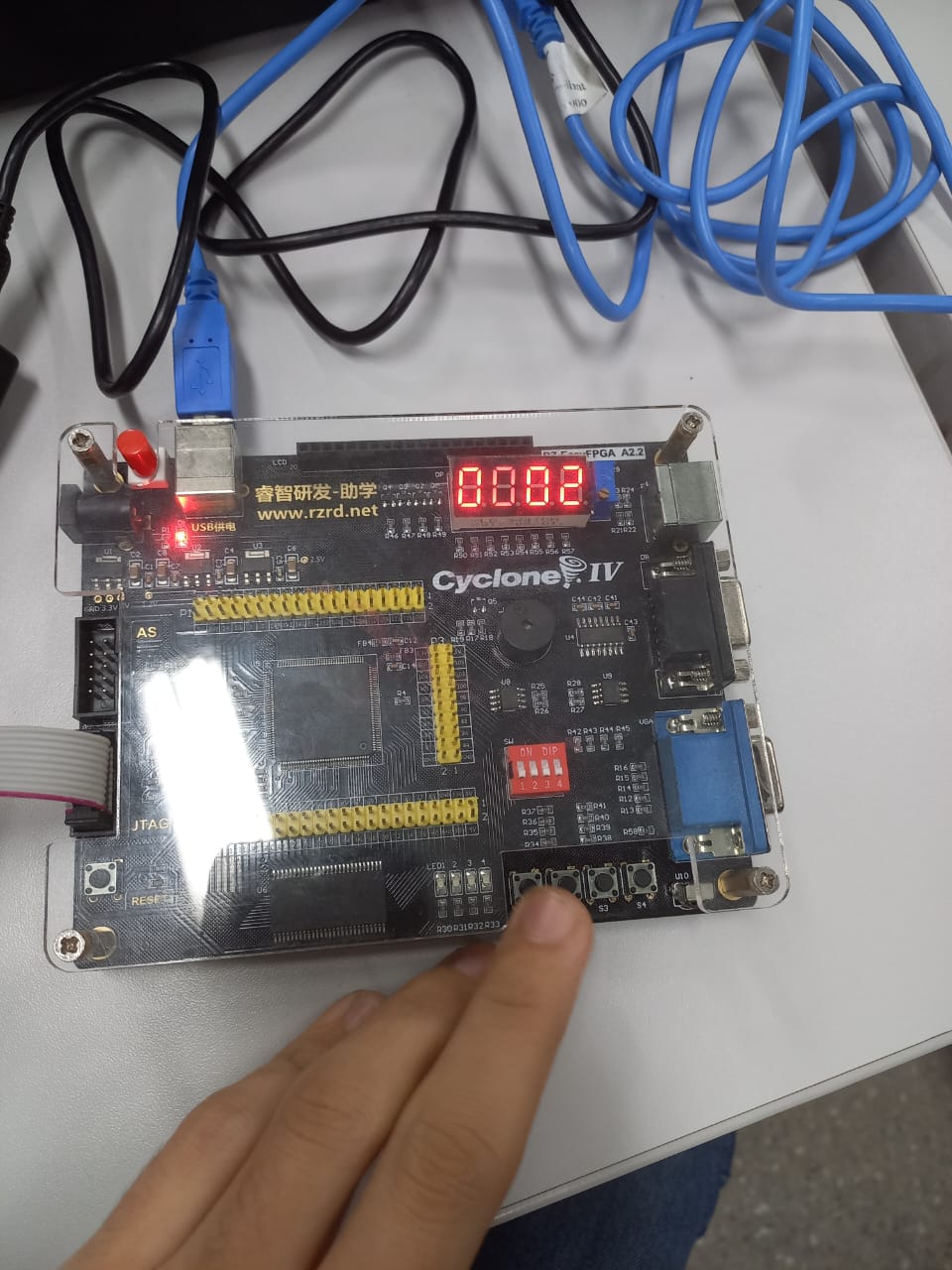
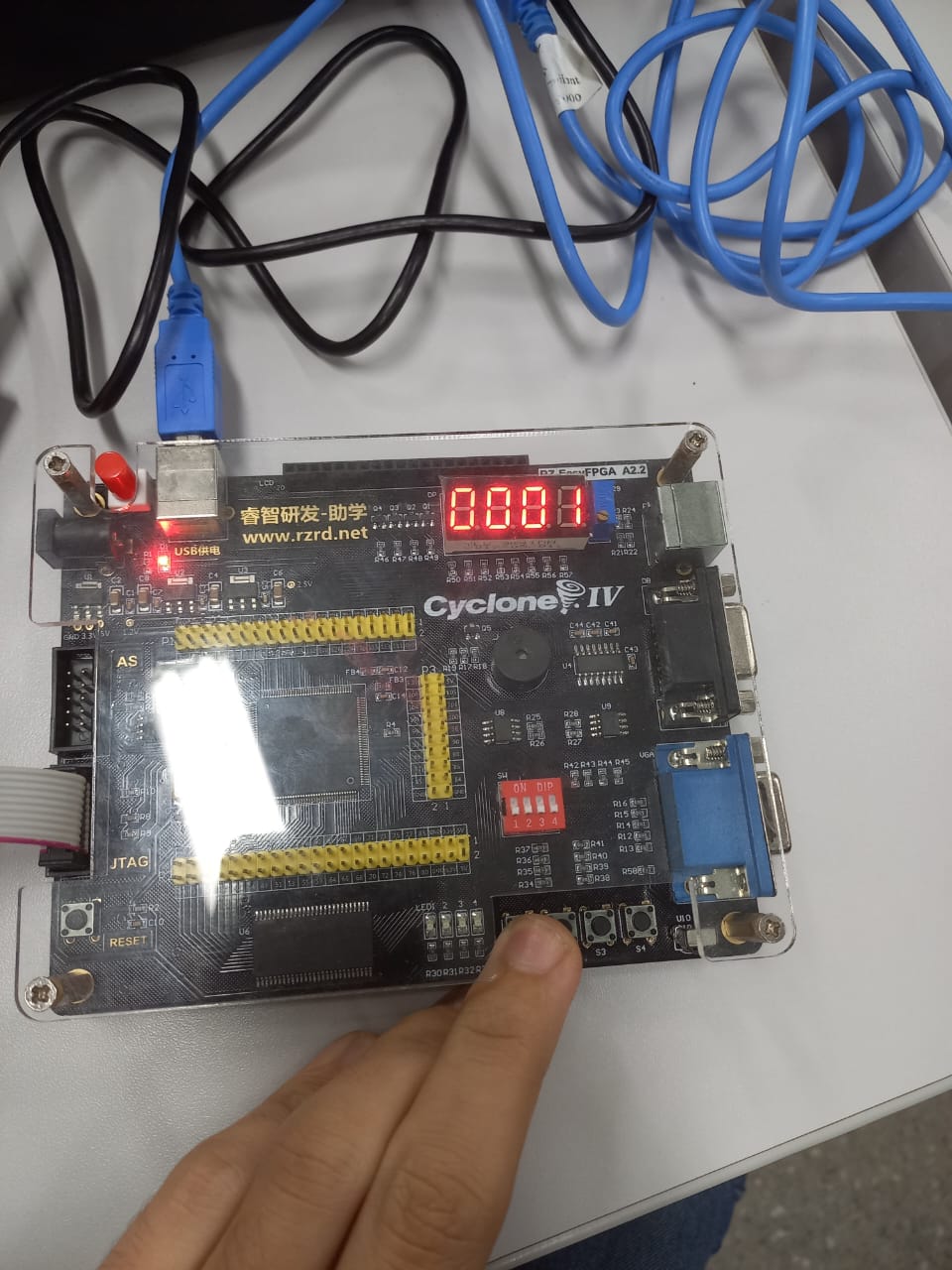
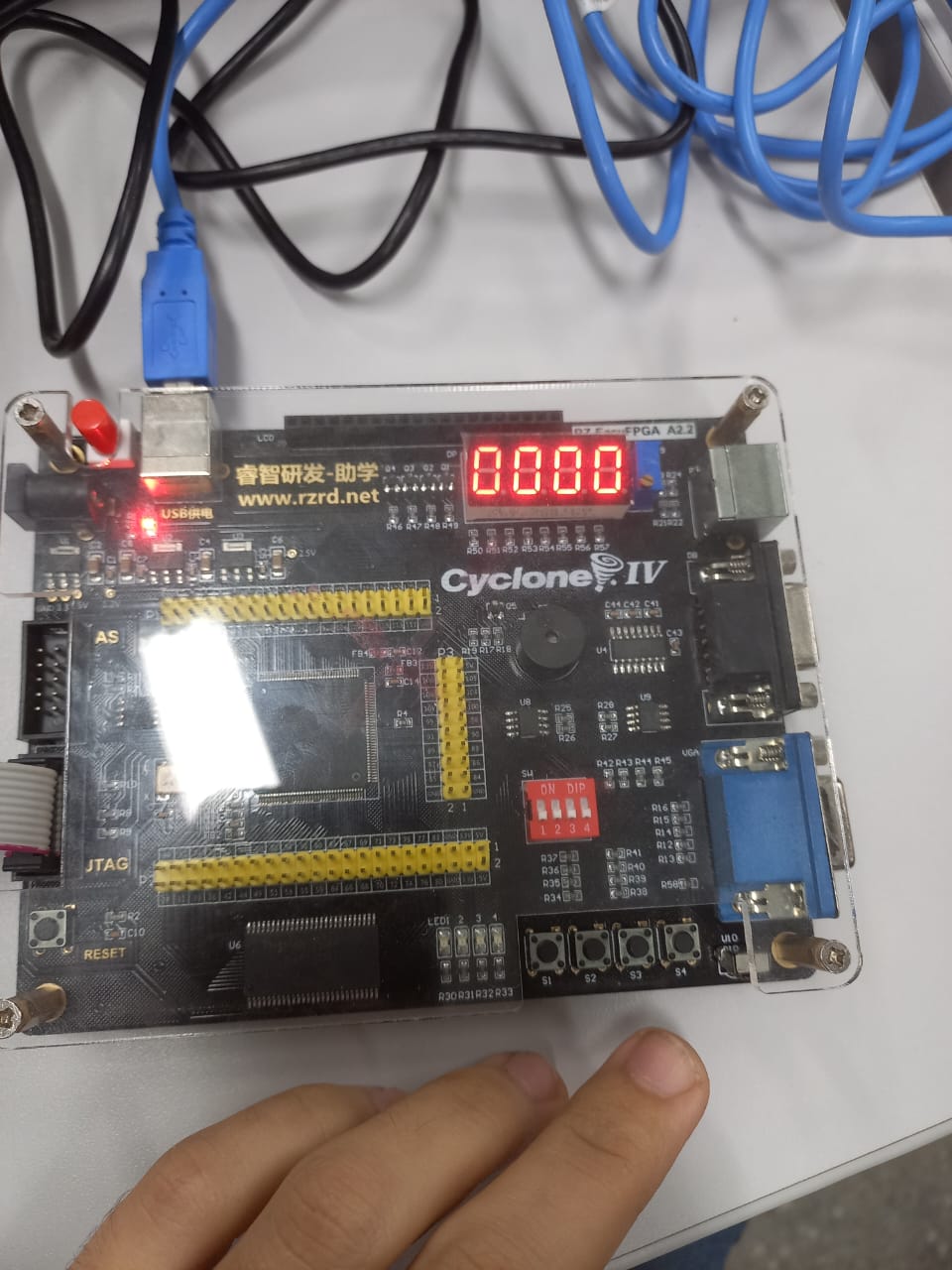
**Pin planner**

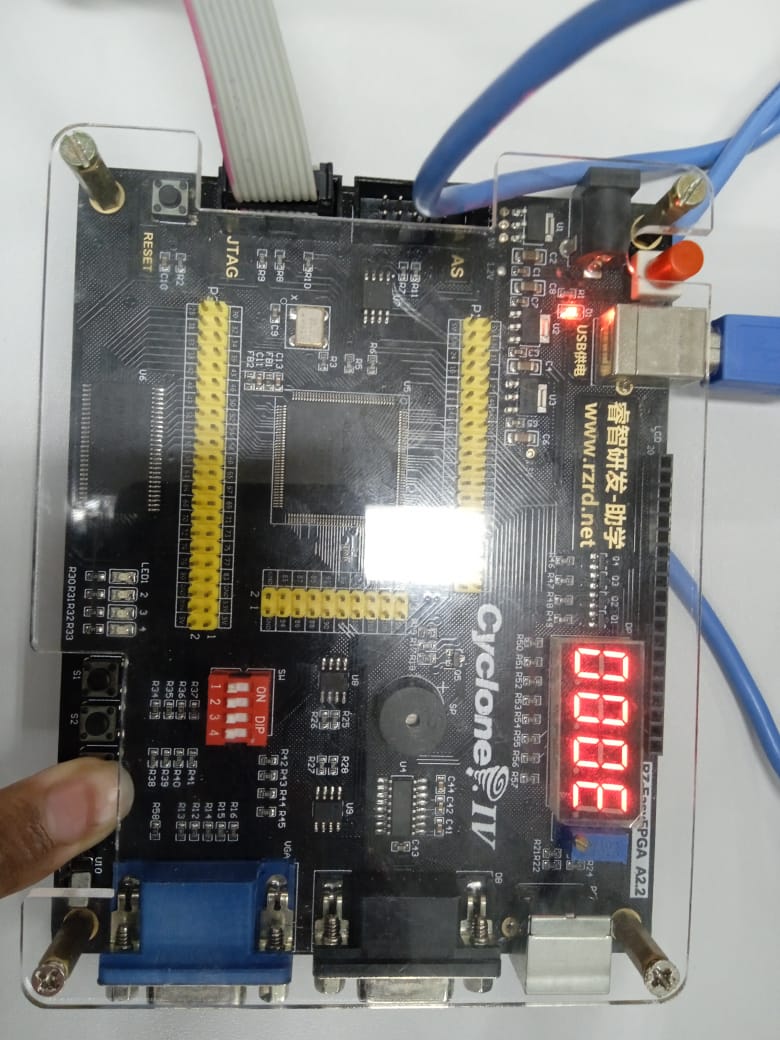




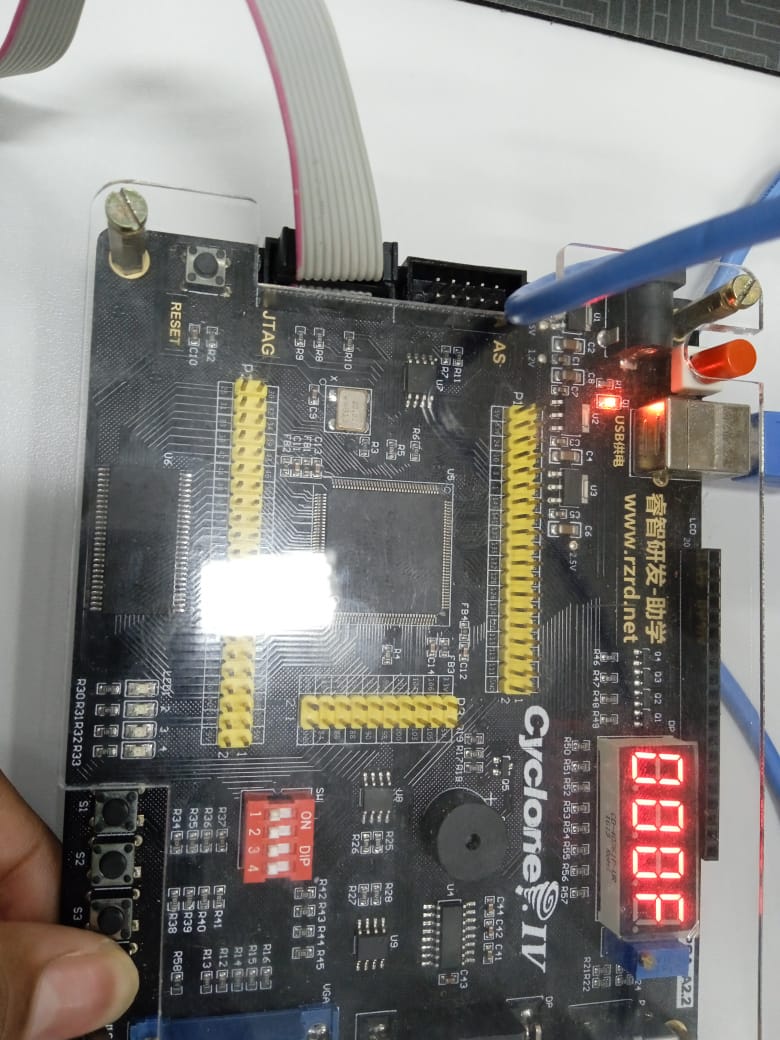
1. **Resultados e Conclusão:**

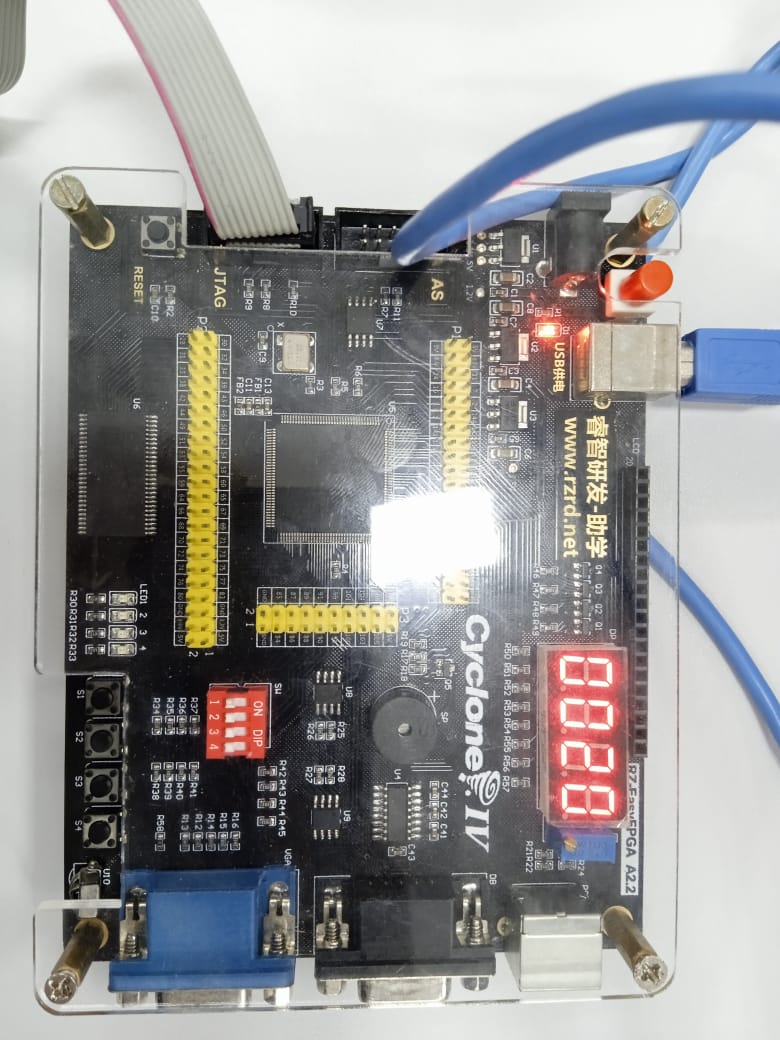
**Botões que ao apertar fazem com apareça simbolos (AA), e atraves do somador é acrescentado + 1, aparecendo nos dois displays de anodo 7 segmento, a somatoria em hexadecimal.**

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1. **Bibliografia**

BROWN, Stephen D. **Fundamentals of digital logic with VHDL design**. Boston: McGraw-Hill, 2000. 840 p. (004.22 B879f).

D’AMORE, Roberto. A Synthesis-Oriented VHDL Course. **ACM Transactions on Computing Education (TOCE)**, v. 10, n. 2, p. 1-24, 2010.

PEDRONI, Volnei A. **Eletrônica Digital Moderna e VHDL**. Elsevier Ltda. Editora, Rio de Janeiro, RJ: 2010. 619 p.