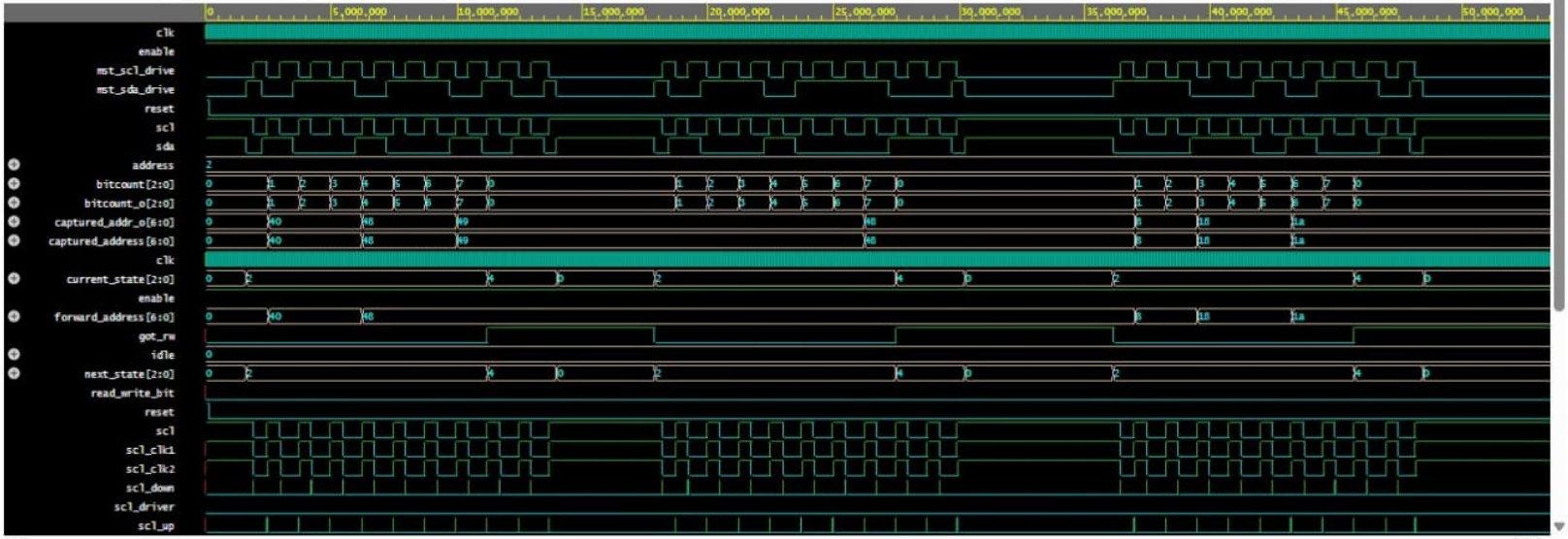
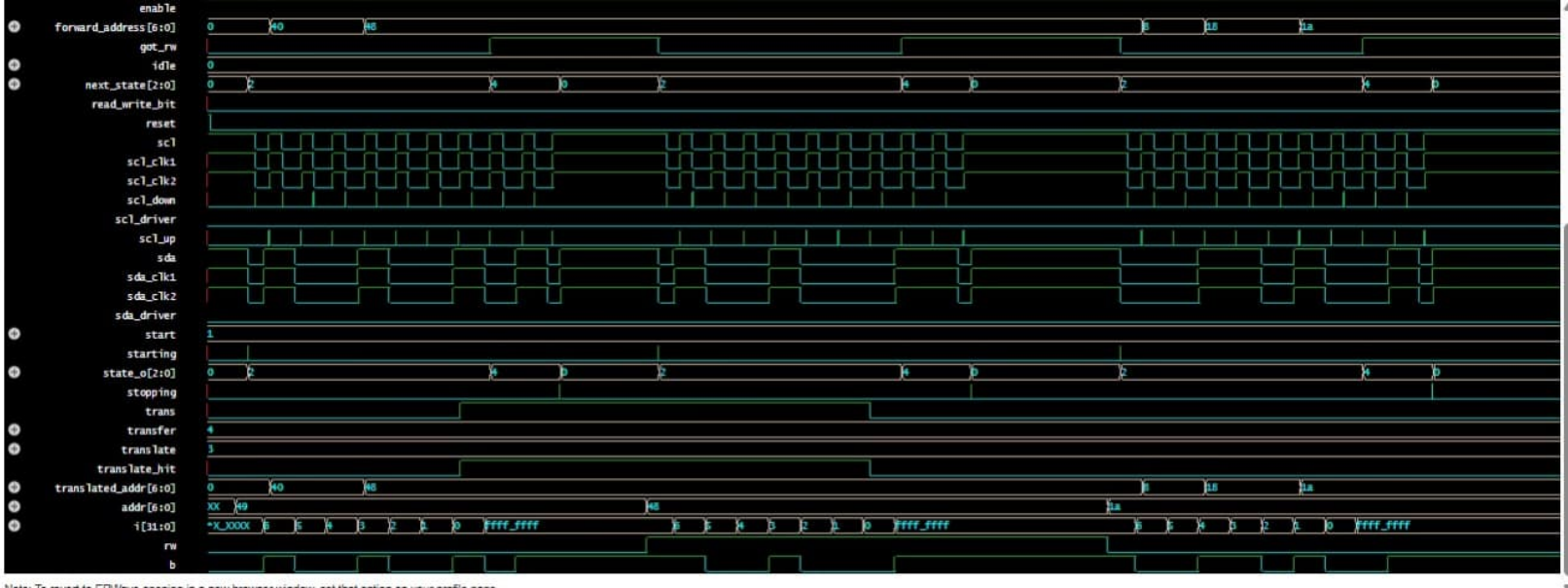
```
TB:Sending address 0x49 (expect translation) at time 1100000
FPGA: Translating virtual address 0x49 -> physical 0x48
TB:Sending address 0x48 (no translation) at time 15100000
FPGA: Forwarding normal address 0x48
TB:Sending address 0x1A (no translation) at time 31100000
FPGA: Forwarding normal address 0x1a
TB:Test is complete at time 47100000
testbench.sv:152: $finish called at 47100000 (1ps)
Finding VCD file...
./i2c_address_translator_tb.vcd
[2025-11-08 06:58:28 UTC] Opening EPWave...
Done
```


0
5,000,000
10,000,000
15,000,000
20,000,000
25,000,000
30,000,000
35,000,000
40,000,000
45,000,000
50,000,000
clk
enable
mst_scl_drive
mst_sda_drive
reset
scl
sda
address
bitcount[2:0]
bitcount_o[2:0]
captured_addr_o[6:0]
captured_address[6:0]
clk
current_state[2:0]
enable
forward_address[6:0]
got_rw
idle
next_state[2:0]
read_write_bit
reset
scl
scl_clk1
scl_clk2
scl_down
scl_driver
scl_up


enable
forward_address[6:0]
got_rw
idle
next_state[2:0]
read_write_bit
reset
scl
scl_clk1
scl_clk2
scl_down
scl_driver
scl_up
sda
sda_clk1
sda_clk2
sda_driver
start
starting
state_o[2:0]
stopping
trans
transfer
translate
translate_hit
translated_addr[6:0]
addr[6:0]
i[31:0]
rw
b