







Cloud based Analog IC Design Hackathon

This is to certify that

Debjit Batabyal

from

Indraprastha Institute of Information Technology, Delhi

has designed the circuit

Memory Read operation using 6T SRAM cell and Conventional Latch type Sense Amplifier

using Synopsys Custom Compiler Platform
She/He has performed an Outstanding/Excellent/Very Good/Good-work.

This program was conducted between 15 February - 1 March 2022 as an initiative of IIT Hyderabad, which has been sponsored by Synopsys in association with VLSI System Design (VSD) Pvt.

Dr Ashudeb Dutta

Program Co-Ordinator, IIT Hyderabad

Dr B Umashankar Chair CCE, IIT Hyderabad

Jacamashanker