Memory Read operation using 6T SRAM cell and Conventional Latch type Sense Amplifier

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***Abstract*—Integrated SRAMs take about 70 percent of the chip area in SoCs. SRAM constitute of 6T cell which is the functional single bit storage element. Sense Amplifiers along with the latching circuit are present in the IO region of the memory unit used to complete the read operation of a SRAM cell. In this paper the read operation of memory composed of SRAM cell is described.**

I. Reference Circuit Details and Working

The reference circuitry consist of SRAM cell connected to bitlines. Bitlines are connected to the precharge circuit and pass gates of sense amplifier. The sense amplifier consist of a precharge circuit as well to preset the internal nodes to logic 1 before every read operation. The internal nodes of Sense Amplifier is connected to latching circuit that produces the final output of read operation.

Before the wordline comes, bitlines are precharged to Vdd. After the WL comes the BL/BLB discharges, depending on which side logic 0 is stored that side's Bitline discharges. The differential across the bitlines is also propagated to the internal nodes of sense amplifier. After sufficient discharge takes place the Sense Enable signal is taken high, which decouples the bitlines from the internal nodes of sense amplifier and turns ON the footer NMOS discharging the internal nodes. Through a positive feedback the internal nodes are resolved to 1 and 0 based on the differential polarity. The latching circuit completes the read operation by taking D_{out} to 1/0 based on the data stored in the cell. Before the next read operation internal nodes and bitlines are again precharged to Vdd.

II. Targeted Specification

The target design specification of the proposed design is as follows:

Parameters	Specification
Operating Voltage	1 V
SEN-Q Latch Delay (Read 0)	150 ps
SEN-Q Latch Delay (Read 1)	150 ps
Bitline Load	100 fF
Estimated Area of SRAM cell (28nm)	1 um sq
Estimated Area of Sense Amplifier and Latching Circuit (28nm)	20 um sq

III. Reference Circuit Diagram and Waveforms

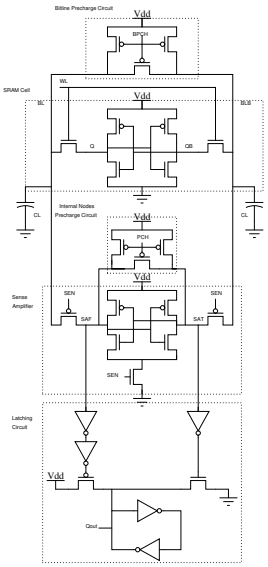

Fig. 1: 6T SRAM cell and Sense Amplifier

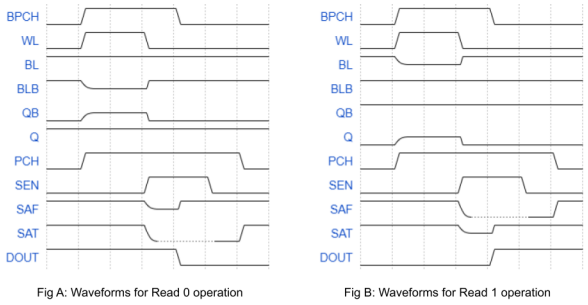

Fig. 2: Waveforms for Read 1 and Read 0

References

[1] A. Saxena et al., "Design Of High Density Memory Cell Library For Low Voltage Operation In 65nm LSTP Technology," 2021 IEEE 18th India Council International Conference (INDICON), 2021

[2] V. Patil, A. Grover and A. Parashar, "Design of Sense Amplifier for Wide Voltage Range Operation of Split Supply Memories in 22nm HKMG CMOS Technology," 2020 33rd International Conference on VLSI Design and 2020 19th International Conference on Embedded Systems (VLSID)