Memory Read operation using 6T SRAM cell and Conventional Latch type Sense Amplifier

Debjit Batabyal
Indraprastha Institute of Information Technology Delhi
28th February, 2022
debjit20318@iiitd.ac.in

***Abstract*—SRAMs take about 70 percent of the chip area in SoCs. SRAM constitute of 6T cell which is the functional single bit storage element. Sense Amplifiers along with the latching circuit are present in the IO region of the memory unit used to complete the read operation of a SRAM cell. In this paper the read operation of memory composed of SRAM cell is described.**

I. Circuit Details and Working

For demonstrating the memory read operation, 6T SRAM cell is connected to a conventional last type sense amplifier via bitlines with a load of 100 fF representing the load of a column of bitcells . First, for demonstrating read 1, Node Q of the SRAM cell is initialized to a logic 0 which results in the discharge of BL and thus the offset appears at the SAF node of the sense amplifier. As soon as SEN (Sense Enable) signal is taken high SAF node discharges and SAT node is taken to VDD resulting in DOUT node to a logic 1.

Similarly, for demonstrating the read 0 operation, QB node of the SRAM cell is initialized to the logic 0 which leads to the discharge of it BLB, Therefore the offset appears at the SAT node of the sense amplifier as soon as the SEN signal is taken high, the SAT node discharges SAF node is taken to VDD. Resulting in DOUT node of the latch to a logic 0. The DOUT node of the latch is connected to a buffer to drive a higher Output load of 10 fF.

II. Targeted Specification

The target design specification of the proposed design is as follows:

Parameters	Specification
Operating Voltage	1 V
SEN-Q Latch Delay (Read 0)	50.5 ps
SEN-Q Latch Delay (Read 1)	63 ps
Bitline Load	100 fF
Output Load	10 fF
Area of SRAM cell (28nm) (Based on device sizing)	1 um sq
Area of Sense Amplifier and Latching Circuit (28nm) (Based on device sizing)	20 um sq

III. Reference Circuit Diagram and Waveforms

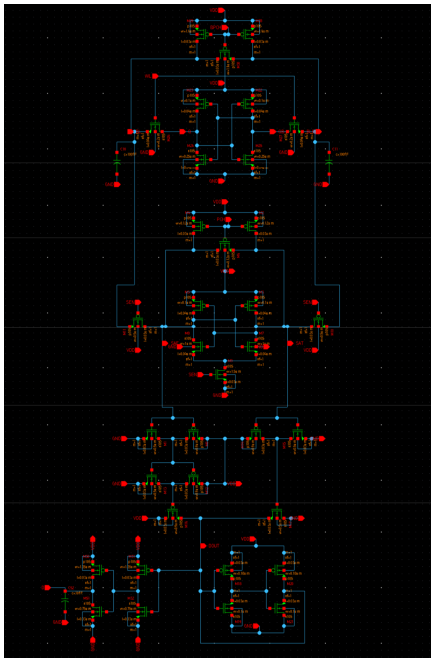

Fig. 1: 6T SRAM cell and Sense Amplifier

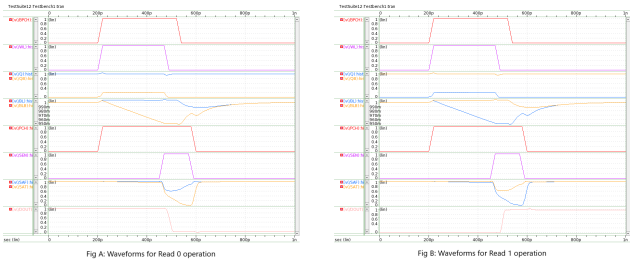

Fig. 2: Waveforms for Read 1 and Read 0

References

[1] A. Saxena et al., "Design Of High Density Memory Cell Library For Low Voltage Operation In 65nm LSTP Technology," 2021 IEEE 18th India Council International Conference (INDICON), 2021

[2] V. Patil, A. Grover and A. Parashar, "Design of Sense Amplifier for Wide Voltage Range Operation of Split Supply Memories in 22nm HKMG CMOS Technology," 2020 33rd International Conference on VLSI Design and 2020 19th International Conference on Embedded Systems (VLSID)