```
*  Generated for: PrimeSim
*  Design library name: deb_lib1
*  Design cell name: comparator
*  Design view name: schematic
.lib '/PDK/SAED_PDK32nm/hspice/saed32nm.lib' TT

*Custom Compiler Version S-2021.09
*Sun Feb 20 08:44:45 2022

.global gnd!
********************************************************************************
* Library         : deb_lib1
* Cell            : comparator
* View            : schematic
* View Search List : hspice hspiceD schematic spice veriloga
* View Stop List   : hspice hspiceD
********************************************************************************
xm3 net30 net30 net57 net57 p105 w=0.1u l=0.03u nf=1 m=1
xm20 vout net18 net57 net57 p105 w=0.5u l=0.03u nf=5 m=1
xm9 net37 net37 net57 net57 p105 w=0.1u l=0.03u nf=1 m=1
xm0 net18 net37 net57 net57 p105 w=0.1u l=0.03u nf=1 m=1
xm8 net23 net30 net32 net32 n105 w=0.1u l=0.03u nf=1 m=1
xm7 net30 net30 net32 net32 n105 w=0.1u l=0.03u nf=1 m=1
xm6 vout net30 net32 net32 n105 w=0.1u l=0.03u nf=1 m=1
xm5 net37 gnd! net23 net23 n105 w=0.1u l=0.03u nf=1 m=1
xm4 net18 net53 net23 net23 n105 w=0.1u l=0.03u nf=1 m=1
c12 vout gnd! c=100f
v18 net32 gnd! dc=-1.05
v15 net57 gnd! dc=1.05
```

v17 net53 gnd! dc=0 ac=1.05 sin (0 600m 1k 0 0 0)

.tran '0.1u' '5m' name=tran

.option primesim_remove_probe_prefix = 0

.probe v(*) i(*) level=1

.probe tran v(vout) v(gnd!) v(net53)

.temp 25

.option primesim_output=wdf

.option parhier = LOCAL

.end