ECE 469
Lab Report - 4

Debojyoti Mazumdar[1] and Sebastian Armstrong[2]

[1]Electrical and Computer Engineering, UIUC
[2]Electrical and Computer Engineering, UIUC

***Abstract*—Two labs were conducted focusing on real components. Lab 7 delved into the modeling of parasitics in capacitors and inductors. Furthermore, in Lab 8, the *Power Board* is introduced and used to demonstrate loss in MOSFET switches.**

I. Introduction

THIS lab report focuses on understanding non-ideal aspects of passive components and switches. When designing practical power converter circuits, we must reconcile with real devices–such as parasitics and lossy switches. These considerations are important whenever efficiency is a concern. Not only does loss result in poorer utilization of energy resources, it also creates heat which impairs the reliability and the power density of our devices. Lab 8 discusses the power loss in MOSFET switches further. Furthermore, parasitics should be taken into account. As will be shown in lab 7, under certain circumstances a capacitor can behave like an inductor and vice-versa.

II. Lab 7 Theory

Real inductors and capacitors exhibit parasitic effects. We can model a capacitor using the following equivalent circuit, shown in Fig. 1.

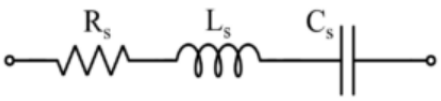

Fig. 1: Model for a capacitor using series connected parasitic elements. R_s is the effective series resistance and L_s is the effective series inductance. Source: [1]

Based on the circuit model in Fig. 1, the equivalent impedance of the capacitor is given by,

$$Z_c = R_s + j\omega L_s - \frac{j}{\omega C}$$

Likewise, a real inductor can be modeled by the circuit shown in Fig. 2.

Based on Fig. 2, the equivalent impedance of the inductor is,

$$\begin{aligned} Z_L &= R_s + \frac{1}{1/Z_c + 1/Z_L} \\ &= R_s + \frac{j}{\frac{1}{\omega L} - \omega C} \end{aligned}$$

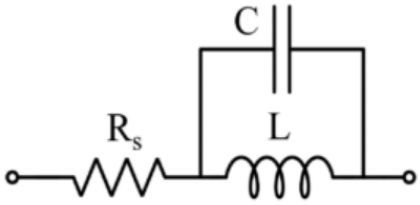

Fig. 2: Model for an inductor using a series parasitic resistor R_s and parallel parasitic capacitor C_p. Source: [1]

Note that in both of the equations above, we can consider two parts of the impedance: the real part (effective resistance) and the imaginary part (reactance). The resonant frequency, ω_r, occurs when the inductive reactance and capacitive reactance effectively cancel each other. In the case of the capacitor, the imaginary part cancels to zero:

$$\begin{aligned} \text{Im}\{Z_c\} = \omega_r L_s - \frac{1}{\omega_r C} &= 0 \\ \omega_r L_s &= \frac{1}{\omega_r C} \\ \omega_r &= \frac{1}{\sqrt{L_s C}} \end{aligned}$$

Similarly, for the inductor model, the terms in the *denominator* of $\text{Im}\{Z_L\}$ cancels out to zero, and this results in the equivalent reactance tending towards a very large value:

$$\begin{aligned} \text{Im}\{Z_L\} &= \frac{1}{\frac{1}{\omega L} - \omega C} \\ \frac{1}{\omega_r L} &= \omega_r C \\ \omega_r &= \frac{1}{\sqrt{L_s C}} \\ \text{Im}\{Z_L\}|_{\omega_r} &\to \infty \end{aligned}$$

III. Discussion of Lab 7

A. Lab 7 methods

The objective of this lab was the estimate the parasitic device parameters for a number of capacitors and an inductor. The following devices were tested:

- 300 μH inductor
- 470 μF electrolytic capacitor (polarized)
- 470 pF ceramic capacitor

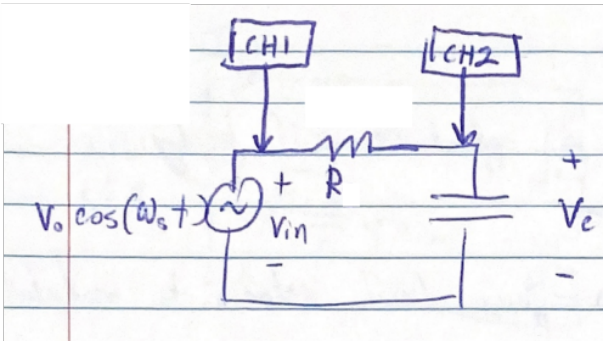

Fig. 3: Circuit diagram of experiment setup. The voltage divider resistor R was varied depending on the test device. When tested, the 300 μH inductor replaced the capacitor in the circuit. CH1 measured the input voltage and CH2 measured the output voltage.

- 15 μF tantalum capacitor (polarized)

To eventually estimate R_s and L_s, each device under test was connected in a voltage divider circuit, as shown in Fig. 3

A function generator was used to provide sinusoidal excitation. For polarized capacitors (which do not accept a negative voltage), the function generator was set to 10 V peak-to-peak and 5 V DC offset. For the remaining non-polarized devices, the DC offset was set to zero.

The voltage divider resistance used to test each device was as follows:

- $R = 100\ \Omega$ for 470 μF and 15 μF capacitors.
- $R = 1\ k\Omega$ for 300 μH inductor and 470 pF capacitor.

Due to the voltage-divider configuration, the impedance of device affected the resulting output voltage magnitude and phase.

The voltage divider equation is given by,

$$V_c = V_{in} \frac{Z}{R + Z}$$

where V_c and V_{in} are phasor quantities.

To collect a wide range of data, the frequency of the function generator was varied over the range 100 Hz to 30 MHz. At least eight frequencies were tested with each device.

Lastly, as an addition point of comparison, an LCR meter was used to measure device parameters.

B. Lab 7 results

1) example waveforms captured on oscilloscope: In total, thirty-five waveforms were captured using the oscilloscope. These waveforms correspond to 8 operating points for the 15 μF capacitor, 11 points for 470 pF capacitor, 8 points for 470 μF capacitor, and 8 points for the 300 μH inductor. Selected waveforms for each device are shown in Figures 4, 5, 6, and 7.

2) Calculation of equivalent impedance from scope data: The equivalent impedance of the device under test can be calculated using the scope data. The known or measured quantities include: the magnitudes of V_{in} and V_c, the value of the divider resistance R, and the phase shift between the

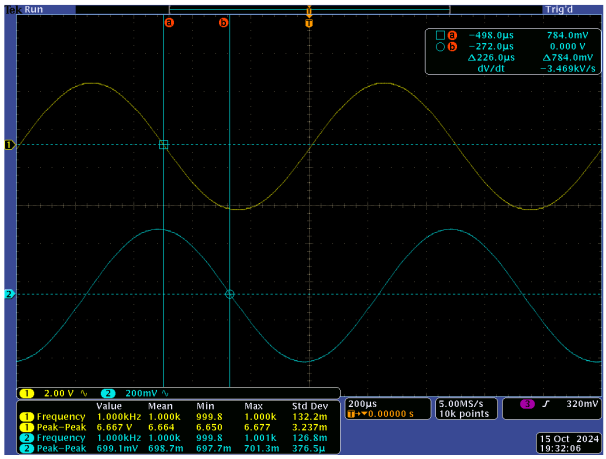

Fig. 4: 15 μF capacitor excited at 1 kHz. At this frequency, the device acts like a capacitor. CH1 is V_{in}, CH2 is V_c.

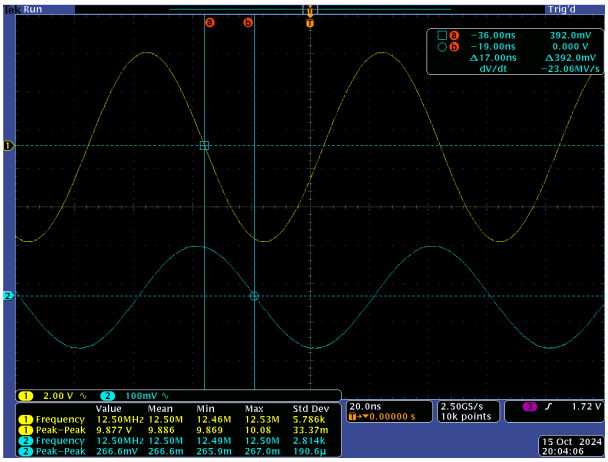

Fig. 5: 470 pF capacitor excited at 12.5 MHz. Note that even at this frequency, the impedance remains capacitive-like, as indicated by V_c leading V_{in}. CH1 is V_{in}, CH2 is V_c.

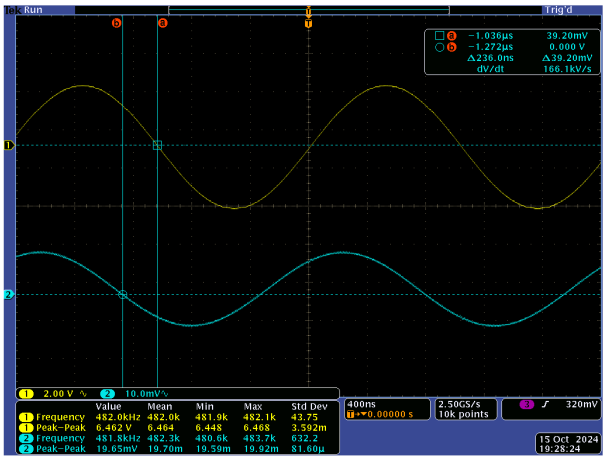

Fig. 6: 470 μF capacitor excited at 482 kHz. This frequency is above the 23.8 kHz resonant frequency for this device. Here the ESL dominates and the device acts like an inductor. CH1 is V_{in}, CH2 is V_c.

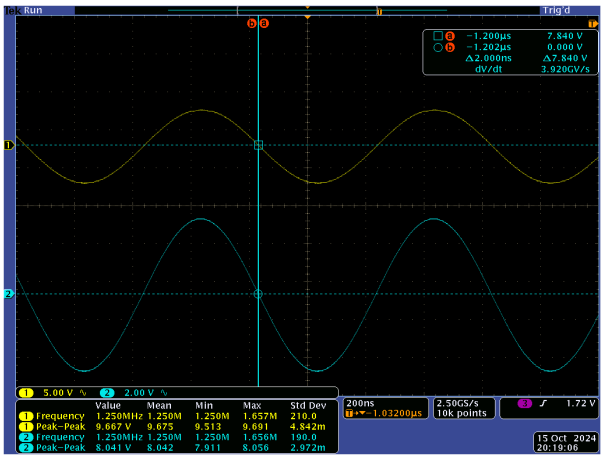

Fig. 7: 300 μH inductor excited at 1.25 MHz. This frequency corresponds to resonance for the inductor, as indicated by the near zero phase lag between V_c and V_{in}. CH1 is V_{in}, CH2 is V_c.

two voltages. Re-arranging the voltage divider formula and solving for the impedance, Z, of the device under test gives,

$$Z = \frac{R}{V_{in}/V_c - 1}$$

Note that V_{in} and V_c are phasor quantities. We assume that $\angle V_{in} = 0$ whereas $\angle V_c$ depends on the phase shift measured using the scope cursors.[1]

If we define the time shift Δt measured on the scope as the difference between the zero crossing of $v_c(t)$ minus that of $v_{in}(t)$, then Δt will be positive whenever V_{in} leads V_c. The relative phase shift, ϕ, between V_{in} and V_c will given by,

$$\phi = -\omega \Delta t$$

where $\omega = 2\pi f$. The negative sign arises so that $V_c \angle \phi$ for $\phi > 0$ corresponds to V_c leading V_{in}. Bode plot results for impedance corresponding to the four test devices are shown in Figures 8, 9, 10, and 11.[2]

3) Calculating ESL and ESR model parameters from scope data: Using the aforementioned plots of impedance vs frequency, the ESL and ESR parameters for the devices can be approximated. To determine the equivalent series inductance (ESL, or L_s) for the capacitors, we can use the measured resonant frequency. Re-arranging the equation for ω_r and solving for L_s gives,

$$L_s = \frac{1}{\omega_r^2 C}$$

Table I shows the resonant frequency found for each capacitor in addition to the corresponding ESL value.[3]

At any given frequency, the equivalent series resistance (ESR, or R_s) can be determined from inspecting the real part of Z.

$$R_s = \text{Re}\{Z\} = \text{Re}\{|Z|e^{j\phi}\} = |Z|\cos\phi$$

[1]Answer to study question 1-lab7
[2]These figures answer study question 2-lab7
[3]Table answers study question 3-lab7

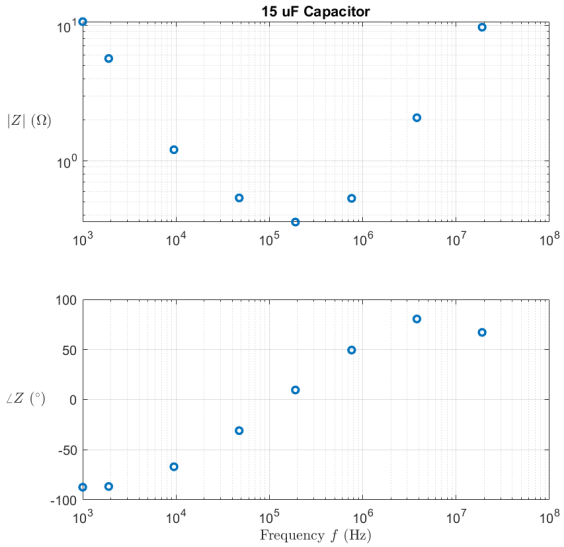

Fig. 8: Impedance Bode plot for 15 μF capacitor.

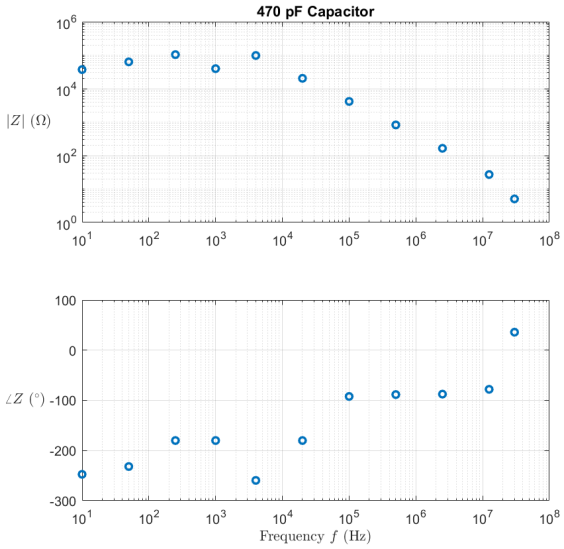

Fig. 9: Impedance Bode plot for 470 pF capacitor.

Using the magnitude and phase data for Z, R_s was calculated for each device at (approximately) their resonant frequency and at $f = 1$ kHz. In some cases, a negative resistance was suggested by the fact that $|V_c| > |V_{in}|$ (by a small difference, less than 1 V). However, these readings do not match the theoretical model for a voltage divider and were assumed to be caused by measurement or calibration error. R_s was assumed positive in all cases. ESR results are shown in Table II.

TABLE I: Calculated ESL for the three capacitors.

device value	f_r	L_s
15 μF	190 kHz	46.78 nH
470 μF	23.8 kHz	95.15 nH
470 pF	30 MHz	59.88 nH

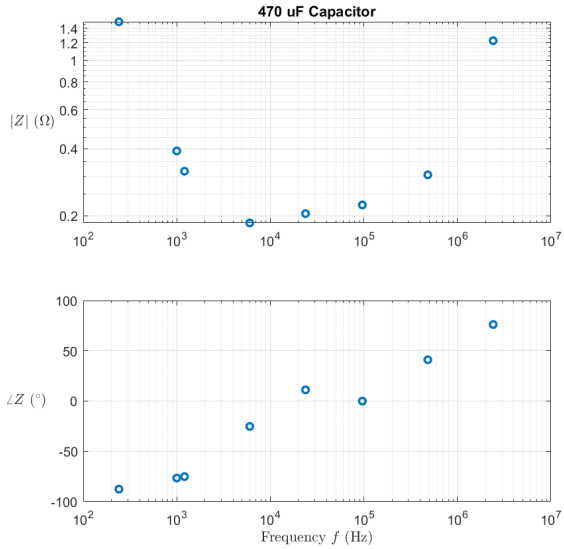

Fig. 10: Impedance Bode plot for 470 μF capacitor.

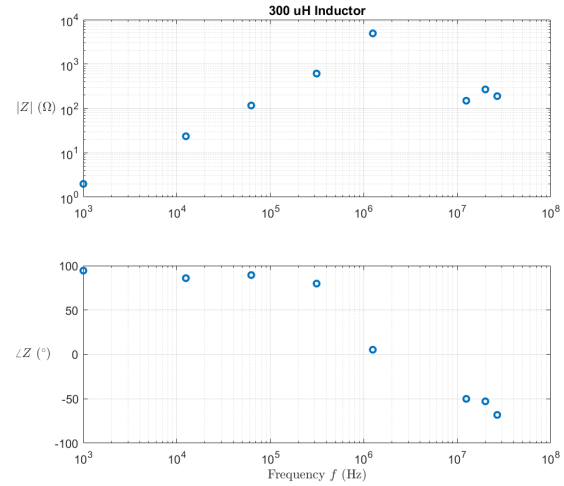

Fig. 11: Impedance Bode plot for 300 μH inductor.

4) Measurements taken with LCR meter: Tables III and IV show the measured parameters for the four test devices and two voltage-divider resistors respectively.

The values for R_s as measured with the LCR meter were compared to those calculated using the Bode plot data at $f =$ 1 kHz. The results of this comparison are shown in Table V. The Bode plot approach seems to largely overestimate the parasitic resistance R_s, as indicated by the large percentage errors. The estimated resistance has highest agreement for the 15 μF capacitor.[4]

TABLE III: Measured device parameters for inductor and capacitors using LCR meter.

	300 μH	470 μF	15 μF	470 pF
C_p	-87.15 μF	448 μF	15.03 μF	418.2 pF
L_s	290.69 μH	-72.3 μH	-1.68 mH	-60.8 H
R_s	0.2 mΩ	7 mΩ	0.357 Ω	12.5 kΩ
R_p	100 kΩ	3.72 Ω	314.5 Ω	11.5 MΩ
D	0.00003	0.124	0.0336	0.032

TABLE IV: LCR meter measured parameters for resistors used in voltage divider.

	1 kΩ	100 Ω
C_p	36 pF	1.67 nF
L_s	-35.3 μH	-16.5 μH
R_s	992.8 Ω	99.4 Ω
R_p	992.8 Ω	99.4 Ω

[4]Answer to study question 4-lab7

TABLE II: Calculated ESR values at 1 kHz and near resonant frequency.

device value	f_r	R_s at 1 kHz	R_s at f_r
15 μF	190 kHz	0.486 Ω	0.35 Ω
470 μF	23.8 kHz	0.091 Ω	0.2 Ω
470 pF	30 MHz	39.6 kΩ	4.11 Ω
300 μH	1.25 MHz	0.15 Ω	4.89 kΩ

TABLE V: Comparison of R_s values calculated using Bode plots and measured via LCR meter. All entries in units of Ω.

	R_s (LCR)	R_s (Bode @ 1 kHz)	% error
300 μH	2.00E-04	0.15	74900%
470 μF	7.00E-03	0.091	1200%
15 μF	0.357	0.486	36%
470 pF	1.25E+04	3.96E+04	217%

IV. Discussion of Experiment-8

In lab-8, we made the power board.

A. Theory

1) Conduction loss: This occurs due to the fact that the voltage drop across a real semi-conductor switch is never zero. So, when the current flows through the switch, there would be some on-state loss called the conduction loss. The amount of power lost during conduction of the switch (P_{cond}) is shown in equation-(1).

$$P_{cond} = V_{on} \times I_{on} \tag{1}$$

Where, V_{on} is the on-state voltage drop across the MOSFET and I_{on} is the current flowing through the MOSFET when the MOSFET is on.

2) Switching loss: This occurs when the switch is turning on and turning off. This occurs because the current and the voltage across the switch during the turn-on and turn-off will be non-zero. This results in a huge amount of power lost across the switch during the turn-on and turn-off operation. The amount of energy lost during turn-on and turn-off is given by the equation-2 and 3.

$$E_{sw-on} = \frac{V_{ds} \times I_d}{2} \times t_{on} \tag{2}$$

$$E_{sw-off} = \frac{V_{ds} \times I_d}{2} \times t_{off} \tag{3}$$

Where, V_{ds} is the voltgae across the MOSFET when the MOSFET is OFF, I_d is the current flowing through it when the MOSFET is ON, t_{on} is the turn-on time of the MOSFET and t_{off} is the turn-off time of the MOSFET. The power lost during the turn-on and turn-off is given by equation-

$$P_{sw-on} = E_{sw-on} \times f_{sw} \tag{4}$$

$$P_{sw-off} = E_{sw-off} \times f_{sw} \tag{5}$$

Where, f_{sw} is the switching frequency of the MOSFET. As can be seen from the equation, the power lost across the MOSFET during turn-on and turn-off increases with increase in switching frequency (f_{sw}).

3) Effect of change of gate resistance on switch loss: The voltage across across the MOSFET and current flowing through the MOSFET during tunr-on and tunr-off is shown in Figure-().

As can be seen from the Figure-(), the turn-on and turn-of time of the MOSFET increases with increase in gate resistance. This would result in higher energy lost across the MOSFET as shown in equation-(2) and (3).

Symbol	Description	Value
$R_{\theta JC}$	Junction to case thermal resistance	2.7 °C/W
$R_{\theta JA}$	Junction to Ambient thermal resistance	65 °C/W

TABLE VI: Table for the different thermal resistances of according to the datasheet of the MOSFET.

4) Estimation of losses using the thermal model: From the datasheet of the MOSFET we found the thermal resistances as shown in Table-VI.

From this table of data, we can calculate the thermal resistance between the case and ambient ($R_{\theta CA}$).

$$\begin{aligned} R_{\theta JA} &= R_{\theta JC} + R_{\theta CA} \\ \Rightarrow R_{\theta CA} &= R_{\theta JA} - R_{\theta JC} \\ \Rightarrow R_{\theta CA} &= 65 - 2.7 = 62.3°C/W \end{aligned}$$

To estimate the value of the thermal resistance between the case and the ambient ($R_{\theta CA}$), we use equation-(6).

$$R_{\theta CA} = \frac{T_C - T_A}{P_{loss}} \tag{6}$$

Where, T_C is the temperature of the case and T_A is the ambient temperature. To estimate the temperature of the junction based on the temperature of the case, we use equation-(7).

$$\begin{aligned} T_J &= T_C + R_{\theta JC} P_{loss} \\ \Rightarrow T_J &= T_C + 2.7 \times P_{loss} \end{aligned} \tag{7}$$

Where, P_{loss} is the power lost across the switch. It is the sum of the power lost due to conduction and due to switching of the MOSFET.

B. Results

1) Conduction Loss in MOSFET: First we begin by measuring the conduction loss of the MOSFET. Table-VII gives the value of the voltage drop across the MOSFET (V_{ds}), inductor current (I_l) and the conduction loss (P_{cond}) calculated from it for the different cases of input voltage (V_{in}) and duty ratio (D) at a switching frequency (f_{sw}) of 100 kHz.

V_{in} (V)	D	f_{sw} (kHz)	V_{ds} (V)	I_L (A)	P_{cond} (W)
5	0.5	100	0.4	3.91	1.564
6	0.5	100	0.47	4.72	2.218
5	0.6	100	0.42	5.11	2.146

TABLE VII: Tabe for measurement of conduction loss (P_{cond}) for different cases.

Now we keep the input voltage (V_{in}) at 5 V and duty cycle (D) at 50 % and change the switching frequency (f_{sw}) and find the conduction loss (P_{cond}) for the different cases.

As we can see from the tables, the conduction loss changes with change in input voltage (V_{in}) and duty ratio (D) but does not change with switching frequency as expected from the equation-(1).

V_{in} (V)	D	f_{sw} (kHz)	V_{ds} (V)	I_L (A)	P_{cond} (W)
5	0.5	80	0.385	3.88	1.494
5	0.5	100	0.4	3.91	1.564
5	0.5	120	0.396	3.96	1.568

TABLE VIII: Table for measurement of conduction loss (P_{cond}) for different cases of switching frequency (f_{sw}).

2) Turn-Off Loss in MOSFET: Figure - 12 shows the scope shot of the gate source voltage (V_{gs}), switch node voltage (V_{sw}) and inductor current (i_L).

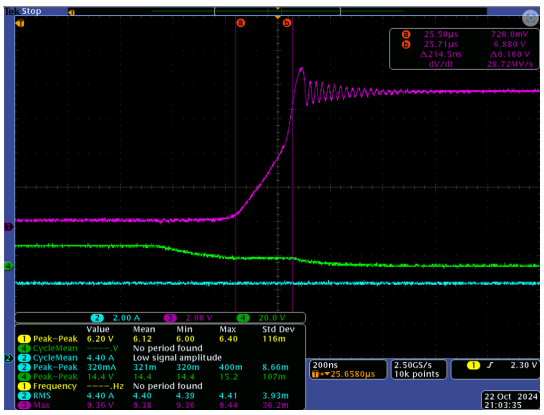

Fig. 12: Scope shot of V_{sw} (purple), V_{gs} (green) and i_L (blue).

From Figure-12, we see a lot of ringing in the switch node voltage (V_{sw}). Also, form the Figure-12, we see that the turn off time (t_{off}) is nearly 214.5 ns. The energy and power lost across the MOSFET during turn-off can be found using the equation-(3) and (5). Table IX shows the turn-off energy loss (E_{sw-off}) and turn-off power loss (P_{sw-off}) for the case of input voltage (V_{in}), duty ratio (D) and switching frequency (f_{sw}).

V_{in} (V)	D	f_{sw} (kHz)	E_{sw-off} (μJ)	P_{sw-off} (W)
5	0.5	100	4.4	0.44

TABLE IX: Table of E_{sw-off} and P_{sw-off} for the given conditions.

3) Turn-On Loss in MOSFET: Figure - shows the scope shot of the gate source voltage (V_{gs}), switch node voltage (V_{sw}) and inductor current (i_L).

From the Figure-13, we see that there is a huge ringing in the switch node voltage (V_{sw}). Also, form the Figure-13, we see that the turn-on time (t_{on}) is 130.5 ns. So, the turn-on time (t_{on}) is much less than the turn-off time (t_{off}). Table X shows the turn-on energy loss (E_{sw-on}) and turn-on power loss (P_{sw-on}) for the case of input voltage (V_{in}), duty ratio (D) and switching frequency (f_{sw}).

V_{in} (V)	D	f_{sw} (kHz)	E_{sw-on} (μJ)	P_{sw-on} (W)
5	0.5	100	4.4	0.268

TABLE X: Table of E_{sw-on} and P_{sw-on} for the given conditions.

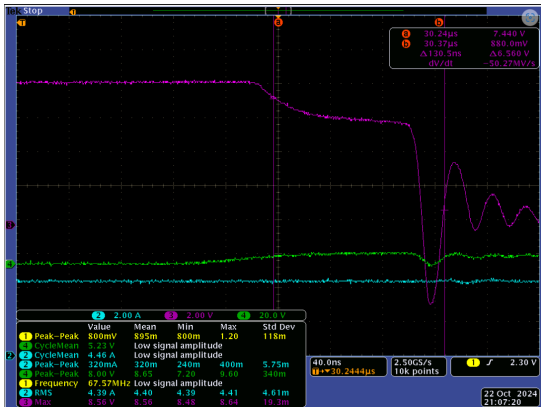

Fig. 13: Scope shot of V_{sw} (purple), V_{gs} (green) and i_L (blue).

4) Effect of gate resistance on conduction loss: Without the gate resistance we get a maximum voltage of 14.5 V. After applying a gate resistance of 47.2Ω the maximum voltage during ringing decreases to 9.36 V.

Figure- and shows the switch node voltage (V_{sw}), inductor current (i_L) and gate source voltage (V_{gs}) during turn-off and turn-on respectively. Table - shows the energy and power lost during turn-on and turn-off respectively.

5) Estimation of losses using thermal model: Figure-14 show the thermal image of the MOSFET. We see that the temperature of the MOSFET is 42.2 °C.

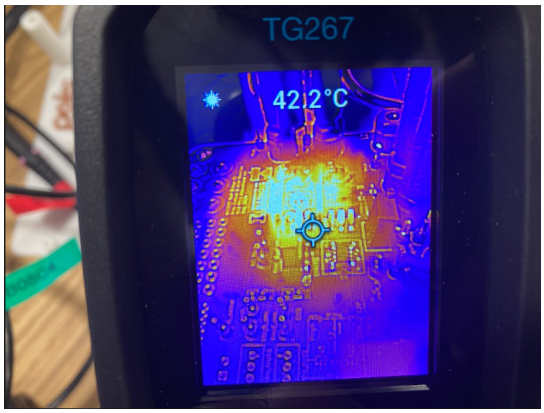

Fig. 14: Thermal Image of the MOSFET.

Table gives the values of the power loss (P_{loss}), case temperature (T_C) and the ambient temperature (T_A) for the case of switching frequency (f_{sw}) of 100 kHz, duty ratio (D) of 0.5 and input voltage (V_{in}) of 5 V.

P_{loss} (W)	T_C (°C)	T_A (°C)
2.208	42.2	25

TABLE XI: Table of E_{sw-on} and P_{sw-on} for the given conditions.

Using equation-(6), we can estimate the thermal resistance between the case and the ambient as 7.79 °C/W. This is much

less than the value from the datasheet. But this is fine because the datasheet mentions it to be the maximum value. Using equation-(7), we estimate the junction temperature as 48.16 °C. This is much less than 175 °C. The hottest part of the board is the MOSFET area. This is because MOSFETs have swiching losses which are much higher than any other parasitic losses in the entire power board.

V. Conclusion

Overall this lab explored real components and switching devices. We learned how to estimate the non-ideal aspects of passive components as well as power loss in MOSFET switches. Construction of the power board was a great learning experience; we gained knowledge of surface mount devices, gate drivers, and tuning gate resistances.

References

[1] ECE 469 lab manual