

ECE 469

Final Project Report

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Abstract—This project involves the design of a rectifier to meet the output voltage and its ripple specs for a range of load power drawn. We were tasked with designing a rectifier to give an average output voltage of 13 V with the ripple of the output voltage being less than 2 V peak-to-peak. This condition should be met for a load power of 0 to 70 W. For this, we implemented a diode bridge rectifier cascaded with a buck converter whose duty cycle will be controlled using the output voltage to provide the closed loop control.

I. INTRODUCTION

THIS project explores the different topologies to provide a very low ripple at the output for a range of output power of 0 to 70 W. We reviewed several different rectifier topologies. The following sections elaborate on the design, simulation, and verification of design on hardware.

II. TOPOLOGY DESIGN

A. Topology Selection

We chose a design which is a single phase full bridge diode rectifier with a buck converter cascaded with it. The circuit diagram is shown in Figure-1.

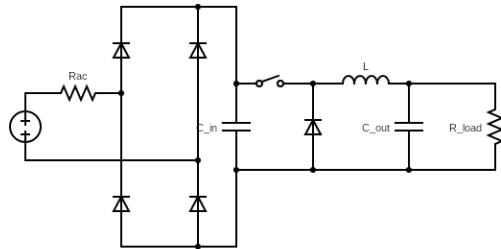


Fig. 1: Circuit Diagram of the Rectifier design.

To meet the ripple specs, we were required to use a closed loop control scheme to control the duty cycle of the buck converter. The complete schematic is as shown in Figure-2.

1) *Reason for using Buck converter:* We started with the simplest form of a rectifier, the single-phase full bridge diode bridge rectifier with a capacitor at the output. The schematic is shown in Figure-3.

But the problem of this topology is that the average output voltage changes for different load resistances, as shown in Figure-4.

So, we would meet the output average voltage spec for some pair of output capacitance and load resistance. This would also

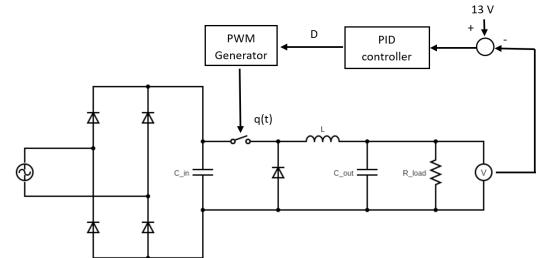


Fig. 2: Complete schematic of the rectifier topology.

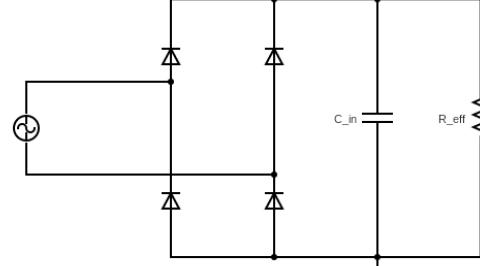


Fig. 3: Circuit Diagram of single-phase full bridge diode rectifier.

mean that the average output voltage spec would not be met for the entire output power range (0 to 70 W). So, we can use a buck converter to step-down the voltage generated in the output capacitor of the single-phase full-bridge diode rectifier (C_{in}) to 13 V at the output.

Another way to look at the buck converter circuit is to consider the effective resistance at the input of a buck converter. Consider Figure-5 of the buck converter.

The effective resistance (R_{eff}) seen at the input of the buck

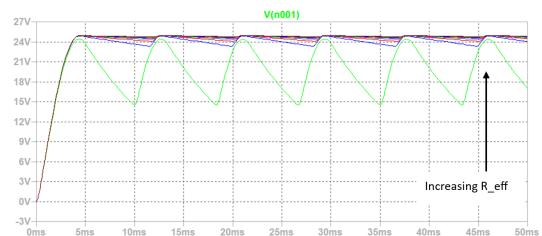


Fig. 4: Plot of the output voltage of the single-phase full bridge diode rectifier for increasing load resistance.

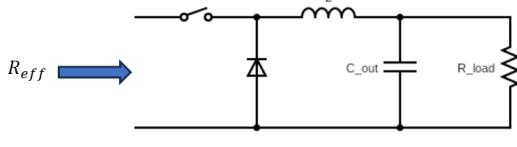


Fig. 5: Circuit Diagram of Buck converter.

converter is given eq-(1) where D is the duty ratio of the buck converter switch.

$$R_{eff} = \frac{R_{load}}{D^2} \quad (1)$$

So, by controlling the duty ratio (D), we can control the effective resistance (R_{eff}) seen by the full bridge rectifier, so that the required output power ($P_{out} \in [0, 70]$) is delivered to the output.

2) *Reason for using closed loop control:* Implementing a closed-loop control further reduces the ripple generated in the output voltage. This reduces the burden on the capacitors and inductors of the circuit to meet the ripple specs.

B. Component Selection

1) C_{in} : This controls the amount of ripple voltage that will be sent into the buck converter. Consider just the full-bridge diode rectifier as shown in Figure-3. The ripple in output voltage is as shown in the plot in Figure-6.

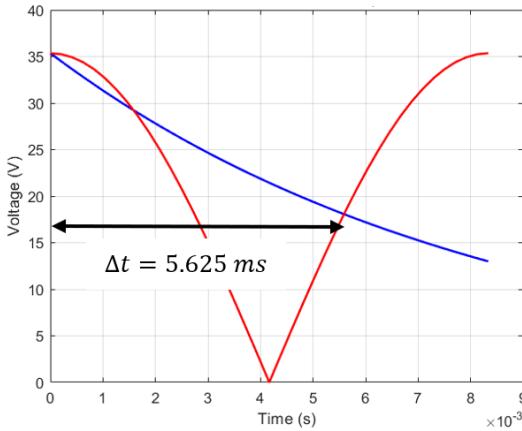


Fig. 6: Plot of the voltage just after diode bridge rectification and voltage across C_{in}

The capacitor voltage decays through R_{eff} . The circuit is as shown in Figure-7.

The equation of the ripple in the voltage across C_{in} is ΔV and is given by the equation-2 .

$$\Delta V = (V_{AC})_{peak} \left(1 - e^{-\frac{\Delta t}{R_{load} C_{in}}}\right) \quad (2)$$

As we are using a buck converter, the input voltage to the buck converter must be more than 13 V so that the buck converter can step it down to 13 V. So, this sets the maximum

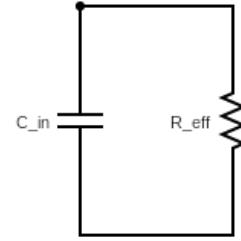


Fig. 7: Capacitor C_{in} discharge circuit.

ΔV to $(25\sqrt{2}) - 13$ V. From Figure-6, we can see that $\Delta t = 5.625$ ms. To obtain the minimum value of C_{in} , we need to set the minimum value of R_{eff} . From equation-1, we can say that $R_{eff} \in [R_{load}, \infty)$. The minimum value of R_{load} occurs at the maximum output power of 70 W.

$$(R_{load})_{min} = \frac{13^2}{(P_{load})_{max}} = 2.414\Omega$$

Using all these values, we get C_{in} to be a minimum of 1.33 mH. For this we are using three 470 μ F capacitors in parallel.

2) L : This value determines whether the buck converter operates in Discontinuous conduction mode (DCM) or Continuous Conduction Mode (CCM). We will be operating our buck converter in CCM mode. The plot for the inductor current in CCM mode of operation is as shown in Figure-8.

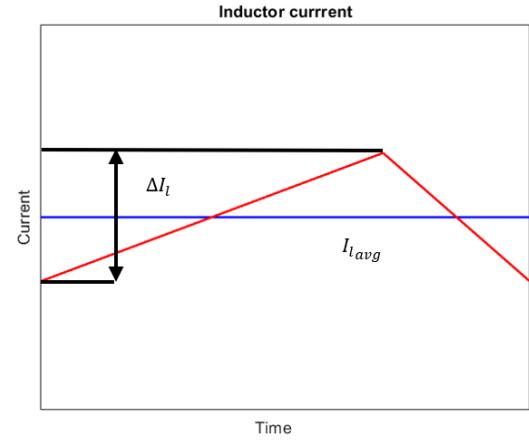


Fig. 8: Plot of inductor current.

From Figure-8 we can say that for the CCM operation of the buck converter, the current flowing through the inductor (i_L) must follow the rule in equation-3.

$$\frac{\Delta i_L}{2} \leq (i_L)_{avg} \quad (3)$$

Considering all the ripple current flows through the output capacitor (C_{out}) and only $(i_L)_{avg}$ flows through the load resistance (R_{load}), we have the following.

$$(i_L)_{avg} = \frac{13}{R_{load}}$$

To consider minimum average, we need to consider maximum load resistance. Ideally, the maximum load resistance (R_{load}) would be ∞ , but in reality we would use a bleed resistor so that the inductor can always be operated in CCM mode. The chosen value of the bleed resistor was 100Ω . Using this value, we get $((i_L)_{avg})_{min} = 0.13$ A. So, from equation-3 we can say that the maximum ripple in the current flowing through the inductor should be 0.26 A. The ripple on the inductor current is given by equation-4.

$$\Delta i_L = (1 - D) \frac{V_{out}}{L \times f_{sw}} \quad (4)$$

To obtain the maximum ripple on the current flowing through the inductor, we need to consider the minimum value of duty ratio (D). We know from the selection of the component C_{in} that the input voltage to the buck converter would be between $25\sqrt{2}$ V and 13 V. So, considering $25\sqrt{2}$ as the input voltage to the buck converter, we can say that the minimum value of the duty ratio of the buck converter would be as follows.

$$\begin{aligned} D_{min} &= \frac{13}{25\sqrt{2}} \\ &= 0.368 \end{aligned}$$

Then using this D_{min} , $V_{out} = 13$ V and a switching frequency (f_{sw}) of 50 kHz, we get the minimum value of L to be $632 \mu\text{H}$. For this we used a 2 mH inductor available in the lab for our design.

3) C_{out} : This value determines the voltage ripple that would be seen at the output of the buck converter for the given inductor current ripple (Δi_L). Figure-9 shows the current flowing through the capacitor. We calculate the charge transferred (ΔQ) to the capacitor in each cycle as shown in Figure-9.

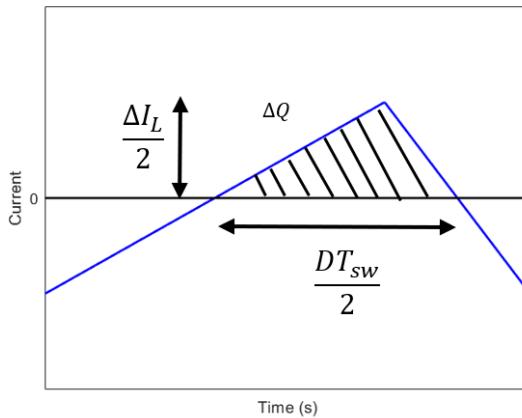


Fig. 9: Capacitor current

$$\begin{aligned} \Delta Q &= \frac{1}{2} \times \frac{\Delta I_l}{2} \times \frac{DT_{sw}}{2} \\ &= \frac{\Delta I_l DT_{sw}}{8} \end{aligned}$$

Using this we calculate the voltage ripple across the capacitor as follows.

$$\begin{aligned} \Delta V &= \frac{\Delta Q}{C} \\ &= \frac{\Delta I_l DT_{sw}}{8C} \end{aligned}$$

To find the absolute upper bound, we can use the maximum ΔI_l of 0.26 A and a D of 1. We consider D to be 1 to find the absolute upper bound limit. Considering the output ripple voltage to be less than 0.5 V (to be on the safe side) we get the minimum value of C_{out} to be $1.3 \mu\text{F}$. For this we are using the capacitors present on the board which is $47 \mu\text{F}$.

Table-I gives a summary of the component values calculated analytically and the values finally chosen to build the circuit.

Component	Analytical Value	Value used
C_{in}	greater than 1.33 mF	$3 \times 470 \mu\text{F}$
L	greater than $632 \mu\text{F}$	2 mH
C_{out}	greater than $1.3 \mu\text{F}$	$47 \mu\text{F}$

TABLE I: Table of component values calculated analytically and values finally chosen.

C. Inductor Design

Table-II shows the design specs that the inductor must meet.

Parameters	Value
L	$700 \mu\text{H}$
max current	5.35 A

TABLE II: Table of design specs to be met by the inductor.

We chose the core T-300A-26. The specs of the core are shown in Table-III.

Parameters	Value
Core	T-300A-26
B_{sat}	0.75 T
inductance per turns squared	160 nH
length of the magnetic path (l_c)	19.8 cm
Cross section area of core (A_c)	1.68 cm^2

TABLE III: Table of design specs to be met by the inductor.

1) Finding number of turns (N):

$$\begin{aligned} N &= \sqrt{\frac{700\mu}{160n}} \\ &= 94 \text{ turns} \end{aligned}$$

2) Finding B in the core:

Figure-10 shows the equivalent magnetic circuit of the inductor.

To calculate the magnetic reluctance of the core we do the following.

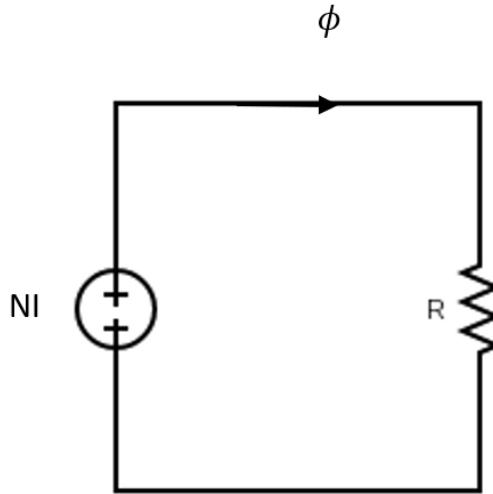


Fig. 10: Equivalent magnetic circuit.

$$R = \frac{1}{\mu_r \mu_0} \frac{l_c}{A_c}$$

$$= 12.505 \times 10^6 \text{ A-turns/ Wb}$$

Using this, we can find the maximum flux passing through the core (ϕ_{max}) as follows.

$$\phi_{max} = \frac{NI_{max}}{R}$$

$$= 39.79 \times 10^{-6} \text{ Wb}$$

Using this, we can find the maximum flux density of the core (B_{max}) when maximum current passes through the inductor.

$$B_{max} = \frac{\phi}{A_c}$$

$$= 0.236 \text{ T}$$

This value is less than the B_{sat} value of 0.75 T. So, the core would not get saturated when maximum current flows through the inductor.

3) *Choosing the wire:* From the data sheet, we found that using AWG-18 would suffice.

D. Simulation results

With the chosen component values, the circuit shown in Figure-11 was simulated in MATLAB SIMULINK. The closed loop simulation was carried out for the extreme cases of load condition and some intermediate load condition by considering the PID constants as $K_p = 1$, $K_I = 0.02$ and $K_d = 0.1$. Figure-12, Figure-13 and Figure-14 are the plots for the output voltage of the complete rectifier circuit along with closed loop control for the extreme cases of $R_{load} = 2.414\Omega$ ($P_{load} = 70$ W), $R_{load} = 100\Omega$ ($P_{load} = 1.69$ W) and $R_{load} = 50\Omega$ ($P_{load} = 3.38$ W). Table-IV gives the output average voltage

and ripple at the output voltage obtained for the mentioned load resistances.

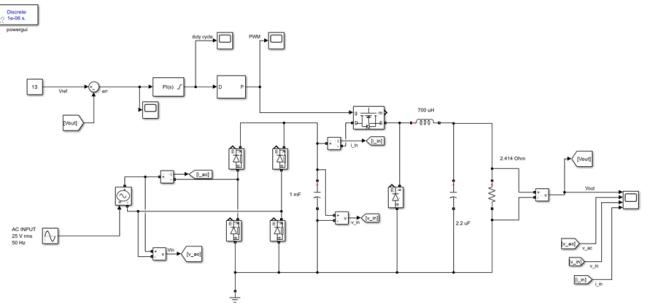


Fig. 11: Closed loop simulation circuit schematic.

R_{load}	average output voltage	output voltage ripple
2.414Ω	12.49 V	0.3 V
50Ω	13.51 V	1.6 V
100Ω	13.1 V	0.7

TABLE IV: Table of the average output voltage and ripple at the output voltage for different load resistances.

E. Modifications done after first testing

The entire calculations were done considering the input could supply at max of 15 A of current. However, the fuse in the input power supply could supply only a current of 3 A rms (4.2 A peak current). Due to this, we had to add an input resistance (R_{AC}) and NTC thermistors.

1) *Reason for using R_{AC} :* This would reduce the rms current drawn from the source. In this way, the fuse would remain safe.

2) *Reason for using NTC Thermistor:* NTCs have high resistance during the start (cold resistance) and then as the temperature of the NTC increases, the resistance of the NTC decreases (hot resistance). This is used to reduce the in-rush current of the capacitors to prevent the fuse from blowing up. Having NTCs instead of a higher R_{AC} would reduce the power lost in R_{AC} thereby increasing the power transferred to the load.

Choosing the values of R_{AC} and NTC as given in Table-V helps keep the in-rush current and the rms current drawn

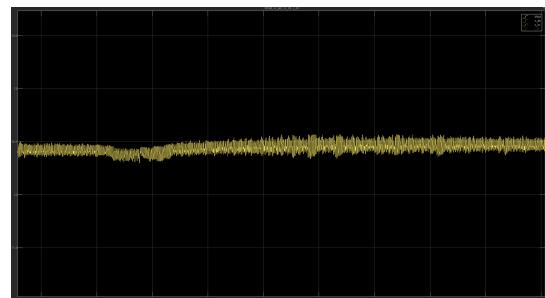


Fig. 12: Plot of the steady-state output voltage for $R_{load} = 2.414\Omega$ ($P_{load} = 70$ W).

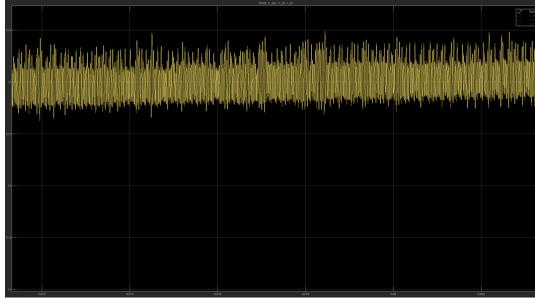


Fig. 13: Plot of the steady-state output voltage for $R_{load} = 100\Omega$ ($P_{load} = 1.69$ W).

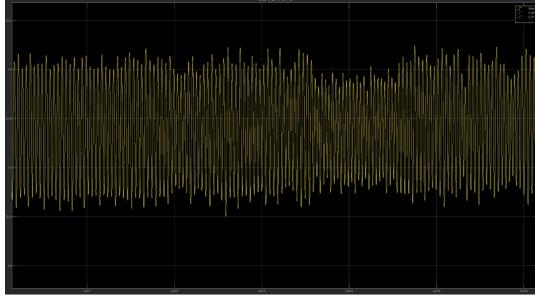


Fig. 14: Plot of the steady-state output voltage for $R_{load} = 50\Omega$ ($P_{load} = 3.38$ W).

from the input within the fuse limit as shown in Figure-14 and Figure-15.

Component	Value
R_{AC}	2
NTC (cold resistance)	9

TABLE V: Table of the values of R_{AC} and NTC.

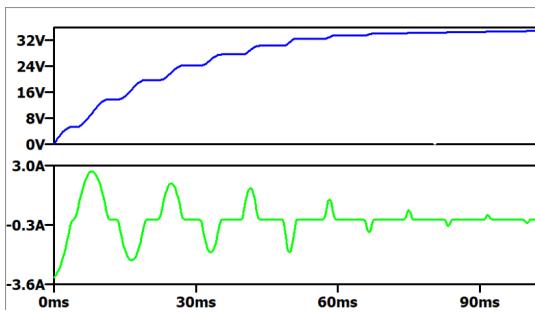


Fig. 15: Simulation result of Voltage across C_{in} (Blue) and input current drawn from the source (Green) for no-load case.

F. Problems with implementation of the modified circuit

1) *Problems associated with R_{AC} :* The presence of R_{AC} causes power being lost across it. This results in maximum output load power being delivered equal to 44.47 W.

2) *Problems associated with Arduino board:* The maximum sampling frequency of the arduino board is 1.5 KHz. This is slow compared to the required sampling frequency. This

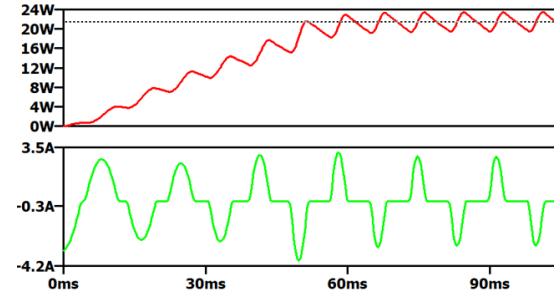


Fig. 16: Simulation result of Output power (Red) and input current drawn from the source (Green) for a load resistance of 40Ω .

results in the output voltage being as shown in Figure-17. This was proved by simulating the circuit topology shown in Figure-11 with a lower sampling frequency. The waveforms obtained after simulation is shown in Figure-18. This prevents us from implementing closed-loop control scheme to our circuit topology. This results in a larger ripple in the output voltage.

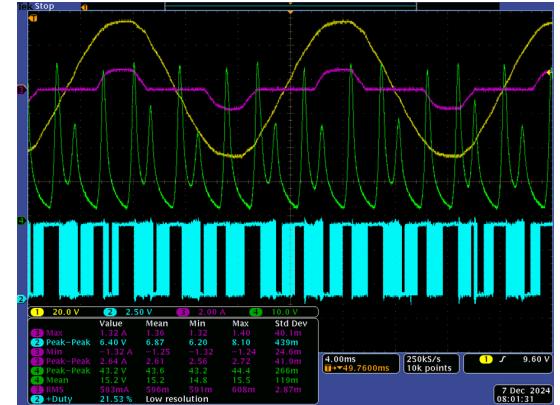


Fig. 17: Scope shot of the Output voltage waveform (Green), Input voltage waveform (Yellow), input current waveform (pink) and switching signal of the MOSFET ($q(t)$) (Teal).

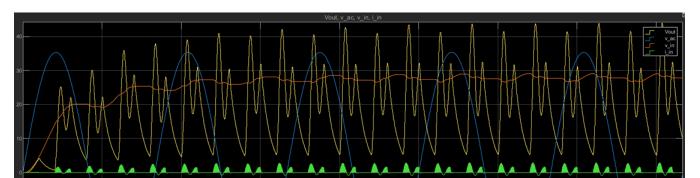


Fig. 18: Simulation result of the SIMULINK circuit with output voltage (Yellow), Input AC voltage (Blue), Voltage across C_{in} (Orange) and Input current from source (Green).

III. RESULTS

We assembled the circuit components as shown in Figure-22. We then performed individual tests on the rectifier and buck converter parts of the circuit.

A. Testing the rectifier part

We tested the rectifier part to check whether the in-rush current is within the limits of the fuse. Figure-19 and Figure-20 shows the waveforms obtained for the no-load and load resistance of $40\ \Omega$. The maximum values of the in-rush currents for both are shown in Table-VI. As can be seen from the values, they are within the fuse limit.

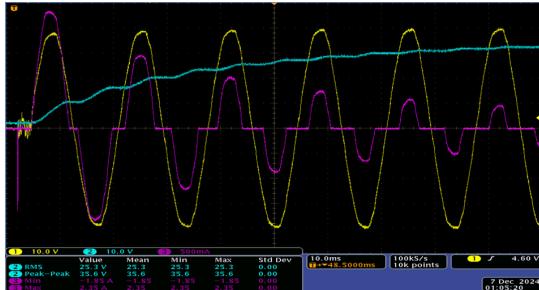


Fig. 19: Scope shot of the voltage across C_{in} (Teal), Input AC voltage (Yellow) and input current drawn from the source (Pink) for the rectifier part of the circuit with no-load.

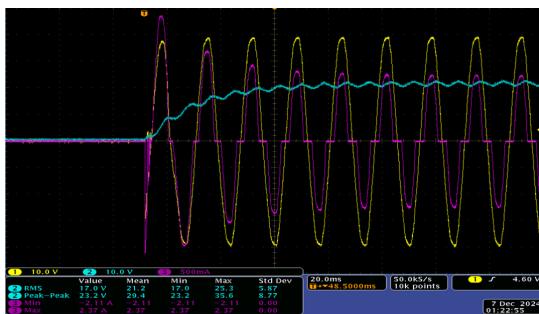


Fig. 20: Scope shot of the voltage across C_{in} (Teal), Input AC voltage (Yellow) and input current drawn from the source (Pink) for the rectifier part of the circuit with load of $40\ \Omega$.

Load resistance	Max in-rush current
$8\ \Omega$	2.35
$40\ \Omega$	2.37

TABLE VI: Table of the values of the maximum in-rush current for different load resistance values at the output of the rectifier part of the circuit.

B. Testing the buck converter part

We tested the buck converter part with the closed-loop control and with a load resistance of $80\ \Omega$. Figure-21 shows the scope shot obtained from testing the circuit. The average output voltage was 13 V and the ripple at the output voltage was 1.2 V, which is in line with the circuit specs.

C. Testing the entire circuit

Then we tested the entire circuit in an open loop control scheme for the load resistance (R_{load}) of $8\ \Omega$ ($P_{load} = 21.125\ W$) and $40\ \Omega$ ($P_{load} = 4.225\ W$). The resulting waveforms

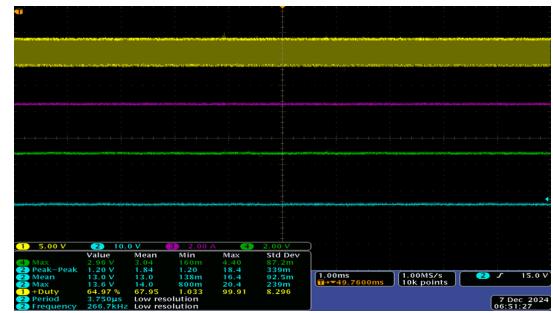


Fig. 21: Scope shot of the Output voltage (Teal), Input voltage (Green), input current (Pink) and switch signal ($q(t)$) (Yellow).

are shown in Figure-23 and Figure-24. Table-VII shows the average output voltage value and the output voltage ripple value for the two cases.

R_{load}	Duty ratio (D)	Avg output voltage	Output voltage ripple
$8\ \Omega$	0.52	13.2 V	3.2 V
$40\ \Omega$	0.41	13.3 V	2 V

TABLE VII: Table of the values of average output voltage and output voltage ripple values for different load resistances.

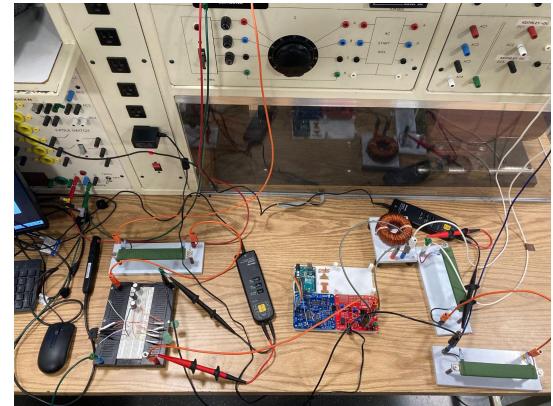


Fig. 22: Complete assembled circuit.

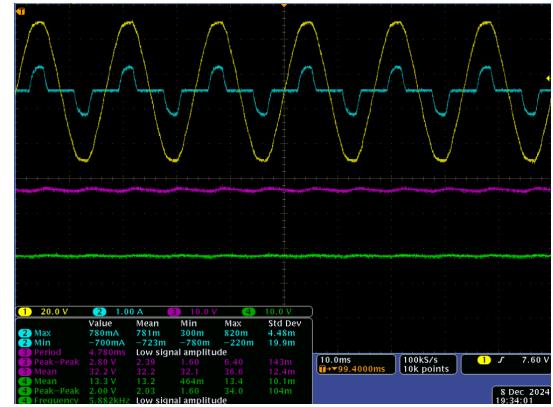


Fig. 23: Scope shot of output voltage (Green), Input AC voltage (Yellow), input current from source (Teal) and voltage across C_{in} (Pink) for $R_{load} = 40\ \Omega$.

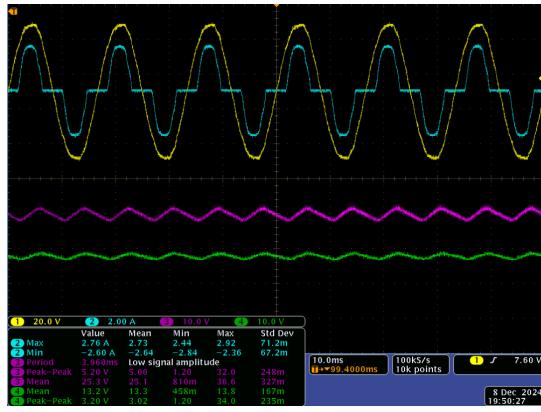


Fig. 24: Scope shot of output voltage (Green), Input AC voltage (Yellow), input current from source (Teal) and voltage across C_{in} (Pink) for $R_{load} = 8 \Omega$.

The important thing to mention here is that the scope shots shown in Figure-23 and Figure-24 were taken before the circuit reached the complete steady state. In complete steady state the NTC thermistor resistance value would be at its lowest (hot resistance). This would reduce the voltage ripple at the output. That is why during the demo we got a much lower output voltage ripple than what is shown here for the 40Ω case.

IV. CONCLUSION

We were able to meet the average output voltage and output voltage ripple specs given for a limited range of load power (1.69 W to 44.47 W).

This could be improved by changing the fuse to a higher current rating. This would help us not use the NTC Thermistors and R_{AC} .

Also, in our design process, we did not consider closed loop control while calculating the values of the components of the circuit. So, the values of our components are much more tighter than what it would have been if we considered closed-loop control while calculating the values of the components of the circuit.

On the control side of things, the entire closed loop control scheme could be implemented using TI's F28379D microprocessor as it has ADCs and DACs which work at a much higher sampling rate than the arduino Uno board used for the testing.

REFERENCES

- [1] ECE 469 lab manual