SVPWM Control Of Multilevel Inverter For Motor Drive Application

Debojyoti Mazumdar
ECE Department
UIUC
dm69@illinois.edu

***Abstract*—This report presents a comprehensive study on the implementation of Space Vector Pulse Width Modulation (SVPWM) for multilevel inverters in motor drive applications. It explores the topology, operation, and switching strategies for Cascaded H-Bridge (CHB) and Diode-Clamped Multilevel (DCML) inverters, emphasizing the use of SVPWM to improve output waveform quality, minimize harmonic distortion, and optimize switching losses. Detailed Simulink-based simulations are conducted to evaluate and compare the performance of both inverter topologies. The results demonstrate effective voltage synthesis, improved harmonic profiles, and dynamic torque response in an induction motor load, validating the efficacy of SVPWM in practical motor drive scenarios.**

I. Introduction

Voltage Source Inverters (VSIs) play a critical role in converting DC voltage to controlled three-phase AC voltage, which is essential for torque generation in electric motor drives. Among various modulation techniques, Space Vector Pulse Width Modulation (SVPWM) offers superior performance in terms of DC bus utilization, reduced total harmonic distortion (THD), and precise control over output waveforms.

Multilevel inverter topologies such as Cascaded H-Bridge (CHB) and Diode-Clamped Multilevel (DCML) inverters are increasingly used in medium- and high-power applications due to their capability to generate high-quality voltage waveforms. However, these topologies present unique challenges in control implementation—particularly in achieving neutral-point voltage stability and minimizing switching losses.

This report presents the modeling and simulation of SVPWM applied to both Cascaded H-Bridge and Diode Clamped multilevel inverters. Provides in-depth analysis of switching states, space vector classification, dwell-time computation, and switching sequence design. The performance of both inverter types is evaluated through MATLAB/Simulink simulations driving an induction motor under variable load conditions.

II. Cascaded H-Bridge Multilevel Inverter

A. Introduction

The Cascaded H-Bridge (CHB) multilevel inverter is a widely used topology in medium-voltage drives due to its modular structure and superior output waveform quality. It consists of multiple identical single-phase H-bridge cells connected in series, each powered by isolated DC supplies. This modular approach facilitates medium-voltage operation without requiring high-voltage switching devices.

B. CHB Circuit Topologies

1) CHB with Equal DC Voltages: A CHB inverter with equal DC voltages stacks H-bridge cells in series. For H cells per phase, the output has $m = 2H + 1$ levels. Redundant switching states are possible, allowing flexibility in modulation. For a three-level multilevel inverter, $H = 1$ cells are required per phase. Figure 1 shows the circuit topology of a three-level CHB multilevel inverter.

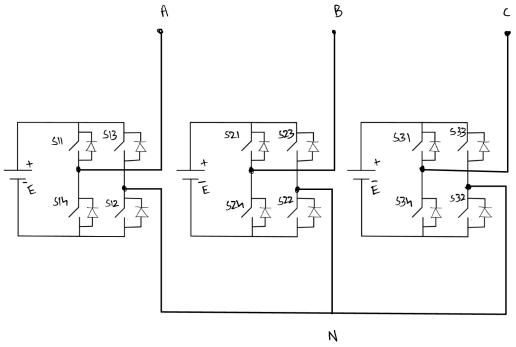

Fig. 1. Three-level CHB inverter configuration

2) CHB with Unequal DC Voltages: CHB topology can also use H-bridge cells with different DC voltages (e.g., E, $2E$, or $3E$). This increases the number of voltage levels but complicates design and eliminates redundancy.

C. Working and switching states

Table I shows the switching states and the corresponding voltage at the output of each inverter leg.

TABLE I
Definition of Switching States

State	S_1	S_2	S_3	S_4	v_{AZ}
P	On	On	Off	Off	$+\frac{V_{dc}}{2} = +E$
O	Off	On	On	Off	0
N	Off	Off	On	On	$-\frac{V_{dc}}{2} = -E$

The switching state where S_1 and S_3 are on and S_2 and S_4 are off is avoided because it results in the A point floating (with no defined voltage).

D. Advantages

- No voltage deviation. As there are no capacitors used, there is no problem of charging and discharging of the capacitor during different switching states.

E. Disadvantages

- Large number of isolated DC supplies. The DC supplies for the CHB inverter are usually obtained from a multipulse diode rectifier employing an expensive phase-shifting transformer.
- High component count. The CHB inverter uses a large number of IGBTs. A nine-level CHB inverter requires 48 IGBTs with the same number of gate drivers.

III. Diode Clamped Multilevel Inverter

A. Introduction

The diode-clamped multilevel inverter (DCMLI), also referred to as the neutral-point clamped (NPC) inverter, is a widely used topology for high power medium voltage drives. It enables multi-level output without switching devices in series. The three-level NPC inverter, employing clamping diodes and a split DC bus, achieves reduced harmonic distortion and $\frac{dv}{dt}$ compared to its two-level counterpart.

B. Circuit Topology and Working

Figure 2 shows the simplified circuit diagram of a three-level NPC inverter. Each leg comprises four active switches (S_1 to S_4) with anti-parallel diodes and two clamping diodes (D_{Z1}, D_{Z2}). The DC bus is split into two capacitors, producing a neutral point Z.

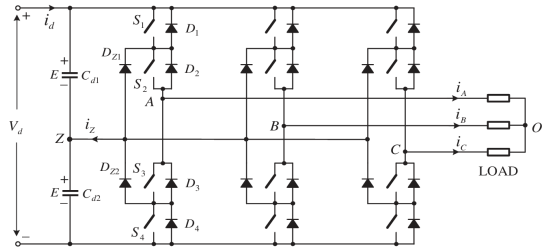

Fig. 2. Three-level NPC inverter circuit

The three switching states and corresponding voltages of the inverter leg are summarized in Table II.

TABLE II
Definition of Switching States

State	S_1	S_2	S_3	S_4	v_{AZ}
P	On	On	Off	Off	$+\frac{V_{dc}}{2} = +E$
O	Off	On	On	Off	0
N	Off	Off	On	On	$-\frac{V_{dc}}{2} = -E$

C. Effects of Switching States

1) Commutation Analysis: The commutation from state O to P is analyzed under two cases:

- **Case 1:** $i_A > 0$ – The current commutates from the clamping diode D_{Z1} to the switch S_1 after the blank interval δ. Figures 3 to 5 show the switching states during commutation in this case. When the switching state is O, the current in the leg flows as shown in Figure 3. During δ time, when S_3 is turned off, the current path remains the same. Then, when the switching state is P, S_1 is turned on. Then the current path changes to as shown in Figure 5.
- **Case 2:** $i_A < 0$ – The current path shifts to free-wheeling diodes during the transition, ensuring voltage sharing among off-state devices. Figures 6 to 8 show the switching states during commutation in this case. When the switching state is [O], the current in the leg flows as shown in Figure 6. During δ time, when S_3 is turned off, the load current forces the free-wheeling diodes D_1 and D_2 to turn-on. Then, when the switching state is [P], S_1 and S_2 are turned on but the current still flows through the free-wheeling diodes as shown in Figure 8.

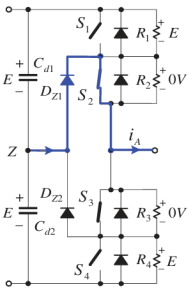

Fig. 3. Switching state [O] in case 1.

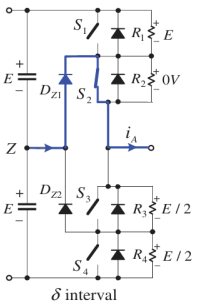

Fig. 4. Interval δ in case 1.

2) Dynamic Voltage Sharing Problem: From Figure 3 to 8, we can say that all the switching devices in the DCML inverter withstand only half of the DC bus voltage during commutation from switching state [O] to [P]. Similarly, the same conclusion can be drawn for the commutation from [P] to [O], [N] to [O] and [O] to [N]. Therefore, DCML inverters do not have dynamic voltage sharing problem.

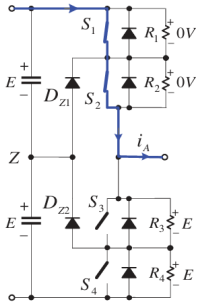

Fig. 5. Switching state [P] in case 1.

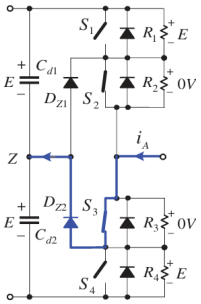

Fig. 6. Switching state [O] in case 2.

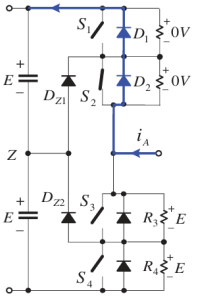

Fig. 7. Interval δ in case 2.

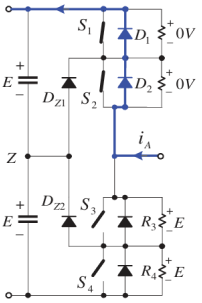

Fig. 8. Switching state [P] in case 2.

3) Prohibited Switching transitions: Switching from [P] state to [N] state and vice versa are prohibited becasue:

- It involves all four switches in an inverter leg, two being turned on and the other two being commutated off, during which the dynamic voltage on each switch may not be kept the same.
- The switching loss is doubled.

4) Neutral-point Voltage Deviation: Neutral point voltage v_Z is defined as the voltage between the neutral point Z and the negative dc bus. Figure 9 show the current flow during each type of switching state. Table III gives a summary of the effect of each type of switching state on V_z.

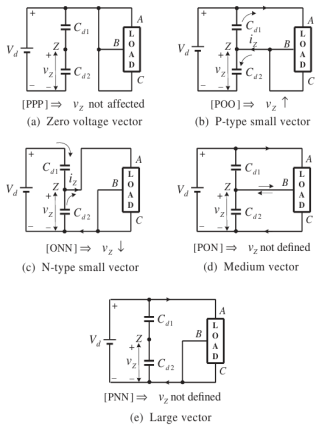

Fig. 9. Effects of Switching States on Neutral Point Voltage.

So, to reduce this, we can modify the switching states such that there is always a P-type and corresponding N-type switching state within a switching cycle. The neutral-point voltage deviation can also occur due to a number of other factors, including

- Unbalanced DC capacitors due to manufacturing tolerances
- Inconsistency in switching device characteristics
- Unbalanced three-phase operation

To minimize the effects of these on switching state, a feedback control scheme can be implemented to keep V_z constant.

TABLE III
SUMMARY OF EFFECT OF SWITCHING STATES ON V_z

Vector Type	Effect on V_z
Zero Vector	No Effect
P-type Small Vector	Increases
N-type Small Vector	Decreases
Medium Vector	not defined
Large Vector	not defined

D. Advantages

- No dynamic voltage sharing problem. Each of the switches in the DCML inverter withstands only half of the total DC voltage during commutation.
- Static voltage equalization without the use of additional components. The static voltage equalization can be achieved when the leakage current of the top and bottom switches in an inverter leg is selected to be lower than that of the inner switches.

- Low THD and dv/dt. The waveform of the line-line voltages is composed of five voltage levels, which leads to lower THD and dv/dt in comparison to the two-level inverter operating at the same voltage rating and device switching frequency.

E. Disadvantage

- DC capacitor voltage balancing. Because of the use of capacitors, there is an issue of charging and discharging of the DC capacitor, which changes the output AC voltage. This increases the THD of the output in practical cases due to parasitic leakages.

IV. Space Vector Modulation

Space Vector Modulation (SVM) is a sophisticated pulse-width modulation technique widely used in power electronics to control inverters. Unlike sinusoidal PWM, which modulates each phase separately, SVM treats the inverter output as a single space vector in the complex plane. By selecting appropriate switching vectors and calculating their dwell times, the SVM synthesizes the desired reference voltage vector while optimizing harmonic performance and reducing switching losses.

A. Two-Level Inverter Space Vector Modulation

1) Switching States and Space Vectors: A two-level inverter has eight possible switching states (six active and two zero states) as shown in Figure 10.

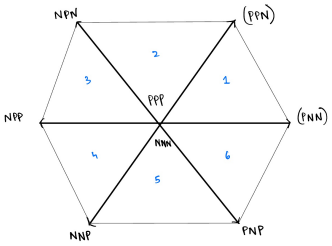

Fig. 10. Space Vector Plot for Two-Level Inverter

The active vectors form a regular hexagon in the α-β plane. Each switching state corresponds to a voltage vector of magnitude $\frac{2}{3}V_{dc}$.

For example, consider a switching state [1 0 0] (A phase high, B and C phase low). The corresponding phase voltages are:

$$V_A = \frac{V_{dc}}{2}, \qquad V_B = -\frac{V_{dc}}{2}, \qquad V_C = -\frac{V_{dc}}{2}$$

Transforming to α-β frame using Clarke transform:

$$V_\alpha = V_A,$$
$$V_\beta = \frac{1}{\sqrt{3}}(V_B - V_C) = 0$$

So, the space vector is $V_{ab} = V_\alpha + jV_\beta = \frac{V_{dc}}{2}$.

2) Nearest Vector Selection: For a given reference vector $\vec{V}_{ref}$ in a sector, the two adjacent active vectors and the zero vector are selected to synthesize the output.

3) Dwell Time Computation: The dwell times T_1, T_2, and T_0 for the two active vectors (V_1 and V_2) and zero vector (V_0) are computed by solving the following equations:

$$\vec{V}_1 T_1 + \vec{V}_2 T_2 + \vec{V}_0 T_0 = \vec{V}_{ref} T_s \tag{1}$$
$$T_1 + T_2 + T_0 = T_s \tag{2}$$

where T_s is the switching period.

4) Switching Sequence: The primary aim of designing the switching sequence is to reduce the switching frequency. For this, the sequence should follow:

- The transition from one switching state to the next involves only two switches in the same inverter leg, one being switched on and the other switched off.
- The transition for $\vec{V}_{ref}$ moving from one sector in the space vector diagram to the next requires no or minimum number of switchings.
- The switching sequence should be symmetric within a switching period (T_s) to reduce higher-order harmonics.

B. Three-Level Inverter Space Vector Modulation

1) Voltage Vectors and Space Vector Diagram: The three-level inverter has 27 possible switching states, yielding 19 distinct voltage vectors categorized as:

- Zero vector: $\vec{V}_0$ (magnitude = 0)
- Small vectors: magnitude = $\frac{V_d}{3}$
- Medium vectors: magnitude = $\frac{\sqrt{3}V_d}{3}$
- Large vectors: magnitude = $\frac{2V_d}{3}$

These vectors form multiple hexagons and triangular sectors in the α-β plane as shown in Figure 11.

These vectors form six hexagonal sectors, which are the main sectors, and each main sector has three triangular sectors which are the sub-sectors. Figure 11 shows the main sectors and sub-sectors of the three phase three level inverter.

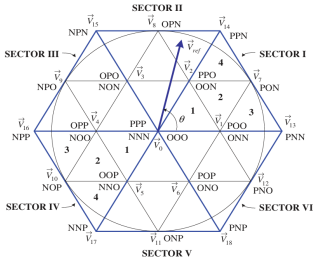

Fig. 11. Space Vector Plot for Three-Level Inverter.

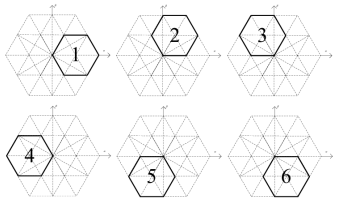

Fig. 12. Main Sectors of the three-level Inverter.

2) Vector Selection Strategy: To identify the three closest vectors, the first step is to find the main sector. The main sectors are identified using Table IV.

TABLE IV
MAPPING ANGLE OF $\vec{V}_{ref}$ TO THE MAIN SECTOR

Angle Range	Sector
$-30°$ to $+30°$	1
$+30°$ to $+90°$	2
$+90°$ to $+150°$	3
$+150°$ to $+210°$	4
$+210°$ to $+270°$	5
$+270°$ to $+330°$	5

After finding the main sector, the sub-sectors can be found using the same logic as used in the two-level SVM. The two vectors that make up the sub-sector is chosen as the two of the three nearest space vectors. The third nearest space vector is the center vector of the main sector.

3) Dwell Time Calculation: The dwell times T_1, T_2 and T_3 for the vectors $\vec{V}_1$, $\vec{V}_2$ and $\vec{V}_3$ are computed by solving the following equations:

$$\vec{V}_1 T_1 + \vec{V}_2 T_2 + \vec{V}_3 T_3 = \vec{V}_{ref} T_s \tag{3}$$

$$T_1 + T_2 + T_3 = T_s \tag{4}$$

where T_s is the switching period.

4) Switching Sequence: The switching sequence should follow the same rules as the two-level SVM. Additionally, redundant states have to be used to reduce the neutral-point voltage deviation in the DCML inverter. There are two cases that arise:

- One small vector among the three nearest vectors. The small vector would have two redundant states, one would be the P-type and the other would be the N-type switching state. For example $\vec{V}_2$ has [PPO] as the P-type switching state and [00N] as the N-type switching state. To reduce the neutral point voltage deviation, the dwell time for the small vector must be equally shared between the P-type and N-type states.
- Two small vectors among the three nearest vectors. In this case, the "dominant" small vector is the small vector toward which the reference voltage $\vec{V}_{ref}$ is more inclined. Then, only the dwell time of the dominant small vector is split between its P-type and N-type states. For the non-dominant small vector, the P-type state is chosen if the main sector is an odd number, and the N-type state is chosen if the main sector is an even number.

V. SIMULATION RESULTS

A. SIMULINK Block

All simulations have been performed in MATLAB SIMULINK. Figure 13 shows the general SIMULINK block diagram for two-level inverter, cascaded H-bridge multilevel inverter and Diode clamped multilevel inverter.

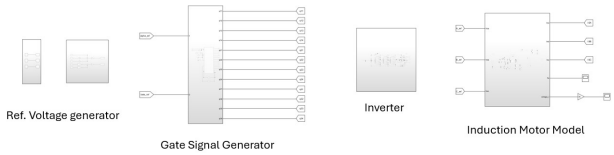

Fig. 13. General Simulink Complete Model

1) Ref. voltage generation block: In this block a reference three-phase voltage is converted to the $\alpha - \beta$ frame of reference.

2) Gate signal generator: In this block, SVM is implemented using a MATLAB Function block. This provides the gate signals for all the switches of the inverter.

3) Induction Machine Model block: In this block, an induction machine is implemented having the steady state equivalent circuit as shown in Figure 14.

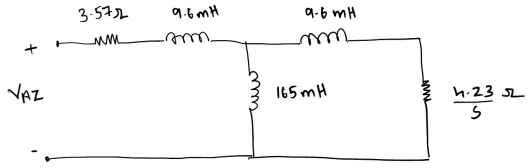

Fig. 14. Steady-State Equivalent Circuit of the Induction Motor.

Where, s is the slip of the rotor.

4) Inverter Block: This block contains the inverter circuit. Figure 15 and Figure 16 show the SIMULINK circuit model for the cascaded H-bridge multilevel inverter and diode clamped multilevel inverter respectively.

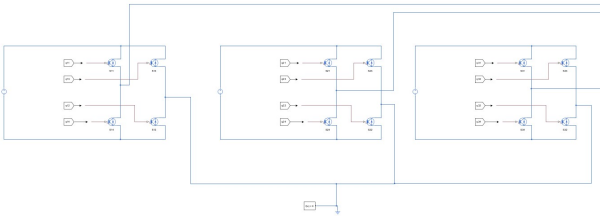

Fig. 15. Cascaded H-bridge Inverter Circuit.

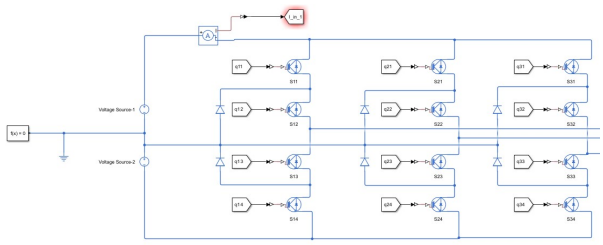

Fig. 16. Diode Clamped Multilevel Inverter Circuit.

B. Results

The following simulations have been performed with a switching frequency (f_{sw}) of 1 kHz and the fundamental frequency of the output AC voltage is $f_e = 100$ Hz. Figure 17 and Figure 18 shows the output waveform per phase for the cascaded H-bridge three-level inverter and neutral-point clamped three-level inverter.

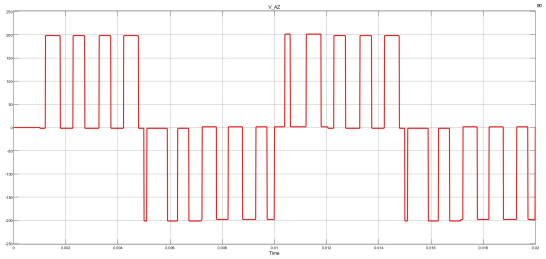

Fig. 17. Per Phase Voltage of Cascaded H-Bridge Three Level Inverter.

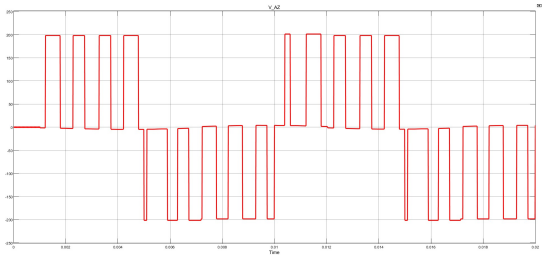

Fig. 18. Per Phase Voltage of Diode Clamped Three Level Inverter.

The voltage vector of the reference signal in the α–β reference frame, along with the three-phase output voltage vectors of the CHB and DCML inverters, are shown in Figures 19,20, and21, respectively.

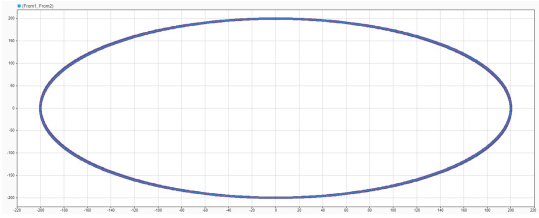

Fig. 19. Reference Voltage Vector Points in $\alpha - \beta$ Domain.

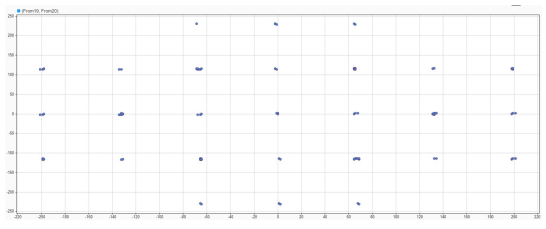

Fig. 20. Three-Phase Output Voltage Vector Points of CHB Inverter in $\alpha - \beta$ Domain for t = 0 to $\frac{2}{f_e}$.

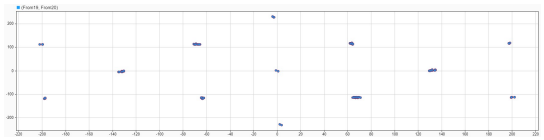

Fig. 21. Three-Phase Output Voltage Vector Points of DCML Inverter in $\alpha - \beta$ Domain for t = 0 to $\frac{2}{f_e}$.

The $\alpha - \beta$ frame voltage plots of the three level inverters are the same. Figure 20 and 21 show instantaneous values. if at every switching frequency ($1/f_{sw}$), the resultant vector points are found, then Figure 19 will be obtained.

Figure 22 and Figure 23 show the line-to-line voltage for the cascaded H-bridge three-level inverter and neutral point clamped three-level inverter.

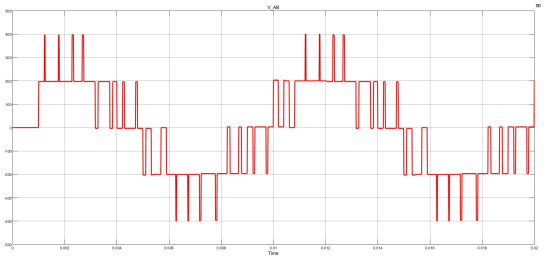

Fig. 22. Five Level Line-to-line Voltage of Cascaded H-Bridge Three Level Inverter.

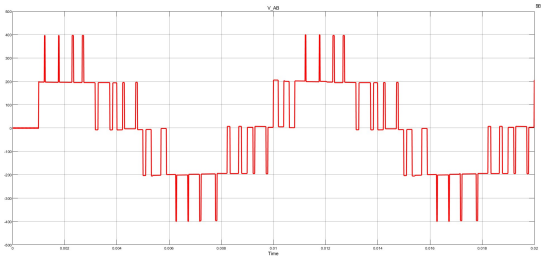

Fig. 23. Five Level Line-to-line Voltage of Diode Clamped Three Level Inverter.

Both the waveforms are nearly the same, but, there is a larger offset from zero volts in the phase voltage of DCML inverter than CHB inverter. This is shown in the magnified image of a time step at which the phase voltage is expected to be zero.

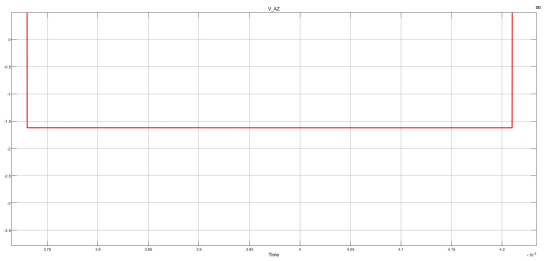

Fig. 24. [O] State Output Voltage for One Phase of CHB Inverter.

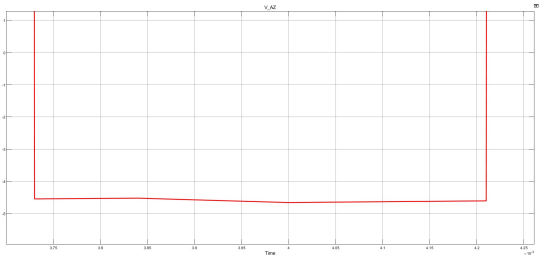

Fig. 25. [O] State Output Voltage for One Phase of DCML Inverter.

This happens because during the [O] state, only the IGBT conducts current in the case of the CHB inverter, but in the case of the neutral-point clamped inverter, the IGBT and the clamping diode conduct current. The current paths for both inverters during the [O] state are shown in Figures 26 and 27. This extra diode voltage drop causes an extra voltage drop in case of the DCML inverters.

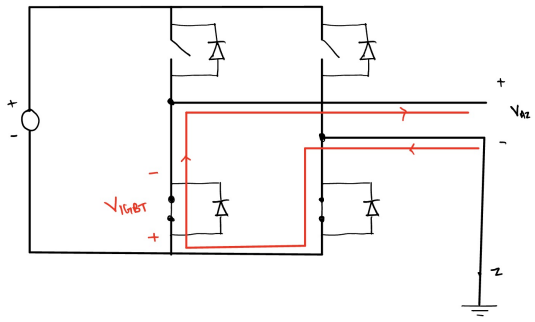

Fig. 26. Current Path During the [O] State of Phase-A of CHB Inverter.

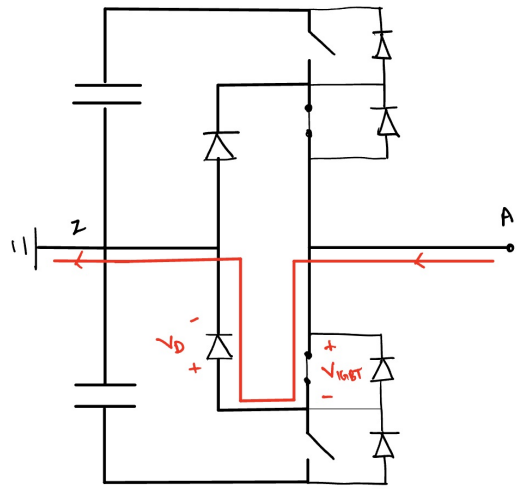

Fig. 27. Current Path During the [O] State of Phase-A of DCML Inverter.

The voltage across the switch S_{11} and the current flowing through the switch S_{11} for the CHB multilevel inverter and DCML inverter are shown in Figure 28 and 29 respectively.

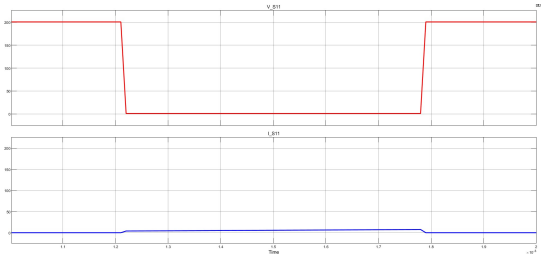

Fig. 28. Voltage and Current in Switch S_{11} of the CHB inverter.

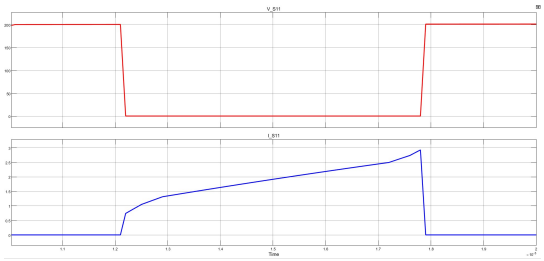

Fig. 29. Voltage and Current in Switch S_{11} of the DCML inverter.

Figure 30 shows the current flowing out of the neutral point Z in the DCML inverter. Using the switching sequence described in the three-level inverter SVPWM technique, the current alternately discharges and charges the capacitors connected around the neutral point Z, thereby contributing to the regulation of the neutral-point voltage. However, the net area under the neutral-point current curve within a switching cycle may not be zero, potentially causing voltage deviation at the neutral point. To mitigate this, a feedback control strategy can be implemented to dynamically adjust the switching durations, ensuring that the net charge drawn from the capacitors over each cycle is effectively zero.

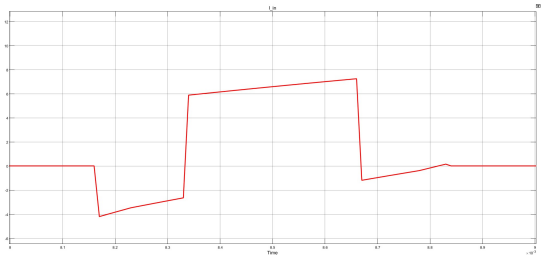

Fig. 30. Current Flowing Out of the Neutral Point Z in the DCML inverter.

The frequency spectrum of the phase and line voltages of the CHB inverter is shown in Figure 31 and 32. The frequency spectrum of the phase and line voltages of the DCML inverter is shown in Figure 33 and 34.

The phase voltage of the CHB inverter has nearly the same (but less) THD as that of the DCML inverter. This shows that the extra diode voltage drop does cause some effect on the THD but not significant.

Connecting the two inverters to the induction machine and applying a load torque of 2 Nm at t = 4 seconds and

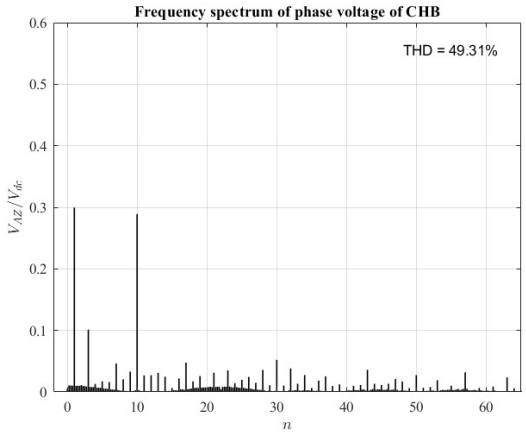

Fig. 31. Frequency Spectrum of the Phase voltage (V_{AZ}) of CHB inverter.

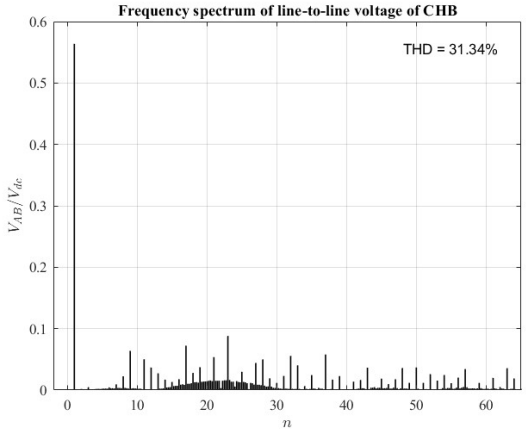

Fig. 32. Frequency Spectrum of the Line-to-line voltage (V_{AB}) of CHB inverter.

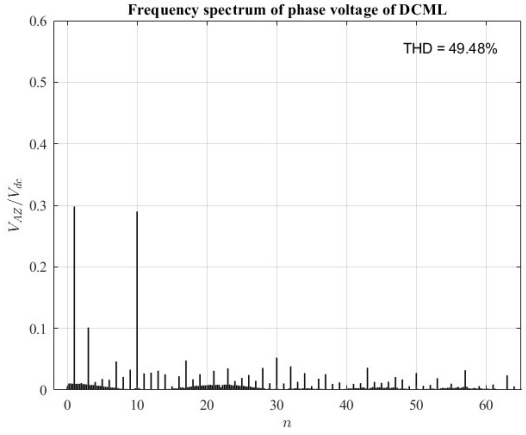

Fig. 33. Frequency Spectrum of the Phase voltage (V_{AZ}) of DCML inverter.

removing the load torque at t = 8 seconds gives an output torque as shown in Figure 35 and 36. For comparison, when supplying the induction machine with ideal three-phase voltage

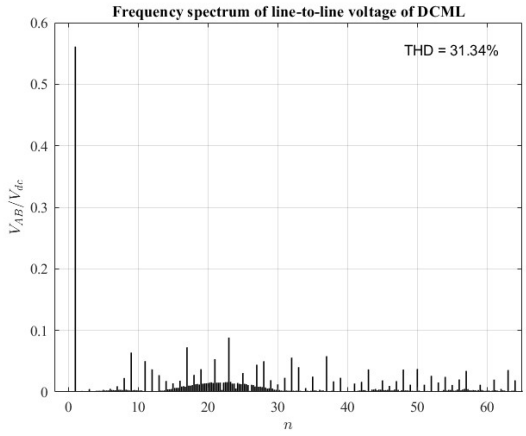

Fig. 34. Frequency Spectrum of the Line-to-line voltage (V_{AB}) of DCML inverter.

waveforms, the output torque is as shown in Figure 37.

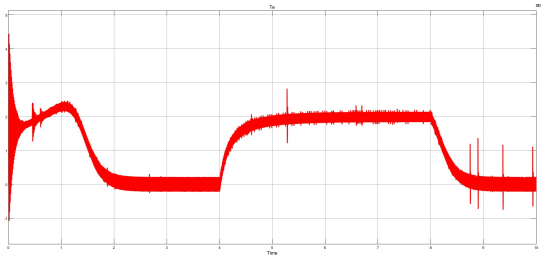

Fig. 35. Output Torque for a Load Torque of 2 Nm using the CHB Inverter.

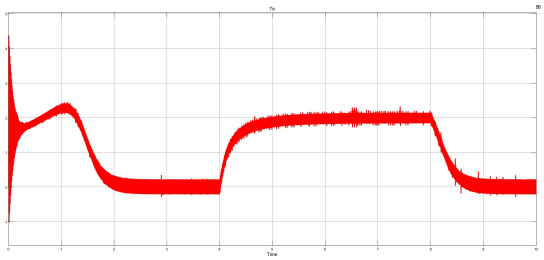

Fig. 36. Output Torque for a Load Torque of 2 Nm using the DCML Inverter.

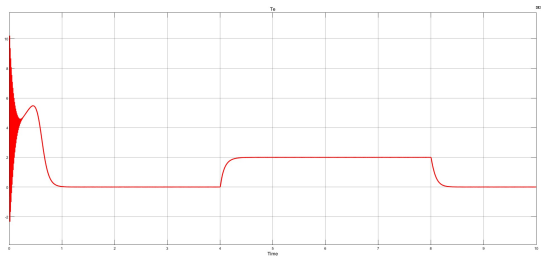

Fig. 37. Output Torque for a Load Torque of 2 Nm using ideal three-phase AC voltage.

It can be clearly observed that the output torque has much

more ripple when the three phase voltage supplied to the motor has higher order harmonics.

VI. Conclusion

In this report, the successful implementation of SVPWM was done for the three-level cascaded h-bridge inverter (CHB) and the diode clamped inverter (DCML). The CHB topology, with its modular structure and lack of voltage imbalance of the capacitor, offers simplicity of control. Meanwhile, the DCML inverter, despite the challenge of neutral-point voltage deviation, benefits from lower device stress and improved harmonic performance when appropriate redundant switching strategies are used.

Simulation results show that the torque produced by the motor connected to these inverters still produces a lot of ripple, due to the high THD, which shows the need for higher-level multilevel inverters.

References

[1] V. Xue, "Center-Aligned SVPWM Realization for 3-Phase 3-Level Inverter," Application Report SPRABS6, Texas Instruments, Oct. 2012.

[2] EE 5200 Course Material, "Power Converter Analysis and Design," Department of Electrical Engineering, Indian Institute of Technology, Madras.

[3] Y. H. Lee, B. S. Suh, and D. S. Hyun, "A novel PWM scheme for a three-level voltage source inverter with GTO thyristors," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 260–268, Mar./Apr. 1996.

[4] ECE 568 Course Material, "Model and Control of Electromechanical Systems," Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Spring 2025.