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IMPLEMENTATION
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    10:53:02 04/23/2024
-- Design Name:
-- Module Name:    siso_shiftreg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.numeric_std.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity siso_shiftreg is
    Port ( DIN : in  STD_LOGIC_VECTOR (3 downto 0);
           MOD1 : in  STD_LOGIC_VECTOR (1 downto 0);
           CLK : in  STD_LOGIC;
           RST : in  STD_LOGIC;
           DOUT : inout  STD_LOGIC_VECTOR (3 downto 0));
end siso_shiftreg;
```

```
architecture Behavioral of siso_shiftreg is
signal MSBIN,LSBIN: STD_LOGIC;
signal temp: STD_LOGIC_VECTOR(3 DOWNTO 0);
begin
MSBIN <= DIN(3);
LSBIN <= DIN(0);

PROCESS(CLK,RST)
BEGIN
IF(RST = '1') THEN
DOUT <= "0000";
temp <= "0000";

ELSIF(CLK'EVENT AND CLK ='1') THEN
CASE MOD1 IS

WHEN "00" =>
                DOUT <= MSBIN & DOUT(3 DOWNTO 1);                --SISO SHIFT RIGHT

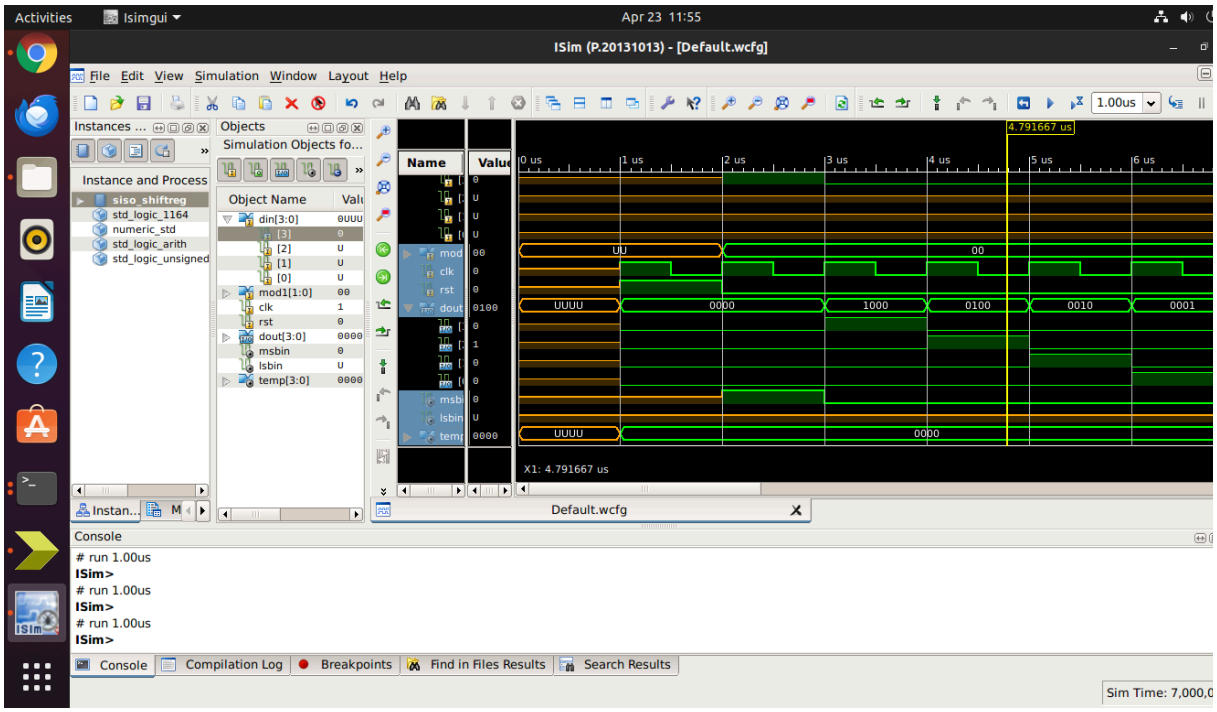
WHEN "01" =>
                                DOUT <= DIN;                                -- PIPO

WHEN "10" =>
                                temp <= MSBIN & temp(3 DOWNTO 1);     --SIPO
                                DOUT <= temp;

WHEN "11" =>
                                DOUT <= DOUT(2 DOWNTO 0) & LSBIN;    -- SISO SHIFT LEFT
WHEN OTHERS =>
                                DOUT <= "0000";
END CASE;
END IF;
END PROCESS;

end Behavioral;
```

1.RST=1
2. RST =0
MOD1=00
DIN=1000



3. MOD1=01
RST=0
DIN=1111