

Transistor biasing and Amplification

Transistor acts as an amplifier. One of the basic requirement during the amplification is that only the magnitude of the signal should increase and there should ~~increase~~ and be no change in the shape or wave form of the signal. This increase in magnitude of the signal without any change in wave form is called amplification.

Condition of amplification :-

i) A copper zero signal collector current :-

Need for stability

Let us consider a npn transistor as shown in fig. When no signal is applied, base current and collector current are zero. Now consider that a sinusoidal signal is applied to the base. For the +ve half cycle of the signal, the base will be +ve w.r.t. emitter and hence forward biased. This will allow the base current and a much larger collector current to flow in the ckt. The result is that the +ve half cycle of the signal is amplified in the collector. However in the negative half cycle base is reverse biased. Therefore the base current and no collector current will flow in the ckt. The result is that there is no output in the -ve half cycle i.e -ve half cycle is completely cut off. Therefore we get an unfaithful amplification.

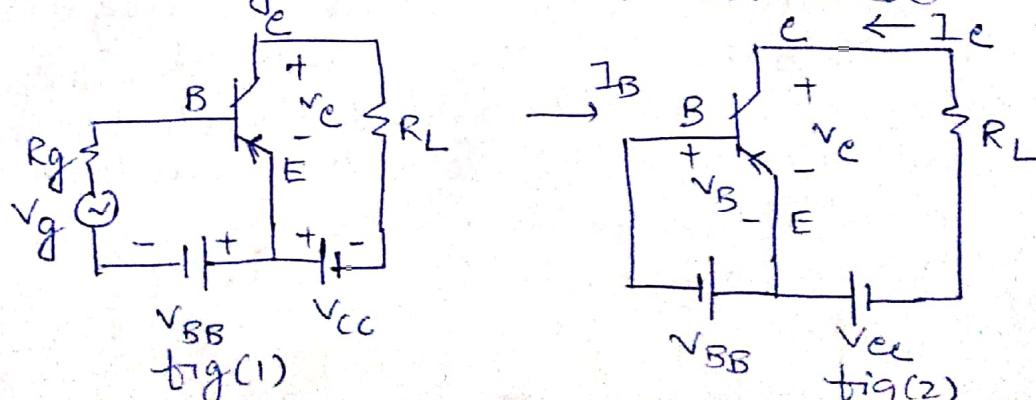
It follows, that arrangement must be provided in the base circuit so that during any part of the signal, the base remain forward biased. This is possible, only if proper zero signal collector current is allowed to flow in the ckt.

xii) Proper collector emitter (V_{CE}) voltage :-

for faithful amplification, it is essential that collector emitter voltage does not fall below a certain minimum value at any instant. This minimum voltage is 0.5 v for Ge transistor and 1 v for Si transistor. When V_{CE} is less than these values, the collector can't attract the charge carriers from emitter and hence a large number of these charge carriers go to the base. In other words collector current decreases and base current increases. This unequal amplification will clearly distort the signal when it appears in the collector ckt. It follows therefore that for faithful amplification V_{CE} should not be allowed to fall below the critical values during any part of the signal.

■ operating point and load line :-

In fig(1) shows a transistor amplifier operating in the CE configuration. The dc operation of the circuit can be studied from fig(2) to which the ckt of fig(1) reduce when the signal source is removed.



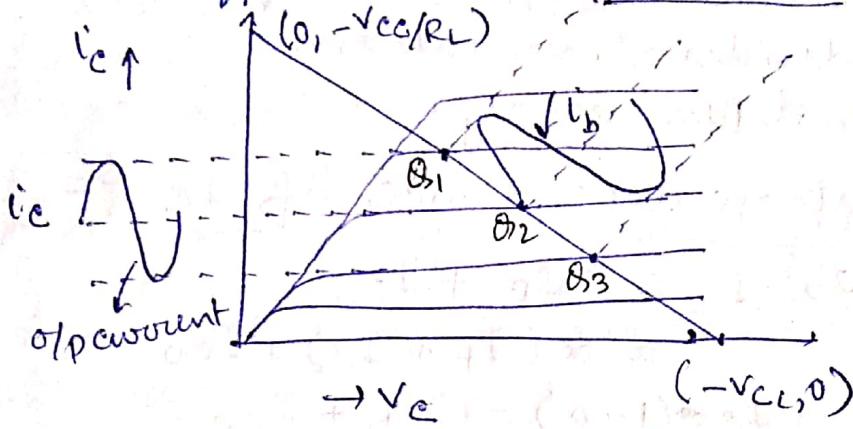
From the o/p of fig(i) we obtain by applying KVL, we get

$$V_{CE} + I_C R_L + V_C = 0$$

$$\therefore I_C R_L = -V_{CE} - V_C$$

$$\therefore I_C R_L = -\frac{V_{CE}}{R_L} - \frac{V_C}{R_L}$$

From this eq, the $I_C - V_C$ plot is a straight line with a slope $(-1/R_L)$. It has an intercept $-V_{CC}/R_L$ on the collector current axis and an intercept ($-V_{CE}$) on the collector voltage axis. The straight line is referred to as load line.



The intersection of the load line with the o/p characteristics yields a set of operating point such as $Q_1, Q_2, Q_3 \dots$. The operating point in the absence of the input signal is called the Q -point of the transistor.

An operating point means a point on the characteristic curves, whose coordinates give the d.c current flowing through the transistor and the d.c voltage actually acting across it.

Transistor Biasing:-

The proper flow of m.e.s signal collector current and selection of proper collector emitter voltage during the passage of the signal and also the establishment of the d.c operating point at suitable location on the active region of the characteristics is called transistor biasing.

The Q point of a transistor change due to i) change in temperature, ii) when transistor is replaced by another of same type. The process of making Q point independent of temperature changes, individual variation is called stabilization.

Need for stabilization:

Stabilization of the Q point is necessary due to the following reasons: —

- i) Temperature dependence of I_c
- ii) ~~Ind~~ Individual variation.
- iii) Thermal run away.

i) Temperature dependence of I_c :

$$\begin{aligned} \text{we know, } I_c &= \alpha I_E + I_{Co} \\ &= \alpha (I_B + I_C) + I_{Co} \\ \Rightarrow I_c \cdot (1 - \alpha) &= \alpha I_B + I_{Co} \\ \Rightarrow I_E &= \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{Co} \\ &= \beta I_B + (1 + \beta) I_{Co}. \end{aligned}$$

Here I_{Co} is the current due to minority carriers. As temperature increases minority carrier increases so that I_{Co} increases.

In fact for each 10°C rise in temperature I_{Co} becomes double. Therefore arrangement must be provided to hold I_c constant inspite of change in temperature. When this is done Q point becomes independent of temperature.

ii) Individual variation:

The value of β and V_{BE} are not exactly same of any two transistors even belonging to the same type. These inherent variation of transistor parameter shift the Q-point when transistor is replaced by another of same

type. Therefore needs must be provided to hold I_c const irrespective of individual variation in temperature.

(iii) Thermal run away :-

The flow of collector current produce heat in the transistor. This increases the transistor temperature so that I_{CO} increases. The increased I_{CO} will further rise the transistor temperature. This further rise in temp. increases I_{CO} still more. In this way the collector current may become too high, thus destroying the transistor. This self destruction in an unstabilized transistor is called thermal runaway. Therefore, in order to avoid thermal run away and consequent destruction of transistor, it is very essential the stabilization done.

Stability factor :-

The stability factor 's', 's'' and 's'' measured the change of the collector current with respect to I_{CO} , V_{BE} and β respectively. The rate of change of collector current with respect to I_{CO} , keeping β and V_{BE} remain constant, is denoted by the stability factor 's'.

$$s = \frac{\partial I_c}{\partial I_{CO}}$$

The variation of I_c with V_{BE} and keeping I_{CO} and β remain constant, is denoted by the stability factor 's'

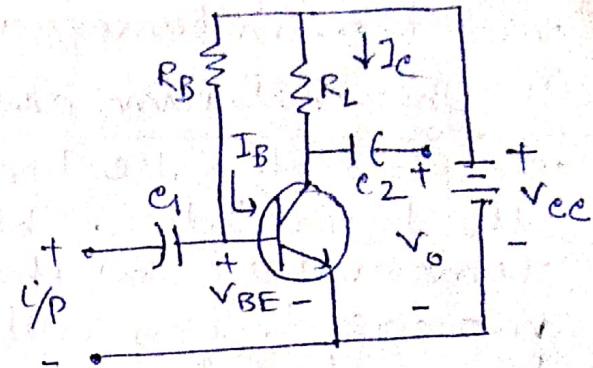
$$s' = \frac{\partial I_c}{\partial V_{BE}}$$

The variation of I_c with β , keeping I_{CO} and V_{BE} constant, is denoted stability factor "s"

$$s'' = \frac{\partial I_c}{\partial \beta}$$

■ Fixed bias arrangement :-

In fig. the signal source of voltage V_{CC} makes the emitter-base junction forward biased and collector-base junction reverse biased.



If R_B is the resistance connecting the base to the positive pole of the voltage source V_{CC} and V_{BE} is the base-emitter voltage drop.

$$\text{The base current is, } I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The collector current is given by;

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) + (1+\beta) I_{CO}$$

So, the stability factor is,

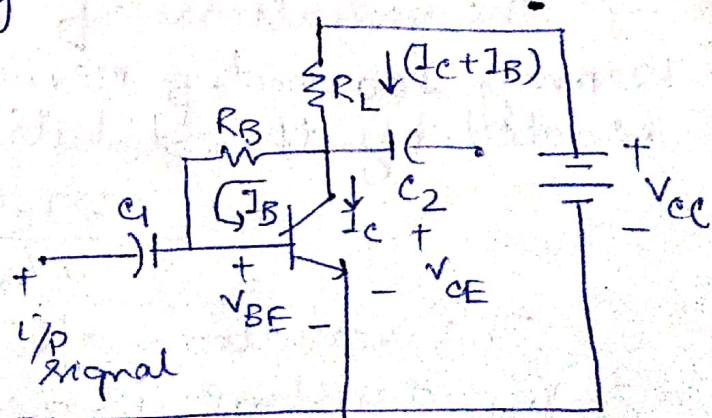
$$S = \frac{\partial I_C}{\partial I_{CO}} = (1+\beta)$$

$$S' = \frac{\partial I_{CO}}{\partial V_{BE}} = -\beta / R_B$$

$$S'' = \frac{\partial I_{CO}}{\partial \beta} = \frac{V_{CC} - V_{BE}}{R_B} + I_{CO}$$

■ Collector-to-base bias arrangement :-

To improve the stability factor of the fixed bias circuit, the resistance R_B is connected between the base and the collector of the transistor.



Applying KVL, we get,

$$V_{CE} = I_B R_B + V_{BE} \quad \text{--- (1)}$$

and $V_{CC} = (I_C + I_B) R_L + V_{CE}$

$$= (I_C + I_B) R_L + I_B R_B + V_{BE} \quad [\text{using eqn. (1)}]$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE} - I_C R_L}{R_B + R_L} \quad \text{--- (2)}$$

The collector current is,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= \beta \left(\frac{V_{CC} - V_{BE} - I_C R_L}{R_B + R_L} \right) + (1+\beta) I_{CO}$$

$$= \beta \left(\frac{V_{CC} - V_{BE}}{R_B + R_L} \right) - \frac{\beta I_C R_L}{R_B + R_L} + (1+\beta) I_{CO}$$

$$\Rightarrow I_C \left(1 + \frac{\beta R_L}{R_B + R_L} \right) = \beta \left(\frac{V_{CC} - V_{BE}}{R_B + R_L} \right) + (1+\beta) I_{CO}$$

so, the stability factor;

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1 + \beta}{1 + \beta R_L / (R_B + R_L)}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta / R_B + R_L}{1 + \beta R_L / (R_B + R_L)}$$

$$= \frac{-\beta}{R_B + R_L (1 + \beta)}$$

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{\left(\frac{V_{CC} - V_{BE}}{R_B + R_L} \right) + I_{CO} - \frac{I_C R_L}{R_B + R_L}}{1 + \frac{\beta R_L}{R_B + R_L}}$$

$$= \frac{V_{CC} - V_{BE} - I_C R_L + (R_B + R_L) I_{CO}}{R_B + R_L (1 + \beta)}$$

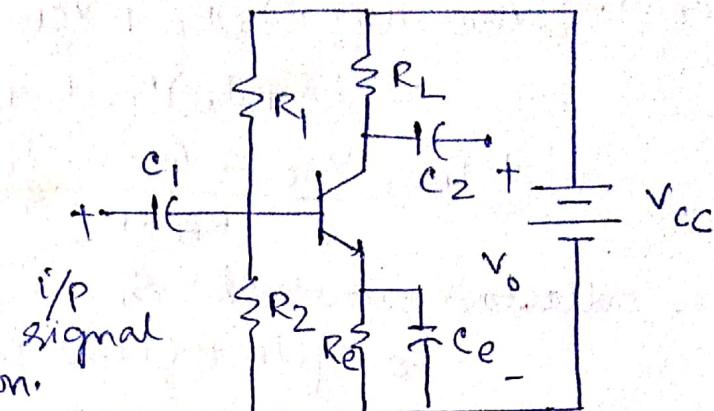
As, $V_{BE} \ll V_{CC}$

$$= \frac{V_{CC} - I_C R_L + (R_B + R_L) I_{CO}}{R_B + R_L (1 + \beta)}$$

Self bias and Emitter bias arrangement

In this method two resistances R_1 and R_2 act as a potential divider and are used to provide biasing.

The emitter resistance R_e provides stabilization.



The combination of R_1 and R_2 is connected across the collector supply V_{CC} .

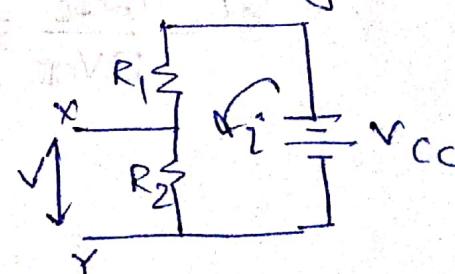
C_e bypassing is connected in parallel with R_e . The ac signal is thus effectively short circuited by C_e , which is known as bypass capacitor. C_2 is the coupling capacitor that couples the ac signal to the o/p terminal but block dc part. The capacitor C_i blocks the dc voltage of previous stage.

The above circuit can be analysed by applying Thévenin's Theorem we get,

$$i = \frac{V_{CC}}{R_1 + R_2}$$

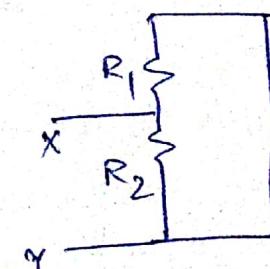
So, equivalent voltage across XY

$$\begin{aligned} V &= iR_2 \\ &= \frac{V_{CC}R_2}{R_1 + R_2} \end{aligned}$$



Equivalent resistance R_B ,

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

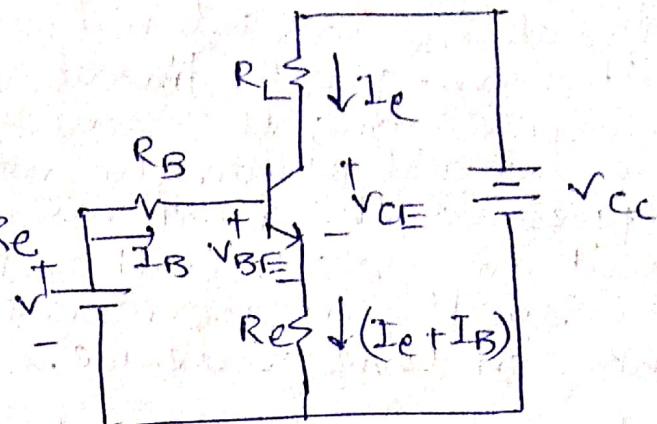


[P.T.O]

Applying KVL
to the i/p ckt
we get,

$$V = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$\Rightarrow I_B = \frac{V - V_{BE} - I_C R_E}{R_B + R_E}$$



collector current I_C ,

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

$$= \beta \left(\frac{V - V_{BE} - I_C R_E}{R_B + R_E} \right) + (1 + \beta) I_{CO}$$

$$= \frac{\beta V}{R_B + R_E} - \frac{\beta V_{BE}}{R_B + R_E} - \frac{\beta I_C R_E}{R_B + R_E} + (1 + \beta) I_{CO}$$

$$\Rightarrow I_C \left(1 + \frac{\beta R_E}{R_B + R_E} \right) = \frac{\beta V}{R_B + R_E} - \frac{\beta V_{BE}}{R_B + R_E} + (1 + \beta) I_{CO}$$

So, the stability factor,

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1 + \beta}{1 + \frac{\beta R_E}{R_B + R_E}} = (1 + \beta) \frac{R_B + R_E}{R_B + (1 + \beta) R_E}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta / R_B + R_E}{1 + \frac{\beta R_E}{R_B + R_E}}$$

$$= \frac{-\beta}{R_B + (1 + \beta) R_E}$$

$$S'' = \frac{\partial I_C}{\partial \beta}$$

$$\therefore \frac{\partial I_C}{\partial \beta} = \frac{V - V_{BE} + I_{CO} (R_B + R_E) - R_E I_C}{R_B + (1 + \beta) R_E}$$

what is the significance of load line?

→ A load line is used in graphic analysis of circuit, having both linear and non-linear part, representing the constraint the other parts of the circuit put on the non-linear transistor. It represents the response of the linear circuit connected to the transistor, diode etc. It is usually drawn on a graph of the I vs V in the non-linear device.

what is operating point? Explain its physical significance.

→ The zero signal values of I_C and V_{CE} are known as the operating point. It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied. It is also known as quiescent point or Q point.

The operating point defines where the ~~transistor~~ transistor will operate on its characteristics curves under dc conditions. For linear amplification, the operating point should not be too close to the maximum power, voltage or current rating, besides avoiding the regions of cutoff and saturation.