2022

ELECTRONIC SCIENCE

Paper : ELCGE-31

(Electronics)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***any five*** questions.

1. (a) What is Fermi level?

   (b) We have two intrinsic semiconductors, SI and S2. The E-k diagram for each of them is shown in Fig. 1 below.

   (i) Which one of them should have higher electron mobility and why?

   (ii) Which one of them is likely to have higher intrinsic carrier concentration at a given temperature? Justify your answer.

   (iii) Where should the Fermi level lie for SI with reference to the middle of the band gap? Justify your answer.

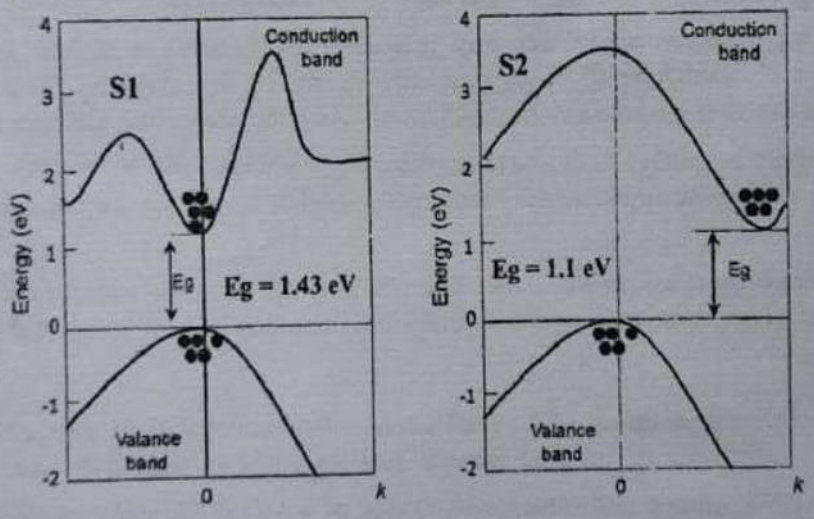

Figure 1

   (c) Calculate the resistivity of an n-type silicon doped with 10^{16} phosphorus atoms/cm^3. Assume, q = 1.6×10^{-19} C and μ_n = 1300 cm^2/V.s. 1+(2+2+3)+2

2. (a) What is diffusion capacitance in connection with a p-n junction diode?

(b) Calculate the contact potential for a p-n junction with $N_A = 10^{17}$ cm^{-3} and $N_D = 10^{16}$ cm^{-3} at room temperature. Given: kT/q = 25.9 mV and $n_i = 9.65 \times 10^9$ at room temperature, where the terms have their usual meanings. Derive the expression used.

(c) Two different p-n junction diodes Dl and D2 are formed using semiconductors SI and S2, respectively. The acceptor doping concentration is 10^{16} cm^{-3} for both Dl and D2. Similarly, the donor doping concentration is 10^{17} cm^{-3} for both Dl and D2. Consider the E-k diagram as shown in Fig. 1 for S1 and S2.

(i) Which one of them is likely to have higher reverse saturation current at a given temperature? Justify your answer.

(ii) Which one of them can be used as an LED and why? 2+4+(2+2)

3. (a) Sketch the input and output characteristics of a transistor operating in the CB configuration. What is base width modulation or early effect? What are the biasing conditions at the junctions of the transistor operating in the active, saturation and cutoff regions? Why does the collector current remain practically constant in the active region of the output characteristics of a transistor?

(b) What are the conditions that must be satisfied in a transistor circuit for faithful amplification? Explain the importance of proper choice of the Q-point.

(c) Draw the fixed bias circuit of a transistor. In a fixed bias circuit of transistor, $V_{CC} = 9$V, $R_B = 100$ kΩ and $R_C = 1.2$ kΩ. If $\beta = 50$, $I_{CO} = 20$ nA and $V_{BE} = 0.7$ V, determine the Q-point and find the thermal stability factor of the bias circuit. 4+3+3

4. (a) Draw the r_e-model of a transistor operating in CB mode. Explain how this model can be established. Draw the r_e-model of a transistor operating in CE mode also.

(b) Draw the h-parameter model for any transistor configuration at low frequency. Why these parameters are called hybrid? Show that only h_{ie} and h_{fe} are important in the h-parameter model. How can these two parameters be calculated from the transistor characteristics?

(c) A CE transistor amplifier is characterized by $h_{ie} = 1200\ \Omega$ and $h_{fe} = 100$. If the load resistance is 1 kΩ, then using the approximate h-parameter model, determine the voltage gain of the amplifier. 4+4+2

5. Schematically draw the equilibrium band diagram of a metal-oxide-semiconductor (MOS) structure. With appropriate diagram explain how accumulation, depletion and inversion capacitance forms in such a MOS structure. 2+8

6. (a) Draw the schematic diagram of a metal-oxide-semiconductor field effect transistor (MOSFET). Explain how pinch-off occurs and current gets saturated in such a device.

(b) Define threshold voltage and trans-conductance of a MOSFET and explain how such parameters can be extracted from the measured current-voltage characteristics. (1+3)+(3+3)

7. (a) What are CMRR and PSRR of an op-amp?

(b) Explain how op-amp is used as a voltage comparator. How can it be used as a zero-crossing detector?

(c) Draw the circuit diagrams for the four feedback topologies. 2+(3+1)+4

8. (a) From the truth table below, determine the standard SOP expression.

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(b) Draw the circuit diagrams of a 4-bit multiplexer and de-multiplexer.

(c) Draw the circuit diagram of a J-K flip-flop using NAND gates. Write its truth table. How to convert a J-K flip-flop to a D flip-flop? 2+(2+2)+(2+1+1)

2019

ELECTRONIC SCIENCE

Paper : ELCGE-31

(Electronics)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***any five*** questions.

1. (a) Define effective mass, carrier mobility and minority carrier life-time.

(b) Show the variation of mobility with temperature and explain its nature.

(c) How does the intrinsic carrier concentration vary with (i) temperature and (ii) band gap?

(d) Write down the current equation and continuity equation for holes in a semiconductor. 3+3+2+2

2. (a) Obtain expressions for electric-field and potential distributions in an abrupt p-n junction diode and discuss them. Also, obtain expressions for the depletion layer width and depletion layer capacitance for such a diode.

(b) Find contact potential of a diode if p- and n-side doping concentrations are 5×10^{16} cm^{-3} and 4×10^{17} cm^{-3}, respectively. Assume $n_i = 1 \times 10^{16}$ cm^{-3} and kT/q = 26 mV, where the terms have their usual meanings. 8+2

3. (a) What is meant by α and β of a transistor? Show that, $\beta = \dfrac{\alpha}{1-\alpha}$.

(b) What are the factors that affect the bias stability of a transistor?

(c) Design a CE collector-feedback bias circuit of an npn transistor to establish a quiescent operating point at I_{CQ} = 1 mA and V_{CEQ} = 8 V. Given that, β = 100, V_{CC} = 12, and V_{BE} = 0.3 V. 4+2+4

4. (a) Draw the r_e — model equivalent circuit of a transistor in CE configuration. Show that, $r_e = \dfrac{26\text{mV}}{I_E}$.

(b) Draw the low-frequency h-parameter equivalent circuit of a transistor operating in CE mode. State the h-parameters of the circuit.

(c) For the transistor amplifier of Fig. Q. 4.(c), determine Z_i, Z_o, A_v and A_i of the amplifier using approximate h-parameter model. Given that, $h_{ie} = 560\Omega$ and $h_{fe} = 120$. 3+4+3

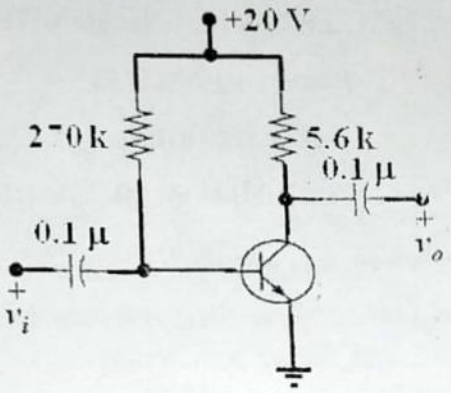

Fig. Q. 4 (c).

5. (a) Convert the decimal number 51926 into its hexadecimal equivalent.

(b) Subtract 11010 from 10110 using 2's complement method.

(c) Find the minimum expression for the function

$$F(X, Y, Z) = \bar{X}\,\bar{Y}\,\bar{Z} + \bar{X}\,\bar{Y}\,Z + \bar{X}\,Y\,\bar{Z} + \bar{X}\,Y\,Z + X\,Y\,\bar{Z}$$

using a Karnough map.

(d) Write down the truth table of a Full-adder. Write the canonical SOP forms for the sum and carry outputs. 2+2+3+3

6. (a) Explain the effect of negative feedback on signal-to-noise ratio.

(b) What is Barkhausen criterion?

(c) Show that for voltage shunt feedback, both the input and output impedance decrease.

(d) How is op-amp used as an integrator? 2+2+(2+2)+2

7. Draw the schematic structure and relevant band diagram of a metal-oxide-semiconductor (MOS) capacitor on p-Si substrate. Assuming an applied voltage varying from negative to positive across its terminals, explain how its capacitance will change. 3+7

8. Draw the schematic structure of a metal-oxide-semiconductor field effect transistor (MOSFET) and explain its operation with relevant current-voltage characteristics. Explain how threshold voltage and trans-conductance of such a device can be measured. 6+4

M.Sc. Semester-III Examination (Under CBCS), 2020

UNIVERSITY OF CALCUTTA

ELECTRONIC SCIENCE

Paper : ELCGE-31

(Electronics)

Full Marks : 50

Total Time – 2 Hours

INSTRUCTIONS TO THE EXAMINEE

(A) Use blank white paper sheets to write down the answers in your own hand writing. Note that no computer-typed answer scripts will be considered for evaluation.

(B) Write down the following on the first page of your answer scripts:

M.Sc. Semester-III Examination (Under CBCS), 2020

Roll No.:-

Registration No.:-

Date of Examination:-

Paper/Course Code:-

Paper/Course Name:

Total no. of pages used (including this page):-

(C) You must write your roll number and page no. on the top margin of each page of your answer scripts.

(D) Write your answers mentioning the appropriate question no. starting from the second page onward.

(E) After completion of the examination **at 2:00 pm**, submit the scanned copies or images of all the pages of your answer scripts making "preferably a **single pdf** file or images in **jpeg** format" in digital mode via e-mail **within 2:20 pm**.

(F) File name of your answer scripts should preferably be: **XXYY.pdf/jpg** and submit your answer scripts to the following e-mail ids: **akelc@caluniv.ac.in, abhijit_mallik1965@yahoo.co.in, scelc@caluniv.ac.in, jselc@caluniv.ac.in,** with a copy to your Head/Principal.

Note-1: **XX** is the abbreviation of your Department/College name.
YY is the last two digits of your roll no.
XX is **PH** for students of the Department of Physics, CU
XX is **AM** for students of the Department of Applied Mathematics, CU
XX is **GC** for students of the Gurudas College
XX is **VC** for students of the Vivekananda College

Note-2:

Question Paper Upload Time	**: 11:50 AM**
Examination Start Time	**: 12:00 Noon**
Examination End Time	**: 2:00 PM**
Answer Scripts Upload Time	**: 2:20 PM**

You must follow and abide by these above-mentioned instructions and timing.

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2020

ELECTRONIC SCIENCE

Paper : ELCGE-31

(Electronics)

Full Marks : 50

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer ***any five*** questions.

1. (a) Define effective mass and mobility.
   (b) Give an account of the variation of the carrier concentration with temperature for an *n*-type semiconductor.
   (c) How does the carrier mobility in a bulk semiconductor vary with temperature and why?
   (d) Calculate the resistivity of an *n*-type silicon doped with 10^{17} phosphorus atoms/cm^3. Assume $q = 1.6\times10^{-19}$ C and $\mu_n = 1200$ cm^2/V.s. 2+3+3+2

2. (a) Derive an expression for the contact potential in a *p-n* junction diode.
   (b) Calculate the contact potential for a *p-n* junction with $N_A = 10^{18}$ cm^{-3} and $N_D = 10^{15}$ cm^{-3} at room temperature. Given: $kT/q = 25.9$ mV and $n_i = 9.65\times10^9$ at room temperature, where the terms have their usual meanings.
   (c) Calculate the reverse saturation current in a Si *p-n* junction diode with cross-sectional area of 2×10^{-4} cm^2. Assume: $N_A = 5\times10^{16}$ cm^{-3}, $N_D = 10^{16}$ cm^{-3}, $n_i = 9.65\times10^9$cm^{-3}, $D_n = 21$ cm^2/s, $D_p = 10$ cm^2/s, and$\tau_n = \tau_p = 5\times10^{-7}$s, where the terms have their usual meanings.
   (d) What is diffusion capacitance? 3+2+4+1

3. (a) Show the experimental set-up to draw the input and output characteristics of a transistor operating in the *CC* configuration. Sketch the input characteristics and explain the nature of the curve qualitatively. Sketch the output characteristics indicating the active, saturation and cutoff regions.
   (b) "The value of α increases with the increasing reverse bias voltage of the collector-base junction." – Why?
   (c) What are the factors that affect the bias stability of a transistor circuit? Give the mathematical expressions of different stability factors.
   (d) In a fixed bias circuit of transistor, $V_{CC} = 15$ V, $R_B = 300$ kΩ and $R_C = 2$ kΩ. If $\beta = 100$, $I_{CO} = 20$ nA and $V_{BE} = 0.7$ V, determine the *Q*-point and find the thermal stability factor of the bias circuit. 4+1+2+3

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4. (a) What is a load line? Explain its significance.
   (b) Define the hybrid parameters for a basic transistor in any configuration.
   (c) A *CE* transistor amplifier is characterized by h_{ie} = 2 kΩ,h_{re} = 2×10^{-4}, h_{fe} = 50, and h_{oe} = 2×10^{-6}℧.If the load resistance is 4 kΩ and the source resistance is 200 Ω, determine the current gain and input impedance. Deduce the formulae you use. 2+3+5

5. (a) What is a junction field effect transistor (JFET)? With an appropriate diagram explain the operation of a JFET. How does the current in such a device saturate? Define trans-conductor of such devices.
   (b) Explain how inversion occurs in a metal-oxide-semiconductor (MOS) capacitor. (1+3+2+2)+2

6. (a) Draw the schematic of a metal-oxide-semiconductor field effect transistor (MOSFET) and label its different regions. Explain how pinch-off occurs in such a device.
   (b) Define threshold voltage of a MOSFET and explain how it can be measured? How does it depend on the substrate doping? What is the need of scaling down of MOSFETs? (1+3)+(4+2)

7. (a) How does negative feedback affect the stability and sensitivity of a circuit?
   (b) A 5 mV, 1 kHz sinusoidal signal is applied to the input of an OP-AMP integrator circuit with R = 100 kΩ and C = 1μF. Find the output voltage.
   (c) Name and draw the configurations of the four feedback topologies. 3+3+4

8. (a) Subtract 111 from 1101 using 1's complement method.
   (b) Explain the operation of a JK-flip flop using NAND gates.
   (c) What is priority encoder?
   (d) Draw the circuit diagram of a 4-bit ripple counter along with its timing diagram. 1+3+3+3

2023

ELECTRONIC SCIENCE

Paper : ELCGE 31

(Electronics)

Full Marks : 50

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer ***any five*** questions.

1. (a) Define effective mass and minority carrier lifetime.

(b) Where does the Fermi level lie for intrinsic silicon? Justify your answer.

(c) What do you mean by direct and indirect band gap semiconductors? Which one of them favours light emission and why?

(d) What is a degenerate semiconductor? 2+3+3+2

2. (a) Sketch typical charge distribution, electric-field distribution and potential distribution in a p-n junction diode with abrupt doping profile.

(b) Which diode, made of Si or Ge, will show higher reverse saturation current and why?

(c) What do you mean by diffusion capacitance and diffusion length?

(d) What will happen to the reverse saturation current if the temperature of the junction is increased?

(e) What is Zener breakdown? 2+2+2+2+2

3. (a) Define the (i) emitter injection ratio or emitter efficiency, and (ii) base transportation factor of a transistor.

(b) What is Early effect of a transistor? How can it account for the input characteristics of a transistor in *CB* mode?

(c) What are I_{CBO} and I_{CEO}? Give the relationship between them. How does I_{CBO} vary with temperature?

(d) Draw and design a *CE* collector-feedback bias circuit of an *npn* transistor to establish a quiescent operating point at $I_{CQ} = 1$ mA and $V_{CEQ} = 8$ V. Given that, $\beta = 100$, $V_{cc} = 12$ V and $V_{BE} = 0.3$ V. 2+2+3+3

4. (a) Explain why biasing and bias stabilization are needed in a transistor circuit? What is meant by 'thermal runaway' of a transistor? How can 'thermal runaway' be avoided in a transistor circuit?

(b) Draw the r_e-model of a transistor operating in *CE* mode. Show that, $r_e = \frac{26mV}{I_E}$.

(c) In the small-signal transistor amplifier in fig. 1, $h_{ie} = 2\ \Omega$, $h_{fe} = 50$; h_{re} and h_{oe} are negligible. Draw the *h*-parameter equivalent circuit for the amplifier and determine : (i) Z_i, (ii) Z_0, and (iii) A_v. 4+3+3

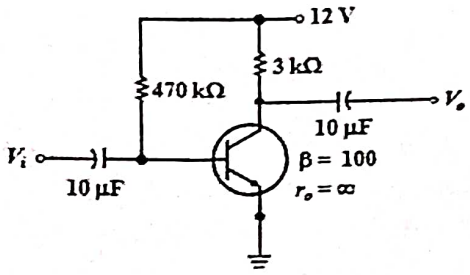


Fig. 1

5. (a) Draw a metal-oxide-semiconductor (MOS) structure and explain how inversion occurs in such a system.

(b) Draw the high frequency and low frequency capacitance-voltage characteristics of such a MOS device and explain why the capacitance values differ. 6+4

6. (a) Draw a neat diagram for the metal-oxide-semiconductor field effect transistor (MOSFET) and label its different areas.

(b) Draw the transfer and output characteristics of a MOSFET and explain the nature of such characteristics.

(c) Explain the purpose of scaling down of geometric dimensions in a MOSFET. What are the rules for constant field scaling? 2+5+3

7. (a) What is the value of R_f in case of a non-inverting op-amp circuit if the gain is 5:5 and R_i is 10 kΩ? The symbols have their usual meaning.

(b) Explain how op-amp is used as :

(i) a phase shifter

(ii) a scale changer.

(c) Explain how negative feedback reduces frequency distortion in feedback amplifiers. 3+(2+2)+3

8. (a) Calculate the octal equivalent of the decimal number 417.

(b) Minimize the following Boolean function :

$F(A, B, C, D) = \Sigma m\ (0, 1, 3, 5, 7, 8, 9, 11, 13, 15)$.

(c) Draw the circuit diagram of a D-Latch using NAND gates. Give its excitation table and K-Map representation.

(d) Explain the working of a Ripple counter and give its timing diagram. 2+2+3+3

2024

ELECTRONIC SCIENCE

Paper : ELC-GE-31

(Electronics)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Symbols have their usual significances.

Answer ***any five*** questions.

1. (a) Deduce the expression for contact potential in a *p-n* junction.

   (b) A Si abrupt *p-n* junction has $N_a = 10^{18}\text{cm}^{-3}$ on one side and $N_d = 5 \times 10^{15}\ \text{cm}^{-3}$ on the other side : (i) calculate the Fermi level positions at 300 K in the *p*- and *n*-regions. Hence find the contact potential; and (ii) draw an equilibrium band diagram for the junction and determine the contact potential V_0 from the diagram. 4+(4+2)

2. (a) Explain with a labeled diagram the different current components in a transistor.

   (b) Define α and β and find the relationship between them.

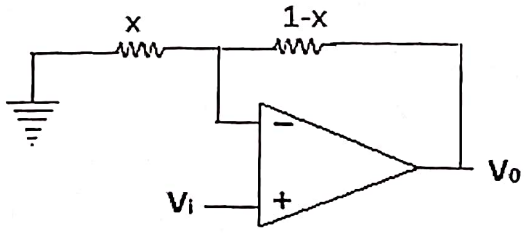
   (c) Explain early effect in transistor and explain how it affects the input and output characteristics of the transistor. 3+4+3

3. (a) Why is the hybrid model only valid for small signals?

   (b) Find the expressions for : (i) input impedance, (ii) current gain, (iii) voltage gain and (iv) output impedance without taking the source resistance into account. 2+8

4. (a) What is the need for level shifter in an OPAMP?

   (b) Show that the gain of the given amplifier is $A_v = 1/X$ with response to the given circuit.



   (c) Derive the expression for voltage gain of a differential amplifier using OPAMP. 2+4+4

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5. (a) Draw a schematic diagram for n-channel JFET and MOSFET.

(b) Explain pinch off effect for JFET and explain its behaviour after pinch off.

(c) Draw the output drain characteristics for a n-channel JFET and mention each region in the characteristics curve.

(d) What is the significance of threshold voltage for EMOSFET and DMOSFET? (1+1)+(2+2)+(1+1)+(1+1)

6. (a) Write down the equation for gain with feedback and hence explain the following conditions :

(i) If $1+A\beta<1$

(ii) If $1+A\beta>1$

(iii) If $1+A\beta=0$

(iv) If $1+A\beta>>1$,

where symbols have their usual meaning.

(b) Compare voltage series and current series feedback.

(c) Mentioning the condition for frequency of oscillation, briefly explain phase shift oscillator. (1+1+1+1+1)+2+3

7. (a) Using IC74153 make an equivalent 8 : 1 MUX.

(b) Why MUX is also known as basic building block for digital circuits? Explain with examples.

(c) Briefly describe the working principle of a 3-bit even parity checker. 2+(1+2)+5

8. (a) Compare between combinational and sequential logic circuits.

(b) What are the disadvantages of S-R FF and what is its remedy?

(c) Draw a neat diagram for MOD-10 asynchronous counter.

(d) Draw the timing diagram of a Serial-In-Serial-Out (SISO) shift register where a steady logical-1 is applied at the serial input line connected to 1st stage of the SISO shift register (Draw up-to 4 clock pulses). 2+(2+2)+2+2