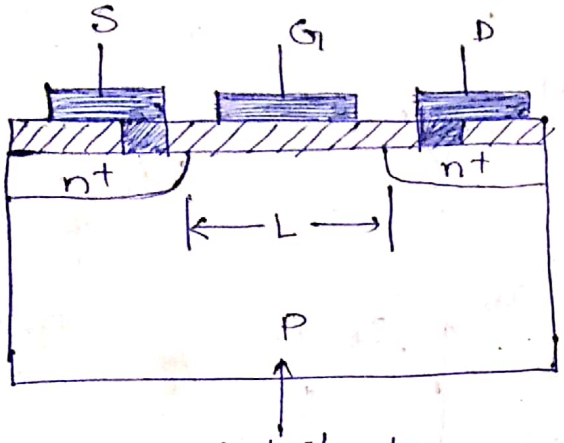
MOSFET

The field effect transistor which has much greater commercial importance than the JFET is the metal oxide - semiconductor field effect transistor (MOSFET). The JFET finds applications in linear and some non-linear circuits whereas MOSFET finds extensive use in digital circuits. The name MOS come from its special structure consisting of layer of metal oxide and semiconductor.



fig(1)

A n-channel MOSFET is shown in fig. It is a four terminal device and consists of a p-type semiconductor substrate in which two n+ regions, the source and drain are formed. The metal plate on the oxide is called the gate. Heavily doped polysilicon or a combination of a silicide and polysilicon can be used as the gate electrode. The fourth terminal is an ohmic contact to the substrate.

Basic characteristics :—

When no voltage is applied to the gate, the source to drain electrodes correspond to two p-n junc. connected back to back. The only current that can flow from the source to drain is the reverse leakage current. When we apply a sufficiently large positive bias to the gate, the MOS structure is inverted so that a surface inversion layer (or channel) is formed between two n+ region, through which a large current can flow. The conductance of this channel can be modulated by varying the gate voltage.

Linear and Saturation region :-

If a voltage is applied to gate, causing an inversion layer at the semiconductor surface. If a small drain voltage is applied, electrons will flow from source to the drain through the channel, the corresponding current will flow from drain

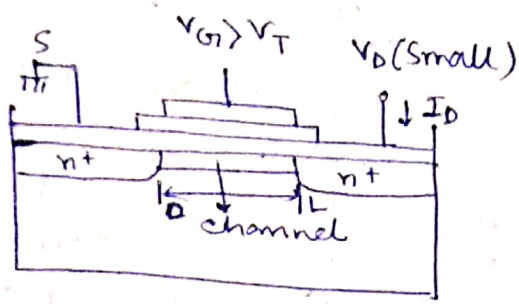
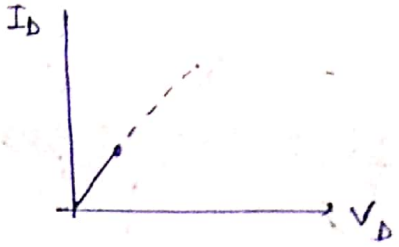


fig 2(a)



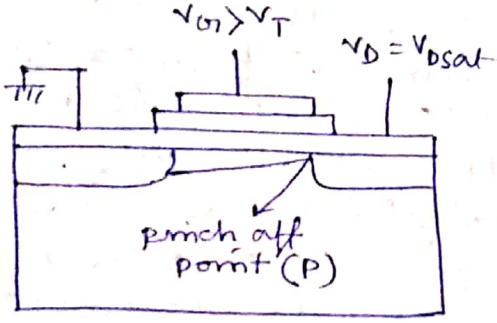
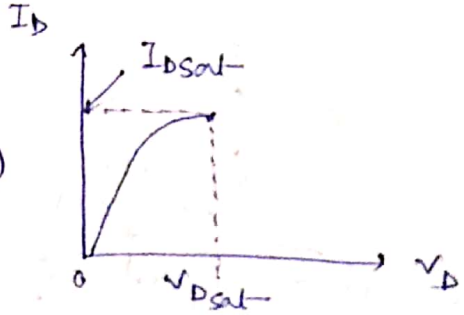


fig 2(b)



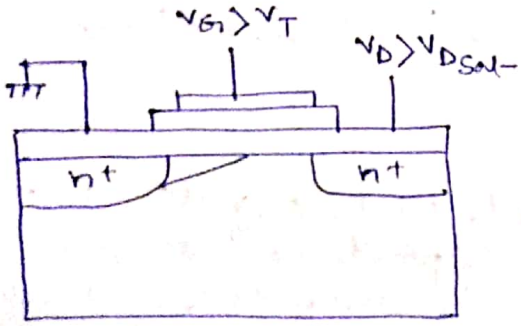
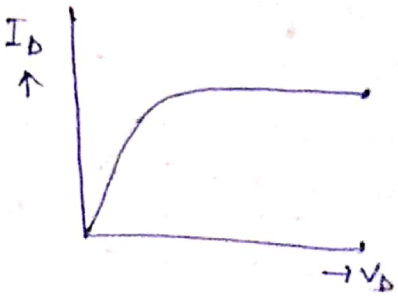


fig 2(c)



to source. Thus, the channel acts as a resistor. The drain current I_D is proportional to the drain voltage. This is the linear voltage/as region as shown in fig2(a).

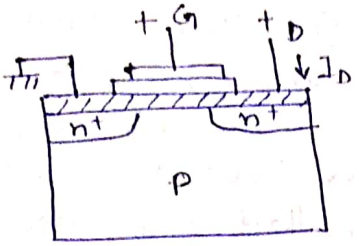
When drain voltage increases upto V_{DSat}, at which the thickness of inversion layer near $y = L$ is reduced to zero, this is called the pinch off point (P). Beyond the pinch off point, the drain current remains essentially the same, because for $V_D > V_{DSat}$, at point P the voltage V_{DSat} remain the same. The no of carrier arriving at point P from source to drain remain same

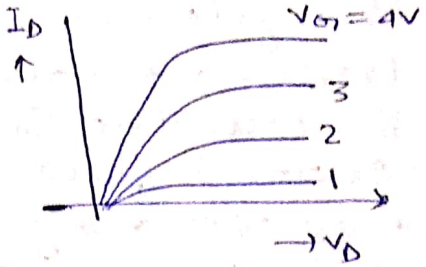
This is the saturation region, since I_D is const regardless of an increasing the drain voltage.

Types of MOSFET :-

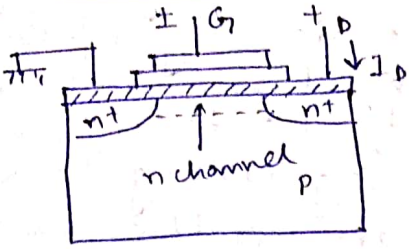
There are basically four type of MOSFETs, depending on the type of inversion layer. If at zero gate bias, the channel conductance is very low, we must apply a positive voltage to the gate to form the n-channel, then the device is a normally enhancement type n-channel MOSFET. Similarly if an n-channel exists at zero bias and we must apply a negative voltage to the gate to deplete carriers in the channel to reduce the channel conductance, then the device is depletion type n-channel MOSFET. Similarly, we have the p-channel ~~of~~ enhancement and depletion type MOSFET.

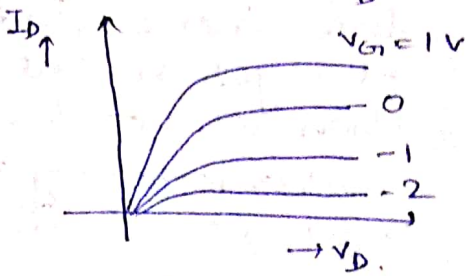
n channel enhancement



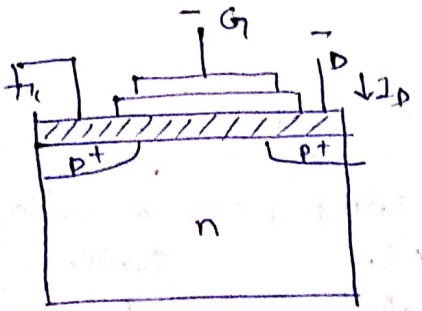


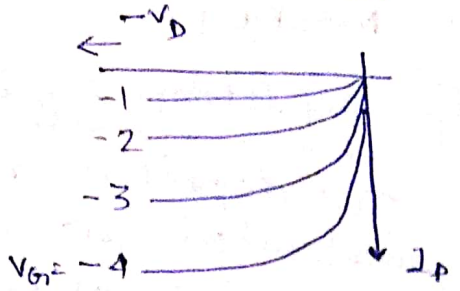
n-channel depletion



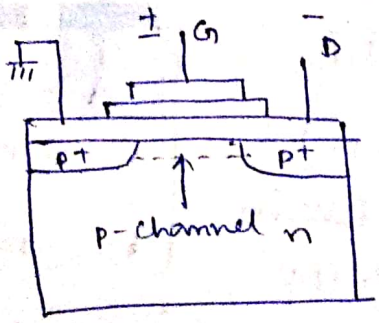


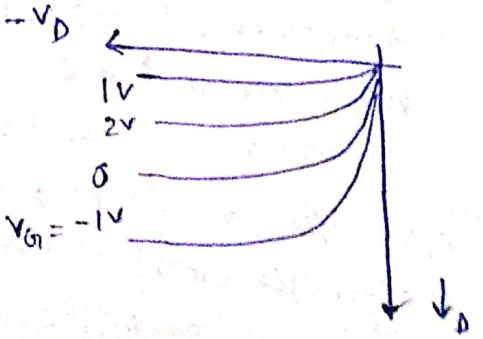
p-channel enhancement





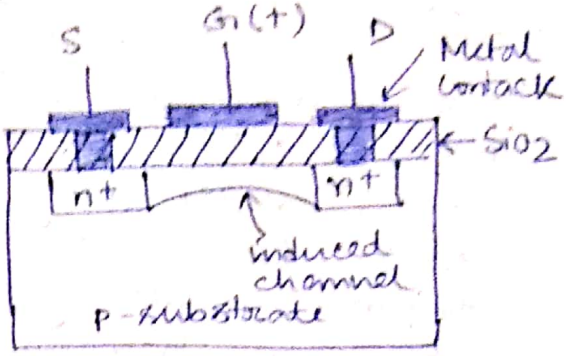
p channel depletion





Enhancement MOSFET :-

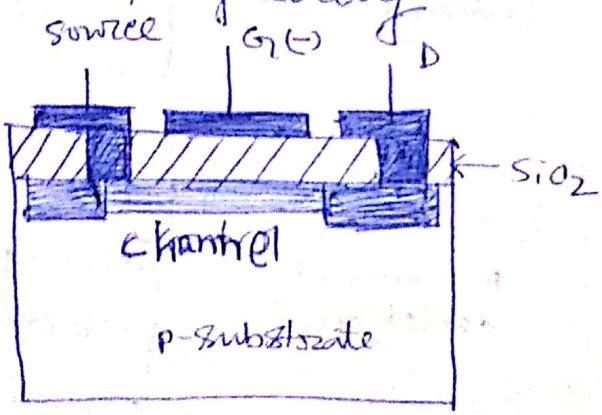
If the source and substrate are grounded, drain to source voltage is set to zero and a positive is applied to the gate of the enhancement NMOS transistor. The positive voltage repels the holes from the surface into the bulk of p-substrate. The minority electrons of the p-substrate are attracted to the positive gate and get accumulated in the region below the SiO_2 layer. These negative charges form an "inversion layer", when the gate-source voltage V_{GS} exceeds a threshold value V_T. The induced charges beneath the SiO_2 layer form an n-channel. current flow between source and drain. This current may be controlled by varying V_{GS}. This increased the density of induced negative charges in the channel increase and increased channel conductivity, hence drain current is enhanced by the negative gate voltage. Hence the device is known as the enhancement MOSFET.



n-channel enhancement MOSFET

Depletion type MOSFET :-

The depletion MOSFET has a physically implanted channel. Thus an n-channel depletion type MOSFET has an n-type silicon region connecting n+ source and the n+ Drain regions at the top of the p-type substrate.

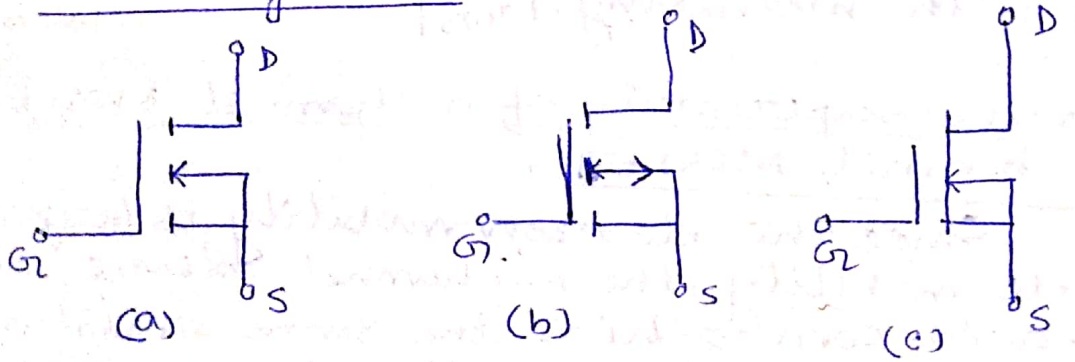


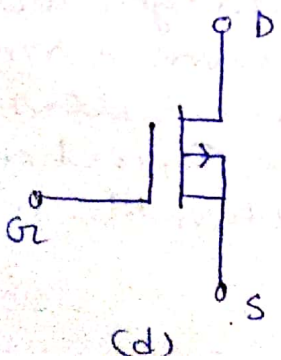
Thus if a voltage V_{DS} is applied between drain and source, a current I_D flows for $V_{GS}=0$. There is no need to induce a channel.

Now if a negative voltage is applied to the gate it repels electrons from the channel region towards the bulk of the P-substrate and attract holes from p-substrate towards the channel. The recombination between holes and causes a depletion of majority carriers in the channel region. This is why the device is called a depletion MOSFET. Enough negative gate voltage causes the channel completely depleted of charge carriers and I_D is reduced to zero even though V_{DS} may be still applied. This negative value of V_{GS} is the threshold voltage of the n-channel depletion type MOSFET.

A Depletion MOSFET can operated in the enhancement mode by applying a positive gate voltage to induce negative charges into the n-type channel. As a result the conductivity of the channel is enhanced and the drain current is increased.

Circuit symbols :-

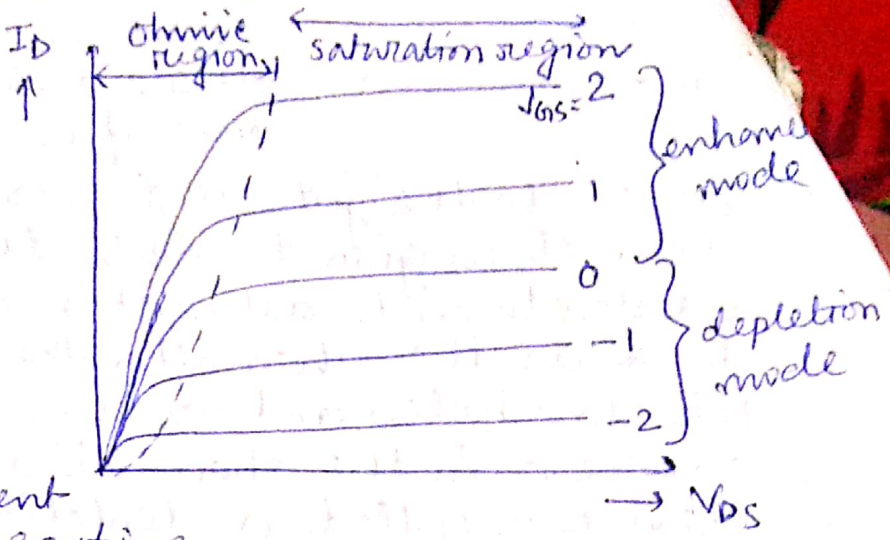




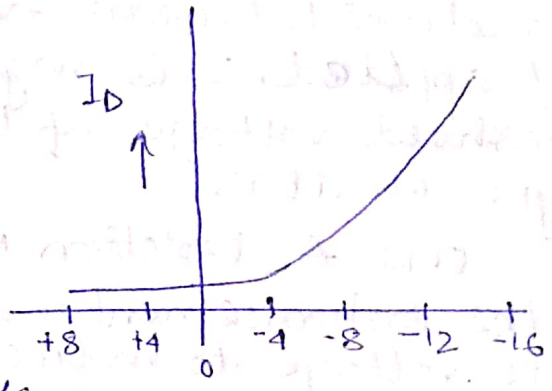
a) enhancement MOSFEM symbols a) n channel b) p-channel c) Depletion MOSFET c) n-channel d) p-channel.

Static characteristics of MOSFET :—

The drain characteristic of an n-channel MOSFET which can be used in either the enhancement mode or the depletion mode as shown in fig. The positive values of gate source voltage V_{GS} produce the enhancement mode whereas the negative values of V_{GS} result in the depletion mode.



The transfer characteristic of the MOSFET is shown in fig. This curve depicts the variation of the drain current I_D with V_{GS} for a given value of V_{DS}. The transfer characteristics shows that for $V_{GS} \geq 0$, drain current I_D is very small (typically a few nA). When V_{GS} is negative, $|I_D|$ rises slowly at first and then rapidly with increasing $|V_{GS}|$



Discuss the superiority of n-channel MOSFET over p-channel MOSFET.

Since the electron mobility is larger than hole mobility, the n-channel device with a small area can achive the same resistance as the p-channel device with a larger area. Hence n-channel MOSFETs can have a small size than p-channel. The n-channel device are faster in switching application. So, n channel device are more desirable than the p-channel structure.

Difference between depletion and enhancement MOSFETs

In depletion MOSFET a channel is diffused between the source and the drain. Thus a significant current flows through the device even when gate to source voltage is zero. Thus it is a normally on MOSFET.

But in enhancement MOSFET there is no channel between the source and drain when $V_{GS} = 0$. Here a channel is induced only when the gate voltage exceeds certain threshold value.

The depletion MOSFET came as part of the evolution towards enhancement MOSFET. A depletion MOSFET can be operated in either the depletion or enhancement mode. However, apart from a few special applications the depletion MOSFET is not used very much.

The enhancement MOSFET is widely used in both discrete and integrated circuits.

Why CMOS circuit have become more popular compared to NMOS/PMOS circuit?

CMOS circuit are high noise immunity and low static power consumption. CMOS devices do not produce as much waste heat as other form of logic, like NMOS. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS become the most popular compare to NMOS/PMOS