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(iii) Connection of the power supply  $\pm V$  to any wrong pin may damage the IC.

(iv) CMRR may be considered as the figure of merit of the OP AMP. Higher is the value of CMRR better is its quality.

### 6.3 OP AMP offset null adjustment :

The input offset voltage is very small (of the order of a few mV) and hence its effect may be ignored in many applications with relatively large enough

input voltages. But there are certain cases where its effect cannot be neglected. For example, in the use of an OP AMP as integrator, a small input voltage on integration may become large. For this various nulling adjustments are in use to minimise the effect of input offset voltage.

Some of the OP AMPS available in the market are provided with (integrated lag network) internal method of offset null adjustment. For example in OP AMP IC 741 for offset null adjustment the two ends of a  $10\text{k}\Omega$

potentiometer are connected to the pins 1 and 5 while the wiper (the potentiometer slider) is connected to  $-V$  dc supply. The OP AMP is operated in closed-loop mode by connecting the resistors  $R_1$  and  $R_2$  as shown in Fig. 6.3-1. Now choosing a convenient set of values of  $R_1$  and  $R_2$  (for example,  $R_1 = 1\text{k}\Omega$ ,  $R_2 = 10\text{k}\Omega$  or  $R_1 = 100\Omega$ ,  $R_2 = 10\text{k}\Omega$ ) the potentiometer knob is adjusted to get zero output voltage. The offset voltage is thus nullified and the OP AMP is now ready for use.

The above internal method of offset balancing has many disadvantages. It can cause significant variation in gain characteristic, it can induce additional voltage drift with temperature, etc. In

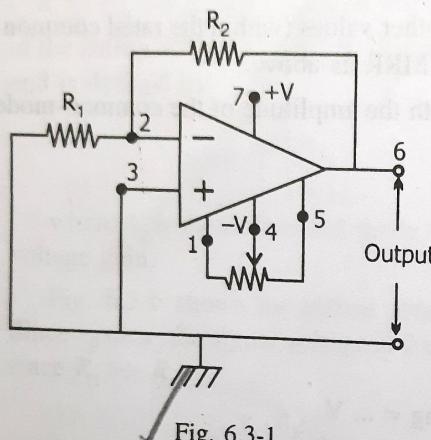


Fig. 6.3-1

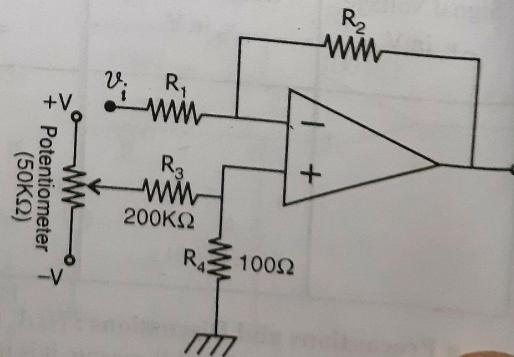


Fig. 6.3-2

versions of OP Universal Balance amplifier. Here the output zero. inverting OP AM

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12 V and  $R_3 =$

Similar tech used for offset non-inverting

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6.4(A) To stud

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• Theory : (a)  
is shown in Fig.

where  $V_o$  and

versions of OP AMP the above technique is not applicable and we use *Universal Balancing Techniques* which do not involve internal circuitry of the amplifier. Here the basic idea is to apply a small *dc* voltage to the input to make the output zero. Fig. 6.3-2 shows the universal offset balancing circuit for an inverting OP AMP. By adjusting the potentiometer knob it is possible to apply

to the inverting input a voltage in the range  $\pm V$ .  $\frac{R_4}{R_3 + R_4} = \pm 6 \text{ mV}$  if  $V = 12 \text{ V}$  and  $R_3 = 200 \text{ k}\Omega$ ,  $R_4 = 100 \Omega$ .

Similar technique can also be used for offset balancing of a non-inverting OP AMP.

The effect of offset voltage can also be minimised by connecting effectively equal resistances to the input terminals as shown in Fig. 6.3-3, where  $R_p = R_1 // R_2$ . With this choice and when output is low, the bias currents, which are usually very nearly the same, flow through equal resistances causing almost equal voltages to appear at the inverting and non-inverting inputs. So there will be no differential input voltage. To take into account differences in  $I_{B1}$  and  $I_{B2}$ ,  $R_p$  can be taken as a variable resistor and adjusted for minimum output offset.

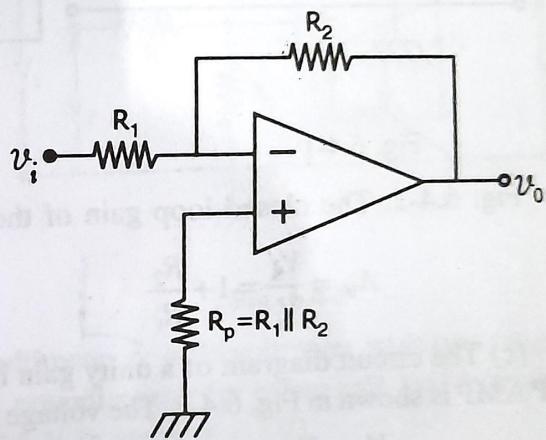


Fig. 6.3-3

**6.4(A) To study the use of OP AMP as (a) an inverting amplifier, (b) a non-inverting amplifier, (c) a unity gain buffer, (d) an adder and (e) a differential amplifier :**

• **Theory :** (a) The circuit diagram of an inverting amplifier using OP AMP is shown in Fig. 6.4-1. The closed loop gain of the inverting amplifier is

$$A_v = \frac{V_o}{V_i} = -\frac{R_2}{R_1} \quad \dots (6.4-1)$$

where  $V_o$  and  $V_i$  are the output and input voltages respectively.

(b) The circuit diagram of a basic non-inverting OP AMP is shown in

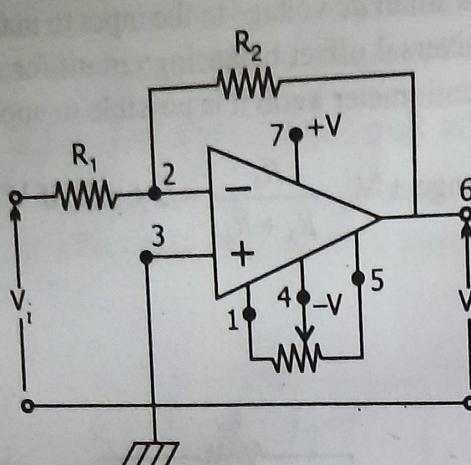


Fig. 6.4-1

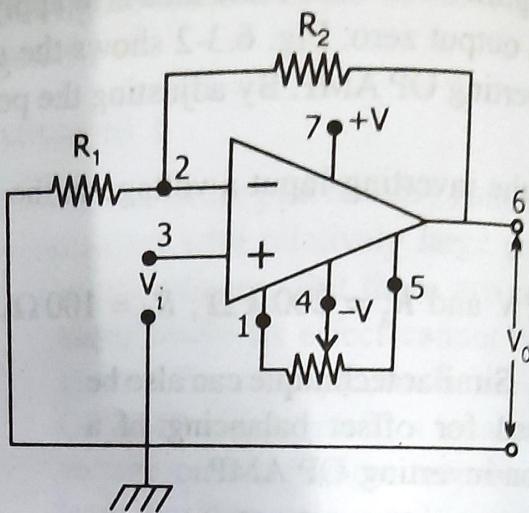


Fig. 6.4-2

Fig. 6.4-2. The closed loop gain of the non-inverting OP AMP is

$$A_V = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1} \quad \dots (6.4-2)$$

(c) The circuit diagram of a unity gain buffer or voltage follower using an OP AMP is shown in Fig. 6.4-3. The voltage gain of the stage is unity and hence

$$V_o = V_i \quad \dots (6.4-3)$$

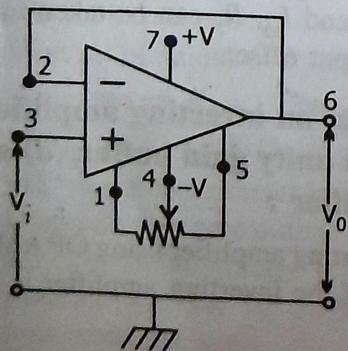


Fig. 6.4-3

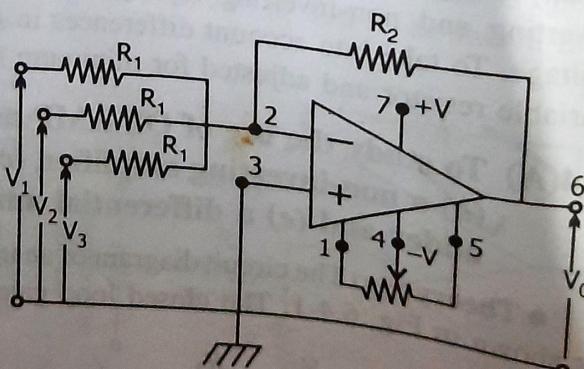


Fig. 6.4-4

(d) The circuit diagram of a three input adder using an OP AMP is shown in Fig. 6.4-4. The output voltage  $V_o$  is given by

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OP AMP : IC 741

Power supply :  $\pm \dots$  V

#### (A) Adjustment for offset null :

TABLE I

No. of obs.	Position of potentiometer slider	Output voltage in V
1	Extreme right	...
2	Extreme left	...
3	Intermediate (1)	...
4	Intermediate (2)	0.00 (offset null)

**(B) Data for inverting amplifier :**

## TABLE II

(C) Data for non-inverting amplifier :

**TABLE III**

[Make a chart similar to TABLE II. Write  $A_v = 1 + \frac{R_2}{R_1}$  in the last column]

(D) Data for unity gain buffer :

**TABLE IV**

No. of obs.	Input voltage $V_i$ in V	Output voltage $V_o$ in V	Experimental gain from graph			Theoretical gain
			$\Delta V_i$ in V	$\Delta V_o$ in V	$A_v$	
1	...	...				
2	...	...				
3	...	...				
...	I					
...			...	...	...	
...						
...						
...						
10	...	...				

(E) Data for Adder :

**TABLE V**

Resistances in $\Omega$		No. of obs.	Input voltage in V			Output voltage $V_o$ in V	
			$V_1$	$V_2$	$V_3$	Experimental	Theoretical $-\frac{R_2}{R_1} (V_1 + V_2 + V_3)$
$R_1$	$R_2$	1	...	...	...	...	...
		2	...	...	...	...	...
		3	...	...	...	...	...
		...	...	...	...	...	...
		10	...	...	...	...	...
		1	...	...	...	...	...
		2	...	...	...	...	...
		...	...	...	...	...	...
		...	...	...	...	...	...
		10	...	...	...	...	...

(F) Input-output data for the differential amplifier :

TABLE VI

Resistances in $\Omega$		No. of obs.	Input voltage in V			Output voltage $V_o$ in V
$R_1$	$R_2$		$V_1$	$V_2$	$V_i = V_2 - V_1$	
...	...	1	...	...	...	...
		2	...	...	...	...
		3	...	...	...	...
		...	...	...	...	...
		10	...	...	...	...
...	...	1	...	...	...	...
		2	...	...	...	...
		...	...	...	...	...
		...	...	...	...	...
		10	...	...	...	...

(G) Comparison of theoretical and experimental gains :

TABLE VII

Resistances in $\Omega$		Experimental gain from graph			Theoretical gain $A_v = \frac{R_2}{R_1}$
$R_1$	$R_2$	$\Delta V_i$ in V	$\Delta V_o$ in V	$A_v = \frac{\Delta V_o}{\Delta V_i}$	
...	...	...	...	...	...
...	...	...	...	...	...

• Precautions and Discussions : (i) The value of closed loop gain and the input voltages should be so chosen that the output voltage remains well below the supply voltage ( $\pm V$ ). This restricts the OP AMP operation over the linear region. With  $\pm 12$  V supply the output should not exceed 8 volts.

(ii) Offset null adjustment is necessary for accurate results.

(iii) In differential amplifier if the input voltage ( $V_2 - V_1$ ) is small and comparable to offset voltage then offset null adjustment is very important before taking readings. However, if the voltage difference  $V_2 - V_1$  is chosen large in comparison to offset voltage then offset null adjustment can be skipped.

(iv) Due to error. This can two inputs. For between the n

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(vi) While should be take the IC.

#### 6.4 (B) To st

- Theory : The output voltage :

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$v_i$

where  $f$  is the

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$2\pi R_1 C_2$  is obtaine

~~(iv)~~ Due to unequal loading of the two input terminals there may be offset error. This can be minimised by connecting effectively equal resistances to the two inputs. For example, in Fig. 6.4-1 a resistance  $R_p = R_1 \parallel R_2$  can be connected between the non-inverting terminal and the ground.

~~(v)~~ The output voltage  $V_o$  may be positive as well as negative. So the polarity of the measuring voltmeter should be changed accordingly.

~~(vi)~~ While connecting the power supply  $\pm V$  to the IC OP AMP special care should be taken. Connection of the power supply to any wrong pin may damage the IC.

#### 6.4 (B) To study the performance of an OP AMP integrator :

- Theory : Fig. 6.4-12 shows the basic circuit of an OP AMP integrator. The output voltage  $v_o$  is found to be proportional to the integral of the input voltage :

$$v_o = -\frac{1}{R_1 C_2} \int_0^t v_i dt + K \quad \dots (6.4-7)$$

where  $K$  is the constant of integration and is proportional to  $v_o$  at  $t = 0$ .

A large capacitor may be used to block the *dc* output of the integrator. So we can assume  $K = 0$ .

If the input voltage is a constant  $v_i = V$ , then the output will be a ramp,

$$v_o = -\frac{V}{R_1 C_2} \cdot t \quad \dots (6.4-8)$$

If the input is a square wave, the output will be a triangular wave.

If the input is sine wave,  $v_i = V_0 \sin \omega t$ , then the output will be a cosine wave,

$$v_o = \frac{V_0}{R_1 C_2 \omega} \cos \omega t \quad \dots (6.4-9)$$

or, 
$$\left| \frac{v_i}{v_o} \right| = R_1 C_2 \omega = 2\pi R_1 C_2 f \quad \dots (6.4-10)$$

where  $f$  is the frequency of the input signal.