## Filld effect transistore

The field effect transistors on FET is a semiconductors device with the output coverent controlled by an electric field. Since the ewvient is causied predominately by one type of cavaiers, the FET is known as a mipolar transistors. Thus it is different from the bipolar transistors conich involves two types of cavaiers i.e electron and holes. FET is a three turninal semiconductors device howing a single P-n Imetion and is extensively in many digital & some analog circuit.

Comparison between FET and BJT:-

i) The input impedence of the FET is very high (about 1 mega-ohm) compeared to that of a BJT. I ii) The operation of FET depends only one type of courier i.e majority courier so it is unipolar device. On the other hand BJT is bipolar device becouse both majority and uninority carrier are involved fore its operation.

iii) The operation of FET depends on applied electric field so it is voltage control device. But the operation of BIT depends on emitter current so it is called current control device.

IN FET IS LESS noisy than BIT

D FET has higher switching speed and can be operated at higher trequency because there is no vimoruty cavilers. 400 BIT is lower switching speed the FET.

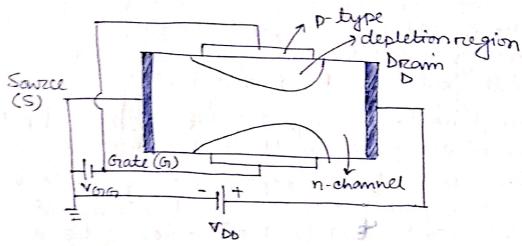
veice

## Field effect transistor

Junction field	d effect transiston	Meta	L oxid Remicon- ore FET (MOSFET)
n-channel JFET	p-channel JFET De	pletion of MOSFET	Enhancement type MosfeT
depletin		- channel Letion type [ n-channi enhancemen	p-channel

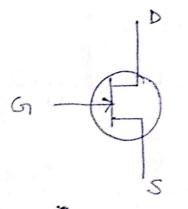
Scanned with CamScanner

The IFET consists of a uniformly doped service ordered bor is usually of Si for GraAs. The bor has obmic contacts at the two ends and Remiconductor Imetions on its two sides. If the Remiconductors bor is n-type, the IFET is called an n-channel IFET. If the bor is p-type, the device is termed a p-channel

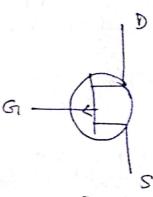


impurities opposite to that of the bor i. e p-type impurities for an n-type bor and vice versa.

Everent is caused to flow through the bar by applying a valtage between the end turnmal. The terminal through which the majority caviers benter the bar is called the drawn source, and through which the majority cavier leave the bar is called the drawn. The region of the bar is called the drawn. The region of the bar between the two gate regions through which majority caviers move from source to drawn is called the channel.



torn-channel

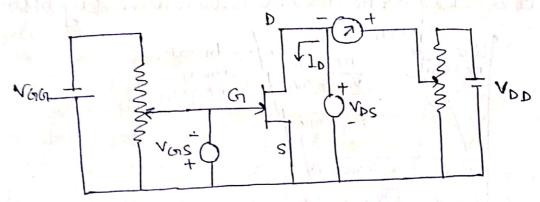


circuit symbol for p-channel JFET:

poperation;

The junction between the bour and the gate is reverse biased by a pplying a veltage voice as shown in fig (1). The resulting depletion regions extend into the bour. The widths of the depletion regions can be controlled by changing the gate to sowrce valtage. The depletion regions are devoid of coverent caviers, so that conductivity of these regions is nominally more. Therefore, the effective erross sectional area through colich the coverent flows in the bour decreases with increasing, reverse bias. It follows that for a given drawn to sowice valtage, the drawn coverent is a function of the gate to sowice valtage. The name field effect is used for the device because the transverse field produced by the gate gives the effect of controlling the drawn coverent.

## Static Characteristics of a IFET: -

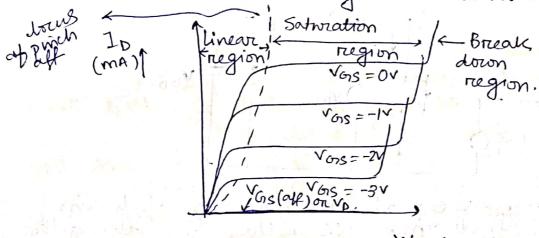


In common source mode the variation of drain current Is with drain source vallage Vs taking the gate source vallage Vs as parameter gives the common source drain characteristics.

Each of characteristic curves can be dinded into three region (i) linear region (ii) saturation region (iii) breakdown region.

for Vors = 0v, the channel between the gate regions is entirely open and the bar acts as a simple resistor. So, as Vos is increased throm yero ID merie ases linearly with it. As ID increases the ohmic veltage drop along the n-type channel region reverse biases the gate Innotions. Depletion

layors are formed and the effective conducting channel crosspection decreases. Because of the gradual ohmic potential drop along the length of the channel the gate becomes more reverse biased near the drain end than at the source end. So, the depletion region mercases as we go from source to dram end. As VDS 18 increased more the channel becomes navvower coursing the resistance between the source and drawn to make This makes ID vs VDS curve nonlinear. At some value of vos, the depletion region meet near the drain to pinchaff the channel. In pinch-off condition the current almost saturates. This value of vos is the souration voltage Vosat. Beyond prich aff, the current ID sativiates at a value I psat. At high values at VDS, Is suddenly rise to large value. This is due to avalanche breakdown across the reverse biased gate Junction, the region of the characteristics is called to breakdown region as shown in tig below.



- VDS(V)

In saturation region ID depends on the reverse biasing gate valtage Vois. The variation of ID with gate to sowice reverse bias valtage Vois at a constant value of VDS gives the transfer characteristic curve as shown in tig. The

TID (MA)

saturation dram coverent at VGS =0 is denoted by IDSS. IDSS represents the upper limit on the JFET currenty The shape of the transfer curve is very nearly parabolic and can be approximately represented by Shockley's equation  $I_{D} = I_{DSS} \left(1 - \frac{V_{GIS}}{V}\right)^{2}$ 

where vp = pinch aff valtage?

Explain BJT is called coverent control device but FET is a valtage control device".

In a BIT, emitter base Junction is forward biosed. So, the impedence of the emitter circuit is low and a coverent flows between the emitter and the base. A change in the emitter coverent causes a change in the collector coverent in a BIT. Thus a BIT is a coverent controlled device.

In a FET, the application of a gate valtage courses a very small gate current since the input impedence at the gate is very high. A change in the gate valtage controls the drawn current. Thus the FET is known as valtage controlled device.

FET parameter:

The analytical method of analysis of JFET amplifiers invalves three parameters, called JFET parameters. These are defined below:

i) Dram resistance (rd): - It is the a.c resistance between drain and source terminals and is defined as the ratio of the small change in drain valtage to the corresponding change in drain current at a constant gate valtage. i.e

ra = dvos | vos = constant.

ii) Mutual conductomel (gm): - It is defined as ratio of small change in drawn current to the consultage and change in the gate vallage at a constant drawn vallage, i.e.,

gm = DID DVGS VDS = constemt. os the small change in drain vallage to the conresponding change in the gate vallage for a constant drain ewvent, i.e.,

 $\mu = -\frac{\delta V_{OS}}{\delta V_{GS}}|_{J_p} = constant.$ cohere -ve sign indicates that any change in

In due to a positive increment up V\_{OS} is to be

counterbalanced by a -ve increment ap V\_{GS}.

Relation between 11, ma & gm -

The drawn current ID 18 a function of drawn voltage VDS & gate voltage Vois 1.e

$$I_{b} = f(Y_{DS}, V_{GS})$$

$$\therefore dI_{b} = \frac{\partial I_{b}}{\partial V_{DS}} \left| dV_{DS} + \frac{\partial I_{D}}{\partial V_{GS}} \right| dV_{GS}$$

It vos and vois are smultaneously so changed that Lo remain constant, then dID=0

$$\frac{\partial l_{D}}{\partial v_{DS}} | \cdot dv_{DS} + \frac{\partial l_{D}}{\partial v_{GS}} | dv_{SS} = 0$$

$$\frac{\partial l_{D}}{\partial v_{DS}} | \cdot \frac{\partial v_{DS}}{\partial v_{SS}} | + \frac{\partial l_{D}}{\partial v_{GS}} | = 0$$

$$\frac{\partial l_{D}}{\partial v_{DS}} | \cdot \frac{\partial v_{DS}}{\partial v_{SS}} | = 0$$

$$\frac{1}{2}\left(-\mu\right)+9m=0$$

drain valtage to the seal mp. B= M Kens

n channel JFET

1) In a channel IFET, coverent coveriers are electron of mobility of electron is large

ii) Imput noise is less iii) transconductance is Large than p-channel JFET

## P-channel JFET

1) In p-channel JFET, coverent evoyers are holes and mobility of holes is poor.

ii) Input noise is more iii) tramsconductance is smaller in p-channel JAET than n-channel JAET.