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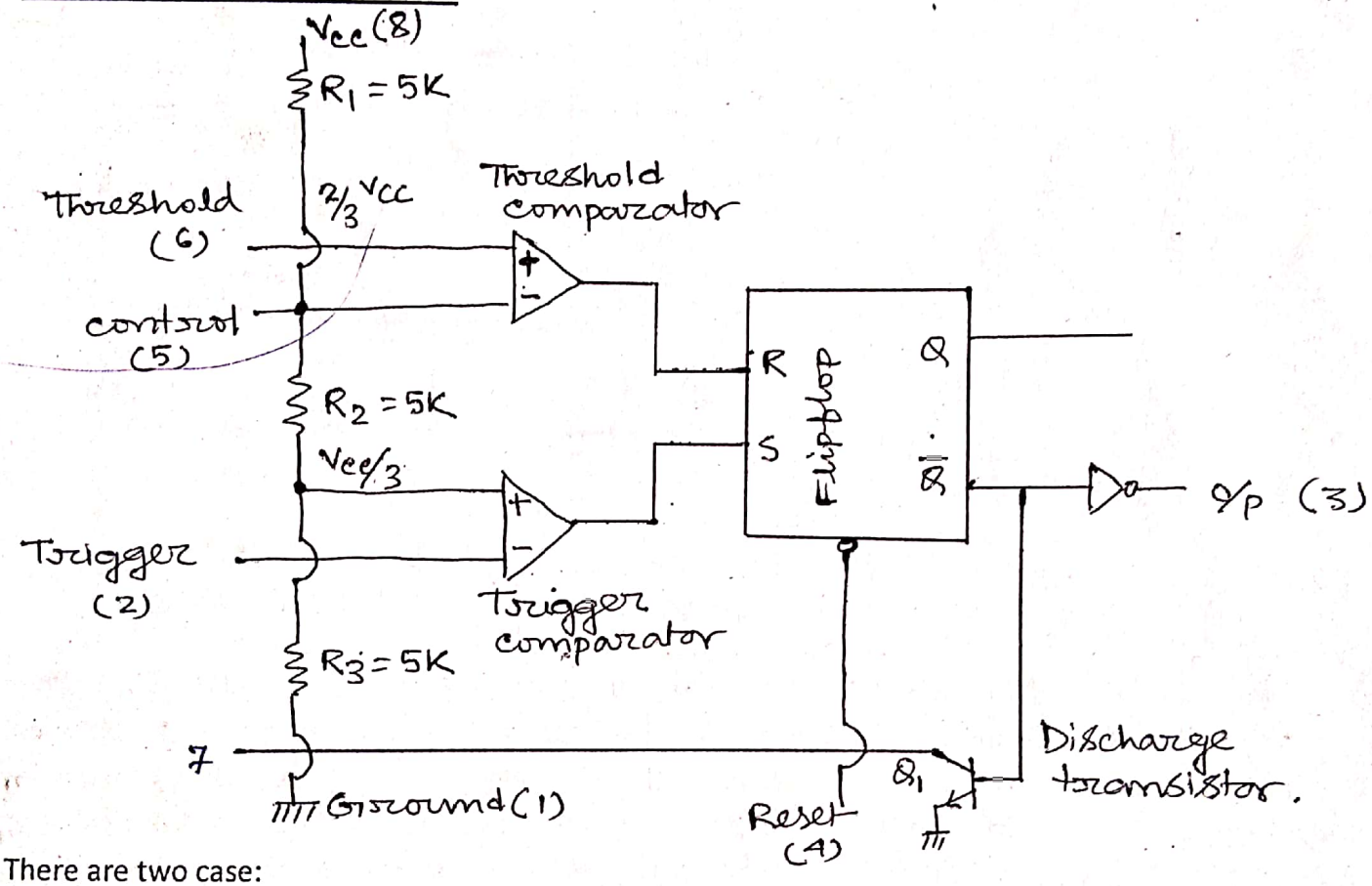
Architecture of 555 timer:



There are two case:

1)The threshold comparator o/p is high when the threshold pin(pin 6) goes above 2Vcc/3 & 2)the trigger comparator o/p is high when the trigger pin (pin 2)goes below Vcc/3.

Case 1:when the voltage at pin 6 exceeds 2Vcc/3, the o/p of the threshold comparator jumps high, which reset the Flip Flop i.e $\overline{Q}$ high & the o/p of the timer become low. When $\overline{Q}$ is high, the internal NPN transistor Q_1 goes into saturation & the discharge pin (pin 7)is pulled down near to the ground by this saturated transistor.

Case 2: When the voltage at pin2 goes below Vcc/3, then the trigger comparator o/p jump high which sets the Flip Flop i.e $\overline{Q}$ is low & o/p of the timer become high. For low o/p at $\overline{Q}$ the transistor Q_1 is cutoff & the discharge pin(7) can not pass any current through the transistor Q_1 i.e pin 7 is virtually disconnected.

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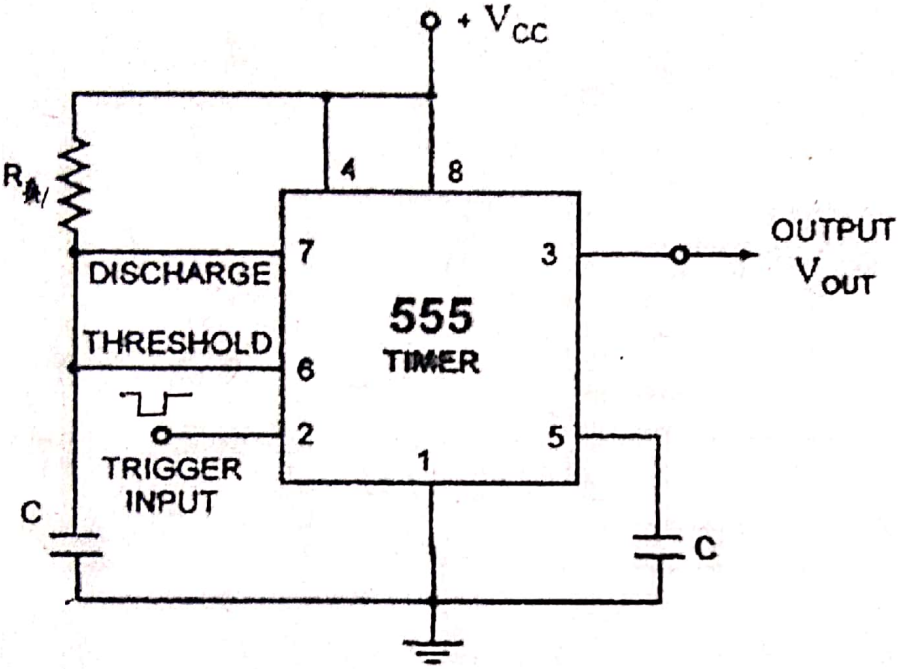
If pin4 is made low then $\overline{Q}$ o/p of the RS filpflop becomes high & o/p becomes low. If the reset pin is not used,then this pin should be made inactive by connecting this to a power supply.

Monostable multivibrator using 555 timer:



Circuit of The Timer 555 as a Monostable Multivibrator

Stable state: In fig. show a monostable multivibrator when the power is switched on before any trigger input, the capacitor c will try to be charged toword V_{cc} through R, while charging, the capacitor voltage will reaches 2Vcc/3 at the threshold pin (pin 6). This will causes the o/p of the threshold comparator to jump high. This will reset the internal RS flipflop. Therefore $\overline{Q}$=1 & the o/p (pin 3) will be low because of the inverter is connected to $\overline{Q}$. The high o/p of $\overline{Q}$ will saturate the internal transistor & for this reason the capacitor C will be fully discharge through the discharge pin(pin 7) & the saturated transistor to the ground. Thus in absence of any trigger the capacitor is completely discharge & the o/p is low. This is the stable state of the circuit.

Quasi stable state: when the trigger pin of the timer is forced to go below Vcc/3 using a negative going pulse, the trigger comparator o/p will be high which set the flipflop ($\overline{Q}$=0),cut off the internal transistor, discharge pin 7 is practically isolated from the ground & the time o/p jump high. The isolation of the discharge pin will allow the capacitor C to charge through the external resistor R toword Vcc with a time const. RC . The timing diagram is shown below.

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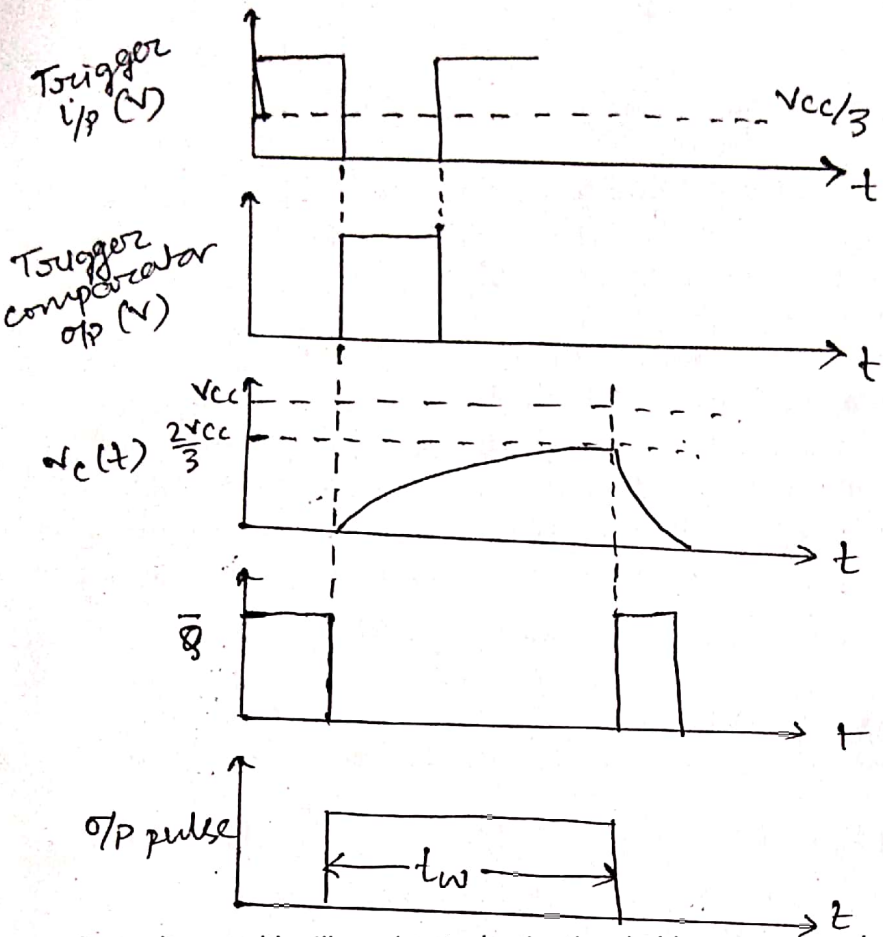
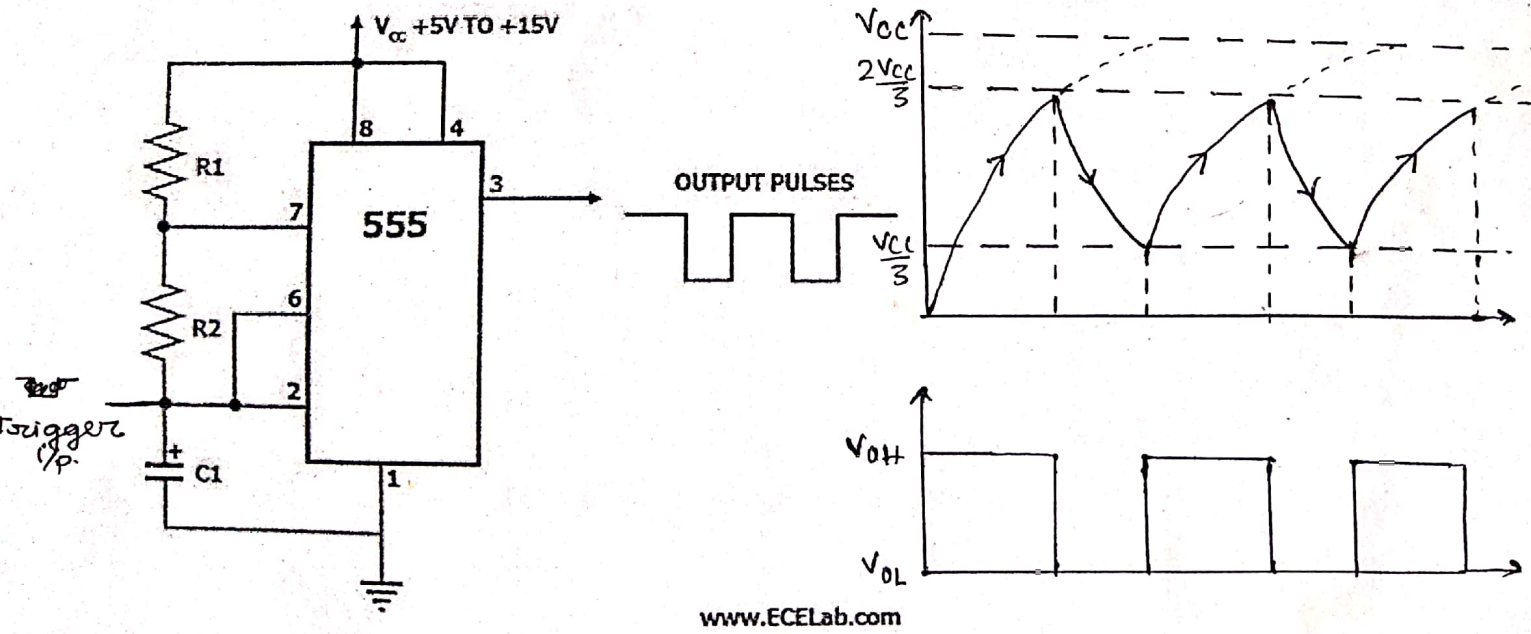


The capacitor voltage Vc(t) will reach 2Vcc/3, the threshold comparator o/p high & reset the RS flipflop. This markes the time o/p low and again saturated the internal transistor. This saturated transistor is now able to discharge pin 7 to the ground & the ckt goes back to the stable state again.

Astable multivibrator using 555 timer:



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When the power supply is switched on the capacitor C_1 acts as a short ckt to ground & the timer is triggered as the capacitor is connected to the trigger pin. So the o/p of the timer becomes high (VoH) &

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the discharge pin is practically isolated from the ground as the internal transistor of the timer is at cutoff condition because of low $\overline{Q}$ o/p of the internal RS flipflop. Thus the capacitor begins to charge towords Vcc through the resistor R_1 & R_2 with time const. $(R_1 + R_2)C$, but as soon as the capacitor voltage Vc(t) reaches 2Vcc/3 the threshold pin (pin 6) sense this voltage & the internal threshold comparator o/p a high voltage which in turn reset the internal RS flipflop of the timer. Thus the $\overline{Q}$ o/p of this flipflop goes high & o/p at pin 3 goes low. Under this condition the internal transistor goes to saturation & the discharge pin is shorted to ground through the saturated transistor. Now the charged capacitor start to discharge through resistance R_2. when Vc(t) at this moment the timer is triggered again. This triggering leads to setting of the internal RS flipflop & so $\overline{Q}$ becomes low, the o/p of the timer becomes high & the discharge path is cut off. Now the capacitor repeats charging again.

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