1. Specification

1-1. Abstract

This document describes the results of Power Integrity Simulation for Spartan-7 Evaluation Board.

1-2. Tools

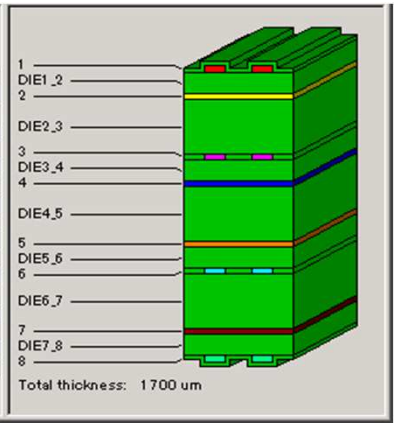
	Product Name	Supplier
Voltage drop simulation	SignalAdviser-PI V2.7 (2.07.00496)	FUJITSU Advanced Technologies

1-3. Analysis conditions

1-3-1. Board structure

	Color	Layer Name	Type	Usage	Thickness um	Er	Loss Tangent
1			Dielectric	Solder Mask	25	3.3	0.02
2		1	Metal	Signal	40	<Auto>	<Auto>
3		DIE1_2	Dielectric	Substrate	115	4.3	0.016
4		2	Metal	Plane	35	<Auto>	<Auto>
5		DIE2_3	Dielectric	Substrate	300	4.3	0.016
6		3	Metal	Signal	35	<Auto>	<Auto>
7		DIE3_4	Dielectric	Substrate	115	4.3	0.016
8		4	Metal	Plane	35	<Auto>	<Auto>
9		DIE4_5	Dielectric	Substrate	300	4.3	0.016
10		5	Metal	Plane	35	<Auto>	<Auto>
11		DIE5_6	Dielectric	Substrate	115	4.3	0.016
12		6	Metal	Signal	35	<Auto>	<Auto>
13		DIE6_7	Dielectric	Substrate	300	4.3	0.016
14		7	Metal	Plane	35	<Auto>	<Auto>
15		DIE7_8	Dielectric	Substrate	115	4.3	0.016
16		8	Metal	Signal	40	<Auto>	<Auto>
17			Dielectric	Solder Mask	25	3.3	0.02

☑ Calculate Er for metal layers from surrounding dielectrics



Volume resistivity: 2.09e-8 [ohm*m] （cupper 70 deg）

1-3-2. Temperature conditions

Environment temperature 70 deg

1-3-3. Analysis Target Nets

a)DC analysis

Net Name	Measurement Poir	Voltage[V]	Maximum Current Consumption[A]	Voltage drop Tolerance[V]
V1.0 (V1.0_FPGA)	U201	1.00	10.0000	0.05

b) impedance analysis

Net Name	Measurement Poir	Voltage[V]	Current Variation[A] (25% Imax)	Voltage Variation Tolerance[%]	Target impedance [mohm]
V1.0 (V1.0_FPGA)	U201	1.00	2.5000	2	8.0

1-3-4. Target impedance

In UG483(v1.14) May 21,2019 7 Series FPGAs PCB Design Guide of Xilinx, there is no description of target impedance, the following value, calculated based onUG583 (v1.16) June 26, 2019 UltraScale Architecture PCB DesignUser Guide are used.

$$Ztarget=\frac{VoltageRailValue \times \frac{\%Ripple}{100}}{StepLoadCurrent} = 0.008\ \Omega$$

@100KHz～10MHz

Ripple	2 %
VoltageRailValue	1 V
StepLoadCurrent	10 A
StepLoad	25 % (VCCINT)

1-3-5. On-chip（On-PKG）capacitance

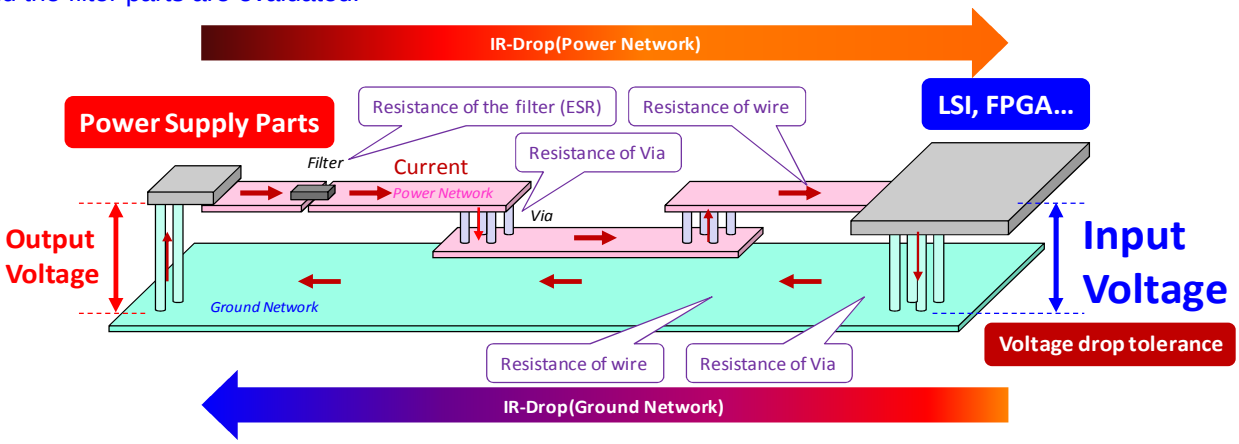
Package capacitor is not included in Spartan-7.

2. Overview of power integrity analysis

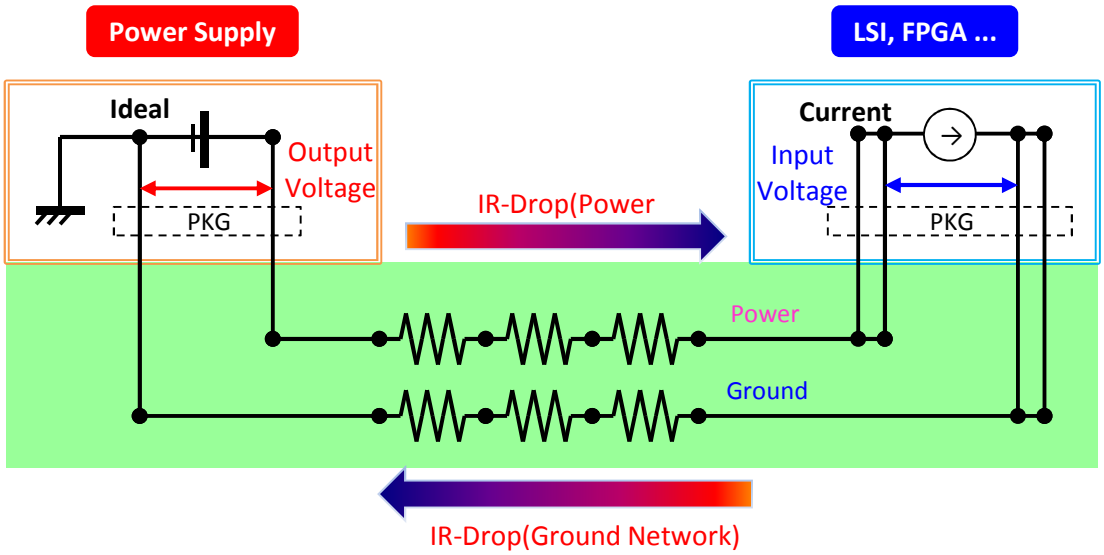
2-1. DC analysis（Voltage drop analysis）

Analyzes the voltage drop affected by pattern of power supply, vias and inserted parts from the power supply parts to the analysis objects. Then the value of voltage drop is checked if it meets the tolerance of the object being analyzed.

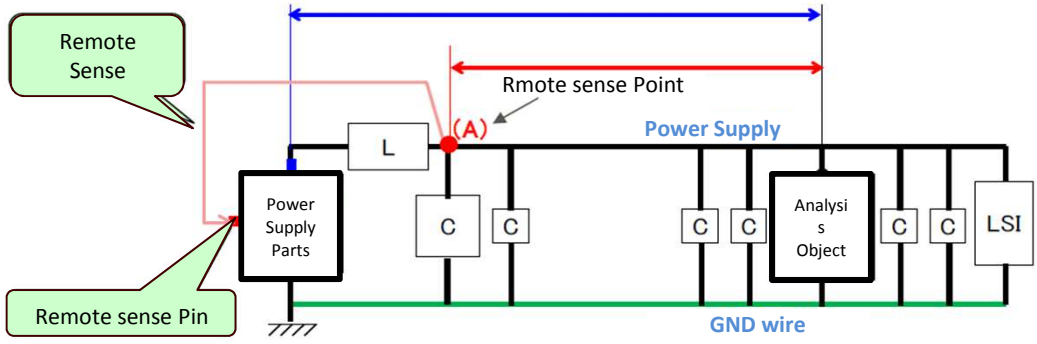
With this analysis, placement of power supply parts and the analysis target object, width or length and route of the pattern of the power supply, board layout structure(copper thickness and number of layers) and the filter parts are evaluated.



Considering the power supply source as an ideal supply, the voltage drop of the power supply system on the board is observed with the models and a current value is given to the analysis object



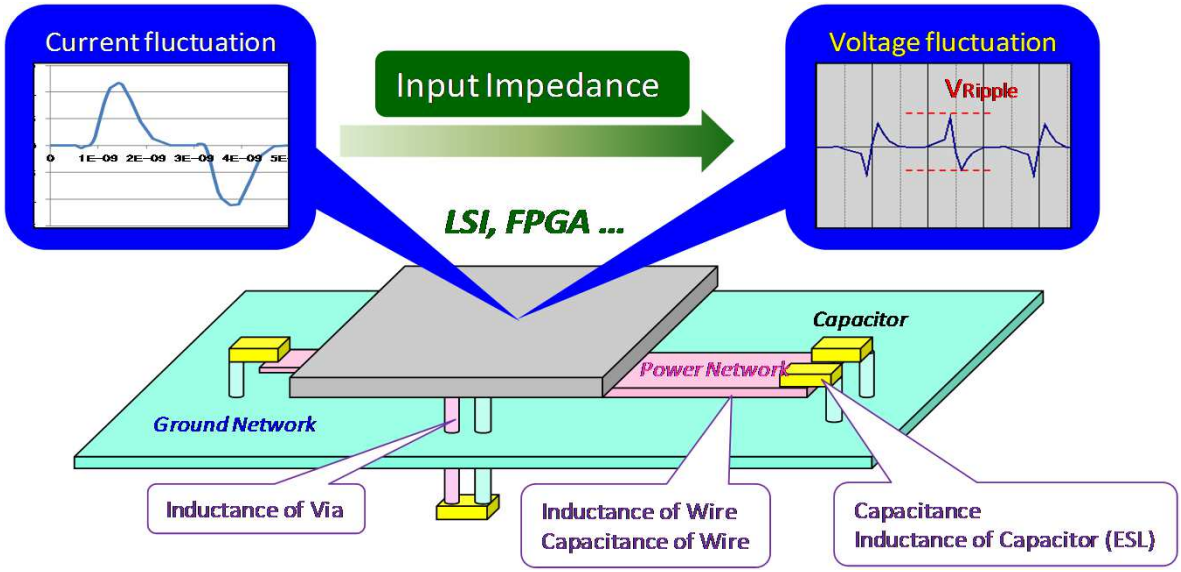
In case that there is a remote sense circuit in the model of analysis object, setting the remote sense pin and the voltage drop (equivalent to the voltage drop from remote sense point (A)) is analized.



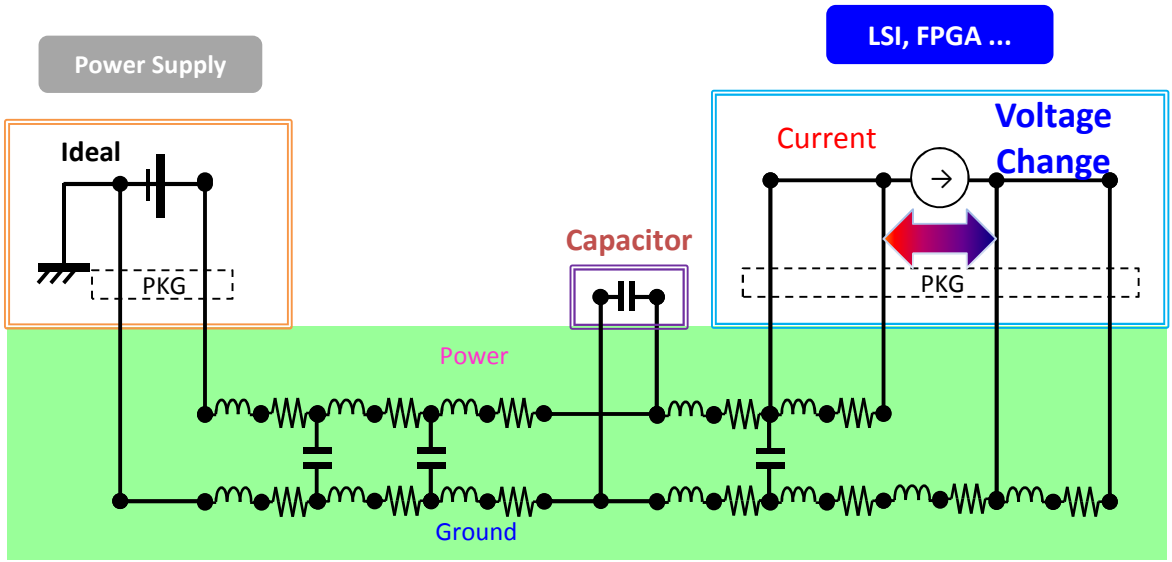
2-2. Impedance analysis

By analizeng the voltage swing coused by swing of current at LSI or FPGA operating as input impedance, it is possible to check if it is within the target impedance of the IC requirement

With this analysis, the capacitance value, number, arrangement of the capacitor,and power supply pattern that determine the input impedance can be evaluated.



With the voltage between power supply and GND when forcing 1A of AC current to analysis object, input impedance of analysis object is observed. Then the input impedance is checked if it is within the target impedance of the device requirement.



The default setting of SoC power supply current characteristics are as follows:

・Maximum operating frequency 100MHz

・Tr, Tf 1/10 of period

3. Results of analysis

3-1. Results of DC analysis（voltage drop analysis）

The voltage drop is assumed to meet the tolerance required by the device
There seems to be no problem in selecting parts like the power supply patterns(width or length of wire, thickness of copper) from the power supply IC to each LSI.

Power Supply	Net Name	Parts (From)	Voltage (From)[V]	Parts (To)	Voltage (To)[V]	ΔV [mV]	Voltage Drop [mV]	Tolerance [mV]	Judgement	Current [A]
1.0V	V_1.0_FPGA	Q1	1.0000	U201	0.8660	134.0	**144.1**	-	-	10.0
	(GND)	Q1	0.0000	U201	0.0101	10.1				
	V_1.0_FPGA	U1	1.0092	U201	0.8660	143.2	**144.2**	-	-	
	(GND)	U1	0.0092	U201	0.0101	1.0				
1.0V	V_1.0_FPGA	U1_14	0.8671	U201	0.8660	1.1	**2.0**	50.0	OK	10.0
	(GND)	U1	0.0092	U201	0.0101	1.0				

* Detail are described in 4. Results of DC analysis.

*1 Voltage drop from the output of power supply IC are large because of including DCR of the coil.
Voltage drop from volage control feedback terminal is low.

*2 Resistance value of feedback terminal is 0.001fohms between power supply to FB terminal and 1000Tohms between FB terminal to GND.（Because feedback control is not supported in simulation.）

3-2. Results of Impedance analysis

It is considered that the number, value and arrangement of mounted capacitors are optimized after meeting the design specification.

Power Supply	Net Name	Monitor Device	Power Supply Voltage[V]	Swing Current [A] Imax/4	Voltage Tolerance[%]	Target Impedance「mΩ]	comment
1.0V	V_1.0_FPGA	U201	1.0	2.5	2	**8 (100KHz～10MHz)**	**Input impedance are within the target**

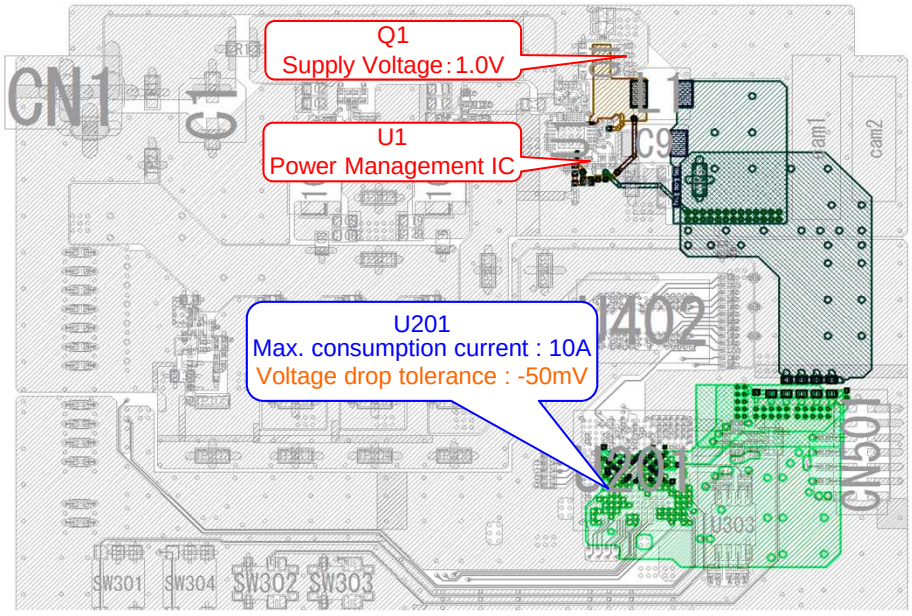
* Detail are described in 5. Results of Impedance analysis.

*1 In impedance analysis, model of coil is treated as shorted.
（To measure the input impedance after LC）

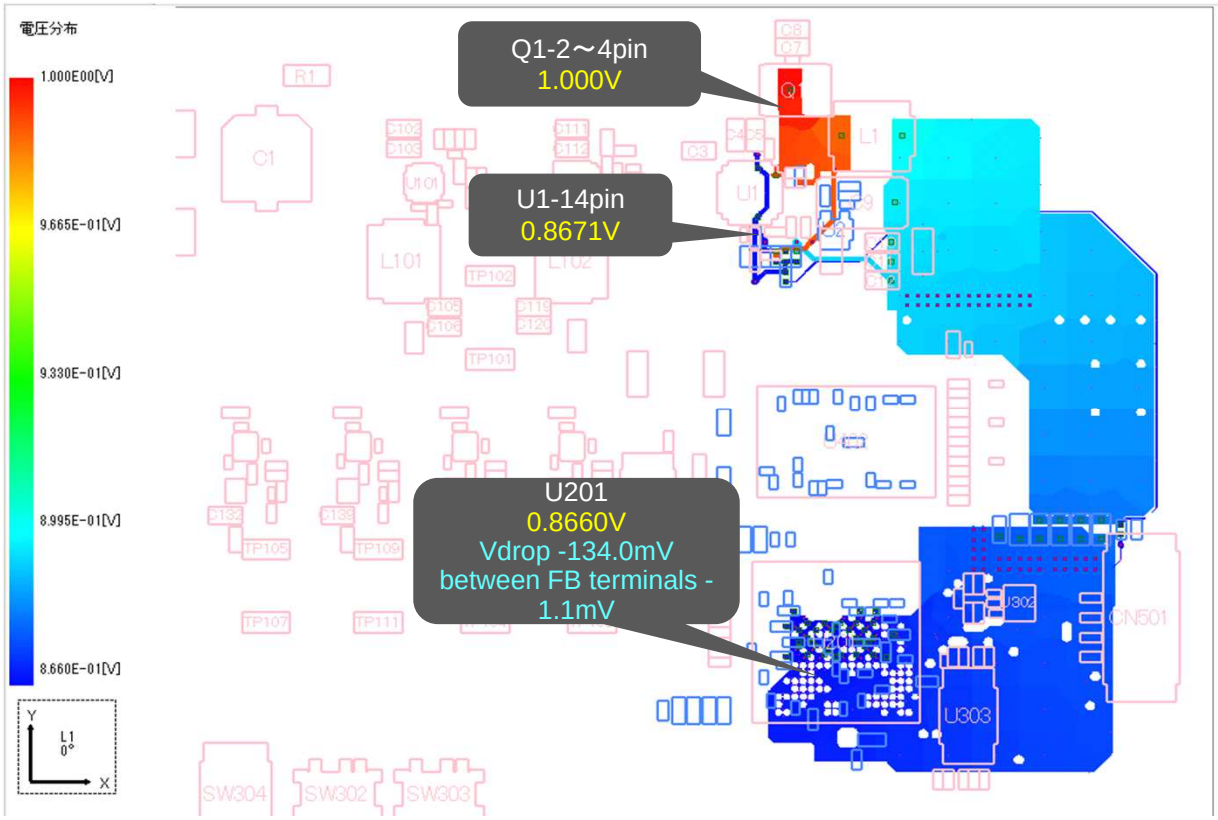
*2 Resistance value of feedback terminal are, 0.001fohms between power supply to FB terminal and 1000Tohms between FB terminal to GND.（Because feedback control is not supported in simulation.）

4. Results of DC analysis

V1.0(V1.0_VFPGA) Diagram



V1.0(V1.0_FPGA) Voltage Distribution Diagram

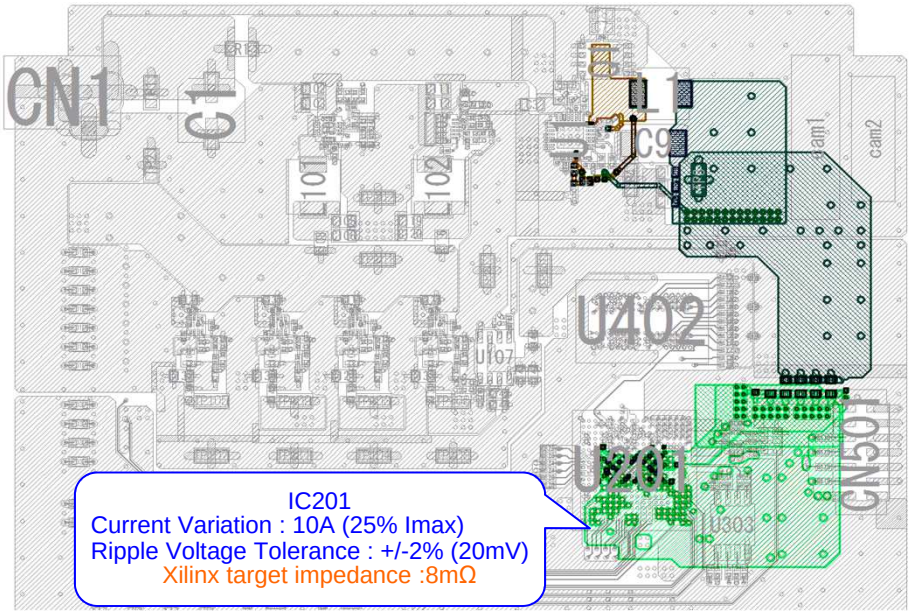


Net Name	Parts (From)	Voltage (From)[V]	Parts (To)	Voltage (To)[V]	ΔV [mV]	Voltage drop [mV]	Tolerance [mV]	Judgement	Current [A]
V_1.0_FPGA	Q1	1.0000	U201	0.8660	134.0	144.1	-	-	10
(GND)	Q1	0.0000	U201	0.0101	10.1				
V_1.0_FPGA	U1	1.0092	U201	0.8660	143.2	144.2	-	-	
(GND)	U1	0.0092	U201	0.0101	1.0				
V_1.0_FPGA	U1_14	0.8671	U201	0.8660	1.1	2.0	50	OK	
(GND)	U1	0.0092	U201	0.0101	1.0				

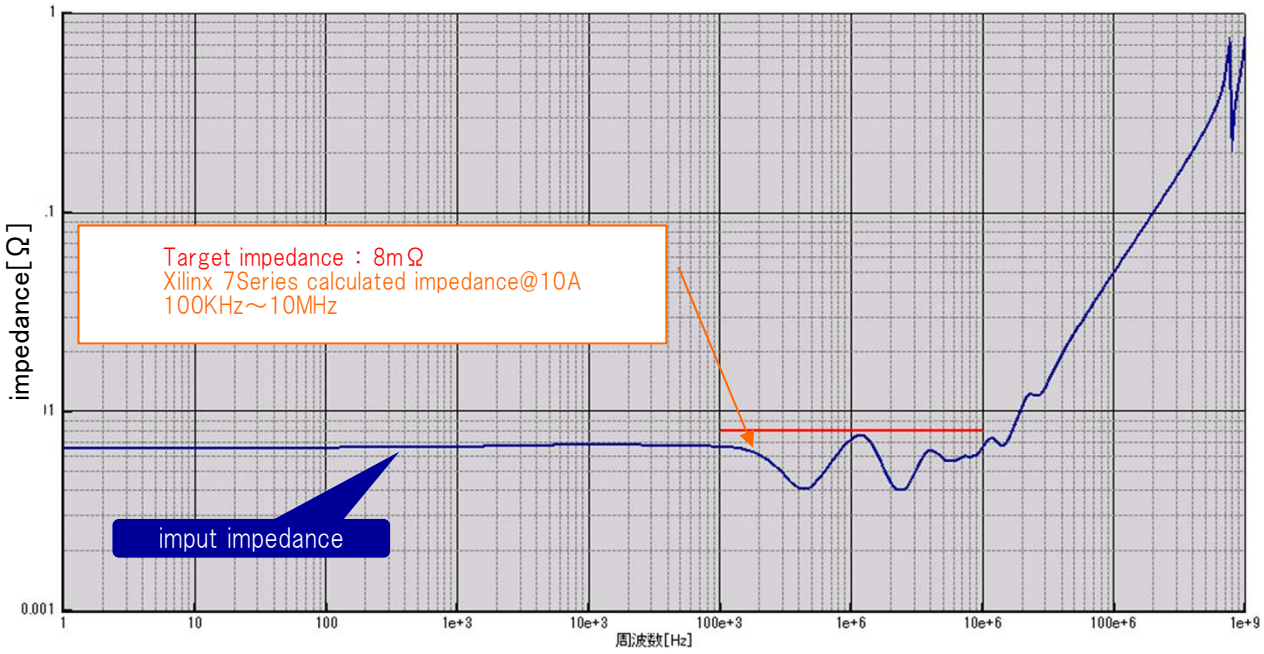
The voltage drop meets the tolerance of the device requirement.
There seems to be no problem with width or length of wire, and thickness of copper of the power supply pattern.

5. Results of impedance analysis

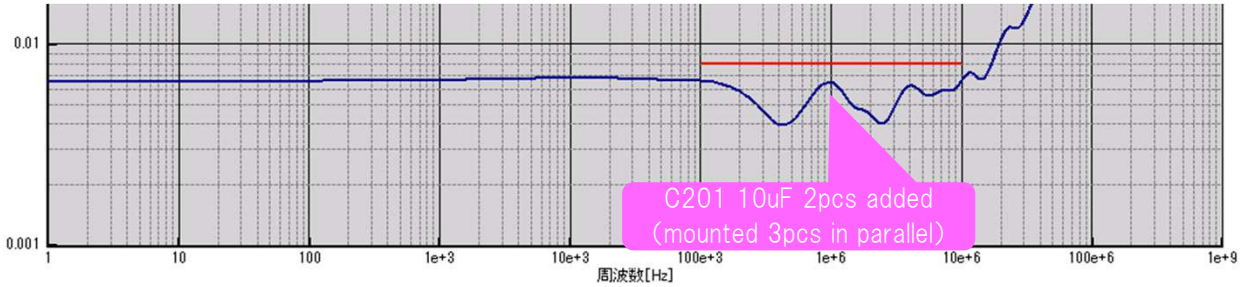
V1.0(V1.0_VFPGA) Diagram



V1.0(V1.0_FPGA) Analysis Results



* To improve the peak at 1MHz, add 2pcs of 10uF.



Although the number of placed parts can be changed, new parts cannot be generated, so the number of existing parts has been increased.