1. Specification

1-1. Abstract

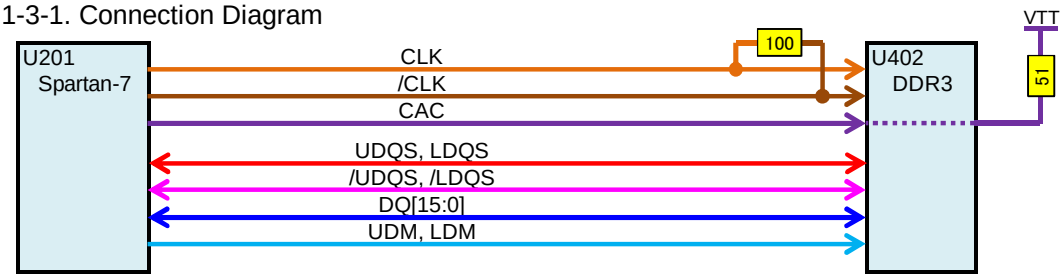
This document discribes the results of Signal Integrity Simulation for Spartan-7 Evaluation Board.

1-2. Simulation Conditions

	Product Name	Supplier
Signal Integrity verification simulation	HyperLynx VX2.4 Update	Mentor Graphics Japan

1-3. Customer Requirment Specification

1-3-1. Connection Diagram



Device Model

Device	Ref.	Part number	Type	File
FPGA	U201	XC7S50-2CSGA324C	IBIS	impl_5.ibs
DDR3L SDRAM	U402	MT41K256M16TW-107P	IBIS	v00h_1p35.ibs

1-3-2. Simulation Conditions

a) Simulation Signal Line

Group	Signal Name	Configuration	Bit Pattern	Operating Speed
CLK	DDR3L_CLK, DDR3L_CLK	1:1 connection differential	Toggle	DDR3-800 400MHz
DQS	DDR3L_UDQS, DDR3L_/UDQS, DDR3L_LDQS, DDR3L_/LDQS,	1:1 connection bidirectional	Toggle	
DQ	DDR3L_DQ[15:0]	1:1 connection bidirectional	Random Bit (128bit)	
DQM	DDR3L_UDM, DDR3L_LDM	1:1 connection		
CAC	DDR3L_A[14:0], DDR3L_BA[2:0], DDR3L_/RAS, /DDR3L_/CAS, DDR3L_/WE, DDR3L_/CS, DDR3L_CKE, DDR3L_ODT	1:1 connection	Random Bit (128bit)	DDR3-800 200MHz

b) DRV/ODT Specification

	Operatig condition		Spartan-7	DRAM		Terminating Resistor
				Drive	ODT	
CLK_Group	Write	to DRAM	SSTL135_F_HR	-	-	100Ω
DQS_Group	Write	to DRAM	SSTL135_F_HR_IN50	-	20Ω/30Ω/40Ω/60Ω/120Ω	-
	Read	from DRAM		34Ω/40Ω	-	-
DQ_Group	Write	to DRAM	SSTL135_F_HR_IN50	-	20Ω/30Ω/40Ω/60Ω/120Ω	-
	Read	from DRAM		34Ω/40Ω	-	-
DM_Group	Write	to DRAM	SSTL135_F_HR	-	20Ω/30Ω/40Ω/60Ω/120Ω	-
CAC_Group	Write	to DRAM	SSTL135_F_HR	-	-	51Ω

The value of terminating resistor at CLK is changed from 80.6Ω to 100Ω
The value of terminating resistor at CAC is changed from 49.9Ω to 51Ω

c) Simulation Settings

Considering the effects of crosstalk, all DDR3L signals(except for the RESET) are analyzed at the die of the receiving end. The analysis pattern is ON/OFF toggle operation of CLK/DQS at operating frequency. Regarding the address and the data, any random bit pattern (128bit) is assigned to every signal net, and observed at the die of the receiving end. The general purpose model for DDR3 prepared by HyperLynx is used as a timing model.

*1 Simulated under the condition of default value of cross talk setting for HyperLynx 9.0 or later.

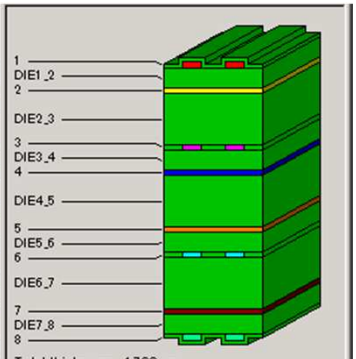
Maximum distance from aggressor D : 0.381mm
Minimum coupling segment length L : 2.54mm

*2 Simulated with ideal power supply and ideal GND.
The waveform may be affected by the noise from power supply and GND in actual environment.

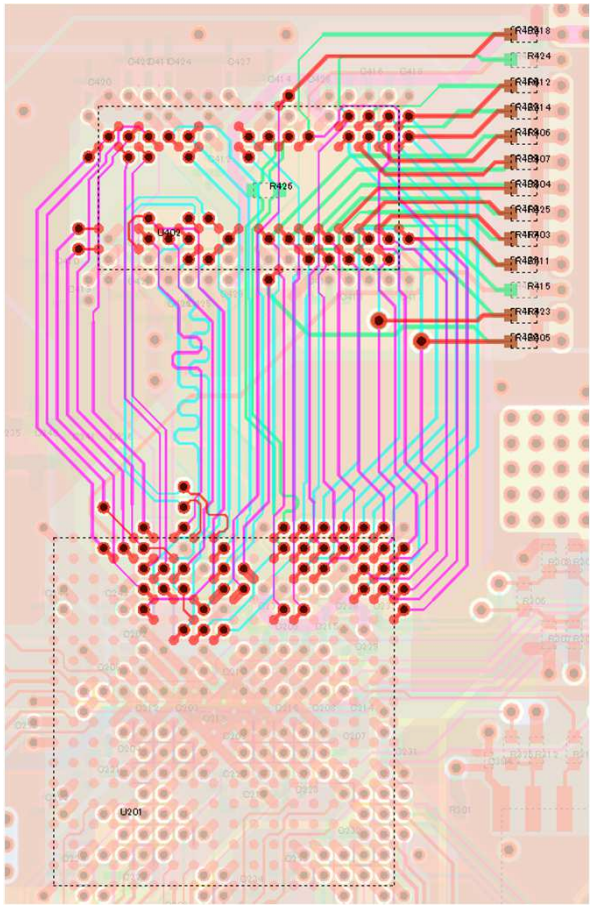
d) Specification of PCB

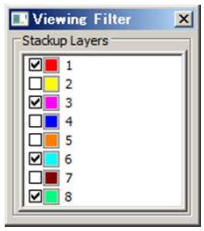
	Color	Layer Name	Type	Usage	Thickness um	Er	Loss Tangent
1			Dielectric	Solder Mask	25	3.3	0.02
2		1	Metal	Signal	40	<Auto>	<Auto>
3		DIE1_2	Dielectric	Substrate	115	4.3	0.016
4		2	Metal	Plane	35	<Auto>	<Auto>
5		DIE2_3	Dielectric	Substrate	300	4.3	0.016
6		3	Metal	Signal	35	<Auto>	<Auto>
7		DIE3_4	Dielectric	Substrate	115	4.3	0.016
8		4	Metal	Plane	35	<Auto>	<Auto>
9		DIE4_5	Dielectric	Substrate	300	4.3	0.016
10		5	Metal	Plane	35	<Auto>	<Auto>
11		DIE5_6	Dielectric	Substrate	115	4.3	0.016
12		6	Metal	Signal	35	<Auto>	<Auto>
13		DIE6_7	Dielectric	Substrate	300	4.3	0.016
14		7	Metal	Plane	35	<Auto>	<Auto>
15		DIE7_8	Dielectric	Substrate	115	4.3	0.016
16		8	Metal	Signal	40	<Auto>	<Auto>
17			Dielectric	Solder Mask	25	3.3	0.02

☑ Calculate Er for metal layers from surrounding dielectrics

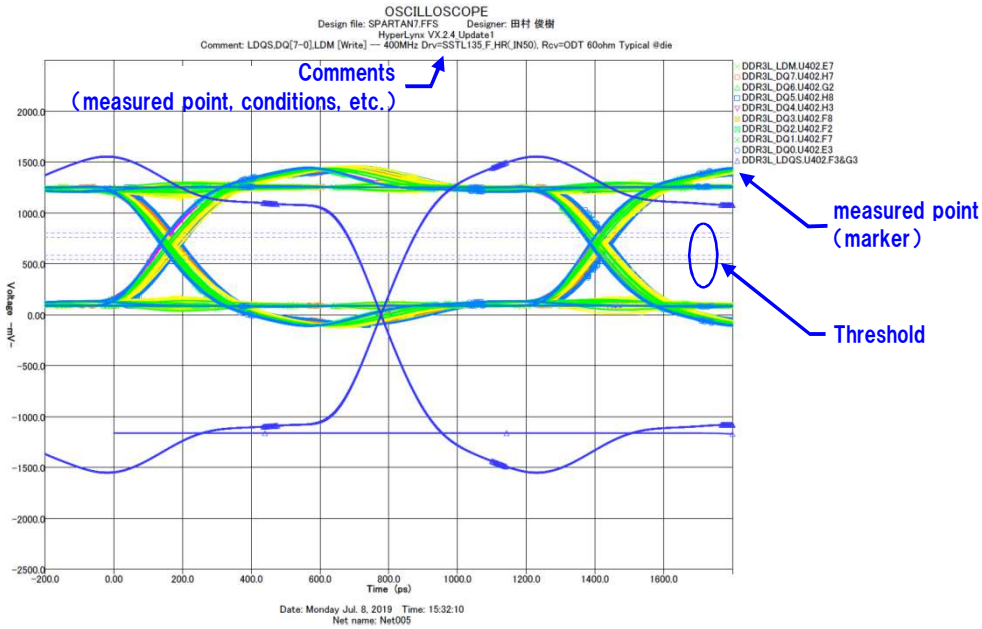


2. Wiring pattern





3. Simulation waveform



4. Timming measurement

Analysis is performed with DDR3-800(1.35V) by DDRx batch simulation of HyperLynx
Note that this is only for reference because this analysis uses the timing models provided by HyperLynx by default for both controller and memory.

* The default controller model prepared by HyperLynx is designed based on the device of FreeScale Smiconductor.

Signal integrity in JEDEC standard is also measured at the same time.

5. Findings

5-1. Value of terminatig resistor

The value of terminating resistor in the initial schematic is 80.6ohms at clock and 40.2ohms at CAC, but the IBIS model of FPGA is output in the default setting of MIG, so the resistance at ODT is 50ohms and IO IN_TERM(Internal Termination Impedance) of FPGA is 50ohms. However the wire impedance in the board layer configuration are 100 ohms in differential or 50 ohms in single, the value of termination resistor is confirmed.

Although there is not much difference, the larger value results in larger amplitude and thus, ringing too, but the impedance of the transmission line Zo=50ohms so, below values looks OK.

R402～R425 : 40.2Ω ⇒ 51.0ohms
R426 : 80.6Ω ⇒ 100.0ohms

Refer to *6-3. the waveform of the termination resistor value confirmation*.

5-2. Analysis Results

The termination resistor condition of analysis is 100ohms at clock, 51ohms at CAC, 60ohms at DRAM ODT and 34ohms at drive. The waveforms are good, the timing margin are secured, and the results passed all signal integrity measurement of JEDEC.
In HyperLynx, the hold margin at reading tends to be less, but enough margin at setup are kept and thus, it is considerd possible to be corrected with timing adjust functions.

Refer to *6-4. the waveform of analysis*.

6. The results of analysis

6-1. The worst value of timing measurement

unit:[ps]

		Typical (Worst)	
【DQS-DQ】Write		t-DS	t-DH
LDQS	DQ[7:0], LDM	220.7	250.9
UDQS	DQ[15:8], UDM	230.5	245.1
【DQS-DQ】Read		t-DQSQ	t-QH
LDQS	DQ[7:0]	164.0	4.8
UDQS	DQ[15:8]	170.1	5.4
【CLK-DQS】DRV=F		t-DQSS	t-DSS
CK	LDQS	444.1	569.1
	UDQS	445.1	569.8
【CLK-CMD/ADD/CTRL】		t-IS	t-IH
CK	CAC	388.9	554.1

Detail results are shown in the file below.

【Spartan-7_Eva_Board】DDR3L_Timing,JEDEC_2018-07-08.xlsx

6-2. Results of JEDEC signal integrity measurement

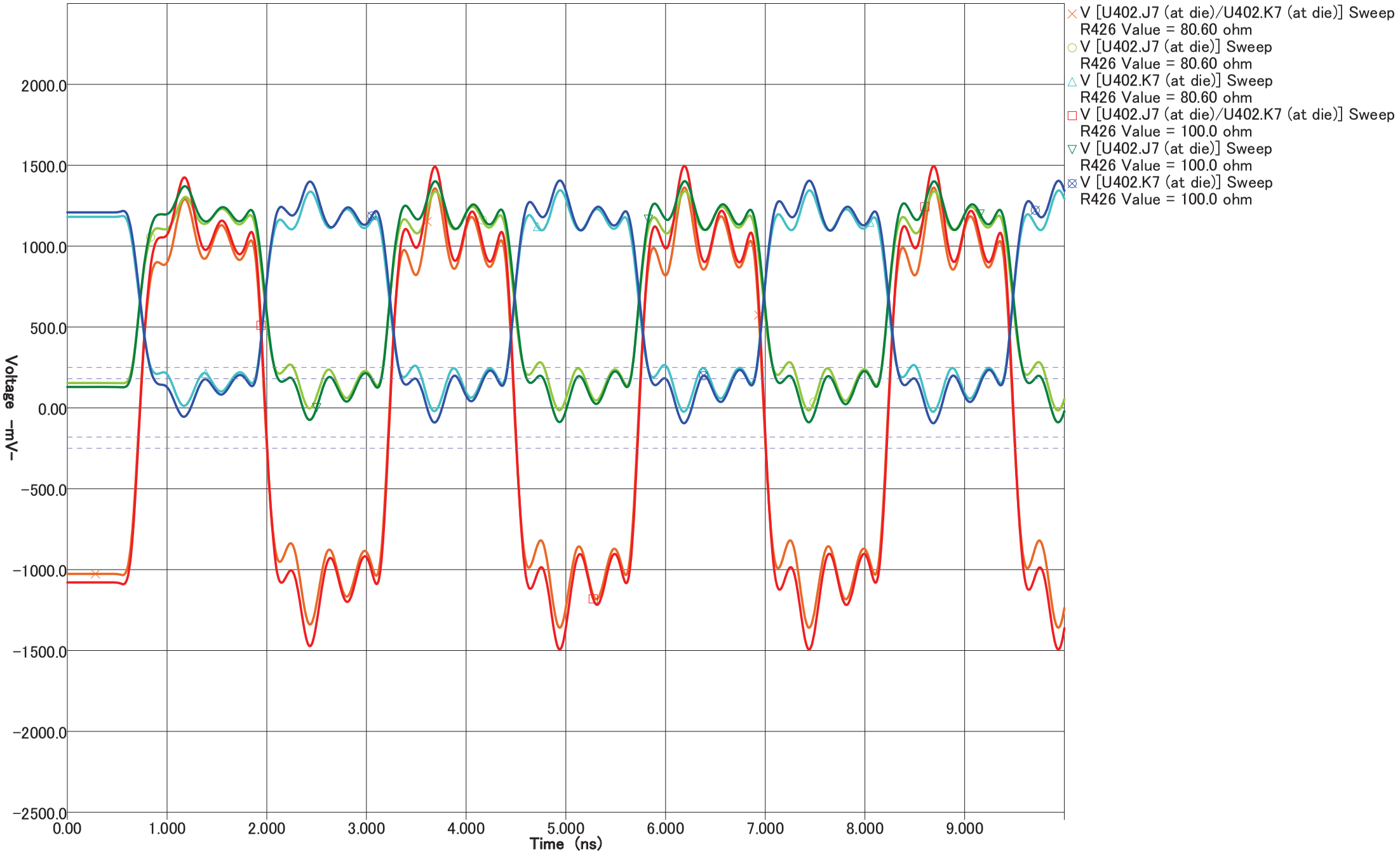
	Typical
Rise Rail Overshoot	Pass
Fall Rail Undershoot	Pass
Rise Rail Overshoot Area	Pass
Fall Rail Undershoot Area	Pass
Monotonic	Pass
VIH/L(AC) Min Limit	Pass
VIH/L(DC) Monotonicity	Pass
Vref Threshold Multi Cross	Pass
Max Slew Time	Pass
VIX	Pass
VID(AC)	Pass
VID(DC)	Pass
VSEH/VSEL	Pass
TVAC/TDVAC	Pass

Detail results are shown in the file below.

【Spartan-7_Eva_Board】DDR3L_Timing,JEDEC_2018-07-08.xlsx

OSCILLOSCOPE

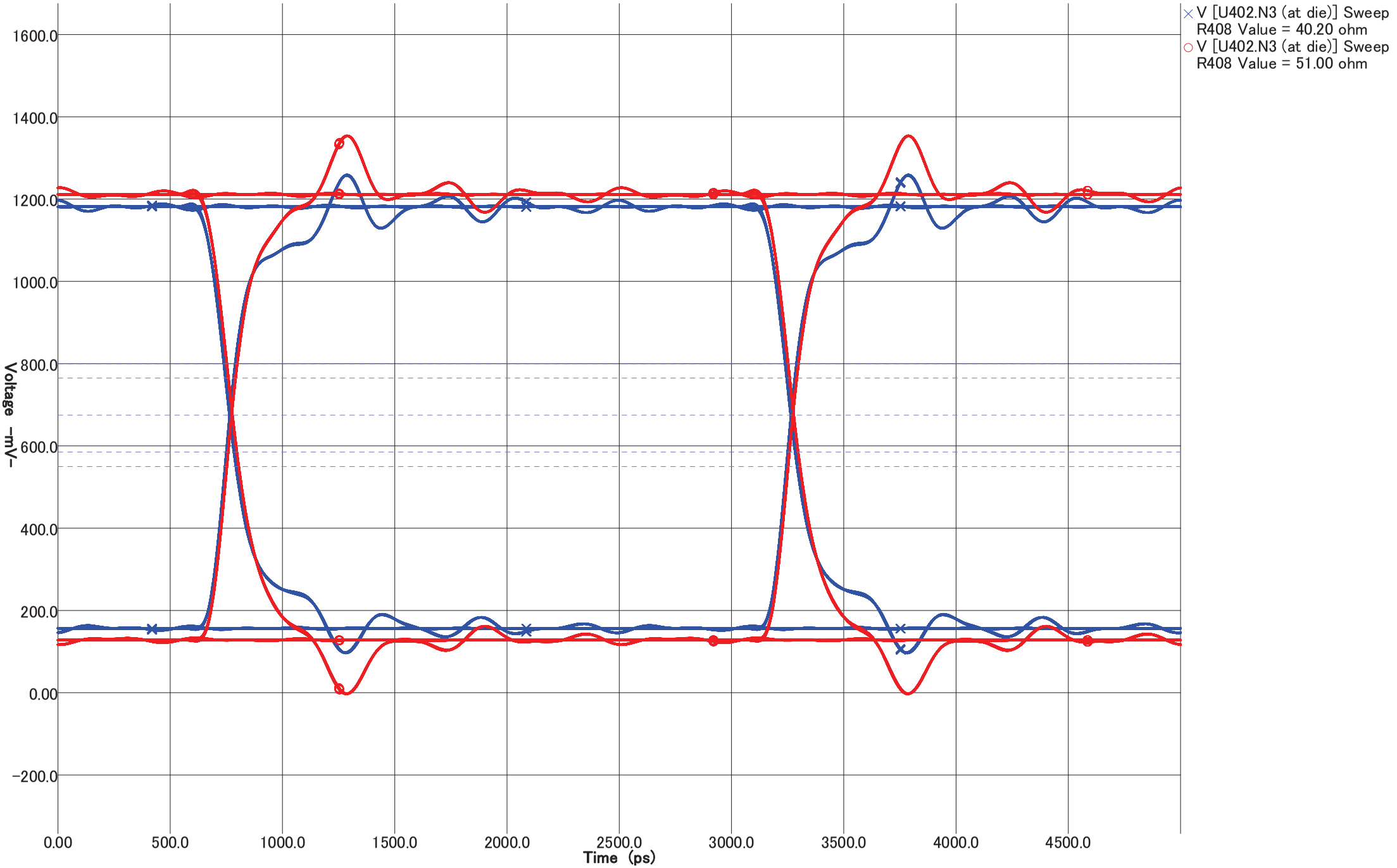
Design file: REFERENCE_BOARD.HYP Designer: 田村 俊樹
HyperLynx VX.2.5_Update1
Comment: CLK 400MHz Rt=80.6ohm and 100ohm Typical @die



Date: Friday Jul. 5, 2019 Time: 9:12:07
Net name: DDR3L_CLK
Show Latest Waveform = YES

OSCILLOSCOPE

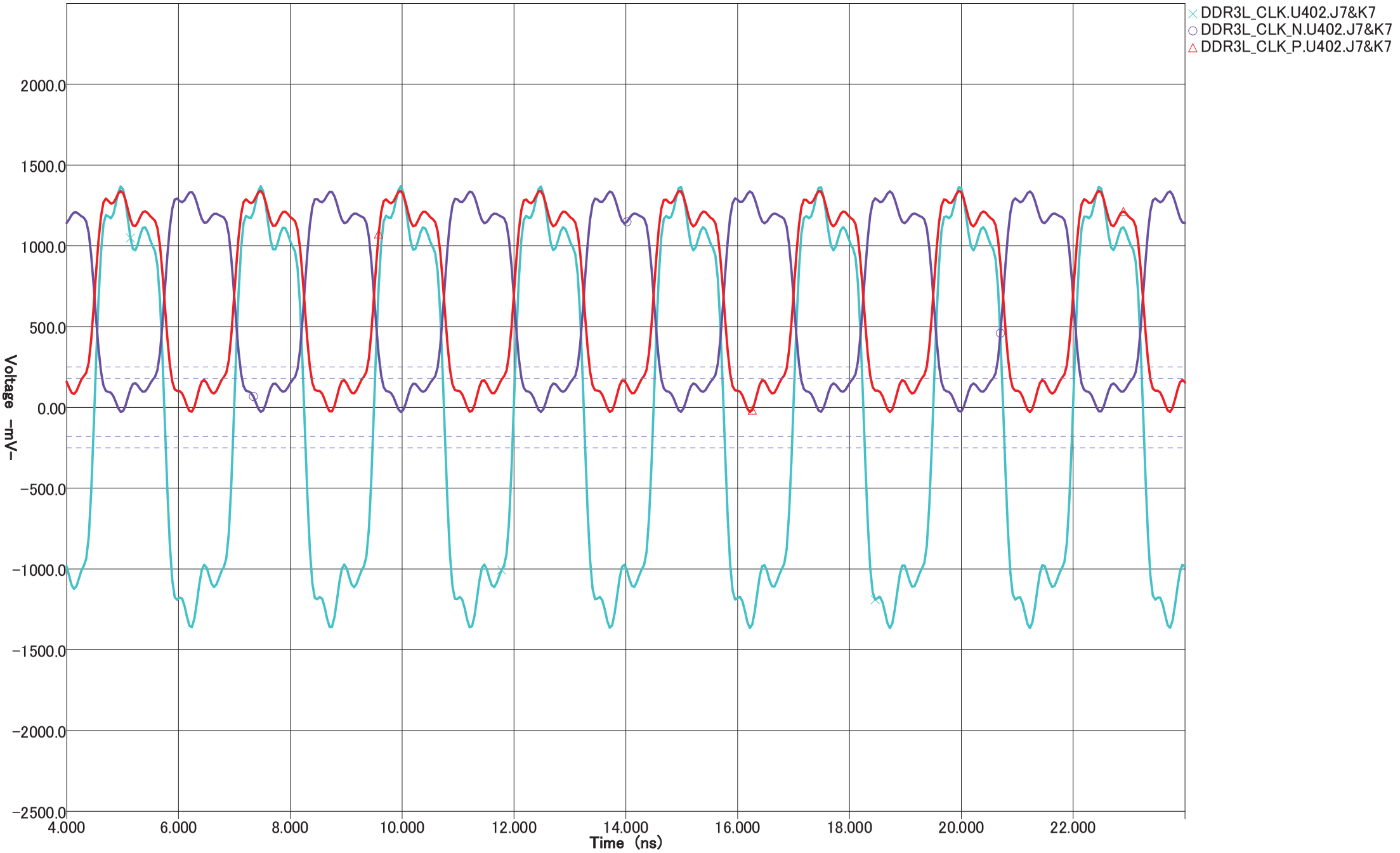
Design file: REFERENCE_BOARD.HYP Designer: 田村 俊樹
HyperLynx VX.2.5_Update1
Comment: A0 DDR3L-800 Rt=40.2ohm and 51ohm Typical @die



Date: Friday Jul. 5, 2019 Time: 9:07:46
Net name: DDR3L_A0

OSCILLOSCOPE

Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
Comment: DDR3L_CK -- 400MHz Drv=SSTL135_F_HR Rt=100ohm Typical @die



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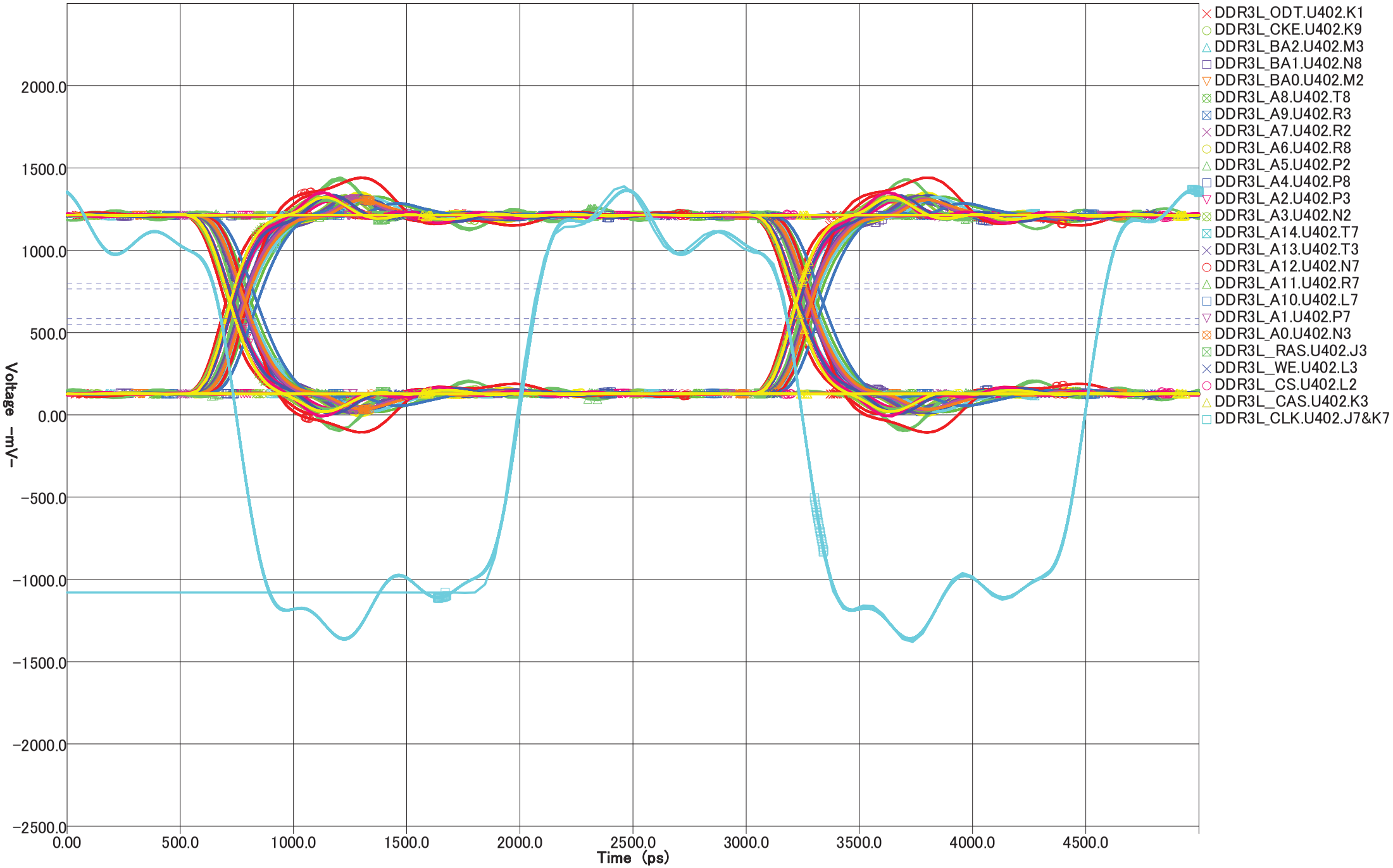
OSCILLOSCOPE

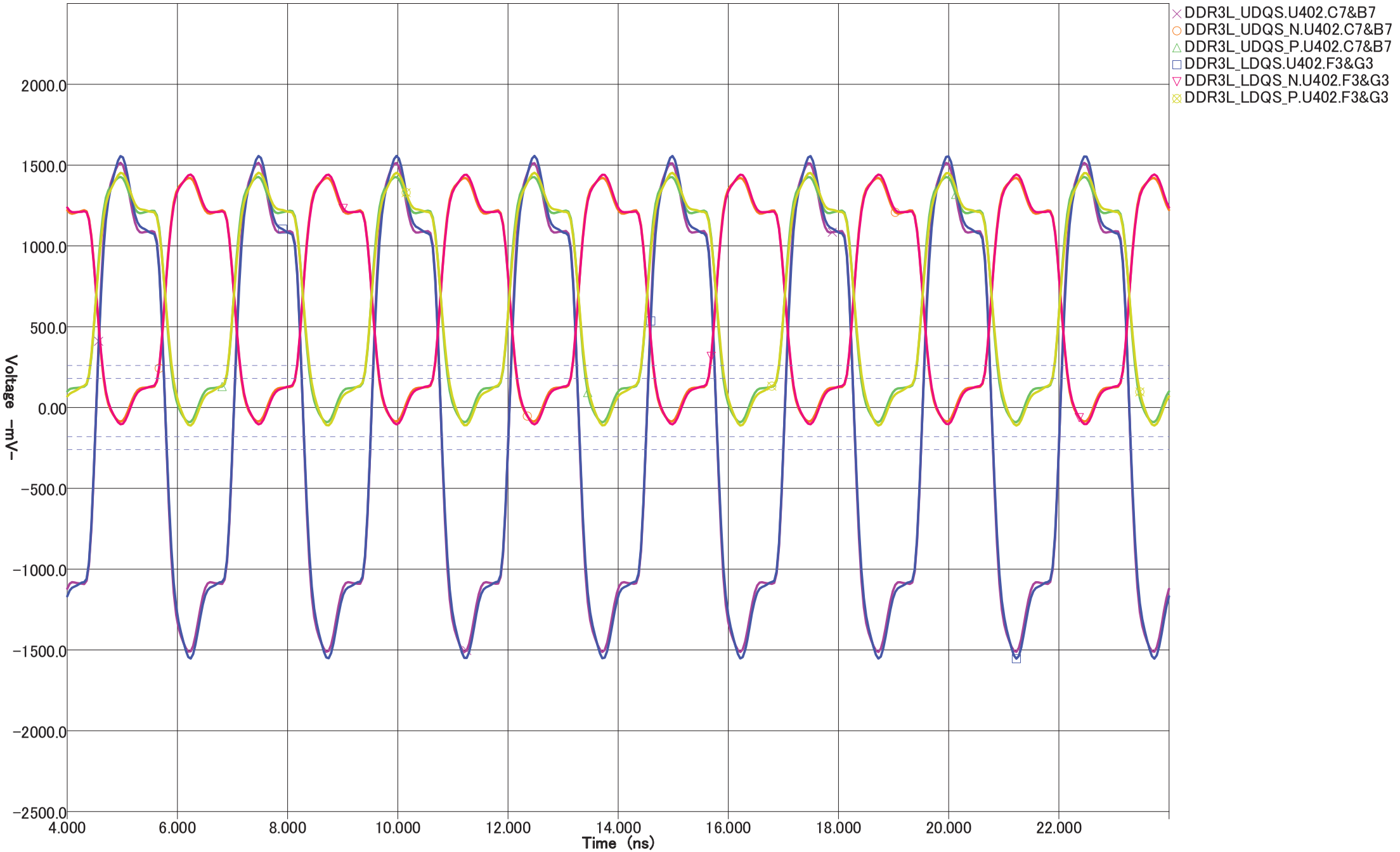
Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
Comment: CK -- 400MHz, CAC -- 200MHz Drv=SSTL135_F_HR Rt=CK 100ohm, CAC 51ohm Typical @die



Date: Monday Jul. 8, 2019 Time: 15:38:58
Net name: DDR3L_A0

OSCILLOSCOPE

Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
Comment: DDR3L_[U,L]DQS [Write] -- 400MHz Drv=SSTL135_F_HR_IN50, Rcv=ODT 60ohm Typical @die



Date: Monday Jul. 8, 2019 Time: 15:29:17
Net name: Net003
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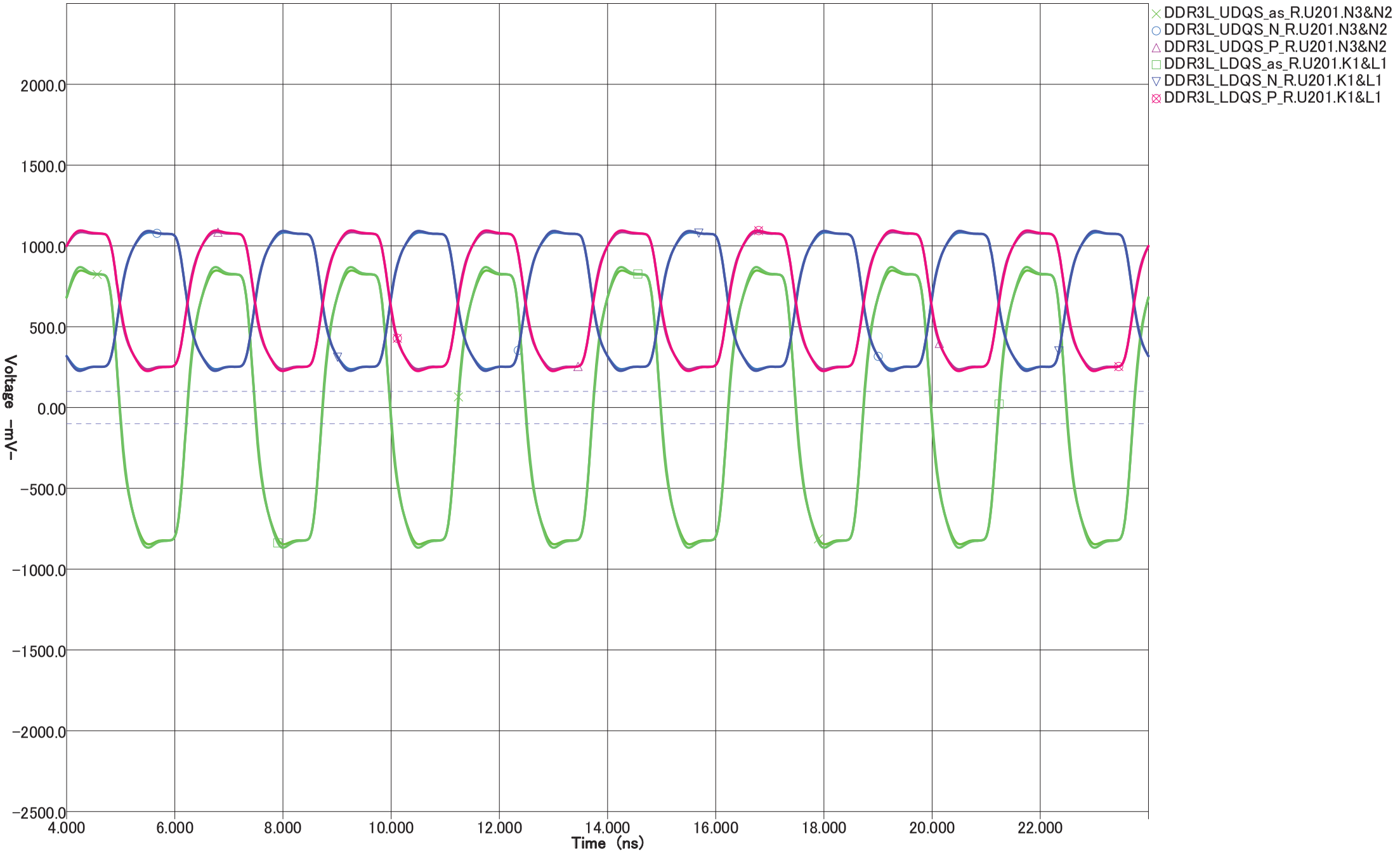
OSCILLOSCOPE

Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
Comment: DDR3L_[U,L]DQS [Read] -- 400MHz Drv=34ohm, Rcv=SSTL135_F_HR_IN50 Typical @die



Date: Monday Jul. 8, 2019 Time: 15:34:23
Net name: DDR3L_/LDQS
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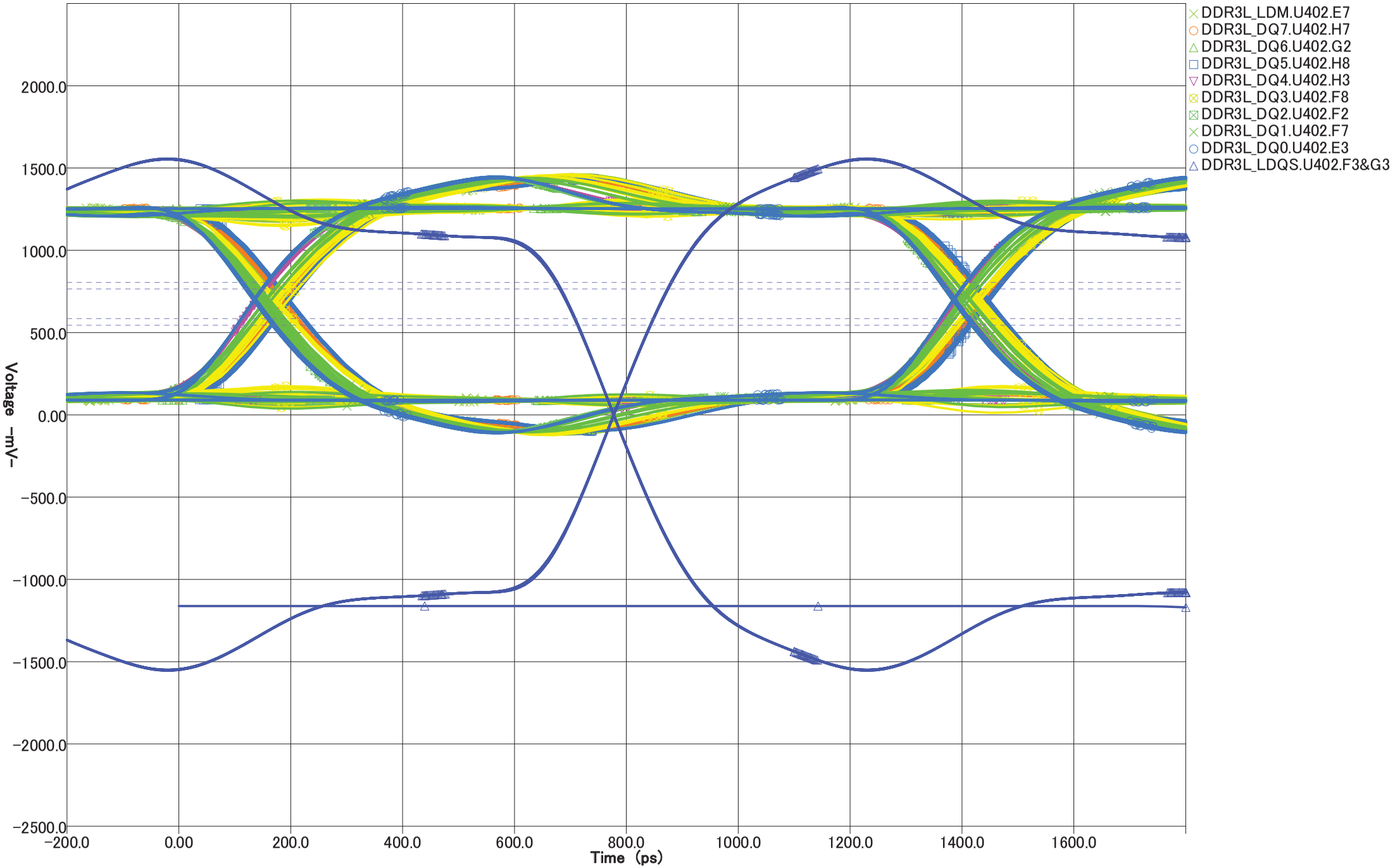
OSCILLOSCOPE

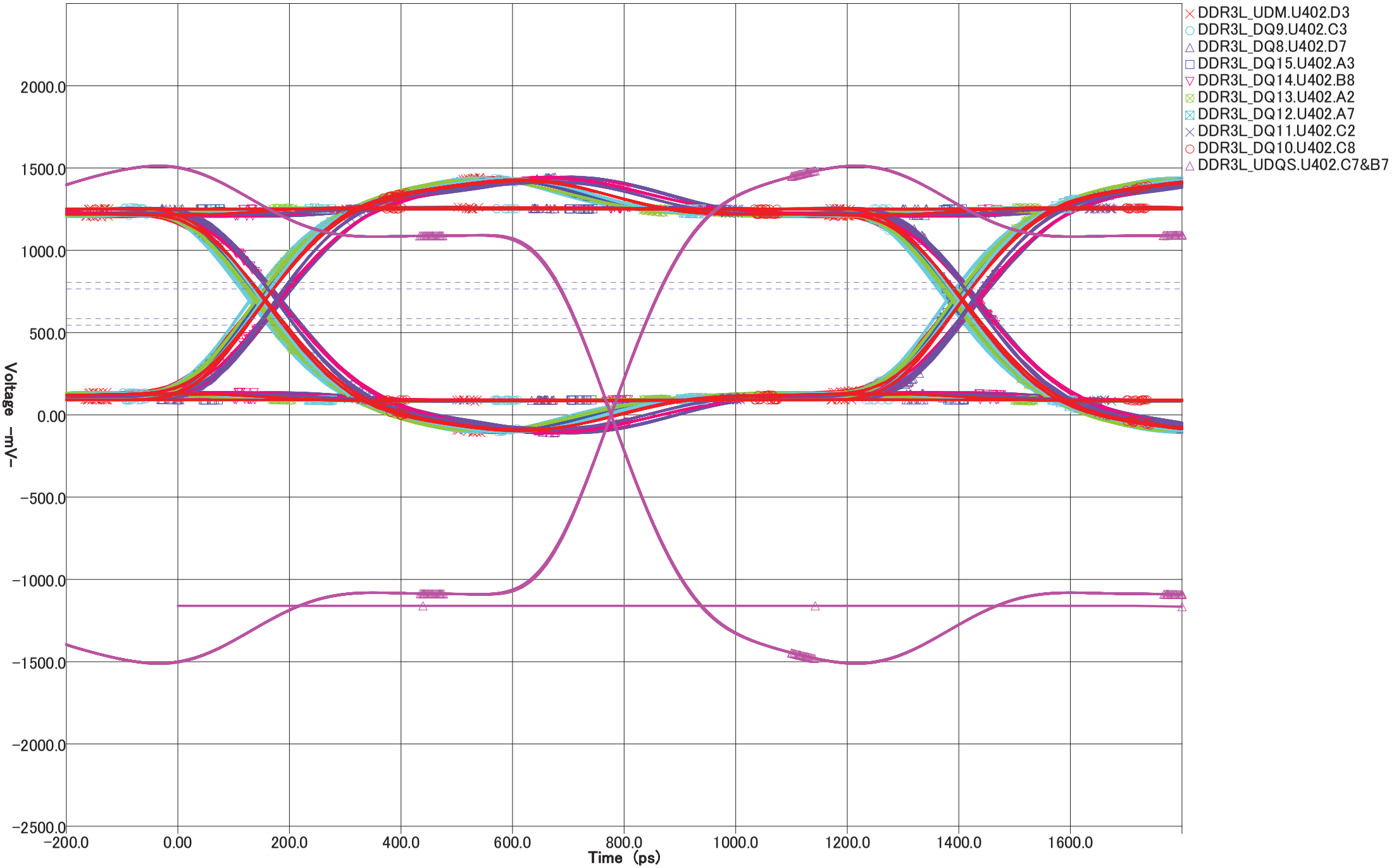
Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
Comment: LDQS,DQ[7-0],LDM [Write] -- 400MHz Drv=SSTL135_F_HR(_IN50), Rcv=ODT 60ohm Typical @die



Date: Monday Jul. 8, 2019 Time: 15:32:10
Net name: Net005

OSCILLOSCOPE

Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
Comment: UDQS,DQ[15-8],UDM [Write] -- 400MHz Drv=SSTL135_F_HR(_IN50), Rcv=ODT 60ohm Typical @die



Date: Monday Jul. 8, 2019 Time: 15:32:34
Net name: Net005

OSCILLOSCOPE

Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
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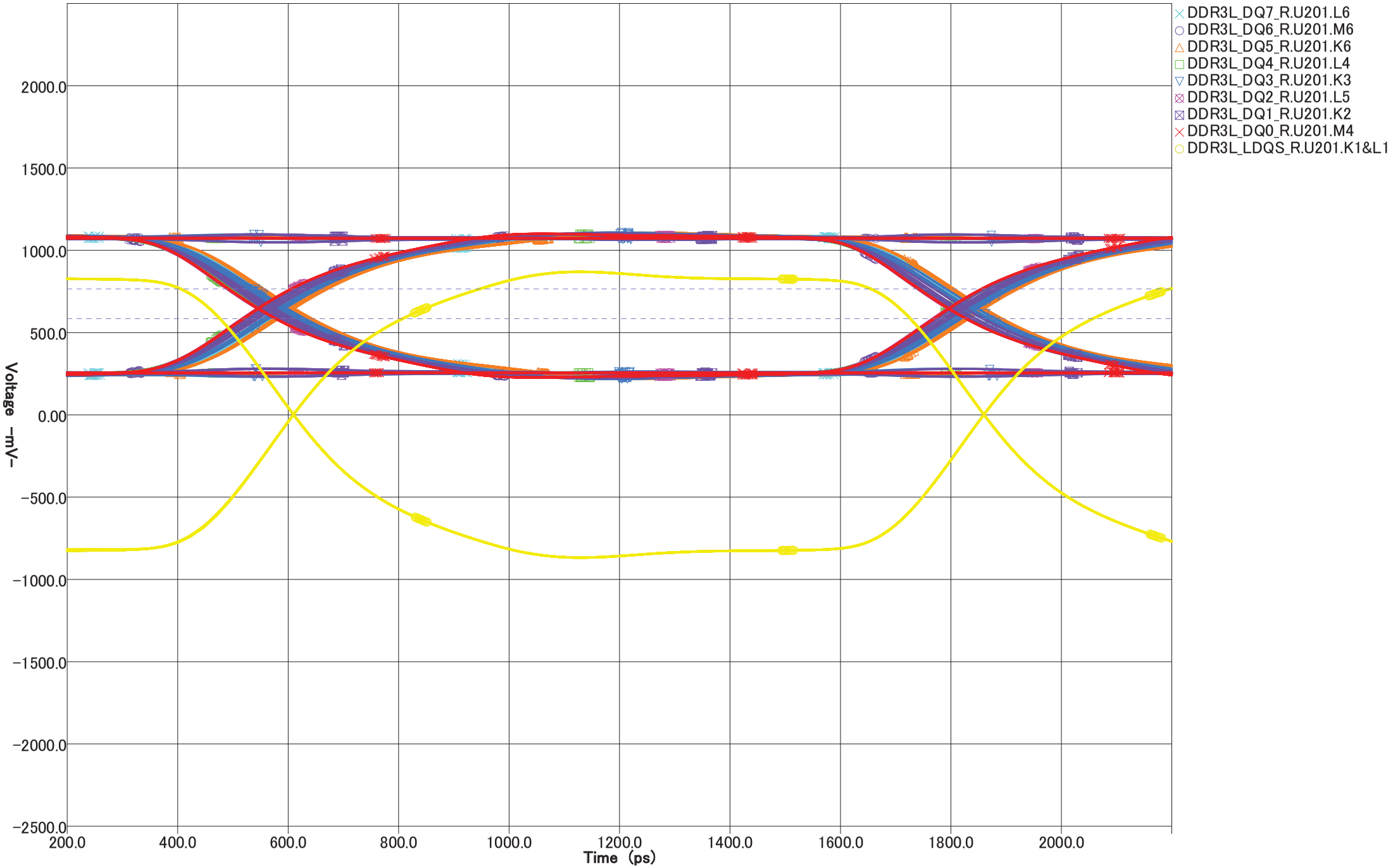
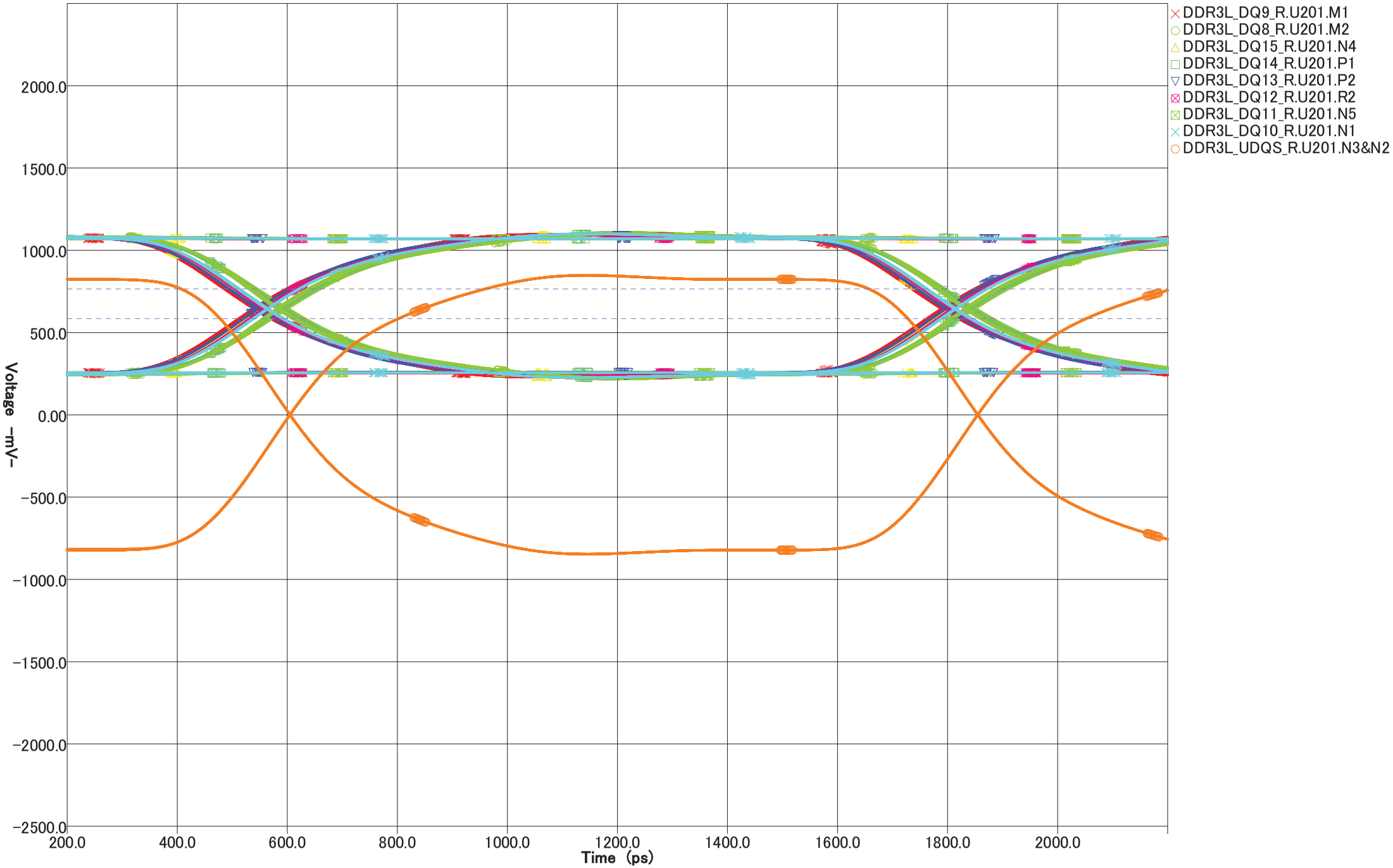


Date: Monday Jul. 8, 2019 Time: 15:37:26
Net name: DDR3L_DQ0

OSCILLOSCOPE

Design file: SPARTAN7.FFS Designer: 田村 俊樹
HyperLynx VX.2.4_Update1
Comment: UDQS,DQ[15-8] [Read] -- 400MHz Drv=34ohm, Rcv=SSTL135_F_HR_IN50 Typical @die



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