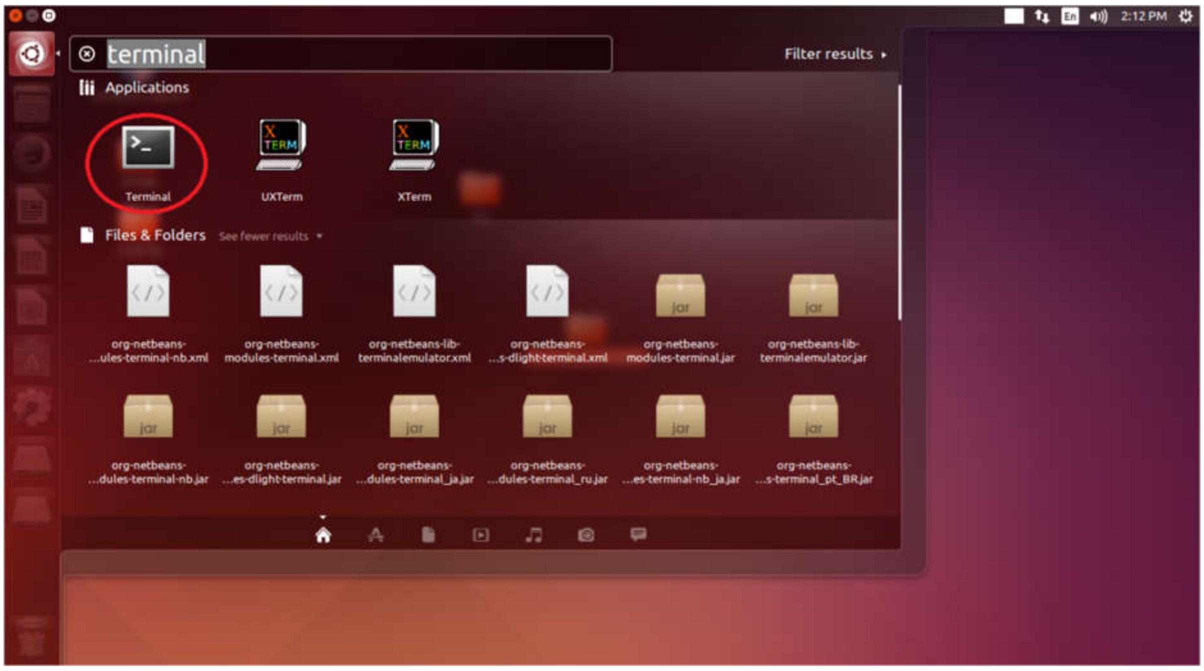
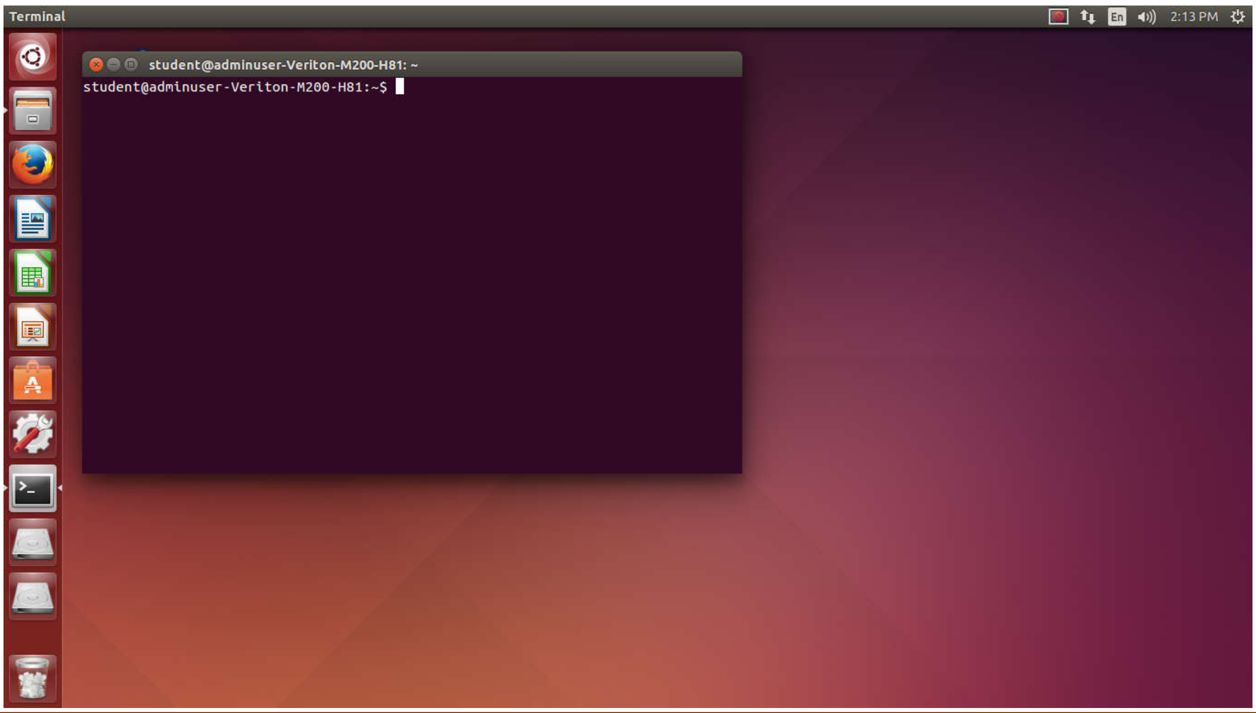
STEPS TO IMPLEMENT THE DESIGN

Step 1: Search for "**terminal**" in the search bar. Once terminal is shown in the results click on it.

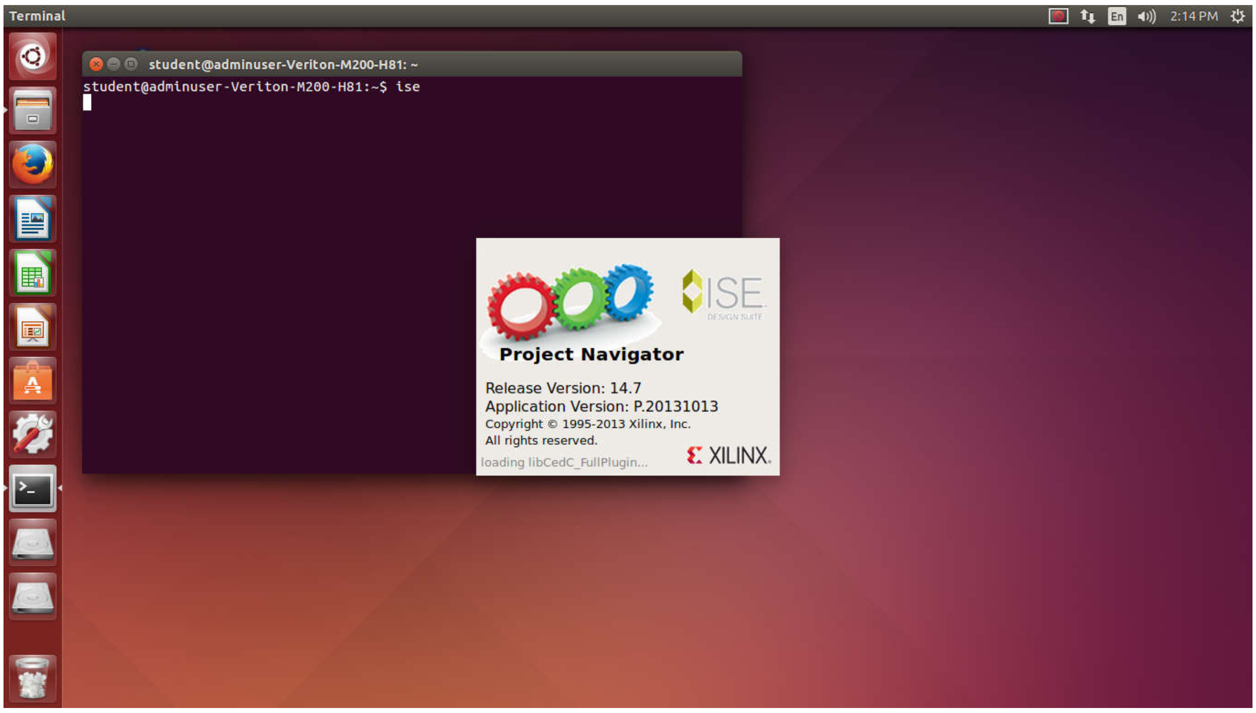

terminal
Filter results
Applications
Terminal
UXTerm
XTerm
Files & Folders
See fewer results
org-netbeans-...ules-terminal-nb.xml
org-netbeans-modules-terminal.xml
org-netbeans-lib-terminalemulator.xml
org-netbeans-...s-dlight-terminal.xml
org-netbeans-modules-terminal.jar
org-netbeans-lib-terminalemulator.jar
org-netbeans-...dules-terminal-nb.jar
org-netbeans-...es-dlight-terminal.jar
org-netbeans-...dules-terminal_ja.jar
org-netbeans-...dules-terminal_ru.jar
org-netbeans-...es-terminal-nb_ja.jar
org-netbeans-...s-terminal_pt_BR.jar
2:12 PM

The terminal window opens.



```
student@adminuser-Veriton-M200-H81:~$
```

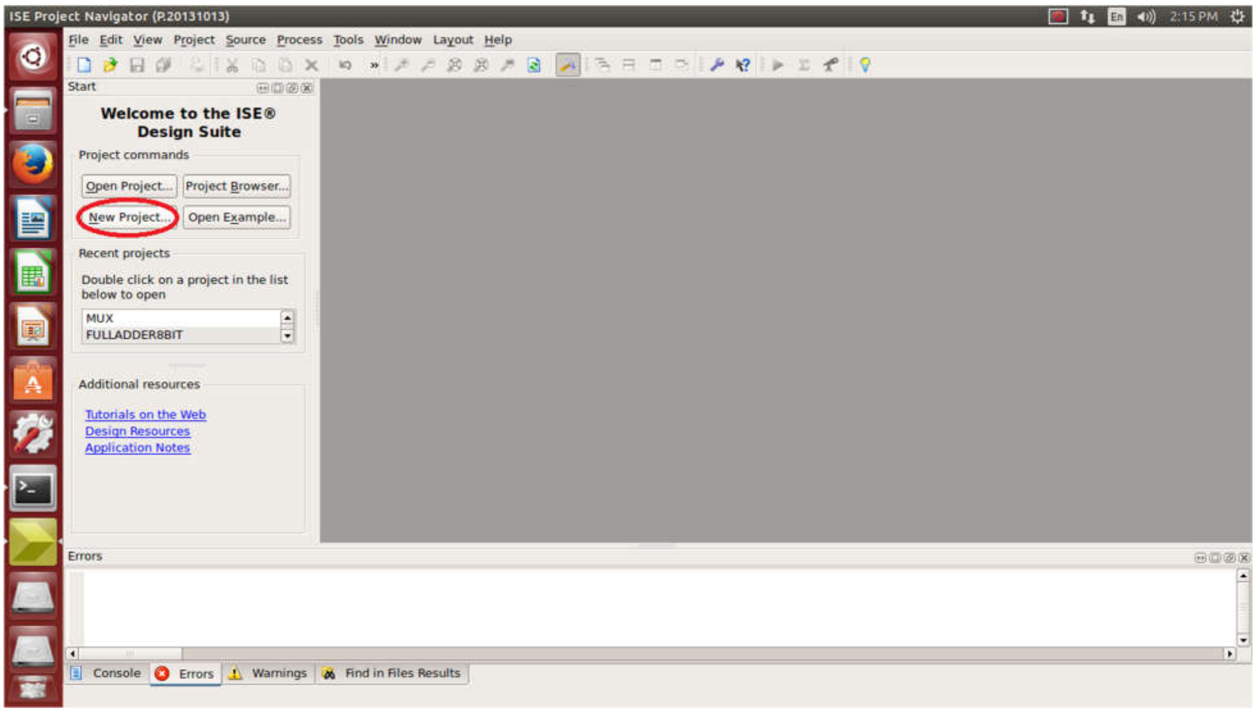
Step 2: Type "**ise**" in the terminal box and press enter. This will open the **Xilinx** window.



```
student@adminuser-Veriton-M200-H81:~$ ise
```

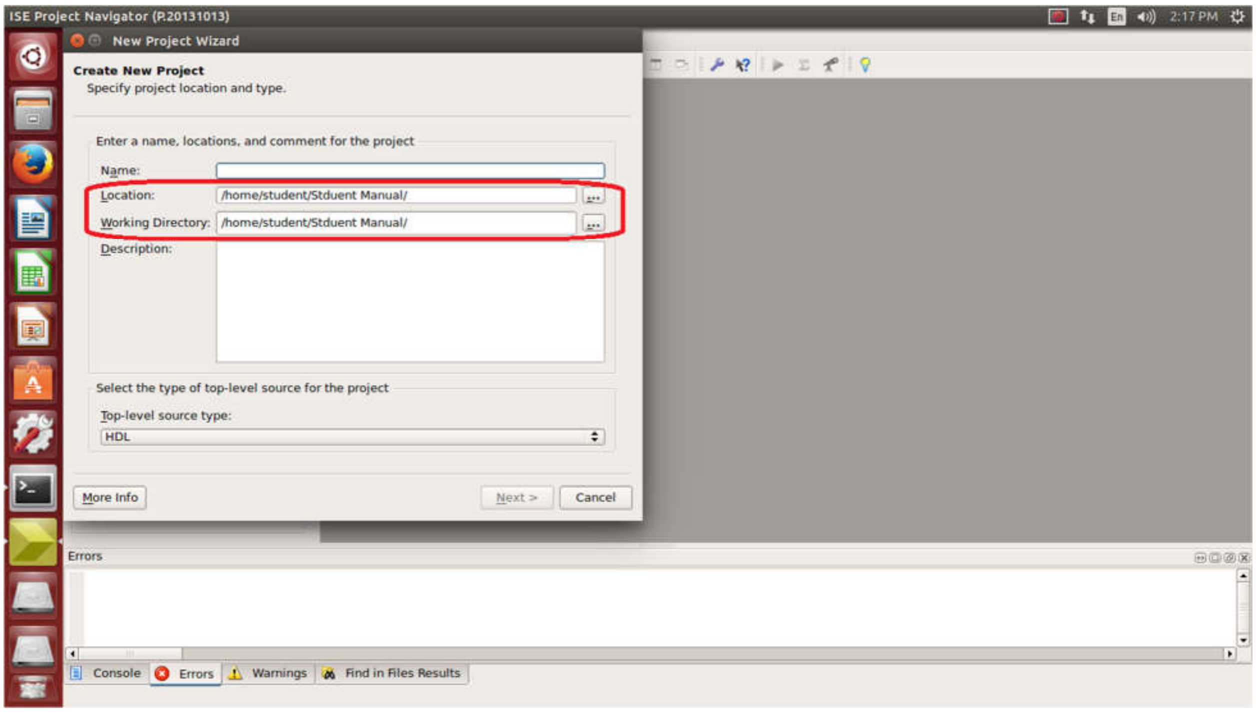
Project Navigator
Release Version: 14.7
Application Version: P.20131013
Copyright © 1995-2013 Xilinx, Inc.
All rights reserved.
loading libCedC_FullPlugin...

Step 3: Once the Xilinx window opens click on **New Project**.



Welcome to the ISE® Design Suite
Recent projects
Double click on a project in the list below to open
MUX
FULLADDER8BIT

Step 4: The **Create New Project** window will appear. Select the *location* where the project should be saved.



ISE Project Navigator (P.20131013)

New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name:

Location: /home/student/Stduent Manual/

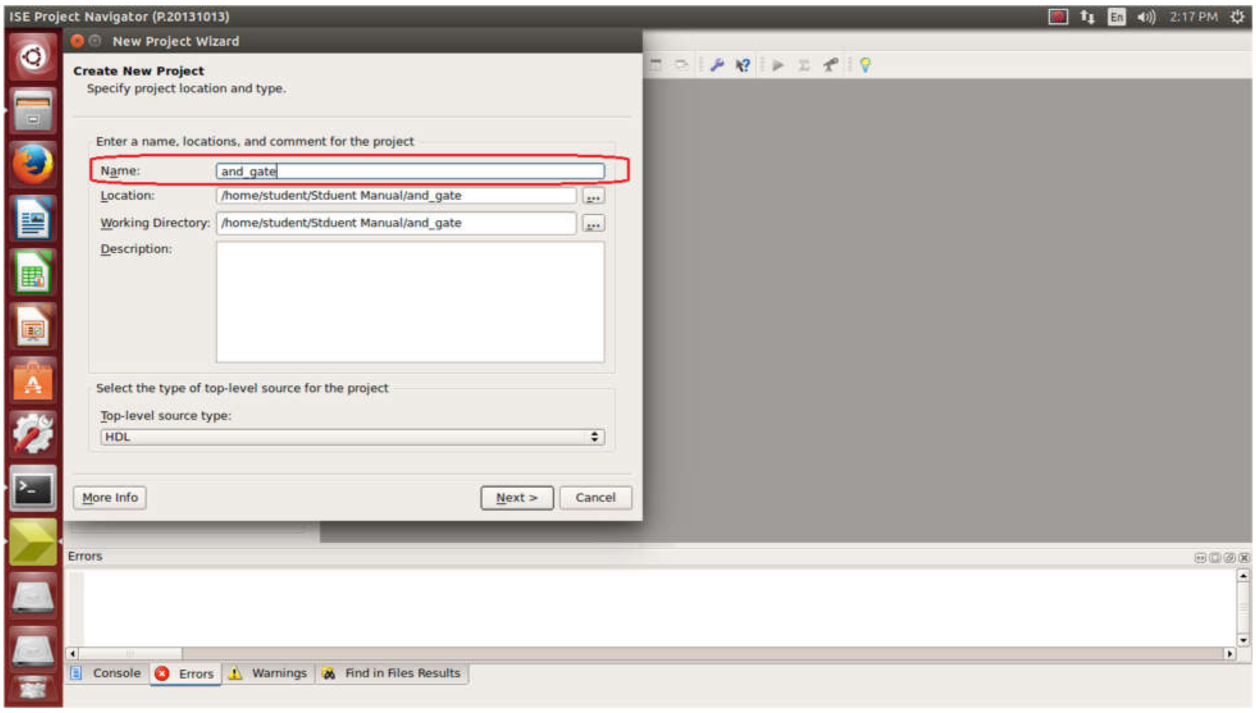
Working Directory: /home/student/Stduent Manual/

Description:

Select the type of top-level source for the project

Top-level source type: HDL

Step 5: Enter a name for the project and click on **Next**.



ISE Project Navigator (P.20131013)

New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: and_gate

Location: /home/student/Stduent Manual/and_gate

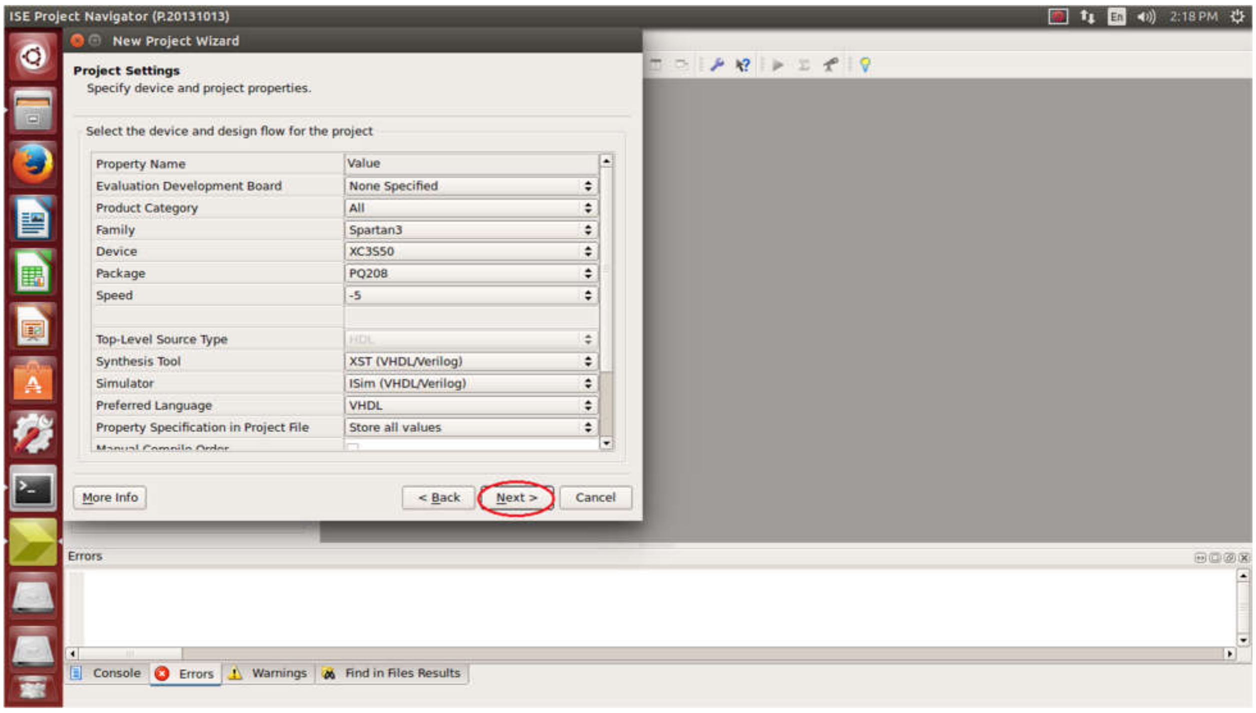
Working Directory: /home/student/Stduent Manual/and_gate

Description:

Select the type of top-level source for the project

Top-level source type: HDL

Step 6: The **Project Settings** window is shown. Make the necessary changes and click on **Next**.

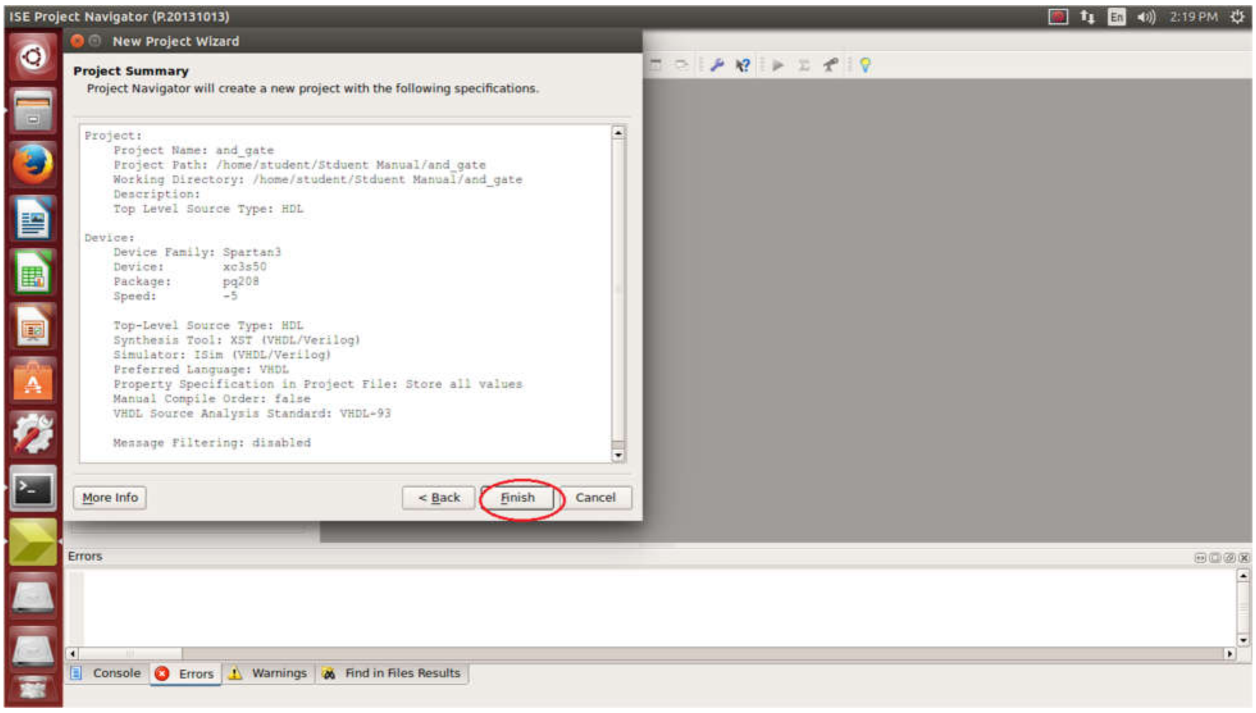


Project Settings
Specify device and project properties.

Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3
Device	XC3S50
Package	PQ208
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	VHDL
Property Specification in Project File	Store all values
Manual Compile Order	

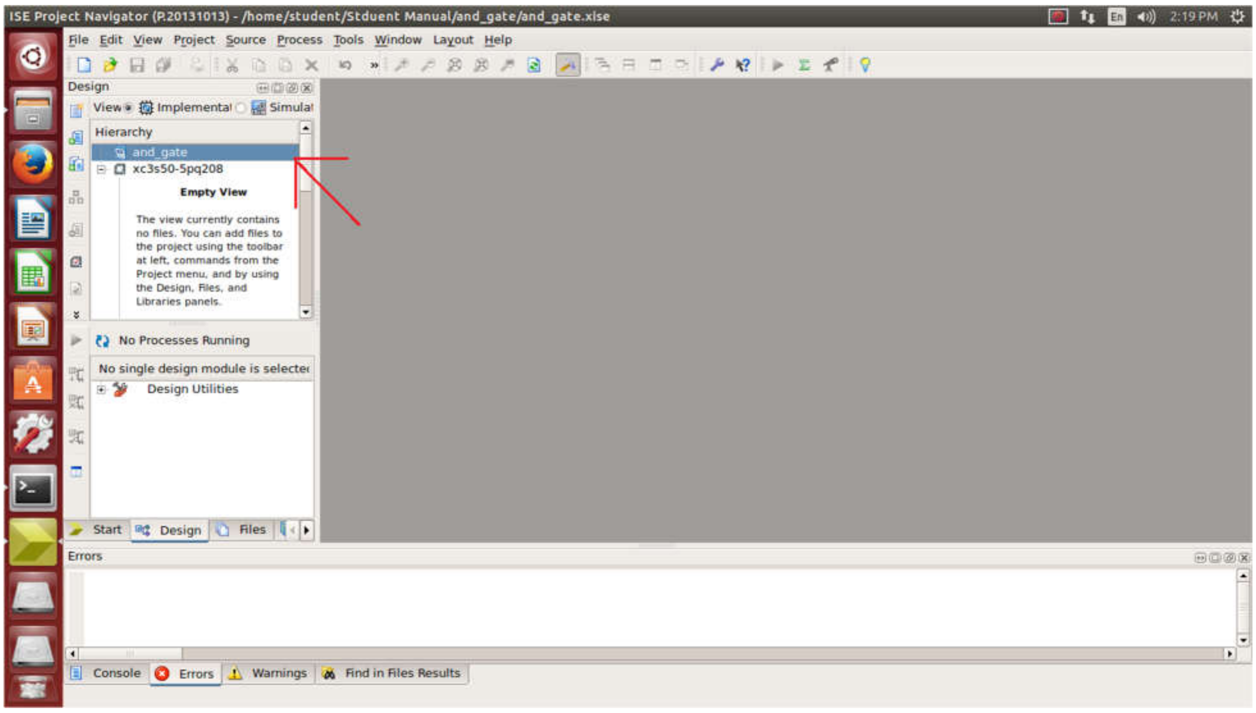
Step 7: The **Project Summary** window is shown. Click on **Finish**.



Project Summary
Project Navigator will create a new project with the following specifications.

```
Project:
    Project Name: and_gate
    Project Path: /home/student/Stduent Manual/and_gate
    Working Directory: /home/student/Stduent Manual/and_gate
    Description:
    Top Level Source Type: HDL

Device:
    Device Family: Spartan3
    Device:        xc3s50
    Package:       pq208
    Speed:         -5

    Top-Level Source Type: HDL
    Synthesis Tool: XST (VHDL/Verilog)
    Simulator: ISim (VHDL/Verilog)
    Preferred Language: VHDL
    Property Specification in Project File: Store all values
    Manual Compile Order: false
    VHDL Source Analysis Standard: VHDL-93

    Message Filtering: disabled
```

Step 8: A new project is created. It is seen that a **Design** panel is placed at the left-most side of the screen. *Right click* on the project name written at the top of the **Design** panel and select **New Source**.

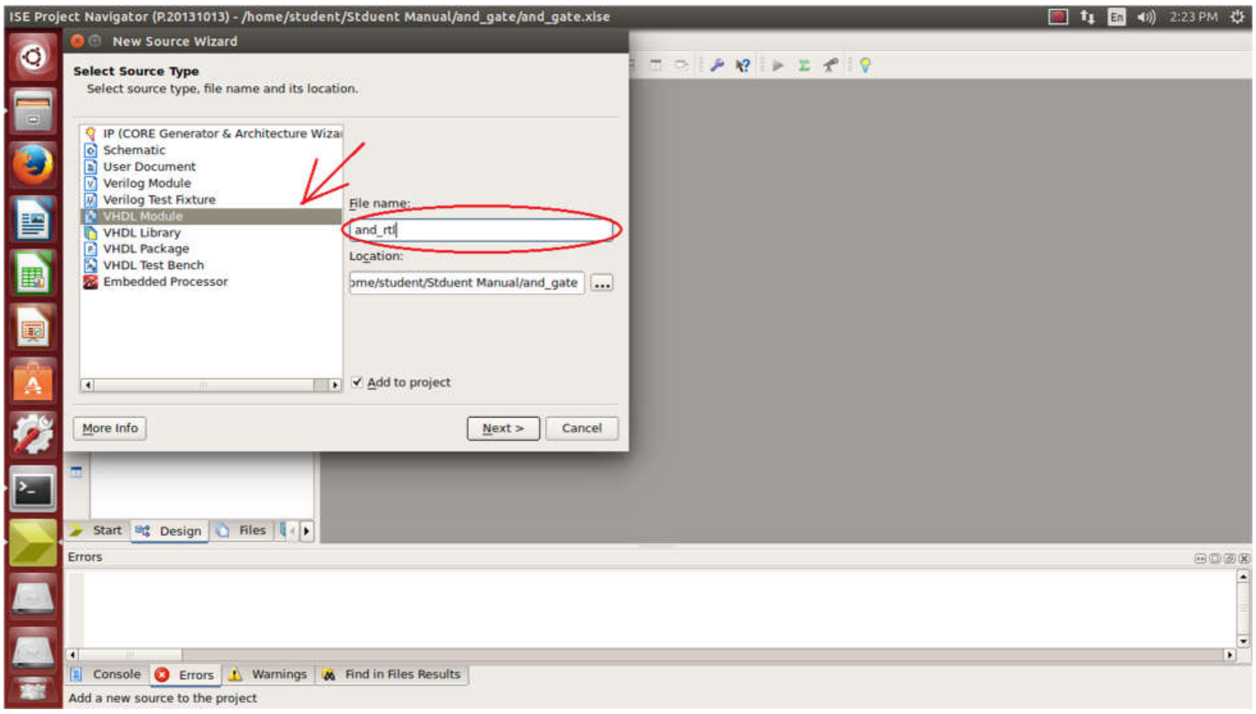

ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
and_gate
xc3s50-5pq208
No Processes Running
Design Utilities
Start Design Files
Errors
Console Errors Warnings Find in Files Results

Empty View

The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.

No single design module is selected

Step 9: The **New Source Wizard** opens. Click on **VHDL Module** and enter the **File name**. After this is done, click on **Next**.



Select Source Type

Select source type, file name and its location.

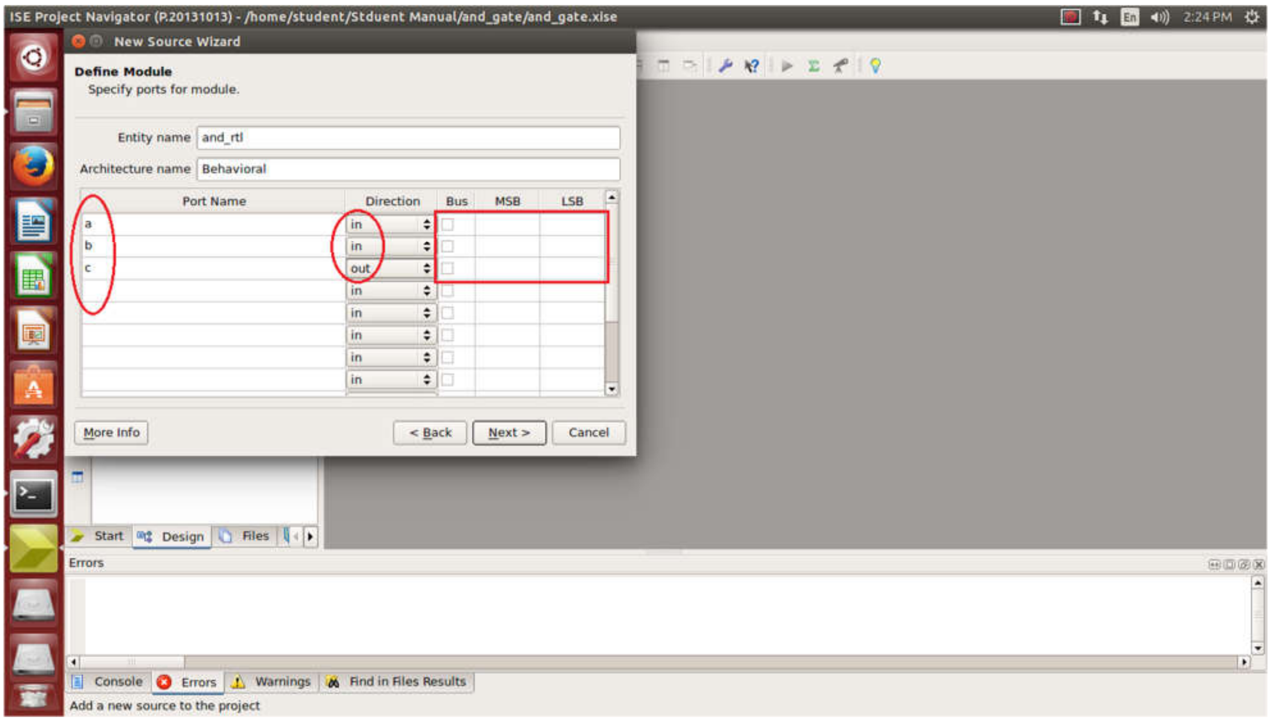
File name: and_rtl

Location: ome/student/Stduent Manual/and_gate

✓ Add to project

Add a new source to the project

Step 10: The **Define Module** window opens to enable us to define the required *ports* and their *characteristics*. Enter the names of the port in the **Port Name** column, select their corresponding *input/output characteristic* in **Direction** column and *bus length* (first select the check box in the **Bus** column if you want it to be a bus then specify the **MSB** and **LSB**) where ever required.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise

New Source Wizard

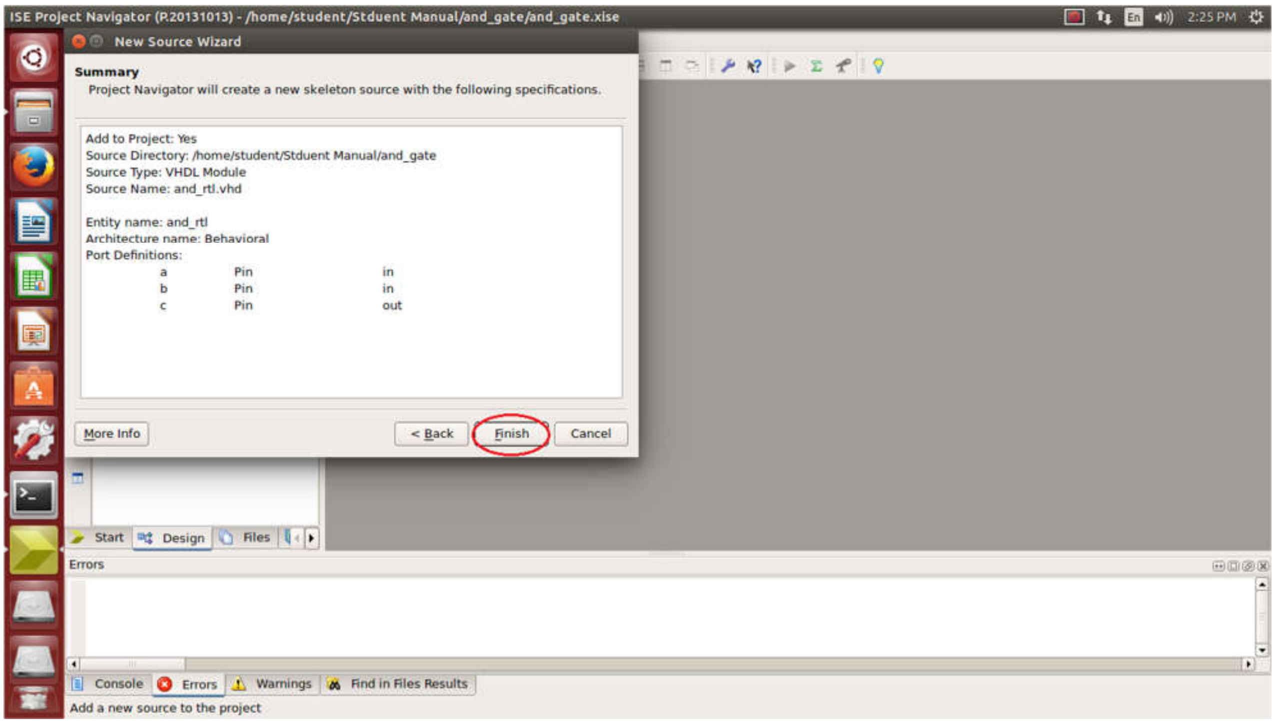
Define Module
Specify ports for module.

Entity name: and_rtl
Architecture name: Behavioral

Port Name	Direction	Bus	MSB	LSB
a	in	☐		
b	in	☐		
c	out	☐		
	in	☐		
	in	☐		
	in	☐		
	in	☐		
	in	☐		

Add a new source to the project

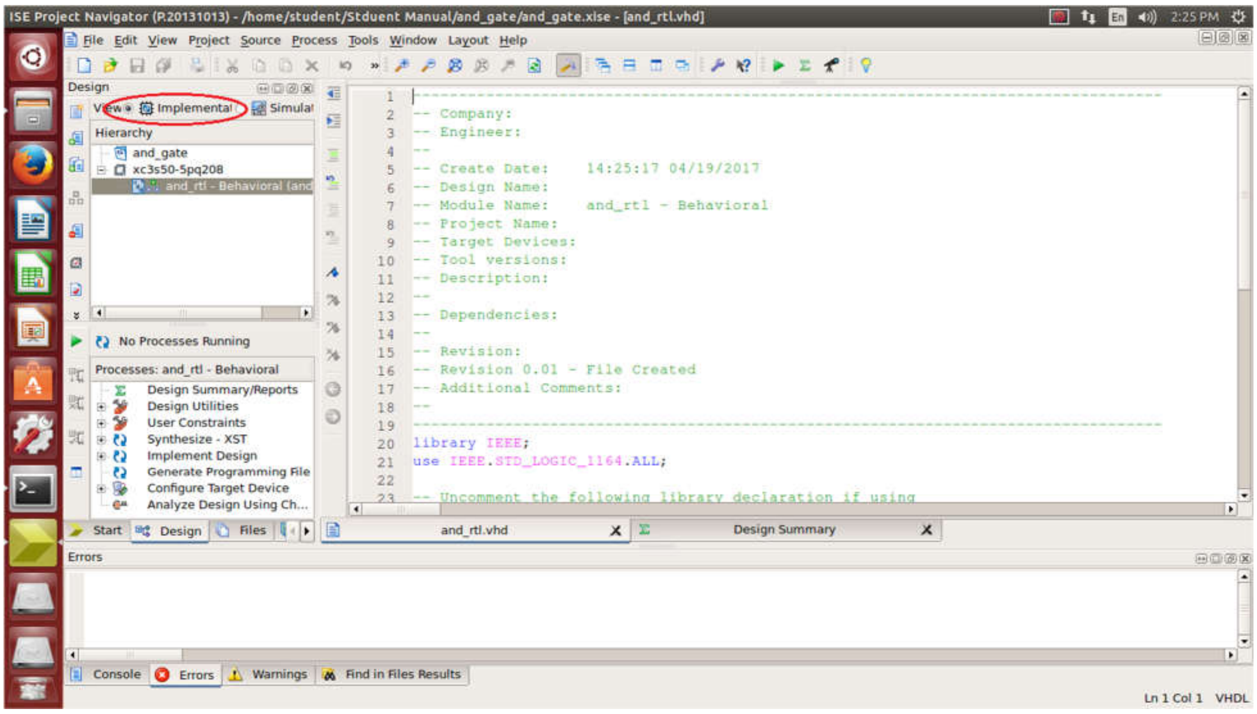
Step 11: The **Summary** window appears which displays the details of the defined module. Click on **Finish.**



```
Summary
  Project Navigator will create a new skeleton source with the following specifications.

Add to Project: Yes
Source Directory: /home/student/Stduent Manual/and_gate
Source Type: VHDL Module
Source Name: and_rtl.vhd

Entity name: and_rtl
Architecture name: Behavioral
Port Definitions:
          a          Pin          in
          b          Pin          in
          c          Pin          out
```

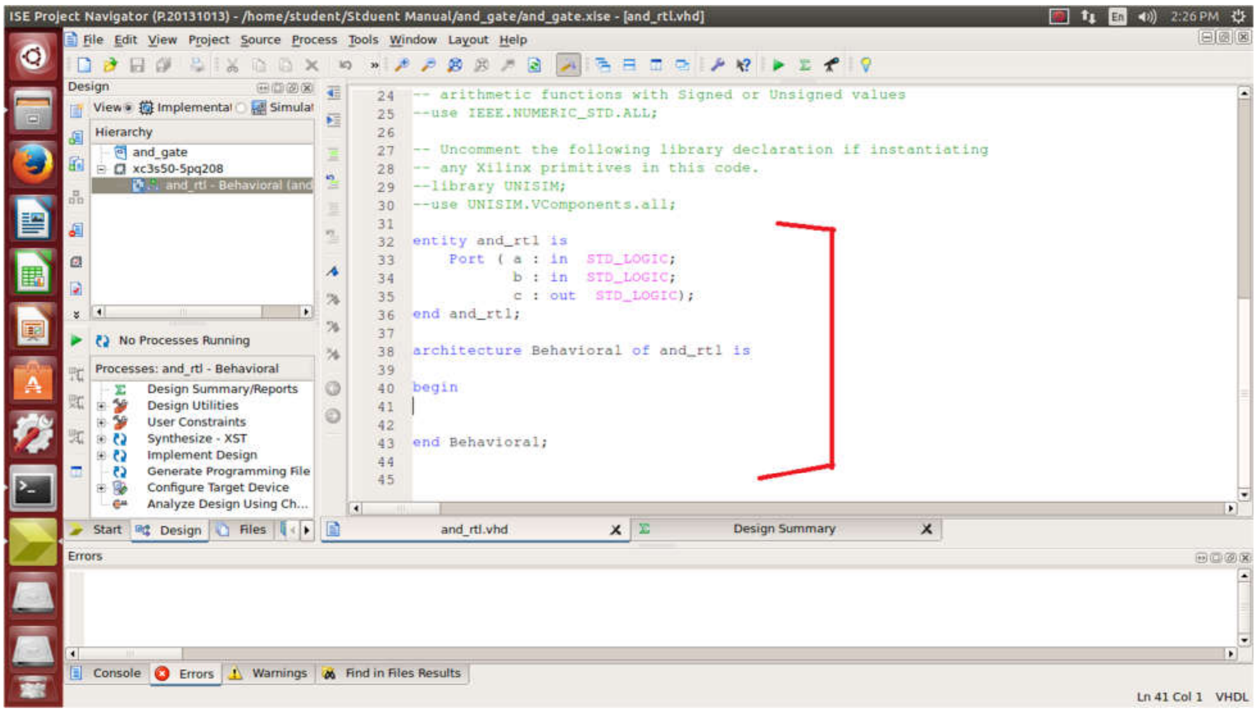
ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise
New Source Wizard
More Info
< Back
Finish
Cancel
Start
Design
Files
Errors
Console
Errors
Warnings
Find in Files Results
Add a new source to the project
2:25 PM

Step 12: The **RTL Behavioral** opens. By default the **Implementation** viewing option is selected in the **Design** panel.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd]
2:25 PM
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
and_gate
xc3s50-5pq208
and_rtl - Behavioral (and
No Processes Running
Processes: and_rtl - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Ch...
Start
Design
Files
and_rtl.vhd
Design Summary
Errors
Console
Errors
Warnings
Find in Files Results
Ln 1 Col 1 VHDL

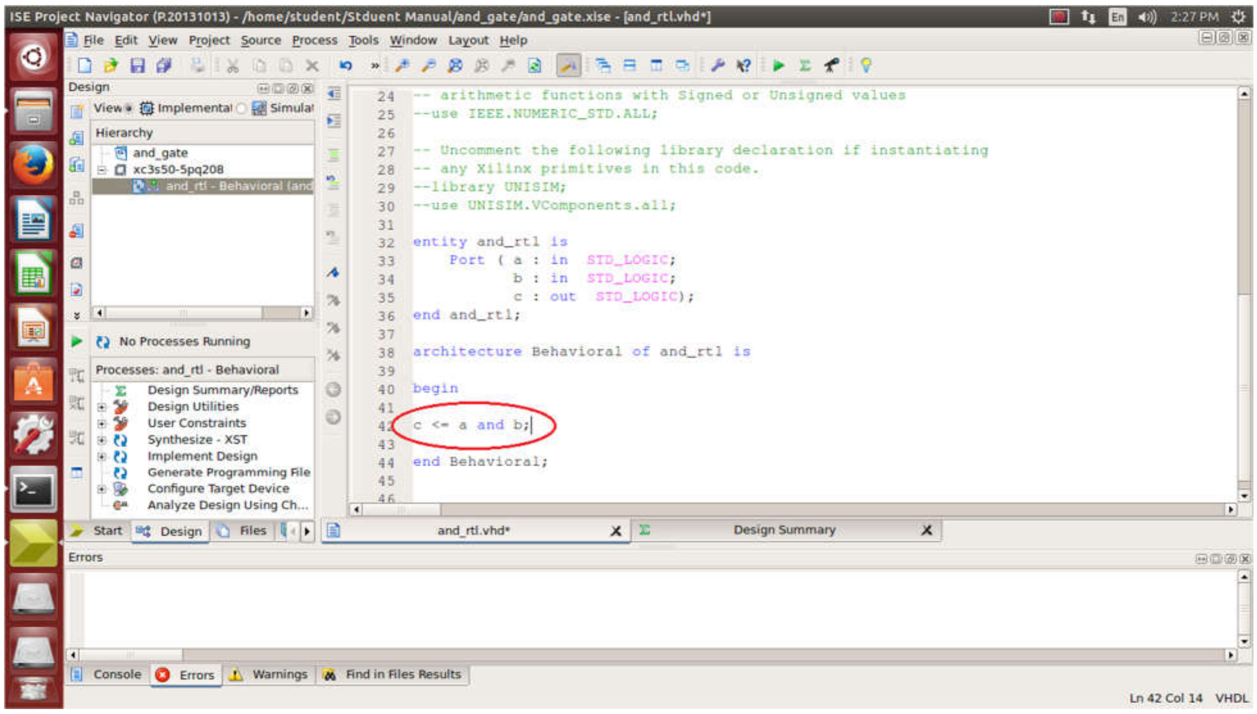
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    14:25:17 04/19/2017
-- Design Name:
-- Module Name:    and_rtl - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
```

Step 13: Scroll down to the part where the **entity** block is defined.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd]
2:26 PM
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
and_gate
xc3s50-5pq208
and_rtl - Behavioral (and
No Processes Running
Processes: and_rtl - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using Ch...
Start
Design
Files
and_rtl.vhd
Design Summary
Errors
Console
Errors
Warnings
Find in Files Results
Ln 41 Col 1 VHDL

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity and_rtl is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end and_rtl;

architecture Behavioral of and_rtl is

begin


end Behavioral;
```

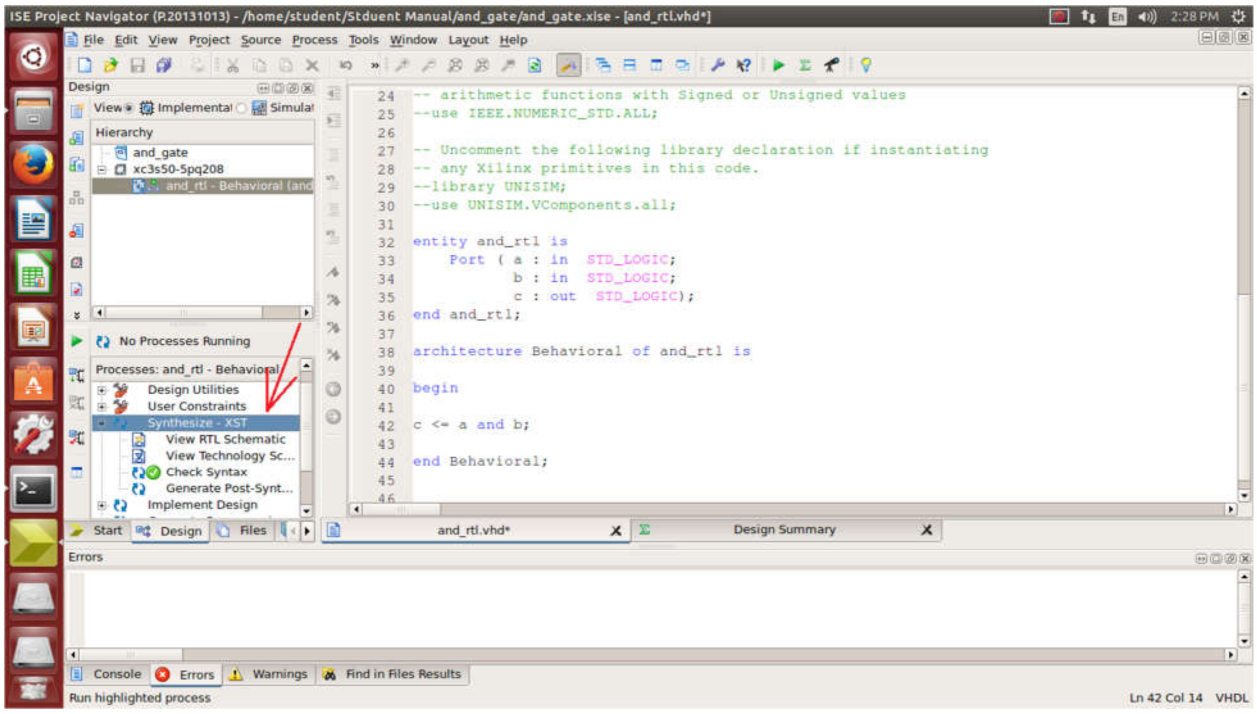
Step 14: Write down the code after the entity block. In the given example, the required code has to be written in the **Behavioral** block. If any additional variables are needed then they are declared *before* the *beginning of the **Behavioral** block.*



ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd*]

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity and_rtl is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end and_rtl;

architecture Behavioral of and_rtl is

begin

c <= a and b;

end Behavioral;
```

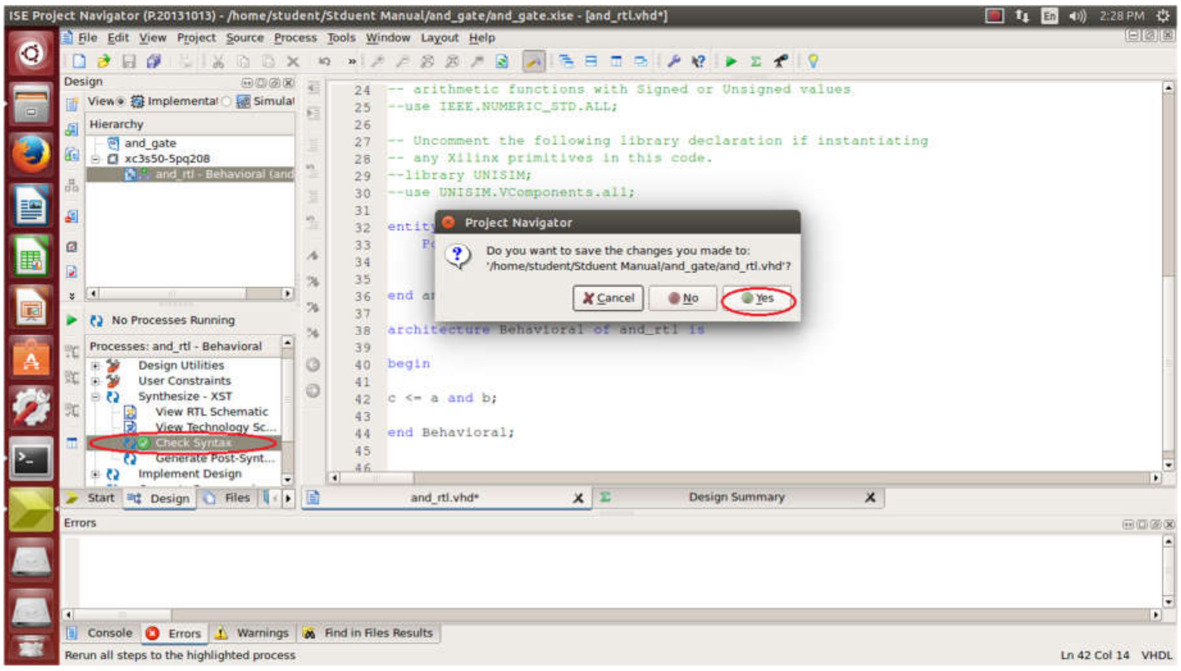
Step 15: After writing the code click and expand the **Synthesize-XST** option present in the **Processes** panel in the *left side* of the screen.



ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd*]

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity and_rtl is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end and_rtl;

architecture Behavioral of and_rtl is

begin

c <= a and b;

end Behavioral;
```

Step 16: Click on the **Check Syntax** option which appears *under* **Synthesize-XST**. On doing that a dialogue box appears asking whether you want to save the changes that have been made. Click **Yes**.



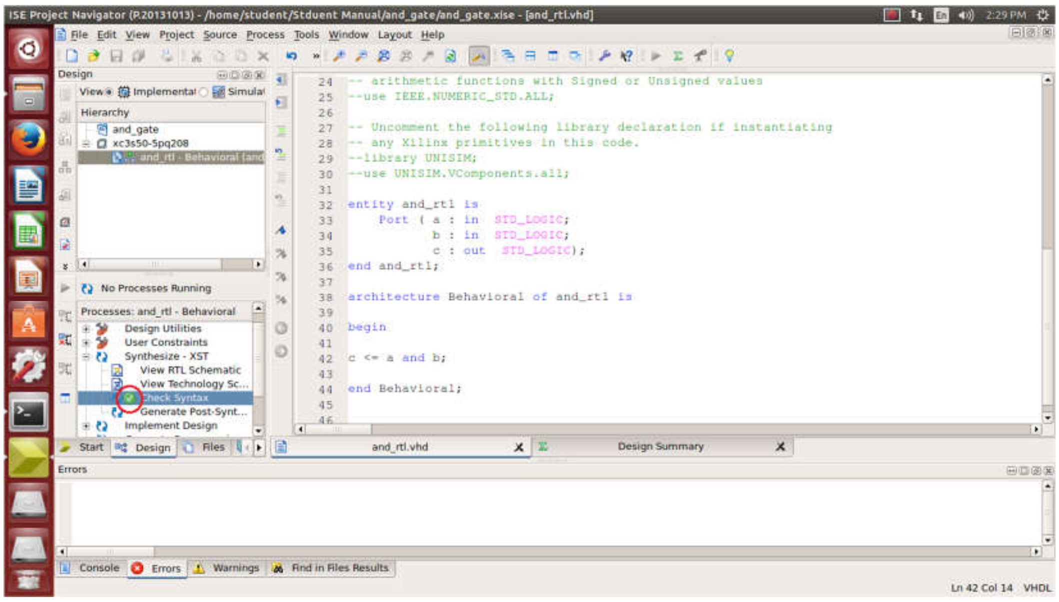
ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd*]

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity
    Po

end a

architecture Behavioral of and_rtl is

begin

c <= a and b;

end Behavioral;
```

Project Navigator

Do you want to save the changes you made to: '/home/student/Stduent Manual/and_gate/and_rtl.vhd'?

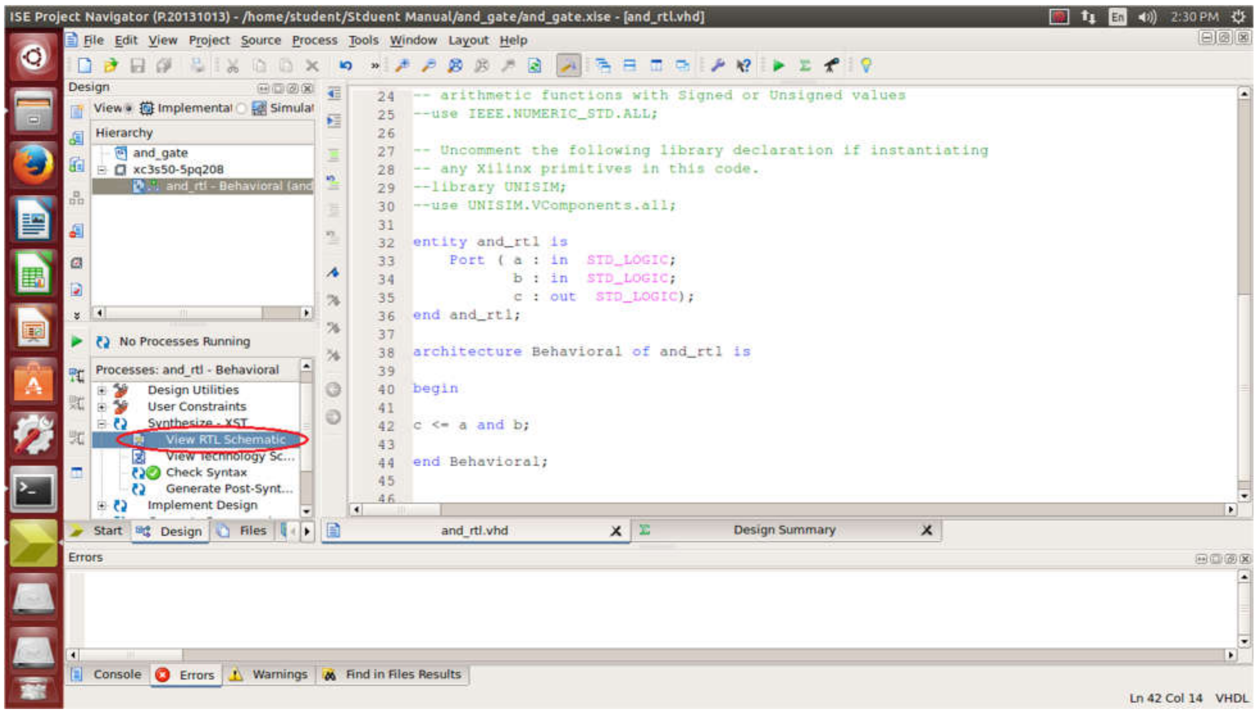
Step 17: The **Check Syntax** checks for *syntactical errors* in the code. If there is *no error* present then a **green tick** appears beside the **Check Syntax** option, or else a **red cross** appears indicating that the code has some *error*. If there are any errors, then make the necessary changes and right click **Check Syntax** and select **Rerun**.



ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd]

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity and_rtl is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end and_rtl;

architecture Behavioral of and_rtl is

begin

c <= a and b;

end Behavioral;
```

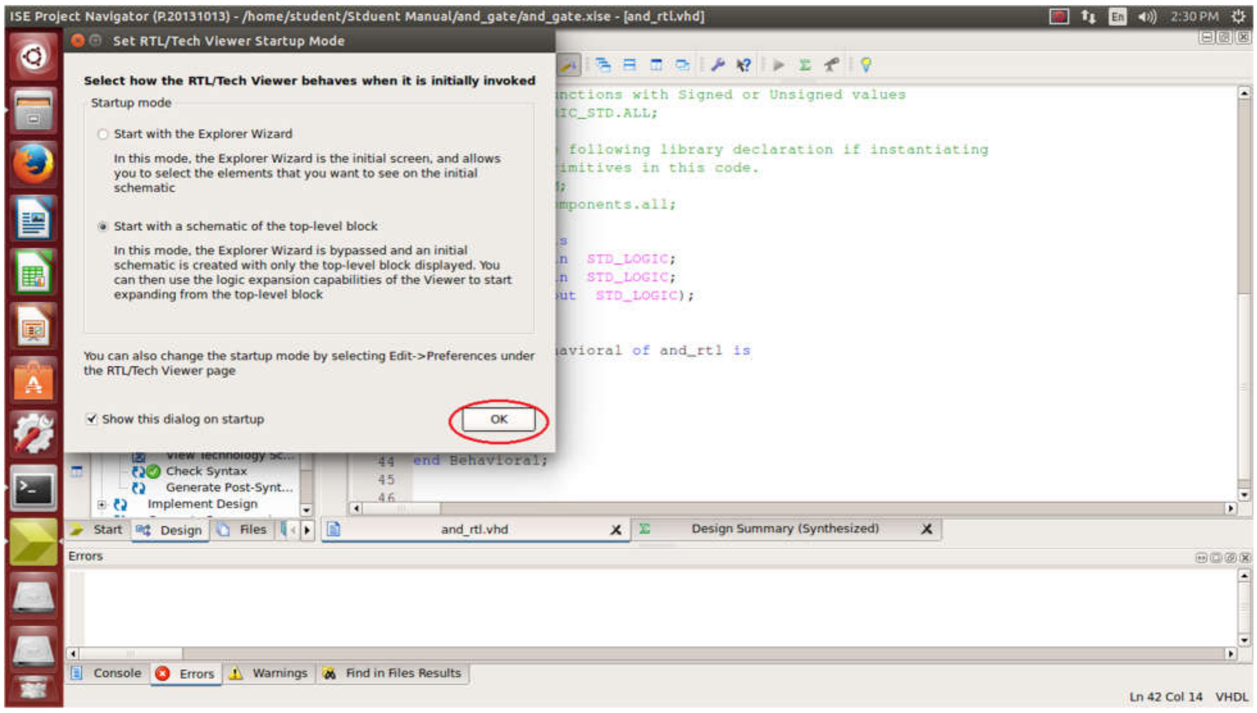
Step 18: Once the green tick appears click on **View RTL Schematic.**



ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd]

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity and_rtl is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end and_rtl;

architecture Behavioral of and_rtl is

begin

c <= a and b;

end Behavioral;
```

Step 19: Select the necessary viewing arrangement in the Startup Mode window and click on **OK** to proceed.



Set RTL/Tech Viewer Startup Mode

Select how the RTL/Tech Viewer behaves when it is initially invoked

Startup mode

( ) Start with the Explorer Wizard

In this mode, the Explorer Wizard is the initial screen, and allows you to select the elements that you want to see on the initial schematic

(●) Start with a schematic of the top-level block

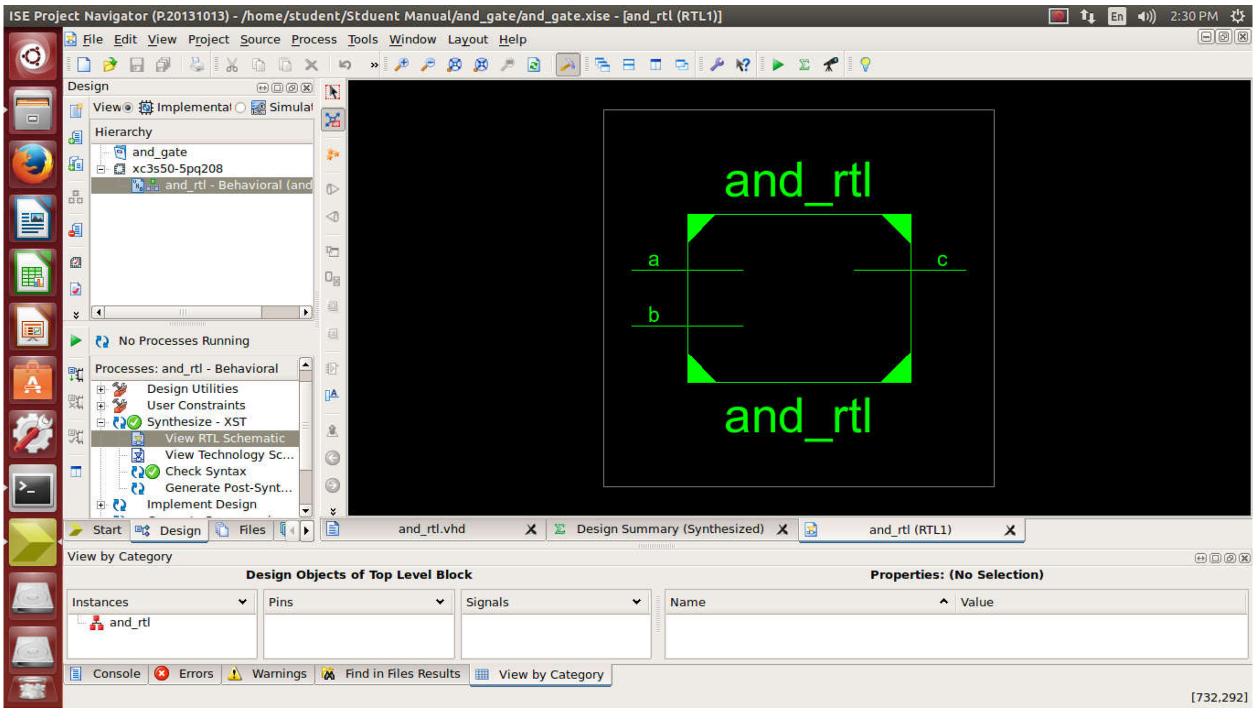
In this mode, the Explorer Wizard is bypassed and an initial schematic is created with only the top-level block displayed. You can then use the logic expansion capabilities of the Viewer to start expanding from the top-level block

You can also change the startup mode by selecting Edit->Preferences under the RTL/Tech Viewer page

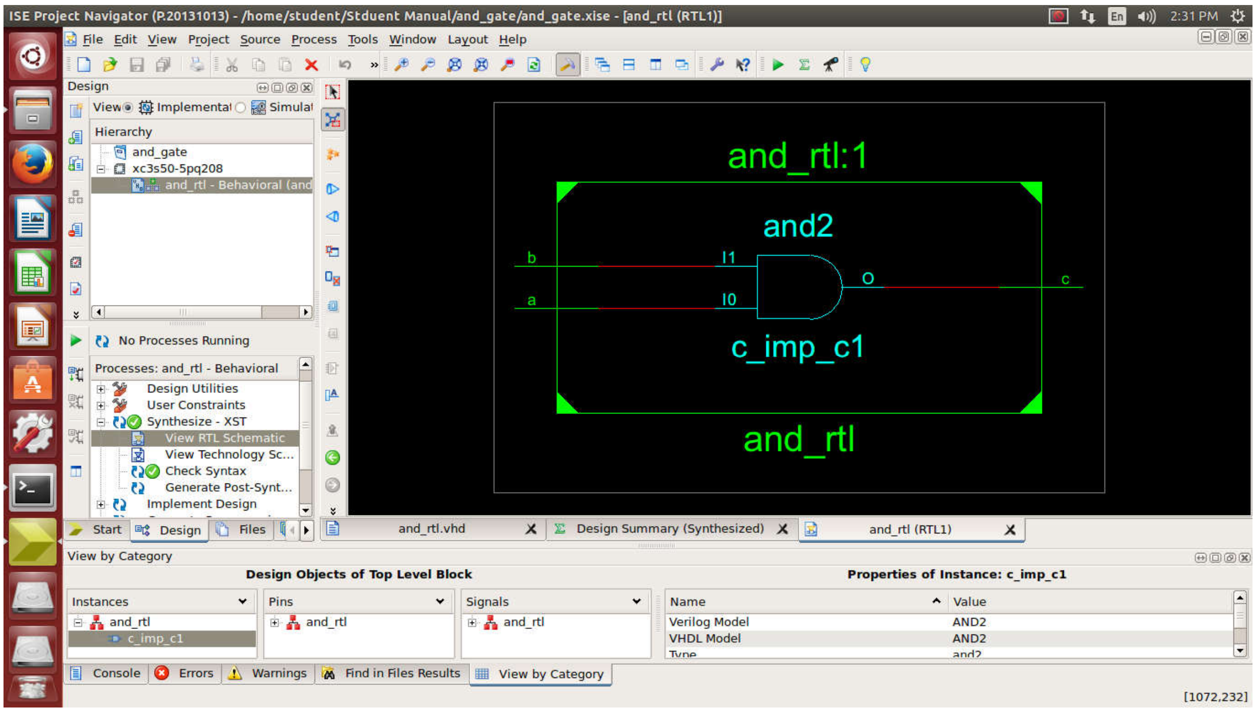
[✓] Show this dialog on startup

OK

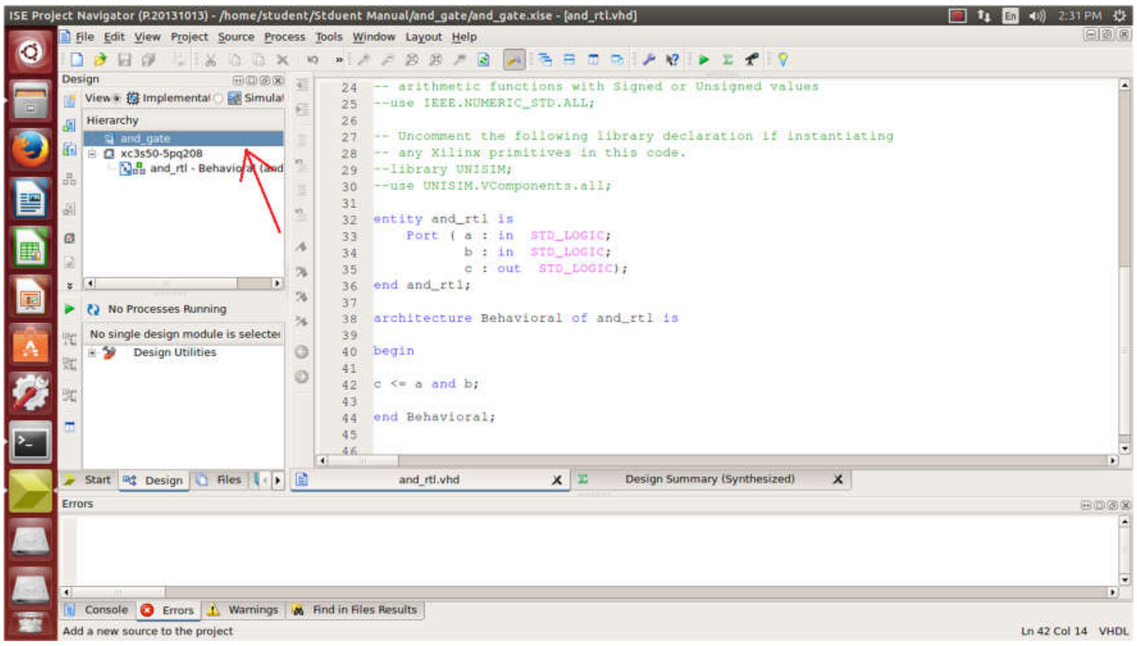
Step 20: The written code is compiled and the **RTL Schematic** is viewed. The window shows a *schematic diagram* of the written code along with the given input and output ports.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl (RTL1)]
and_rtl
a
b
c
and_rtl
No Processes Running
Processes: and_rtl - Behavioral
View RTL Schematic
Design Objects of Top Level Block
Properties: (No Selection)
Instances
and_rtl

Double click on the schematic for a detailed view.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl (RTL1)]
and_rtl:1
and2
b
I1
a
I0
O
c
c_imp_c1
and_rtl
Design Objects of Top Level Block
Properties of Instance: c_imp_c1
Verilog Model AND2
VHDL Model AND2
Type and2

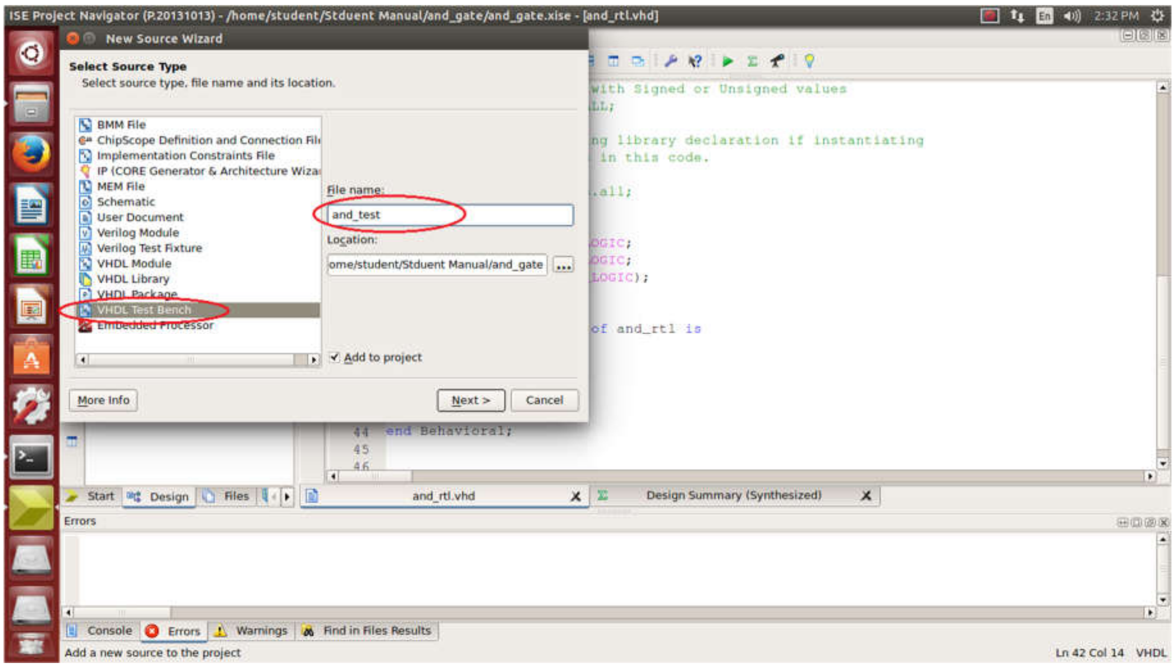
Step 21: After the RTL Schematic has been created, test cases have to be provided to the input ports to get the output waveform and check the whether the output is as desired. For this we need to create a **Test Bench**. *Right click* on the project name written at the top of the design panel and select **New Source**.



ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd]

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity and_rtl is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           c : out  STD_LOGIC);
end and_rtl;

architecture Behavioral of and_rtl is

begin

c <= a and b;

end Behavioral;
```

Step 22: The **New Source Wizard** opens. Select the **VHDL Test Bench** option and name the test bench module in the **File Name** box (name should be different than the VHDL Module name created in step 9). After completing this task click **Next** to proceed.



New Source Wizard

Select Source Type

Select source type, file name and its location.

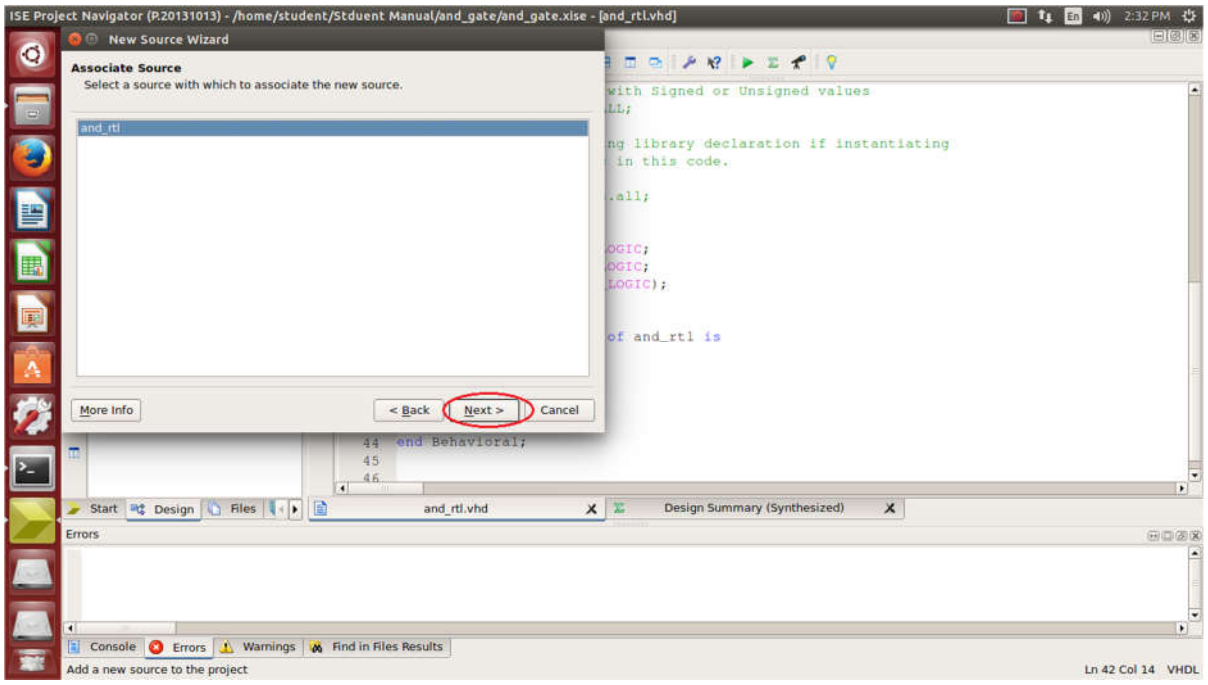
- BMM File
- ChipScope Definition and Connection File
- Implementation Constraints File
- IP (CORE Generator & Architecture Wizard)
- MEM File
- Schematic
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench
- Embedded Processor

File name: and_test

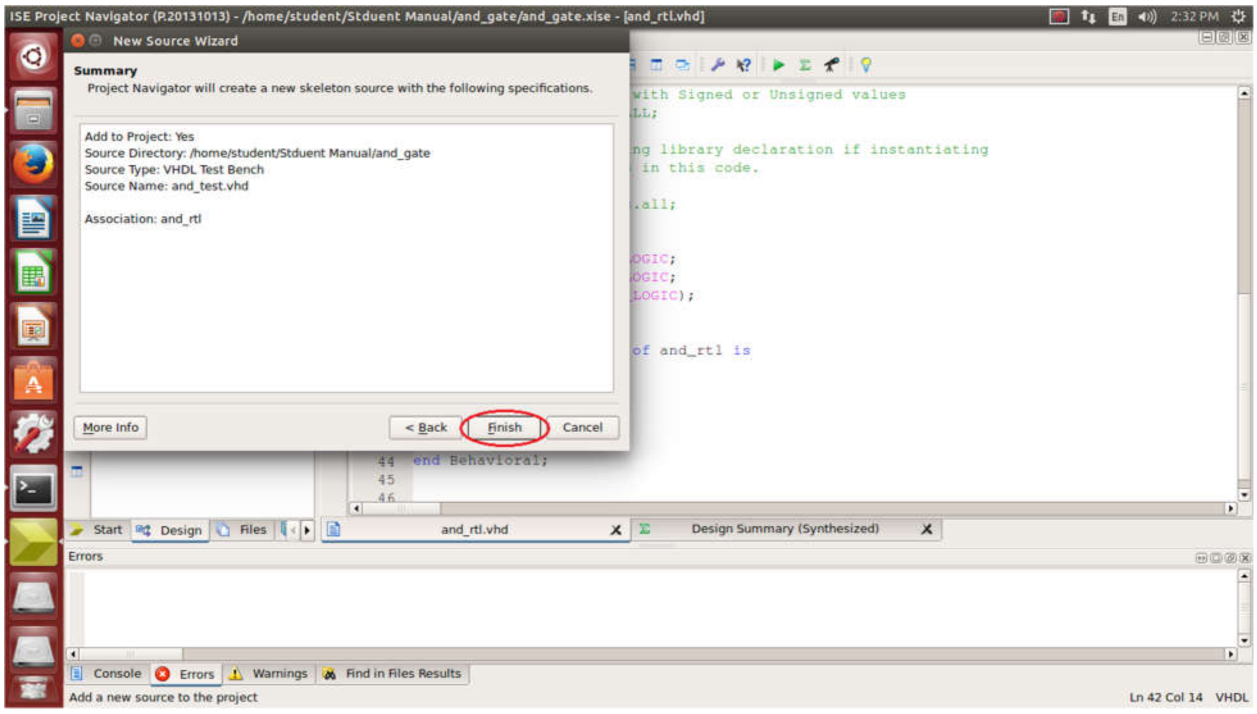
Location: ome/student/Stduent Manual/and_gate

✓ Add to project

Step 23: Xilinx automatically associates this test bench file with the RTL file that had been created earlier. Click **Next** to proceed.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd]
New Source Wizard
Associate Source
Select a source with which to associate the new source.
and_rtl
More Info
< Back
Next >
Cancel
Start
Design
Files
and_rtl.vhd
Design Summary (Synthesized)
Errors
Console
Warnings
Find in Files Results
Add a new source to the project
Ln 42 Col 14 VHDL

Step 24: Check the details of the test bench veing created in the **Summary** window and click Finish to create the test bench.

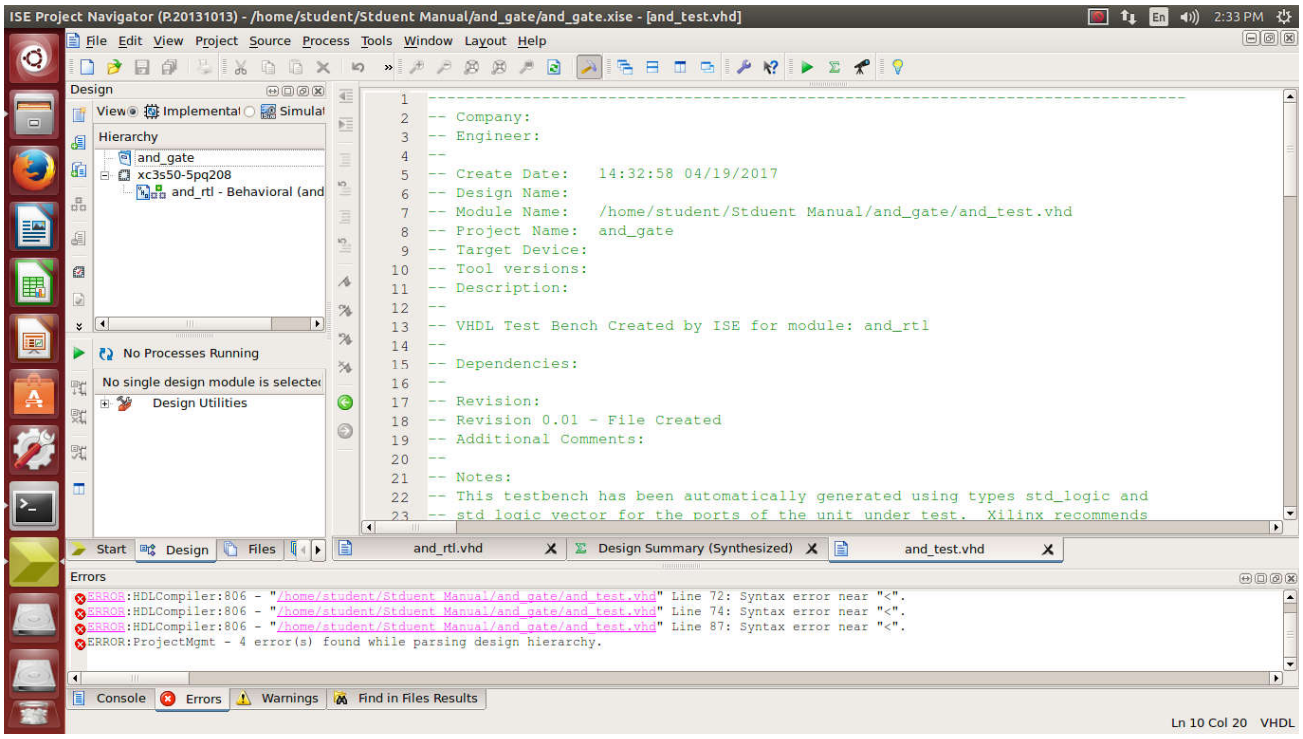

ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_rtl.vhd]
New Source Wizard
More Info
< Back
Finish
Cancel
Start
Design
Files
and_rtl.vhd
Design Summary (Synthesized)
Errors
Console
Warnings
Find in Files Results
Add a new source to the project
Ln 42 Col 14 VHDL

Summary
Project Navigator will create a new skeleton source with the following specifications.

Add to Project: Yes
Source Directory: /home/student/Stduent Manual/and_gate
Source Type: VHDL Test Bench
Source Name: and_test.vhd

Association: and_rtl

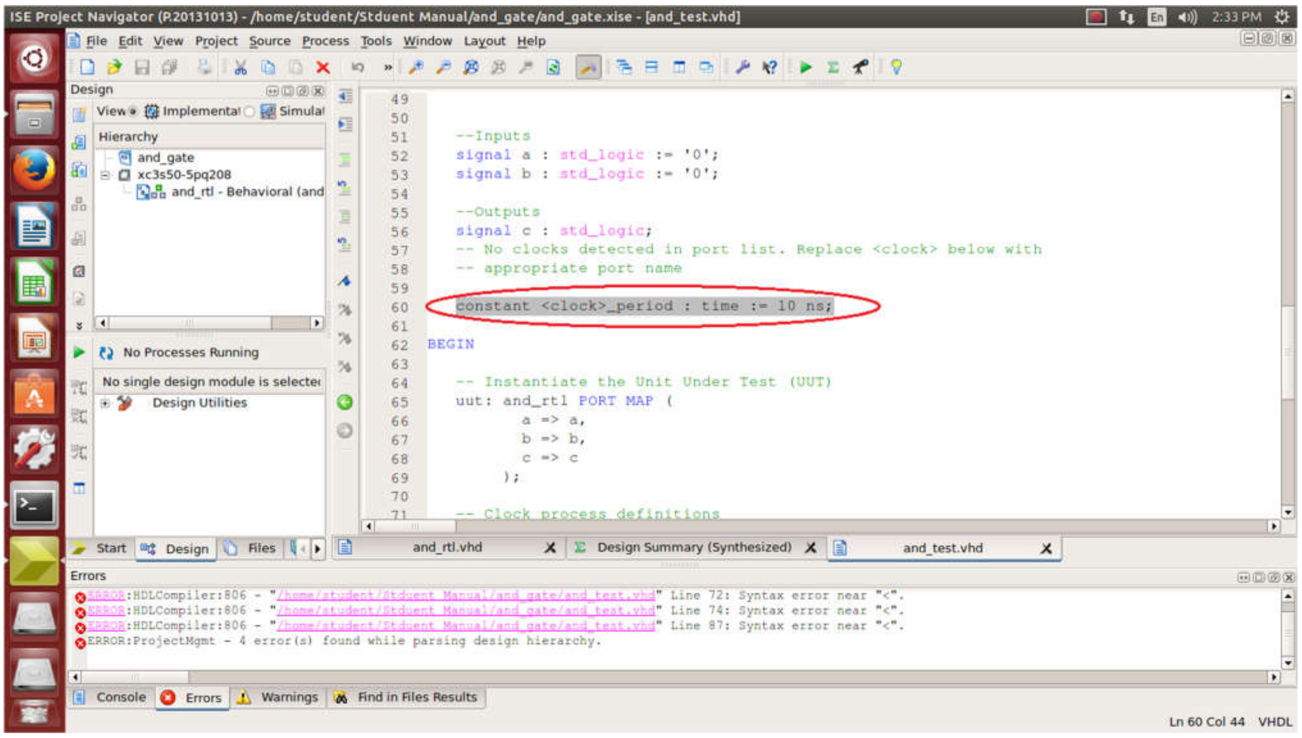
Step 25: The window for the test bench code opens.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View Implementation Simulation
Hierarchy
and_gate
xc3s50-5pq208
and_rtl - Behavioral (and
No Processes Running
No single design module is selected
Design Utilities
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 10 Col 20 VHDL

```
--------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:   14:32:58 04/19/2017
-- Design Name:
-- Module Name:   /home/student/Stduent Manual/and_gate/and_test.vhd
-- Project Name:  and_gate
-- Target Device:
-- Tool versions:
-- Description:
--
-- VHDL Test Bench Created by ISE for module: and_rtl
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-- Notes:
-- This testbench has been automatically generated using types std_logic and
-- std_logic_vector for the ports of the unit under test.  Xilinx recommends
```

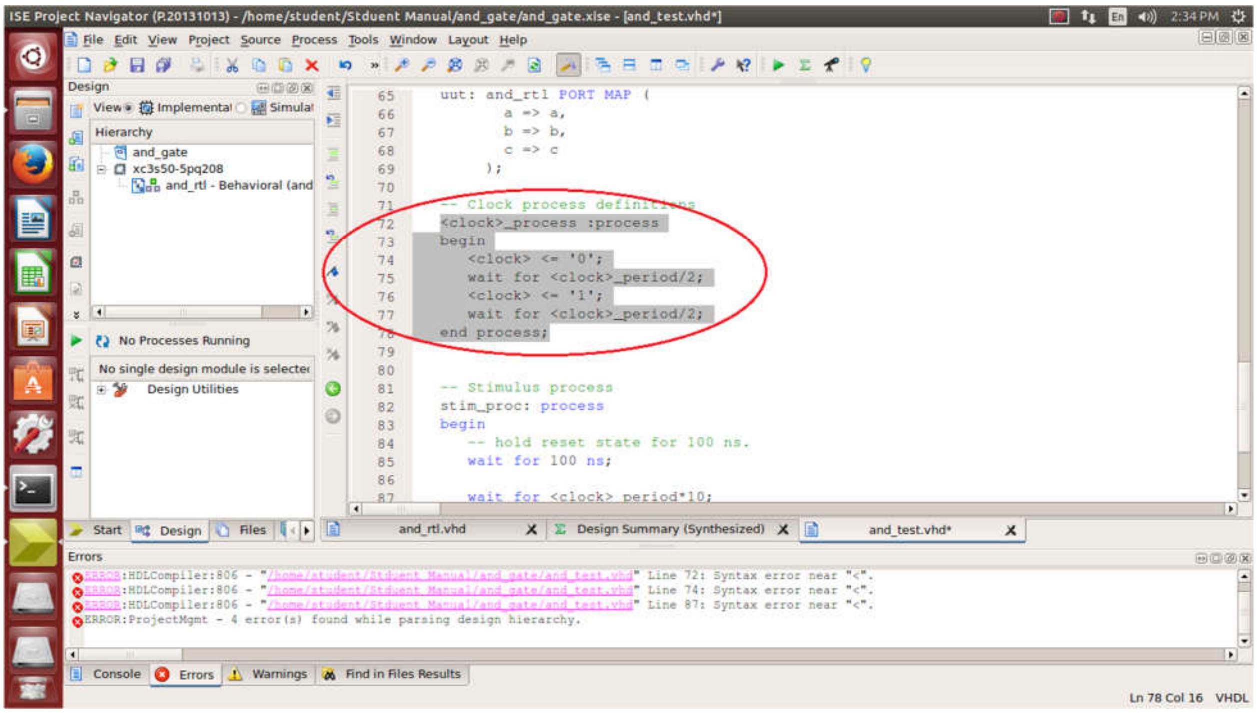
```
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 72: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 74: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 87: Syntax error near "<".
ERROR:ProjectMgmt - 4 error(s) found while parsing design hierarchy.
```

Step 26: Go throught the already written part of the code (deafult blocks of code) and *remove* the unwanted *clock commands*.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View Implementation Simulation
Hierarchy
and_gate
xc3s50-5pq208
and_rtl - Behavioral (and
No Processes Running
No single design module is selected
Design Utilities
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 60 Col 44 VHDL

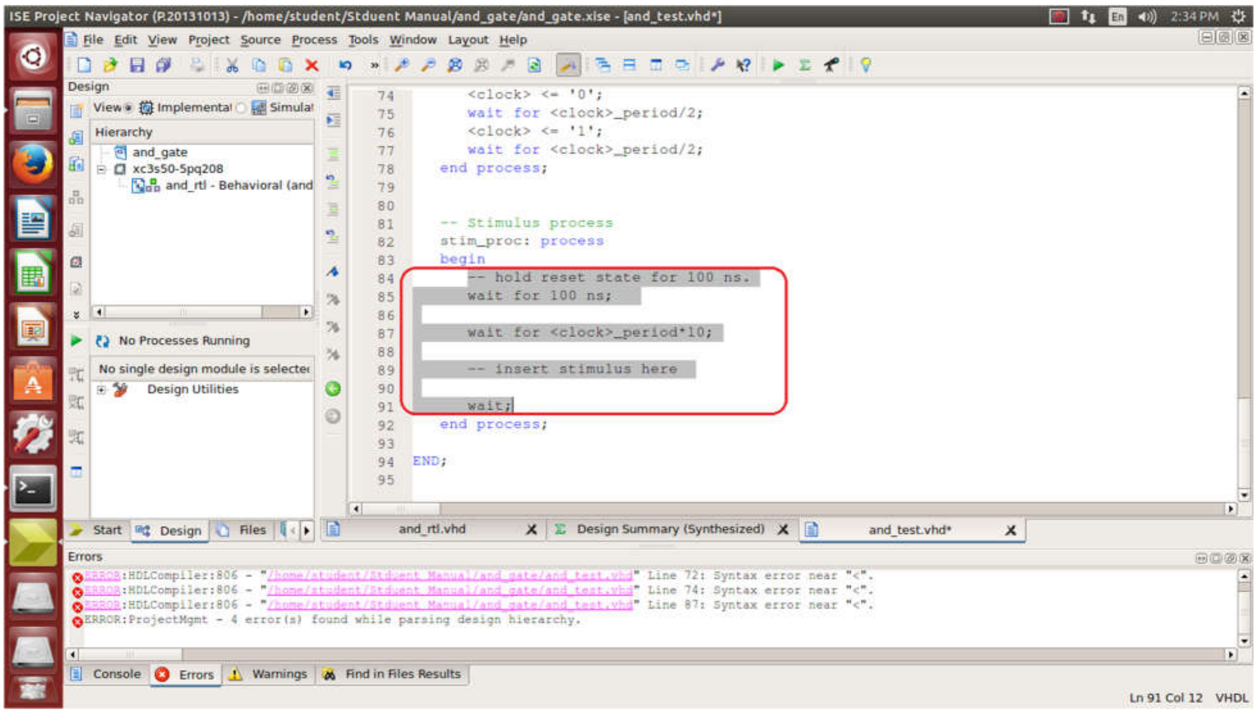
```


   --Inputs
   signal a : std_logic := '0';
   signal b : std_logic := '0';

   --Outputs
   signal c : std_logic;
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

   constant <clock>_period : time := 10 ns;

BEGIN

   -- Instantiate the Unit Under Test (UUT)
   uut: and_rtl PORT MAP (
          a => a,
          b => b,
          c => c
        );

   -- Clock process definitions
```

```
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 72: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 74: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 87: Syntax error near "<".
ERROR:ProjectMgmt - 4 error(s) found while parsing design hierarchy.
```


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd*]
File Edit View Project Source Process Tools Window Layout Help
Design
View ◉ Implementation ○ Simulation
Hierarchy
and_gate
xc3s50-5pq208
and_rtl - Behavioral (and
No Processes Running
No single design module is selected
Design Utilities
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd*
Console Errors Warnings Find in Files Results
Ln 78 Col 16 VHDL

```
   uut: and_rtl PORT MAP (
          a => a,
          b => b,
          c => c
        );

   -- Clock process definitions
   <clock>_process :process
   begin
      <clock> <= '0';
      wait for <clock>_period/2;
      <clock> <= '1';
      wait for <clock>_period/2;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 100 ns;

      wait for <clock>_period*10;
```

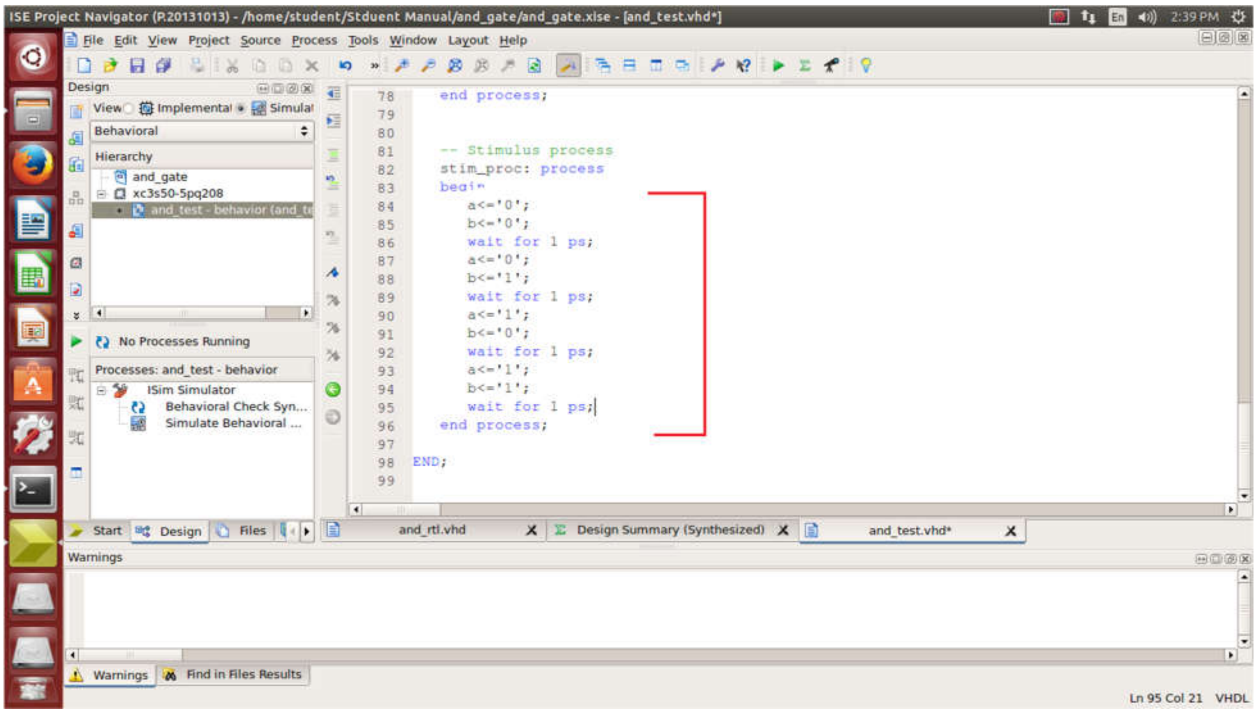
```
Errors
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 72: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 74: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 87: Syntax error near "<".
ERROR:ProjectMgmt - 4 error(s) found while parsing design hierarchy.
```


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd*]
File Edit View Project Source Process Tools Window Layout Help
Design
View ◉ Implementation ○ Simulation
Hierarchy
and_gate
xc3s50-5pq208
and_rtl - Behavioral (and
No Processes Running
No single design module is selected
Design Utilities
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd*
Console Errors Warnings Find in Files Results
Ln 91 Col 12 VHDL

```
      <clock> <= '0';
      wait for <clock>_period/2;
      <clock> <= '1';
      wait for <clock>_period/2;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 100 ns;

      wait for <clock>_period*10;

      -- insert stimulus here

      wait;
   end process;

END;
```

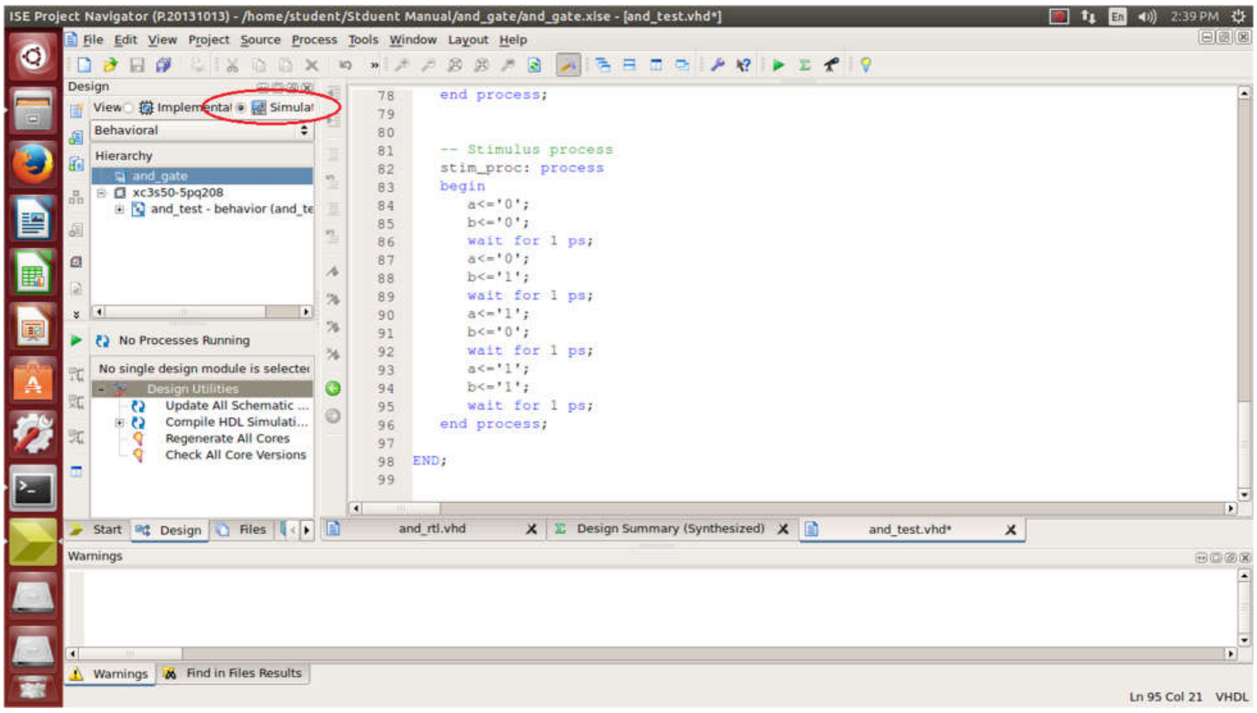
```
Errors
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 72: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 74: Syntax error near "<".
ERROR:HDLCompiler:806 - "/home/student/Stduent Manual/and_gate/and_test.vhd" Line 87: Syntax error near "<".
ERROR:ProjectMgmt - 4 error(s) found while parsing design hierarchy.
```

Step 27: Write down the *test cases* for the input portals in in the **stim_proc** block.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_gate
xc3s50-5pq208
and_test - behavior (and_te
No Processes Running
Processes: and_test - behavior
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd*
Warnings
Find in Files Results
Ln 95 Col 21 VHDL

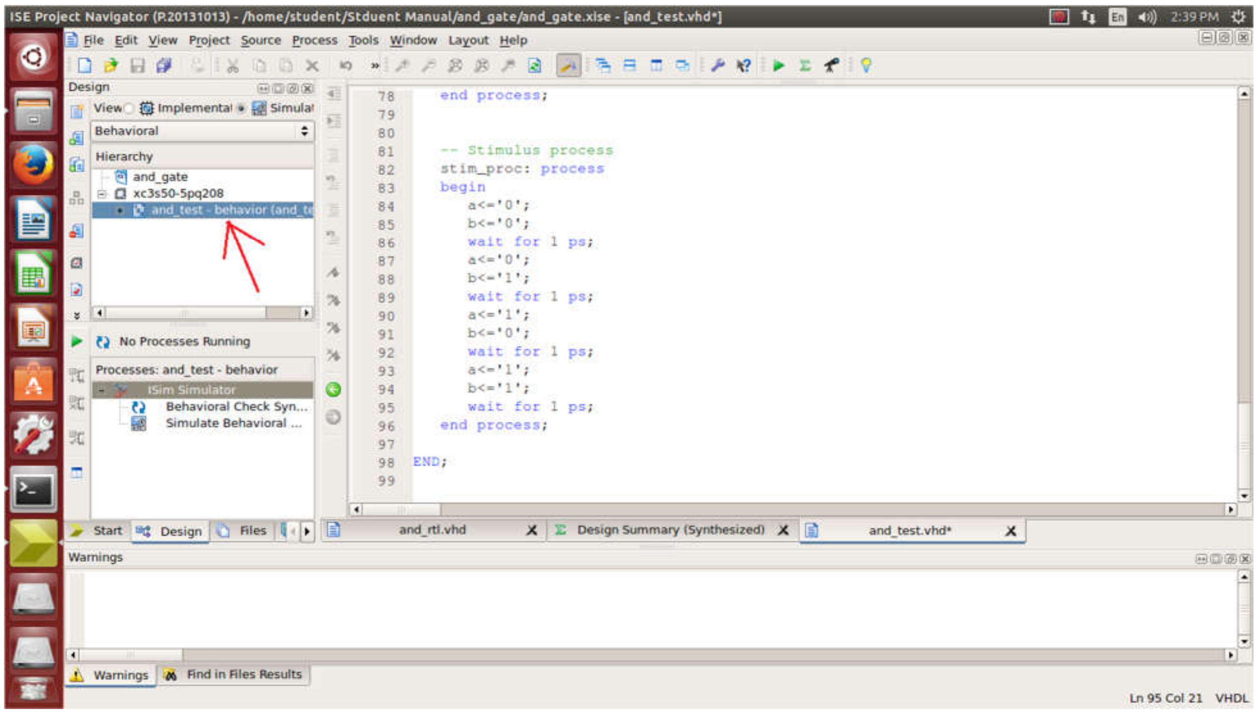
```
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        a<='0';
        b<='0';
        wait for 1 ps;
        a<='0';
        b<='1';
        wait for 1 ps;
        a<='1';
        b<='0';
        wait for 1 ps;
        a<='1';
        b<='1';
        wait for 1 ps;
    end process;

END;
```

Step 28: After writing the code for test bench, select the **Simulation** viewing option in the **Design** panel, which is on the left side of the screen.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd*]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_gate
xc3s50-5pq208
and_test - behavior (and_te
No Processes Running
No single design module is selected
Design Utilities
Update All Schematic ...
Compile HDL Simulati...
Regenerate All Cores
Check All Core Versions
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd*
Warnings
Find in Files Results
Ln 95 Col 21 VHDL

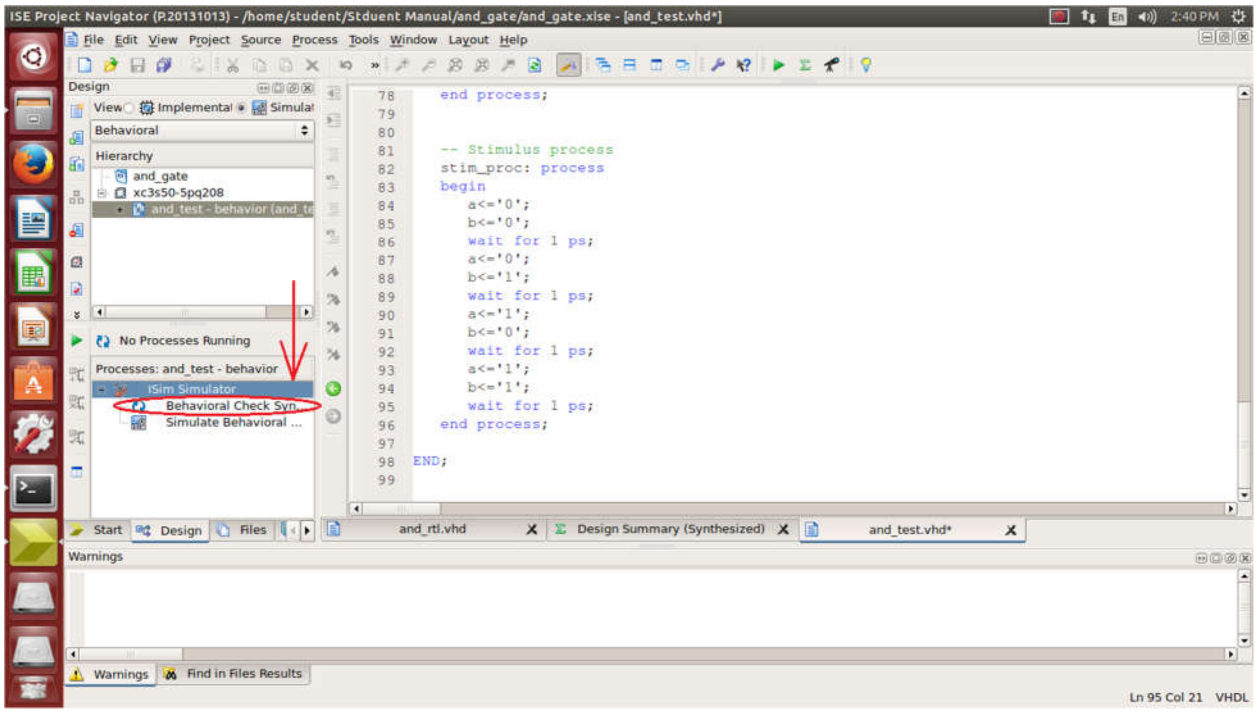
```
    end process;

    -- Stimulus process
    stim_proc: process
    begin
        a<='0';
        b<='0';
        wait for 1 ps;
        a<='0';
        b<='1';
        wait for 1 ps;
        a<='1';
        b<='0';
        wait for 1 ps;
        a<='1';
        b<='1';
        wait for 1 ps;
    end process;

END;
```

Step 29: Select the behavior option in the Design panel.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd*]
2:39 PM
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_gate
xc3s50-5pq208
and_test - behavior (and_te
No Processes Running
Processes: and_test - behavior
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start
Design
Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd*
Warnings
Warnings
Find in Files Results
Ln 95 Col 21 VHDL

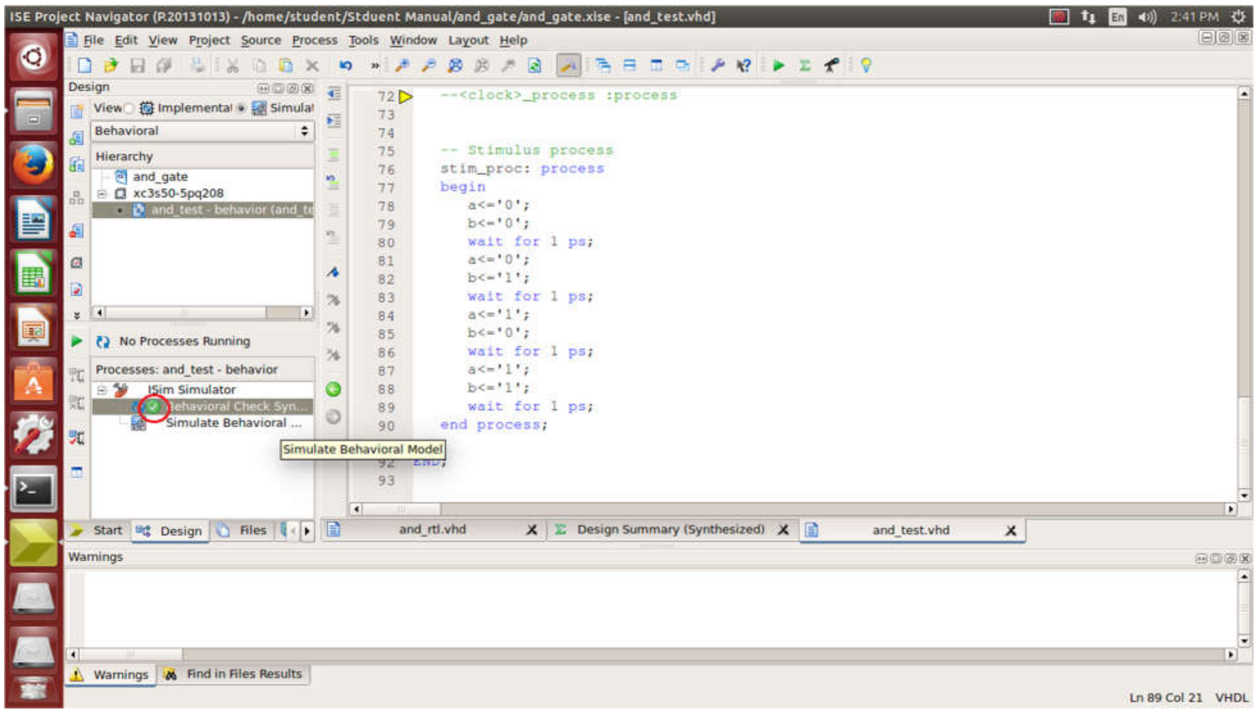
```
   end process;

   -- Stimulus process
   stim_proc: process
   begin
      a<='0';
      b<='0';
      wait for 1 ps;
      a<='0';
      b<='1';
      wait for 1 ps;
      a<='1';
      b<='0';
      wait for 1 ps;
      a<='1';
      b<='1';
      wait for 1 ps;
   end process;

END;
```

Step 30: Select and expand the **ISim Simulator** option in the **Processes** panel and click on **Behavioral Check Syntax**.


ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd*]
2:40 PM
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_gate
xc3s50-5pq208
and_test - behavior (and_te
No Processes Running
Processes: and_test - behavior
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start
Design
Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd*
Warnings
Warnings
Find in Files Results
Ln 95 Col 21 VHDL

```
   end process;

   -- Stimulus process
   stim_proc: process
   begin
      a<='0';
      b<='0';
      wait for 1 ps;
      a<='0';
      b<='1';
      wait for 1 ps;
      a<='1';
      b<='0';
      wait for 1 ps;
      a<='1';
      b<='1';
      wait for 1 ps;
   end process;

END;
```

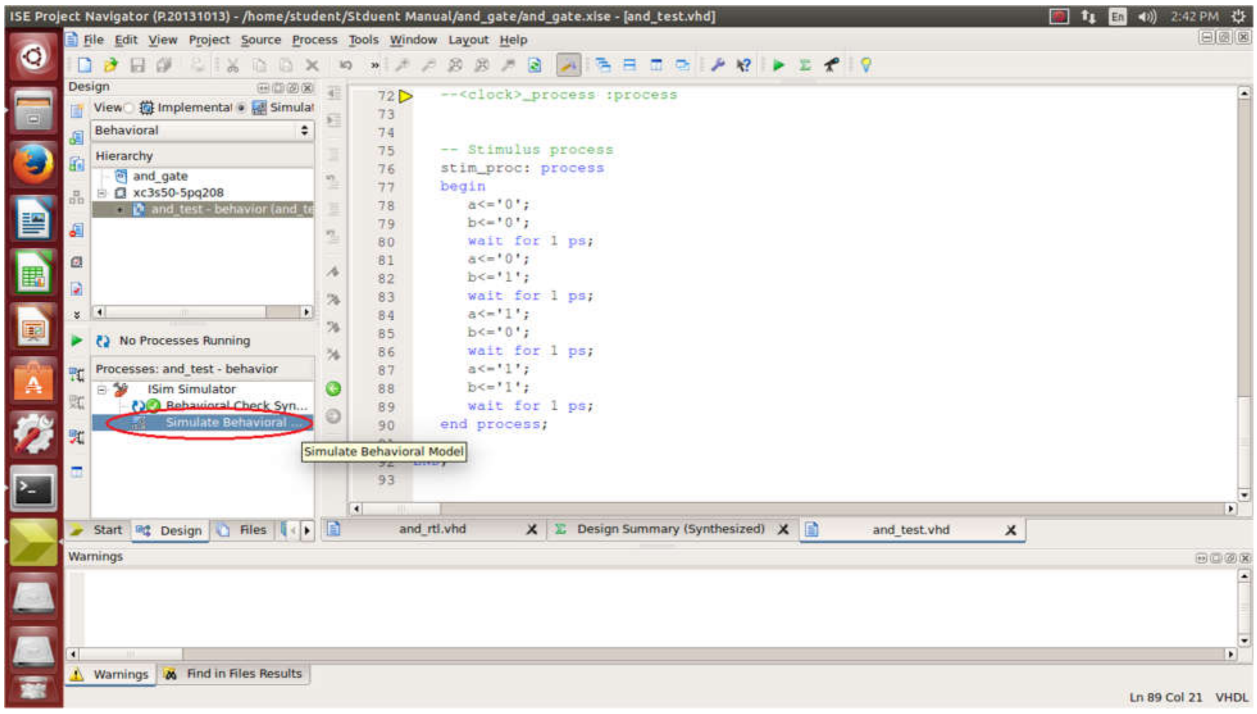
Step 31: If there are no syntactical errors in the code then a *green tick* appears beside the **Behavioral Check Syntax** option, or else a *red cross* appears indicating that the program is not error-free.



```
--<clock>_process :process

-- Stimulus process
stim_proc: process
begin
    a<='0';
    b<='0';
    wait for 1 ps;
    a<='0';
    b<='1';
    wait for 1 ps;
    a<='1';
    b<='0';
    wait for 1 ps;
    a<='1';
    b<='1';
    wait for 1 ps;
end process;
```

ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_gate
xc3s50-5pq208
and_test - behavior
No Processes Running
Processes: and_test - behavior
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Simulate Behavioral Model
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd
Warnings
Find in Files Results
Ln 89 Col 21 VHDL

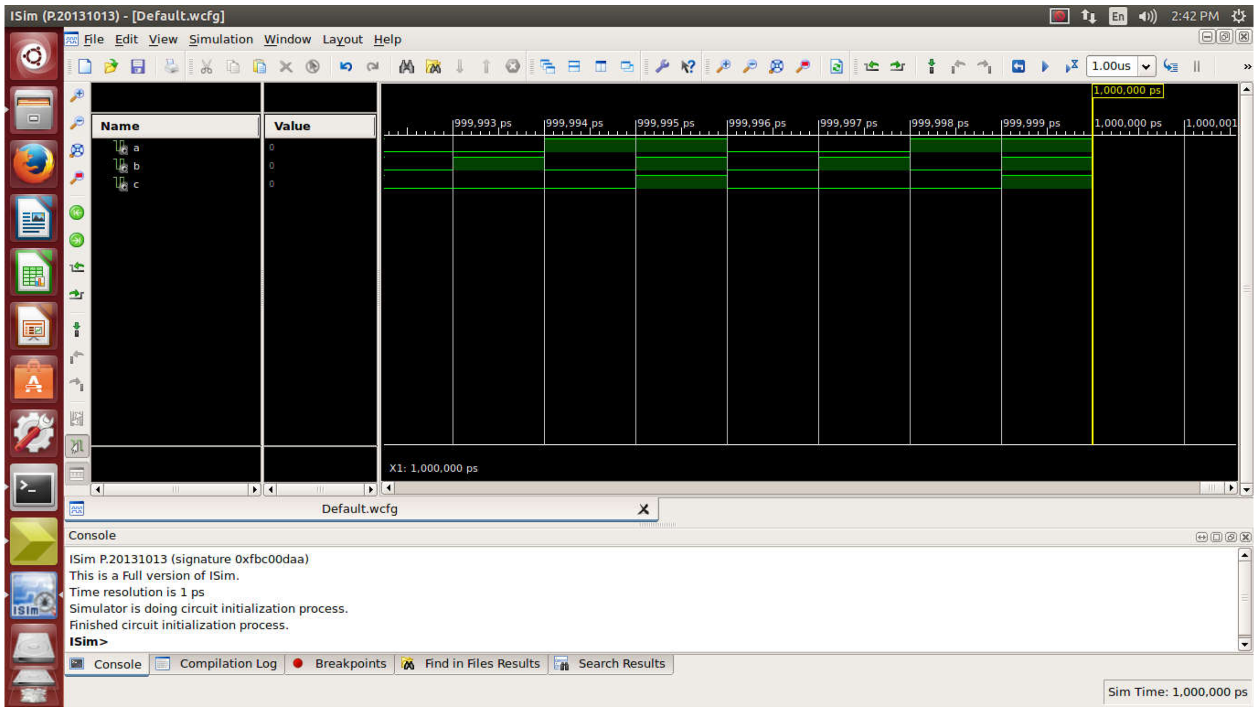
Step 32: Once the *green tick* apperas and it is clear that the code has no errors then click on the **Simulate Behavioral** option.



```
--<clock>_process :process

-- Stimulus process
stim_proc: process
begin
    a<='0';
    b<='0';
    wait for 1 ps;
    a<='0';
    b<='1';
    wait for 1 ps;
    a<='1';
    b<='0';
    wait for 1 ps;
    a<='1';
    b<='1';
    wait for 1 ps;
end process;
```

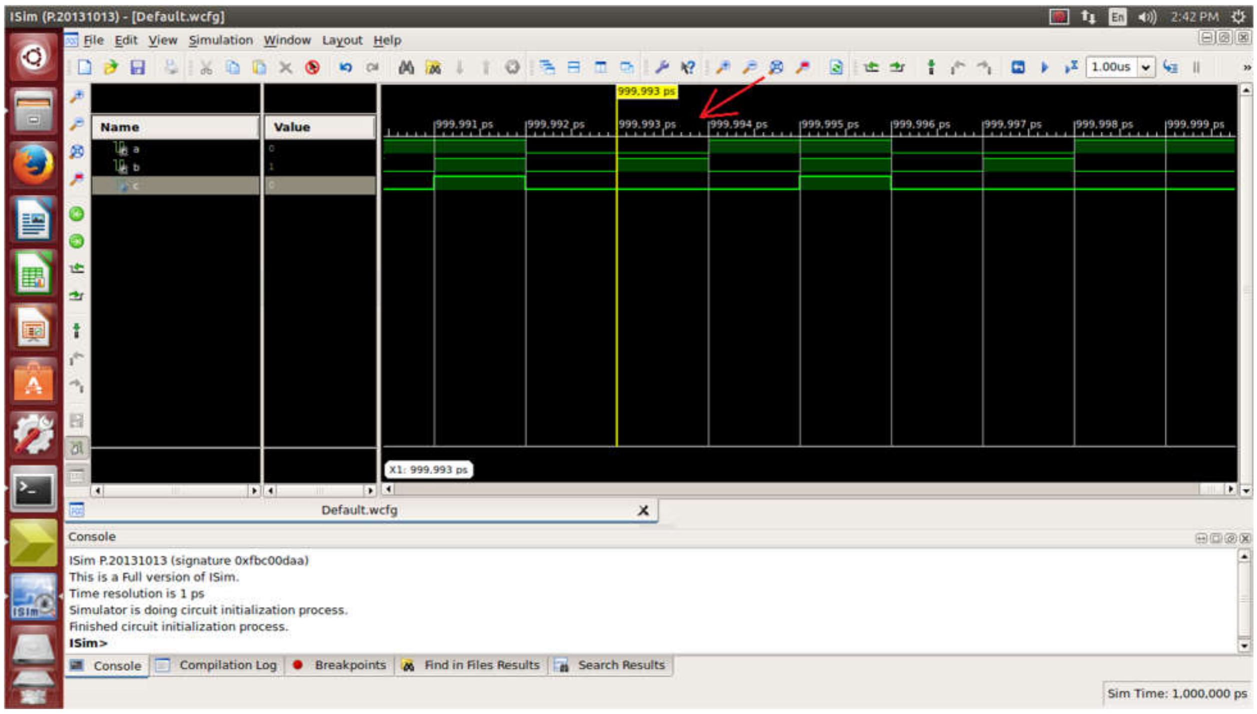
ISE Project Navigator (P.20131013) - /home/student/Stduent Manual/and_gate/and_gate.xise - [and_test.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
and_gate
xc3s50-5pq208
and_test - behavior
No Processes Running
Processes: and_test - behavior
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Simulate Behavioral Model
Start Design Files
and_rtl.vhd
Design Summary (Synthesized)
and_test.vhd
Warnings
Find in Files Results
Ln 89 Col 21 VHDL

Step 33: The *output waveform* for the given test cases is displayed.



```
ISim P.20131013 (signature 0xfbc00daa)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

Press ctrl+home to view the first input test cases and the corresponding output and then use the left and right arrow keys to navigate to the next or previous input.



```
ISim P.20131013 (signature 0xfbc00daa)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```