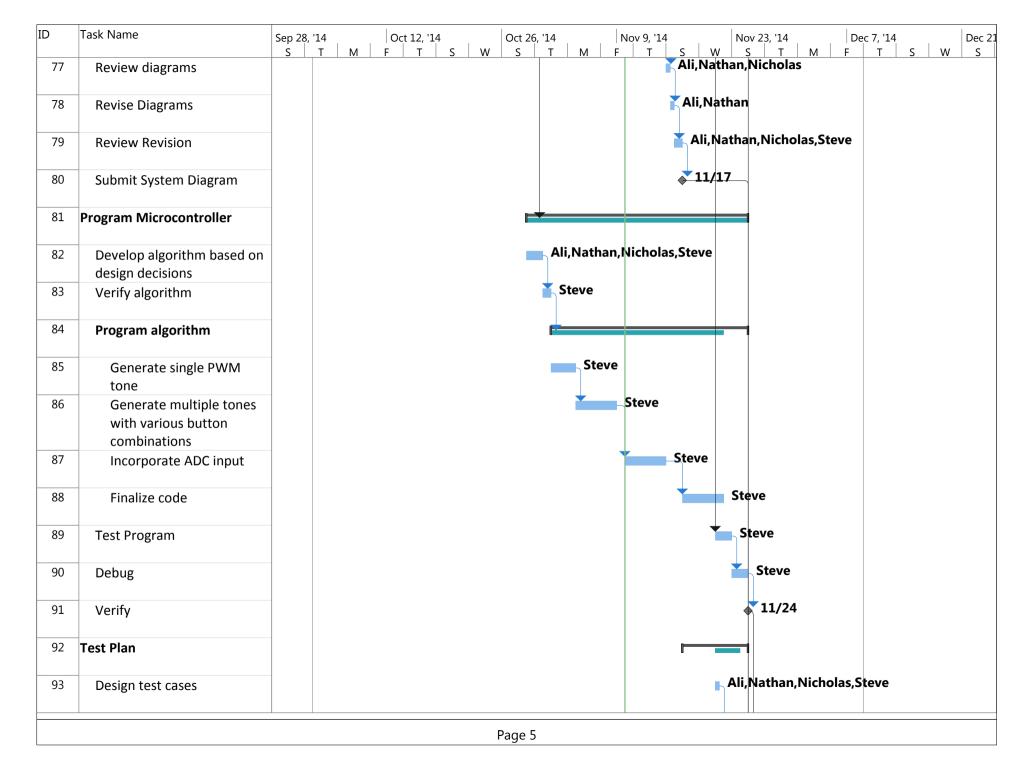


ID	Task Name	Sep 28	3, '14 T	M	Oc F	t 12, '1 T	L4 S	W		t 26, '	'14 T	М	N F	lov 9, '	14 S	W	Nov 2	23, '14 T	М	[F	Dec 7, '1	4 S	W	Dec 22
43	Arrange board in Eagle	3		IV	<u> </u>	<u> </u>	3	_ VV	3			Niche	ola		3	VV		<u> </u>	IVI	F	1	3	VV	3
44	Route the board											Nich	ola	as										
45	Check for errors											Nicl	ho	as										
46	Review board											Nat	hai	n										
47	Review Revision											Nic	cho	las										
48	Submit layout											1	L 1/ !	5										
49	Prototype Board													1										
50	Arrange single sided prototype board												λli,I	Nich	olas									
51	Route prototype board												Nic	hola	s									
52	Check for errors												Ni	chola	ıs									
53	Revise for errors											K	Ni	chola	as									
54	Review Revision											F	Ali	i,Nat	han,N	ichola	as							
55	Generate gerber files												N	ichol	as									
56	Print board and assemble											ì		Ali,N	ichola	s,Moı	ney,P0	СВ М	achir	e,boa	ard ma	terial	,Circı	uit con
57	Begin using prototype board											\rightarrow	11	/7										
58	Project Schedule													٦										
59	Determine necessary milestones												Ali	i,Nat	han									
									Pag	e 3														

D	Task Name	Sep 28	8, '14 T	М	ct 12, '	14 S	W	Oct 20	5, '14 T	М	r F	Nov 9	9, '14 T	s	W	No	v 23, '1		м	De F	c 7, '14 T	S	W	Dec 2
60	Evaluate and set deadlines	3		IVI	 1		VV			IVI	A	li,N	lath	an,Ni	icho	las,S	steve		IVI	Г	I	_ 3	VV	_ 3
61	Create project schedule											Ali												
62	Review Project Schedule										5	Ali,	Nat	han										
63	Revise Schedule											Ali	i											
64	Review Revision										ì	Al	li,Na	than										
65	Submit schedule										<	1	1/10	0										
66	Send PCB files to vendor																							
67	Add final amp to board										Nat	han	1											
68	Complete Final Schmatic										N	ath	nan,l	Nicho	olas									
69	Complete Final Layout											Nat	than	,Nich	nola	s								
70	Peer review layout											Cla	ass p	eers										
71	Generate gerber files										Ì	Ni	chol	las,Na	atha	ın								
72	Send CAM files to OSH Park											—	11/:	10										
73	System Diagram											-												
74	Draw Level 0 block diagram													Natha	an,N	licho	olas							
75	Draw Level 1 block diagram												4	Ali,N	lichc	olas,	Natha	an						
76	Draw Level 0 block diagrams for each Level 1 subcomponent	_											F	Natl	han,	Nicl	olas,	Ali						
			· ·					Page 4	<u> </u>						'									



ID	Task Name	Sep 28, '14 Oct 12, '14 Oct 26, '14 Nov 9, '14 Nov 23, '14 Dec 7, '14 Dec 7 S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M F T S W S T M S T
94	Implement cases into test	Ali, Nathan, Nicholas, Steve
	plan	
95	Submit test plan	11/24
96	Build Housing	in l
97	Design Housing	Ali, Nathan, Nicholas
98	Laser cut or 3D print design	Ali, Nathan, Nicholas
99	Working Prototype	
100	Assemble PCB	
101	Solder parts to board	Ali, Nicholas
102	Check connections	Ali,Nicholas
103	Debug	Ali,Nathan,Nicholas
104	Verify	11/26
105	Confirm board functionality	Ali, Nathan, Nicholas, Steve
106	Make adjustments/debug	Ali, Nathan, Nicholas, Steve
107	Verify	11/29
108	Assemble parts	Ali,Nathan,Nicholas,Steve
109	Test Prototype using test plan	Ali, Nathan, Nicholas, Steve
110	Debug	Ali, Nathan, Nicholas, Steve

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ID	Task Name	Sep 28,	, '14 Oct 12, '14 T M F T	4 Oct 26, '14 S W S T N	Nov 9, '14 M	Nov 23, '14 D S T M F	ec 7, '14 Dec 21
111	Verify	3	1 1 1 1 1		VI I I I S VV		12/7
112	Demo					*	12/8
				Page 7			