1 Radiation hardness of nanoscale CMOS technologies

Contents

In the Microelectronics field, the rapid evolution of technological scaling has allowed for an uninterrupted increase in the performance and complexity of analog and digital integrated circuits. The very high integration density allows CMOS technology to have a very large diffusion in analog and digital circuits in different fields, including detectors signal processing. Nevertheless, due to this uninterrupted evolution, continuous analysis is needed to evaluate static and noise characteristics, in order to classify pros and cons of the technology in study.

Thanks to the *technology scaling* phenomenon, a reduced channel length L and a

thinner gate oxide t_{ox} are obtained. It is possible to take advantage of these properties in applications where rad-hard integrated CMOS circuits (IC) are required, such as in High Energy Physics (HEP), space radiation detectors and medical imaging detectors. Nowadays several HEP experiments such as ALICE, CMS and ATLAS have their frontend electronics designed in 250 nm technology and their upgrades are going to be designed in more scaled process. As an example, in next generation detectors, such as CMS phase 2, the frontend electronics of the inner tracker will be designed entirely in a 65 nm CMOS technology in order to achieve better results in terms of spacial resolution.

The aim of this chapter is to quantify how much the investigated devices are able to withstand the ionizing radiation levels expected in experiments such as CMS at High Luminosity LHC, X-ray imaging and space radiation detectors, where electronic chips will be exposed to very high doses, from a few Mrad up to 1 Grad of Total Integrated Dose. Great attention was focused on the study of the characteristics of components in the noise voltage spectrum (white and 1/f noise) which are usually of great importance in amplifying and filtering stages, thus they were examined in depth. In addition, other fundamental parameters such as the transconductance g_m and the threshold voltage V_{Th} were evaluated as well. This work is concentrated on applications in which power dissipation is critical, therefore, in order to satisfy this requirement, MOSFETs in the analog section of the processing chain have to be biased in the low current density range (from a few µA to a few hundreds of µA).

1.1 Noise Sources

Electronic noise is the result of spontaneous fluctuations occurring in some active and passive circuit components appearing as voltage or current variations whose temporal evolution is governed by statistical laws. Noise is a time-continuous stochastic process caused by some fundamental physical phenomena, such as thermal excitation of charge carriers in conductors or the granular structure of the electric charge. Electronic noise should not be confused with enviroment interferences (i.e. power supplies fluctuation, electromagnetic induction, etc...). Such interferences, ideally, can be removed by filtering techniques and shielding, wherease stochastic noise cannot be removed because it is directly linked to the operating principles of devices and circuit components. The study of noise characteristics in electronic circuits is important because noise limits the precision of the measurement of a signal. Since noise is a purely random phenomenon, the value of its waveform cannot be predicted for any time. As a consequence, noise variables are described quantitatively by the

mean square value (or the square root of the mean square value) and, in frequency domain, by their noise spectral density.

1.1.1 Spectral Power Density

The mean square value is associated with the concept of spectral power density that is valid under the hypothesis of *stationarity* and *ergodicity*:

- *Stationarity*: a process is stationary when its statistical properties (mean value, average quadratic value, etc ...) are invariant over time.

- *Ergodicity*: a stochastic process is called ergodic when the output waveform can be considered representative of the system.

Supposing that the noise is represented by a function $x(t)$ (see Figure 1.1) and considering that $x(t)$ in the range $[-T, T]$ can be represented by the following expression:

$$\begin{cases} x_T(t) = x(t) & \text{for } t < |T| \\ x_T(t) = 0 & \text{for } t > |T| \end{cases} \tag{1.1}$$

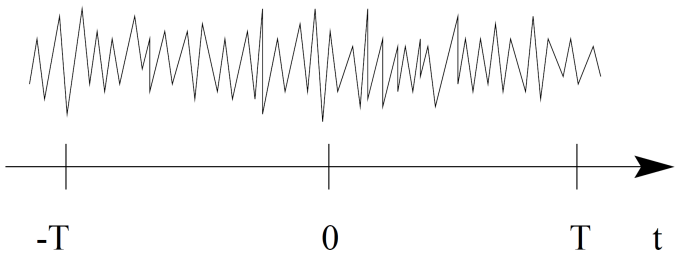


Figure 1.1: Noise waveform.

the mean square value of the limited $x(t)$ is:

$$\overline{x_T^2(t)} = \frac{1}{2T} \int_{-T}^{T} x_T^2(t) dt \tag{1.2}$$

and expressing it as its inverse Fourier transform it is possible to obtain:

$$\begin{aligned}\overline{x_T^2(t)} &= \frac{1}{2T}\int_{-T}^{T} x_T \frac{1}{2\pi}\int_{-\infty}^{\infty} V_T(\omega)e^{j\omega t}d\omega dt \\ &= \frac{1}{2T}\int_{-\infty}^{\infty} V_T(\omega)\frac{1}{2\pi}\int_{-T}^{T} x_T e^{j\omega t}dtd\omega \\ &= \int_{-\infty}^{\infty}\frac{V_T(\omega)^2}{2T}df \end{aligned} \tag{1.3}$$

where:

$$V_T(\omega) = \int_{-T}^{+T} x_T(t)e^{-j\omega t}df \tag{1.4}$$

and due to the fact that $x_T(t)$ is real: $V_T(-\omega) = V_T^*(\omega)$. For $T \to \infty$ it is possible obtain the mean square value of $x(t)$:

$$\overline{x_T^2(t)} = \int_{-\infty}^{\infty}\lim_{T\to+\infty}\frac{V_T(\omega)^2}{2T}df \tag{1.5}$$

Spectral Power Denisty of noise variable *x(t)* is the limit within the integral:

$$\frac{\overline{dx^2}}{df} = \lim_{T\to+\infty}\frac{V_T(\omega)^2}{2T} = S_x(\omega) \tag{1.6}$$

thus, knowing the power spectral density, the mean square value is:

$$\overline{x_T^2(t)} = \int_{-\infty}^{\infty} S_x(\omega)df \tag{1.7}$$

that represents the bilateral spectral density. In the following the unilateral spectral density is used.

1.1.2 Shot Noise

Shot noise is present in all devices when a relatively small number of charges have to cross a potential barrier. Shot noise can be represented by a current source whose power spectral density is:

$$\frac{\overline{di^2}}{df} = 2qI \tag{1.8}$$

where I is the device average current and q is the electron charge ($q = 1.6 \cdot 10^{-19}C$).

1.1.3 Thermal Noise

Random thermal electrons motion is the cause of *Thermal Noise*. It is independent of the presence of a direct current, whereas it depends on the temperature. Resistor thermal noise can be represented by a voltage source, according to the equivalent Thévénin circuit, with a power spectral density of:

$$\frac{\overline{de_R^2}}{df} = 4k_BTR \tag{1.9}$$

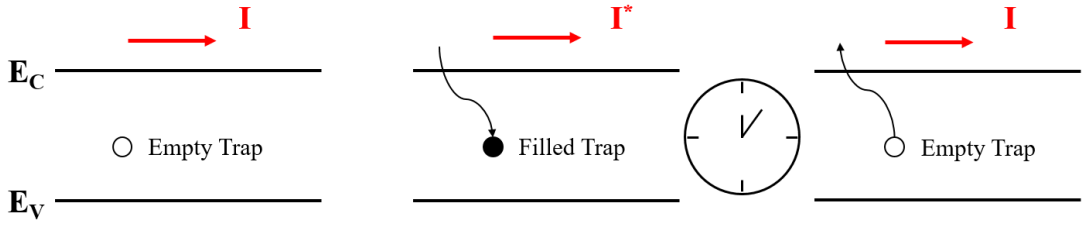
where k_B is the Boltzmann's constant ($k_B = 1.38 \cdot 10^{-23} J/K$) and T is the temperature. In alternative it can be represented by Norton equivalent circuit, with a current source with a noise spectrum density of:

$$\frac{\overline{di_R^2}}{df} = \frac{4K_BT}{R} \tag{1.10}$$

1.1.4 Flicker Noise

Flicker Noise is present in all active components and some discrete passive components such as carbon resistors. Flicker noise in the current of a semiconductor device is characterized by a power spectral density that is inversely proportional to frequency and for this reason is also known as "1/f noise". Such behaviour can be explained considering that there are a certain amount of donor/acceptor impurity atoms in the semiconductor whose energy level is more or less localized in the band gap. Although the trapping and emission process associated with these defects has little effect on static current behavior, noise is affected in the low frequency region. As one can see in Figure 1.2, a trapped charge will be released in an average time τ that depends on both the nature and the position of the trap. In Figure 1.2 I indicates the ideal channel current, if no trap are activated during the passage of the charges, q is the elementary charge, N_{TOT} is the total number of charge carriers, V_{BIAS} is the voltage bias, L is the channel length and I^* is the channel current if one trap is activated during the passage of the charge carriers. For a time τ, the current is varied by $\Delta I = {}^{I}/_{N_{TOT}}$. For frequency signals greater than $1/\tau$, no differences are noticeable, since the trap is always full or empty throughout the evolution of the signal. For signal frequencies lesser than $1/\tau$, effects are not negligible, in fact, the trap may act during the evolution of the signal.

As already mentioned each time the charge is trapped, the average stay time is τ. It is possible to modelize the phenomena as if a low frequency trapping filter handles the process. As a consequence, the noise voltage spectrum is expected to



$$I = qN_{TOT}\mu\frac{V_{BIAS}}{L^2} \qquad I^* = q(N_{TOT}-1)\mu\frac{V_{BIAS}}{L^2} \qquad I = qN_{TOT}\mu\frac{V_{BIAS}}{L^2}$$

Figure 1.2: Schematic of current fluctuations due to the trapping of charges.

be somewhat proportional to the square of such low pass filter transfer function $1/(1+(\omega\tau)^2)$. As a matter of fact, that is what one can observe. In particular, since all the impurity atoms should not be of the same species, τ will change both from one atom to another and with the temperature. The resulting noise is due to the overlapping of all these effects. The higher the number of impurities, the more the slope of the resulting noise becomes similar to 1/f (see Fig. 1.3).

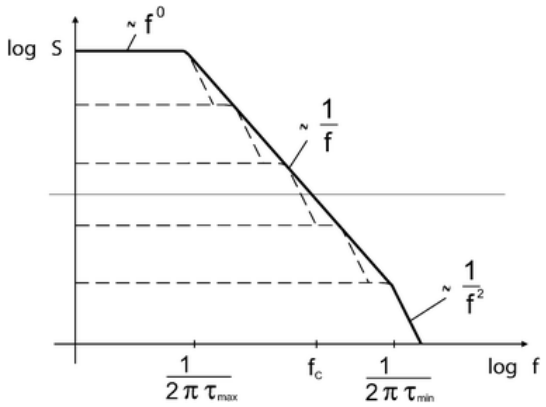


Figure 1.3: Schematic of current fluctuations due to the trapping of charges.

This situation is almost always verified for the traps present in the silicon dioxide, since in these cases τ depends also on the distance traveled by charged carriers in the oxide itself and a continuous distribution of values is assumed. Flicker noise is always associated with a current flux and has the following spectral density:

$$\frac{\overline{di_R^2}}{df} = k_1\frac{I^a}{f^b} \tag{1.11}$$

where I is the direct current, k_1 is a constant depending on the technology and dimensions of the device, a is a constant in the range $[0.5, 2]$ and b is a constant

approximately equal to 1. Flicker noise is different from other noise sources because it is not expressed by well-known physics constants like resistors or currents. k_1 is a not-known a-priori term and it may vary by several orders of magnitude from one technology to another and with different dimensions of the devices. For this reason, it is necessary to measure the power spectral density of the flicker noise.

1.1.5 MOSFET

The gate referred noise voltage spectrum of a MOSFET device $S_e^2(f)$ can be modeled by means of the following equation:

$$S_e^2(f) = S_W^2 + S_{1/f}^2(f) \tag{1.12}$$

The two terms of such equation will be discussed in what follows.

Channel Thermal Noise

The first term in (1.12) is determined by channel thermal noise and noise contributions from parasitic resistances (gate, bulk and source/drain resistance), which also exhibit thermal noise [1]. In the low current density operating region, the white noise voltage spectrum S_W^2 is dominated by channel thermal noise and can be expressed by means of the following equation:

$$S_W^2 = 4k_B T \alpha_W \frac{n\gamma}{g_m} \tag{1.13}$$

where T is the absolute temperature, $\alpha_W \geq 1$ is an excess noise factor, n is a coefficient proportional to the inverse of the subthreshold slope of I_D as a function of V_{GS} and γ is a coefficient ranging from 1/2 in weak inversion to 2/3 in strong inversion.

This coefficient can be calculated according to the following relationship for each I_D value:

$$\gamma = \frac{1}{1 + \frac{I_D L}{I_Z^* W}} \left[\frac{1}{2} + \frac{2}{3} \frac{I_D L}{I_Z^* W} \right]. \tag{1.14}$$

In equation (1.14) I_Z^* is a characteristic normalized drain current:

$$I_Z^* = 2\mu C_{OX} n V_T^2 \tag{1.15}$$

where μ is the channel mobility, C_{OX} is the effective gate capacitance per unit area and $V_T{=}k_B T/q$ is the thermal voltage. The thermal noise in the channel current

can also be expressed in terms of an equivalent resistance:

$$R_{eq} = \frac{S_W^2}{4k_BT} = \alpha_W \frac{n\gamma}{g_m} \tag{1.16}$$

Flicker Noise

The second term in (1.12) is determined by flicker noise and is characterized by a power spectral density that is inversely proportional to frequency. It can be modelized by the following relationship:

$$S_{1/f}^2(f) = \frac{K_f}{C_{OX}WL} \frac{1}{f^{\alpha_f}} \tag{1.17}$$

where K_f is an intrinsic process parameter, C_{OX} is the effective gate capacitance per unit area and the exponent α_f determines the slope of this low frequency noise term [1].

1.2 Radiation Effects on MOSFETs

The study of radiation effects on MOSFETs is very important because it provides essential informations to IC analog designers where rad-hard CMOS integrated circuits (IC) are required, such as in space, imaging and high energy physics detector applications. Interaction of radiation with matter can lead to three different types of effects:

- **Ionization (Total Ionizing Dose, TID)**: damage due to the increase of the trapped charge in SiO_2 structures. It occurs when the energy deposited by the passage of ionizing radiation creates electron-hole pairs within the oxide: holes are trapped inside the oxide region, because of their very low mobility, whereas electrons are swept away. Such phenomenon causes an increasing concentration of positive charge. This type of effect is mainly due to exposure to X-rays, γ-rays and most charged particles, however the effects depend mainly on the amount of energy deposited and not by the particular type of source.

- **Bulk Damage or Displacement**: it occurs when incident particles, along their trajectory inside the device, strike and bounce a silicon atom from the crystalline lattice of the substrate, altering its electrical properties. Displacement damage is caused especially by protons, neutrons and heavy ions.

- **Single Event Effects**: caused by the deposition of a large amount of charge, induced by the passage of a single highly ionizing particle (generally a heavy

ion) through an integrated circuit, causing the immediate malfunctioning of one or more transistors.

Bulk damage and *single event effects* have limited effects in CMOS analog circuits. For this reason, this thesis is focused on *Total Ionizing Dose* (TID) effects in view of the design of analog front-end circuits for silicon detectors.

1.2.1 Ionization Damage

An ionizing particle passing through the structure of a MOSFET deposits a certain amount of energy both in silicon and in silicon dioxide, ionizing the two materials and leaving along its path a column of electron-hole pairs, proportional to the energy released. A fraction of the pairs can recombine immediately after being generated, whereas the rest, due to the effect of the electric field of bias applied to the transistor, are separated before recombination and consequently start drifting. While the charges cross the silicon oxide layer between the gate and the substrate, the electrons maintain a high mobility, typically around $20\,\mathrm{cm^2V^{-1}s^{-1}}$, whereas the holes move slower, with a mobility from 5 to 12 orders of magnitude less than the one of the electrons. Once the holes are carried to a few nanometers from the Si/SiO_2 junction, they are highly likely to occupy the many trap states present in the region, created by imperfections in the reticular structure generated during silicon oxidation. As a result, a growing concentration of positive net charge close to the conductive channel of the MOSFET is created, which interferes with the behavior of the device. In modern CMOS technologies, the thickness of gate oxide is reduced to a few nanometers, so that the effects of trapped holes in the oxide have become almost negligible because holes are quickly removed by direct tunneling. On the contrary, external oxides have retained, in comparison, remarkable thicknesses, from 100 nm to 1 µm, and therefore have the potential to become areas of high accumulation of positive charge. Therefore, holes trapped in **shallow trench isolation (STI)** oxides became much more important. The basic structure of the MOSFET is generally surrounded by an area of silicon dioxide, which has the function of electrically isolating it from other components present in the same chip [2]. External insulation oxides undergo the same trapping phenomenon as for gate oxide with a radiation-induced progressive charge buildup as shown in Figure 1.4. If this occurs in an NMOS, the amount of positive charge in the insulating oxides can become large enough to attract a large number of electrons in the substrate and create a conductive channel linking the source and drain by circumventing the primary transistor, as highlighted in Figure 1.5. The new system formed by source, external channel and drain takes the name

of a *lateral parasitic transistor*, as it leads to the increase in the volume of the charge conduction area, and thus to a general increase in current. These parasitic effects are mainly visible through an increase in the current at $V_{GS} \approx 0\,\mathrm{V}$ (a.k.a *leakage current*), because for $V_{GS} \leq V_{th}$ the main transistor does not transmit significant current, whereas the external channels, which are kept energized by the deposited charge, allow conduction.

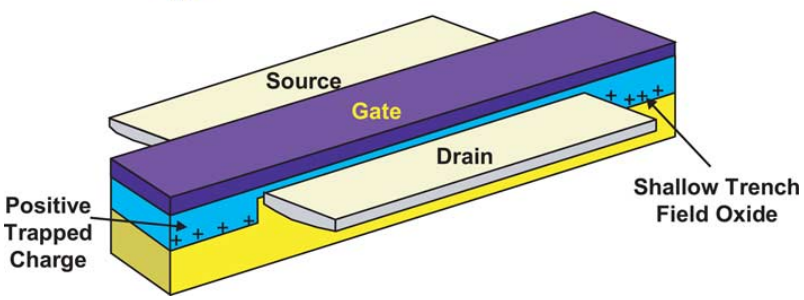


Figure 1.4: Trapped holes in STI regions.

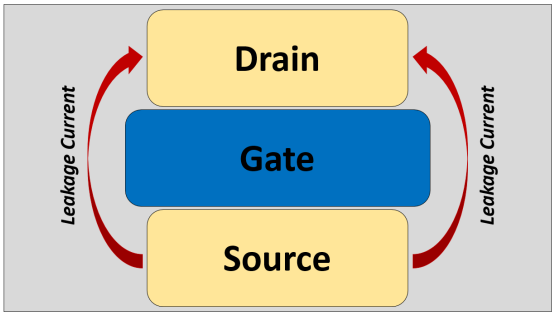


Figure 1.5: Leakage current possible paths.

Another important effect of ionizing radiation is the variation of the threshold voltage. As already mentioned, if a MOSFET is exposed to ionizing radiation its threshold voltage undergoes an alteration due to the parasitic charges accumulated within the gate oxide and the interface. In the case of NMOS this positive charge attracts the electrons that form the channel. Such effect is added to that of the positive voltage applied to the gate, so that the channel will be opened at a gate voltage less than would have been required under normal conditions. In the case of PMOS, in order to attract the holes that form the conductive channel the gate voltage must be negative. The presence of the positive charge in the oxide rejects these holes. It is therefore necessary that the voltage applied to the gate is smaller than the initial one, in order to balance the repulsive effect. As a result, in both cases the charges in the oxide reduce the threshold voltage.

Another non-negligible effect appearing at high dose, i.e. greater than 100 Mrad, is the fact that negative are trapped in the interface states at STI oxides. In case of PMOS devices this effect is in addiction to the trend given by the oxide-trapped charge, whereas for NOMS devices effects of inteface states can compensate oxide-trapped positive charge and even become dominant.

1.3 Experimental Details

1.3.1 Investigated devices

The MOSFETs studied in this work are standard threshold voltage (SVT) devices belonging to a 110 nm CMOS process and to a Low Power (LP) 65 nm CMOS process.

For 110 nm technology, the maximum allowed supply voltages V_{DD} is 1.4 V for core devices and 2.5 V for I/O devices with thicker gate oxide. The electrical oxide thickness t_{ox} is 3 nm for NMOS and 3.2 nm for PMOS which corresponds to a gate capacitance per unit area C_{ox} of about 10.8 fF/µm^2 for NMOS and 11.5 fF/µm^2 for PMOS. For 110 nm CMOS technology three types of devices are available for measurements:

- **Core devices with open layout:** the MOSFETs are laid out using a standard open structure, interdigitated configuration, with gate finger width of $W_f = 20$ µm, with the exception of the NMOS with $W/L = 600/0.12$ which is available also with $W_f = 10$ µm and 40 µm.
- **Core devices with enclosed layout:** NMOS devices are designed with an enclosed layout (ELT). Ten parallel devices are used for each geometry.
- **I/O devices with open layout:** these MOSFETs have a thicker gate oxide which allows for a maximum supply voltage $V_{DD} = 2.5$ V. Devices are laid out using a standard open structure, interdigitated configuration, with gate finger width of 30 µm.

Devices with enclosed geometry (edgeless layout transistor or ELT) are characterized by having a ring structure instead of a linear structure for the gate terminal. Such geometry in principle should not exhibit any radiation induced leakage current [3]. Gate dimensions (channel width W and length L) of 110 nm technology devices available for measurements are shown in Table 1.1. As shown in the Table 1.1, for some geometries, I/O devices with a gate oxide t_{OX} of 5.6 nm for NMOS and 5.9 nm for PMOS (thick gate oxide), and a deep N-well NMOS (DNW) are also available.

		Core Open		Core ELT		I/O Open	
W[µm]	L[µm]	N	P	N	P	N	P
100	0.12	∗	∗				
	0.24	∗	∗				
	0.36	∗	∗				
	0.72	∗	∗				
200	0.12	∗	∗	∗			
	0.24	∗	∗	∗			
	0.36	∗	∗				
	0.72	∗	∗				
600	0.12	∗	∗	∗			
	0.24	∗	∗	∗			
	0.34					∗	
	0.36	∗	∗				
	0.37						∗
	0.72	∗	∗	∗			

Table 1.1: 110 nm technology: gate geometries of the available N-channel and P-channel devices. Option availability is indicated with ∗ symbol.

For what concernes 65 nm technology, the maximum allowed supply voltage V_{DD} is 1.2 V. The electrical oxide thickness t_{ox} is 2.6 nm for NMOS and 2.8 nm for PMOS which corresponds to a gate capacitance per unit area C_{ox} of about 13 fF/µm^2 for NMOS and 12 fF/µm^2 for PMOS. Devices available for measurements are MOSFETs laid out using a standard open structure, interdigitated configuration MOSFETs designed with an enclosed layout (ELT). Gate dimensions (channel width W and length L) of devices available for measurements are shown in Table 1.2: the same geometries are available for both device polarity.

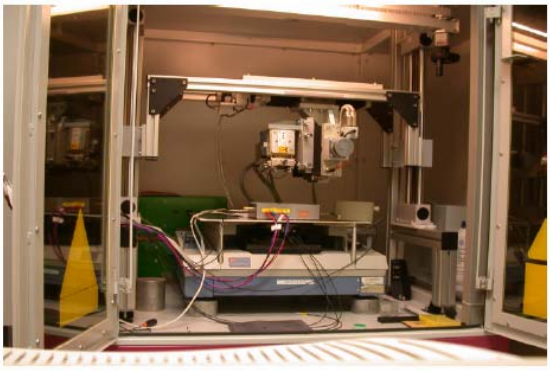
1.3.2 Irradiation Procedures

110 nm CMOS devices were irradiated at CERN facility, whereas 65 nm CMOS devices were irradiated at Laboratori di Legnaro, INFN. In all irradiations, the machine used is of the type Seifert model RP149 [4], Figure 1.6a, capable of supplying a maximum voltage of 50 kV and a maximum current of §50mA. It is equipped with electronic control of the X-Y position of the radiogenic tube, the power and intensity of the beam. The distance from the source to the target can be adjusted manually. The spectrum radiation, Figure 1.6b, of the tungsten anode consists of

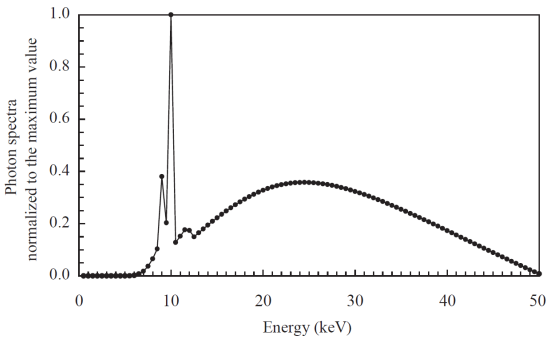
W[µm]	L[µm]	Note
0.12	0.065	
0.24	0.065	
	0.065	ELT
	0.50	
0.48	0.065	
1	0.065	
100	0.13	
	0.35	
200	0.065	
	0.13	
	0.35	
	0.50	
	0.70	
600	0.065	
	0.13	
	0.35	
	0.35	50 f
	0.35	120 f
	0.50	
	0.70	

Table 1.2: 65 nm technology: available gate geometries of channel N and P devices.

level L characteristic peaks, around 10 keV, and of the Bremsstrahlung component. The lower spectrum components are filtered by an aluminum foil of 150 µm. To change the dose rate, measured by a silicon diode, it is possible to act on the source power supply, or on the sample distance from the tube.



(a) X-ray radiation source.



(b) Normalized tungsten spectrum.

Figure 1.6: Irradiation setup and source spectrum.

The devices were irradiated with a dose rate of 9 krad(SiO_2)/s up to a total ionizing dose (TID) of 200 Mrad-600 Mrad and 5 Mrad (SiO_2) for 65 nm and 110 nm

technology respectively. The choice of the dose rate was dictated by the fact that a very high total dose had to be reached in a reasonable short time. During the irradiations, MOS devices were biased in the so called worst-case configuration (as reported in [5]). All terminals were connected to ground, except in the case of NMOS devices, where the gate was connected to the maximum bias voltage allowed by the technology. In such configuration, the transport of radiation-generated holes towards the Si-SiO_2 interface is maximized.

1.3.3 Measurements Setup

Measurements of static and signal parameters were carried out with an Agilent E5270B Precision Measurement Mainframe with E5281B SMU Modules. For Core and ELT devices the following measurements have been performed to study the static behavior:

- I_D-V_{GS} characteristics
  - V_{GS} from $-0.3\,\mathrm{V}$ to V_{DD} with $5\,\mathrm{mV}$ step
  - V_{DS} from $0\,\mathrm{V}$ to V_{DD} with $0.2\,\mathrm{V}$ step + $V_{DS} = 10\,\mathrm{mV}$
- I_D-V_{DS} characteristics
  - V_{DS} from $0\,\mathrm{V}$ to V_{DD} with $5\,\mathrm{mV}$ step
  - V_{GS} from $0\,\mathrm{V}$ to V_{DD} with $0.2\,\mathrm{V}$ step

For I/O devices measurements have been extended to a maximum supply voltage of $V_{DD} = 2.5\,\mathrm{V}$.

The value of the transconductance g_m was extracted from I_D-V_{GS} curves and its behavior has been studied as a function of the gate-to-source voltage V_{GS} and of the drain current I_D.

From the standpoint of ionizing radiation effects, the variation of the following static parameters is of utmost importance:

- **Threshold voltage (V_{Th}):** obtained with the quadratic extrapolation method from the $I_D - V_{GS}$ plot measured at $V_{DS} = 1.2\,\mathrm{V}$ for Core and ELT devices and at $V_{DS} = 2.5$ V for I/O devices.
- **OFF current (I_{off}):** subthreshold leakage current measured at $V_{GS} = 0$ and $V_{DS} = 1.2$ V for Core and ELT devices and at $V_{DS} = 1.2\,\mathrm{V}$ for I/O devices.
- **ON current (I_{on}):** maximum drive current measured at $V_{GS} = V_{DS} = 1.2$ V for Core and ELT devices and at $V_{GS} = V_{DS} = 2.5$ V for I/O devices.

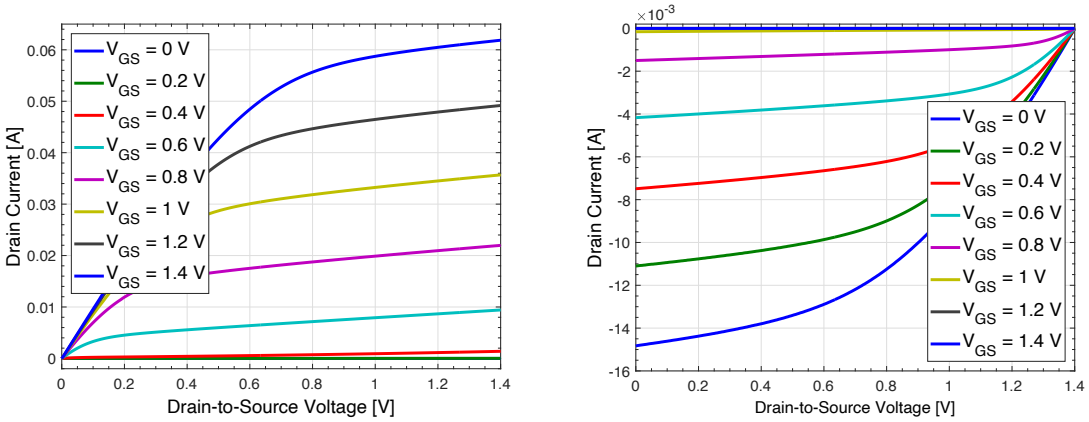
- **Maximum transconductance ($g_{m,max}$):** maximum value of the channel transconductance extracted from the $I_D - V_{GS}$ curve measured at $V_{DS} = 1.2\,\text{V}$ for Core and ELT devices and at $V_{DS} = 1.2\,\text{V}$ for I/O devices.

The spectral density of the noise in the the channel current was studied by measuring the equivalent noise voltage spectrum referred to the gate. These measurements were carried out with a Network/Spectrum Analyzer (Agilent 4395A). This instrument allows for noise measurements within the 100 Hz - 200 MHz frequency range [6]. In order to measure the noise power spectral density of a single device (or also an integrated circuit), an ad-hoc interface circuit able to amplify noise to be measured is needed. In the case of single device, such circuit has to correctly polarize the device. This circuit is called preamplifier and has been designed in order to show negligible noise component with respect to those featured by the devices under test.

1.4 Experimental Results - Static and Signal Parameters

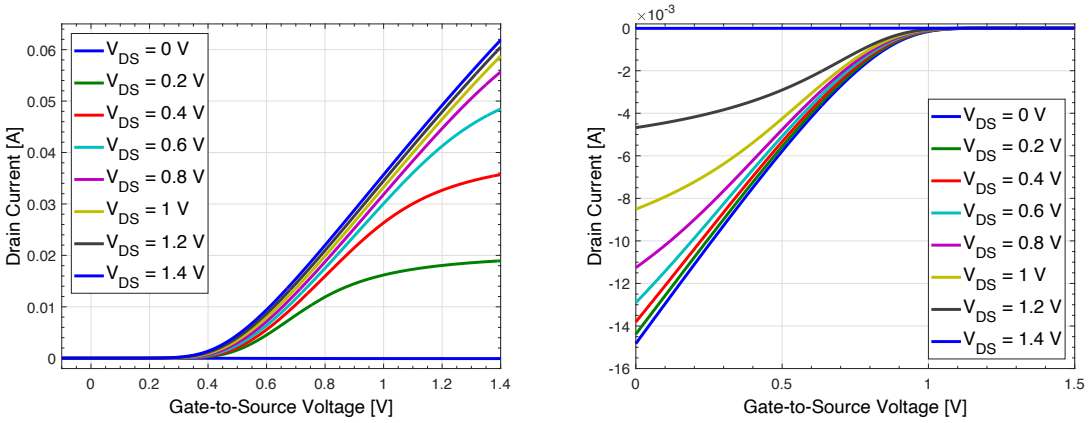
1.4.1 110 nm technology

A typical set of plots obtained from static and signal measurements of two packages (package #5 for NMOS devices and package #2 for PMOS devices) have been gathered in Fig. 1.7a, 1.7b, 1.8a, 1.8b, 1.9a and 1.9b.



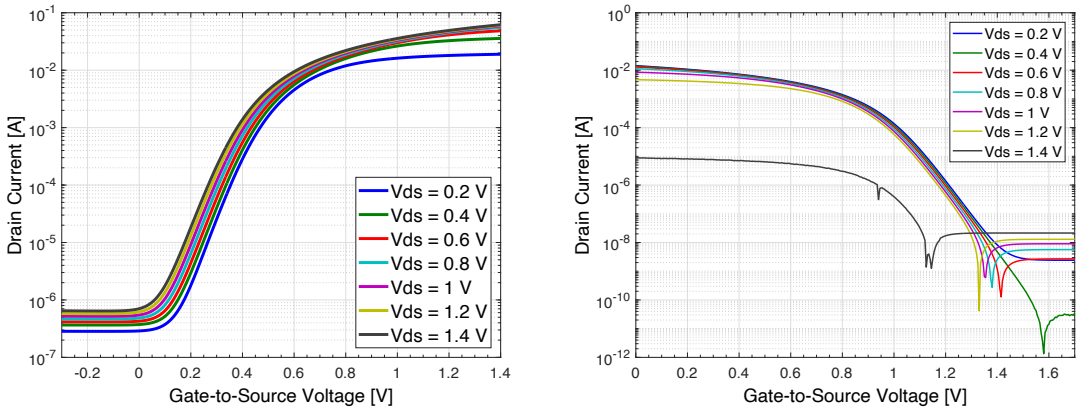
(a) N-channel $W/L = 100/0.12$. **(b)** P-channel $W/L = 100/0.12$.

Figure 1.7: Drain current I_D as a function of V_{DS} with V_{GS} as parameter.



(a) N-channel $W/L = 100/0.12$. **(b)** P-channel $W/L = 100/0.12$.

Figure 1.8: Drain current I_D as a function of V_{GS} with V_{DS} as parameter.



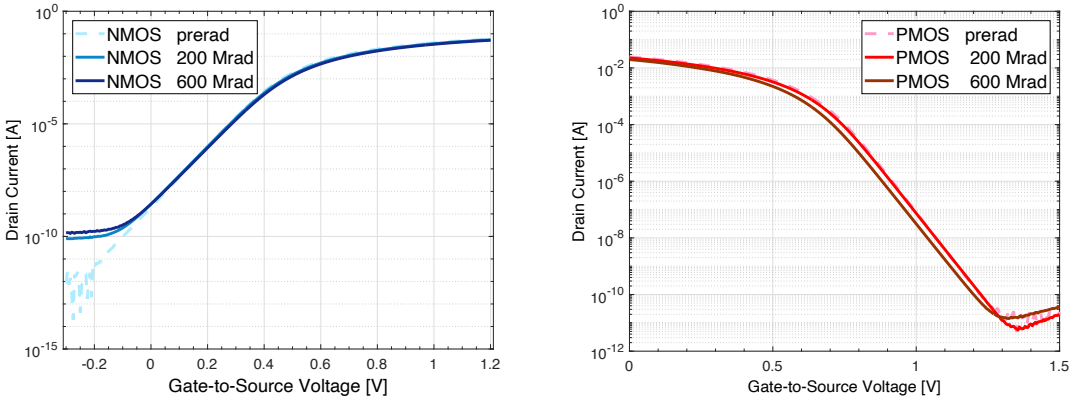
(a) N-channel $W/L = 100/0.12$. **(b)** P-channel $W/L = 100/0.12$.

Figure 1.9: I_D as a function of V_{GS} in log scale with V_{DS} as parameter.

Drain Current Characteristics

Figures 1.10a and 1.10b show the typical behaviour of the drain current as a function of gate-to-source voltage for an NMOS and a PMOS devices respectively, before and after irradiation at 5 Mrad of 110 nm technology. Little variations of the leakage current are observed. As expected such difference is more appreciable in NMOS devices than PMOS devices.

Regarding current measurements, the OFF current (I_{off}) was measured at $V_{GS} = 0\,\text{V}$ and $|V_{DS}| = 1.4\,\text{V}$ for Core and ELT devices and at $|V_{DS}| = 2.5\,\text{V}$ for devices of the I/O type before and after irradiation. It is possible to observe that there is an appreciable increase of this constant leakage current for NMOSFETs of the order of hundreds of nA, whereas for PMOS devices there is a very tiny decrease (less than 1 nA). As a matter of fact, positive charge accumulated in PMOSFETs oxides tends



(a) N-channel with $W = 200\,\mu m$ and $L = 0.12\,\mu m$.

(b) P-channel with $W = 200\,\mu m$ and $L = 0.12\,\mu m$.

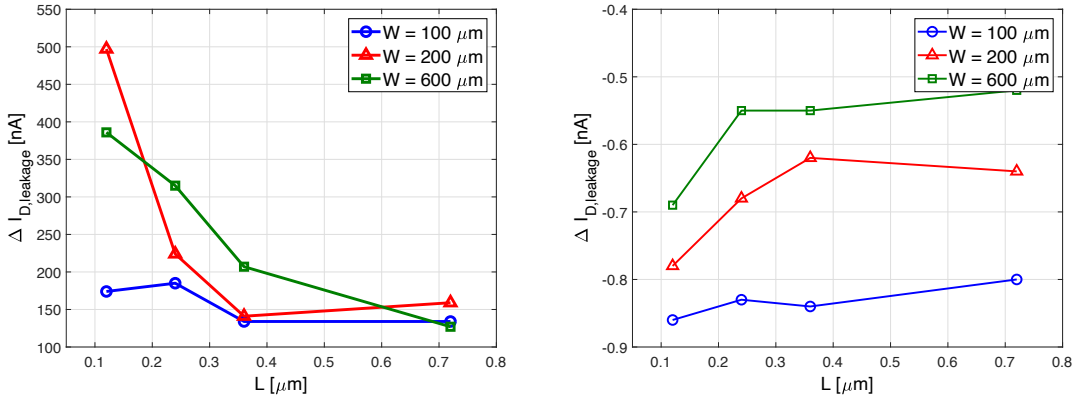
Figure 1.10: Drain current I_D with respect to V_{GS} for devices biased at $|V_{DS}| = 1.4\,V$ and $V_{BS} = 0\,V$, before and after irradiation up to 5 Mrad TID.

to switch off parasitic leakage current paths. On the contrary the increase of the NMOS leakage current is probably caused by edge effects due to radiation-induced charge at shallow trench isolation (STI) oxides [7], [8]. Table 1.3 reports all measured I_{off} of 110 nm CMOS technology devices. Figures 1.11a and 1.11b show the trend of $\Delta I_{D,leakage}$ as a function of the channel length L for different channel widths W, respectively for NMOSFETs and PMOSFETs. It is possible to observe a larger increment for shorter channel devices.

W/L	**# finger**	**NMOS I_{off} [nA]**			**PMOS I_{off} [nA]**		
		Before	**5 Mrad**	**ΔI_{off}**	**Before**	**5 Mrad**	**ΔI_{off}**
100/0.12	5	756	930	174	9.27	8.41	-0.86
100/0.24	5	752	937	185	9.38	8.55	-0.83
100/0.36	5	752	886	134	9.51	8.67	-0.84
100/0.72	5	749	883	134	9.61	8.81	-0.8
200/0.12	10	762	1259	497	9.92	9.14	-0.78
200/0.24	10	756	980	224	9.72	9.04	-0.68
200/0.36	10	758	899	141	9.9	9.28	-0.62
200/0.72	10	759	918	159	9.9	9.26	-0.64
600/0.12	30	786	1172	386	10.53	9.84	-0.69
600/0.24	30	768	1083	315	10.29	9.74	-0.55
600/0.36	30	768	975	207	10.32	9.77	-0.55
600/0.72	30	766	893	127	10.32	9.8	-0.52

Table 1.3: I_{off} measurements of all 110 nm CMOS technology.

The ON current (I_{on}) was measured at $|V_{DS}| = |V_{GS}| = 1.4\,V$ for Core and ELT devices and at $|V_{DS}| = |V_{GS}| = 2.5\,V$ for thick oxide I/O devices of 110 nm



(a) N-channel devices. **(b)** P-channel devices.

Figure 1.11: $\Delta I_{D,leakage}$ with respect to the length L for different widths W.

technology and $|V_{DS}| = |V_{GS}| = 1.2\,\text{V}$ for Core and ELT devices of 65 nm technology. This parameter was measured before and after irradiations.

Data point out that there are no significant changes due to ionizing radiation, in fact the highest increase is around 0.2% with respect to the initial I_{ON}, for Core, Enclosed Layout and thick oxide I/O.

Threshold Voltage

Threshold voltage (V_{Th}) was obtained with the quadratic extrapolation method from the $I_D - V_{GS}$ plot measured at $|V_{DS}| = 1.2\,\text{V}$ for Core and ELT devices and at $|V_{DS}| = 2.5\,\text{V}$ for thick oxide I/O devices [9].

Ionizing radiation seems to cause no appreciable effects for $|V_{GS}| \geq |V_{Th}|$ either for Core, Enclosed Layout and I/O devices. The threshold voltage shift averaged on all samples for linear and enclosed layout ΔV_{Th} is very small: $\Delta V_{Th} = -0.6\,\text{mV}$ for N-channel MOS devices and $\Delta V_{Th} = 1.9\,\text{mV}$ for P-channel MOS devices. Thick oxide I/O devices show a higher threshold voltage shift $|\Delta V_{Th}| \approx 10\,\text{mV}$. This phenomenon can be ascribed to their thicker gate oxide. Table 1.4 reports all measured threshold voltage of 110 nm technology linear core devices.

Transconductance

Transconductance g_m is an index regarding the amplifying characteristics of the MOSFET, because drain current is a function of gate to source voltage. The transconductance is defined as the derivative of I_D with respect to V_{GS}:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{1.18}$$

W/L	# finger	NMOS V_{th} [mV] Before	5 Mrad	ΔV_{th}	PMOS V_{th} [mV] Before	5 Mrad	ΔV_{th}
100/0.12	5	288.5	287.9	-0.6	327.8	329.0	1.2
100/0.24	5	337.4	337.1	-0.3	365.5	366.4	0.9
100/0.36	5	333.1	332.5	-0.6	363.8	365.7	1.9
100/0.72	5	324.8	323.5	-1.3	361.9	363.7	1.8
200/0.12	10	264.0	264.2	0.2	305.6	308.2	2.5
200/0.24	10	318.7	318.3	-0.3	352.6	354.8	2.2
200/0.36	10	314.8	314.5	-0.3	352.2	354.5	2.3
200/0.72	10	307.9	307.2	-0.6	354.3	356.5	2.1
600/0.12	30	221.4	220.6	-0.8	267.3	269.3	2.0
600/0.24	30	280.9	279.8	-1.1	324.2	326.5	2.3
600/0.36	30	279.1	278.4	-0.7	326.4	328.7	2.3
600/0.72	30	275.0	274.4	-0.6	332.8	334.2	1.4

Table 1.4: V_{th} measurements of all 110 nm CMOS technology.

The value of the transconductance g_m was extracted from $I_D - V_{GS}$ curves and its behavior has been studied as a function of the gate-to-source voltage V_{GS} and of the drain current I_D before and after irradiations. Figure 1.12 shows the transconductance g_m as a function of the drain current I_D, up to $I_D = 1\,\text{mA}$, before and after exposure to X-rays, for PMOS and NMOS devices with $W/L = 100/0.36$ biased at $|V_{DS}| = 0.6\,\text{V}$ and $V_{BS} = 0\,\text{V}$. As expected from the $I_D - V_{GS}$ curves, ionizing radiation seems to give no appreciable variations of the transconductance. All other devices (Core, ELT and I/O) show the same behaviour for all the considered drain to source voltage.

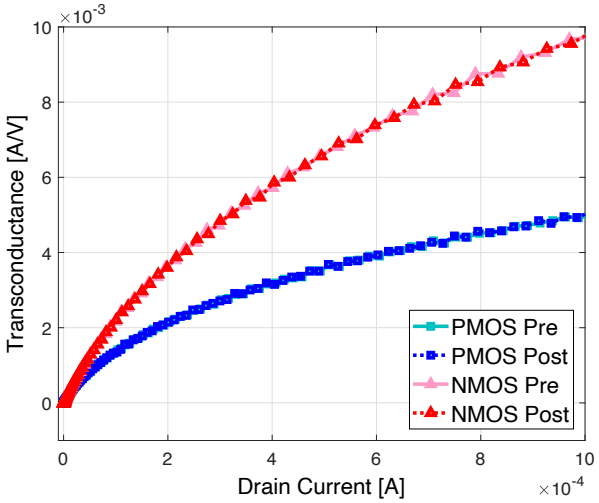
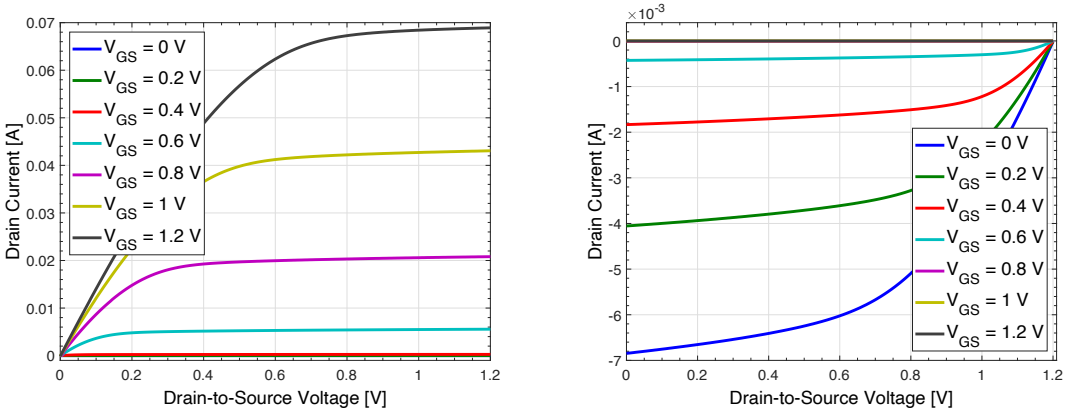


Figure 1.12: Transconductance g_m as a function of the drain current I_D, before and after irradiation up to 5 Mrad total dose, for PMOS and NMOS devices with $W/L = 100/0.36$ biased at $|V_{DS}| = 0.6\,\text{V}$ and $V_{BS} = 0\,\text{V}$.

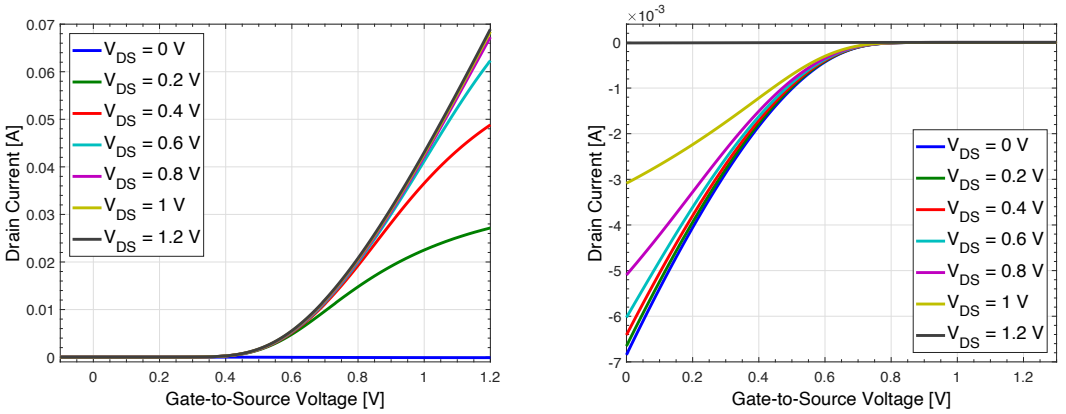
1.4.2 65 nm technology

A typical set of plots obtained from static and signal measurements of two packages (package #1 for NMOS devices and package #2 for PMOS devices) have been gathered in Fig. 1.13a, 1.13b, 1.14a, 1.14b, 1.15a, 1.15b, 1.16a and 1.16b.



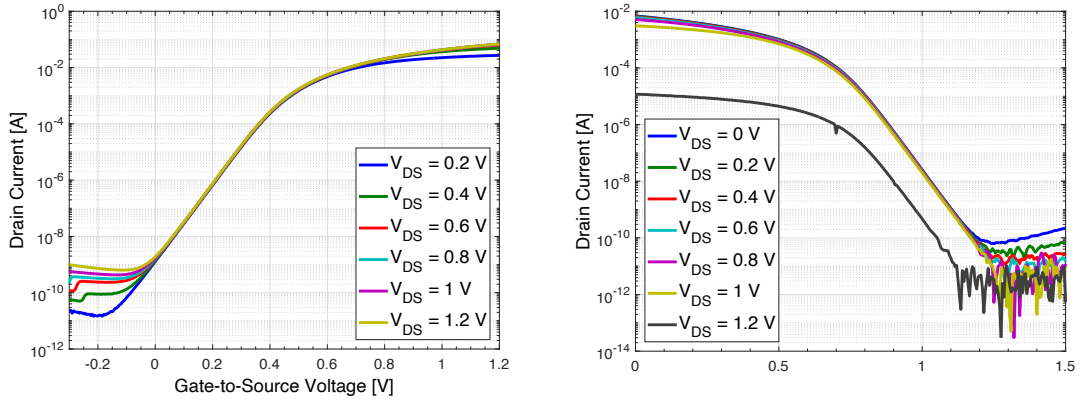
(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

Figure 1.13: Drain current I_D as a function of V_{DS} with V_{GS} as parameter.



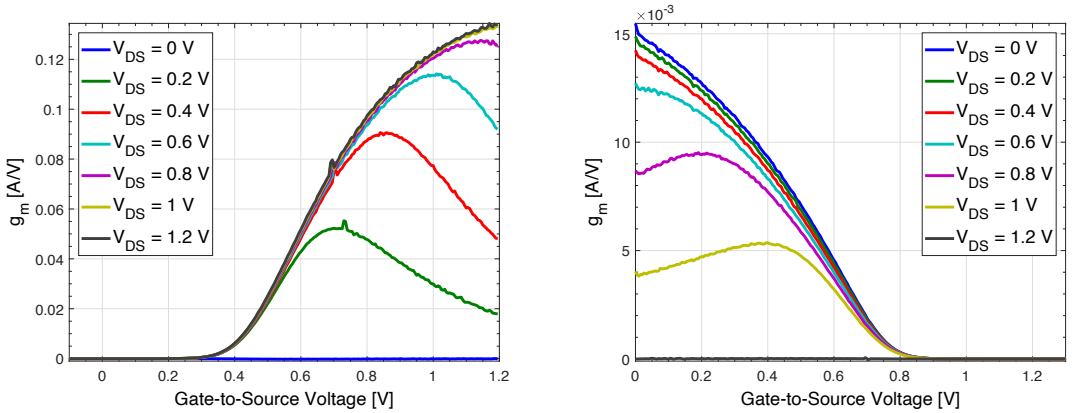
(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

Figure 1.14: Drain current I_D as a function of V_{GS} with V_{DS} as parameter.



(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

Figure 1.15: I_D as a function of V_{GS} in log scale with V_{DS} as parameter.



(a) N-channel $W/L = 600/0.50$. **(b)** P-channel $W/L = 100/0.35$.

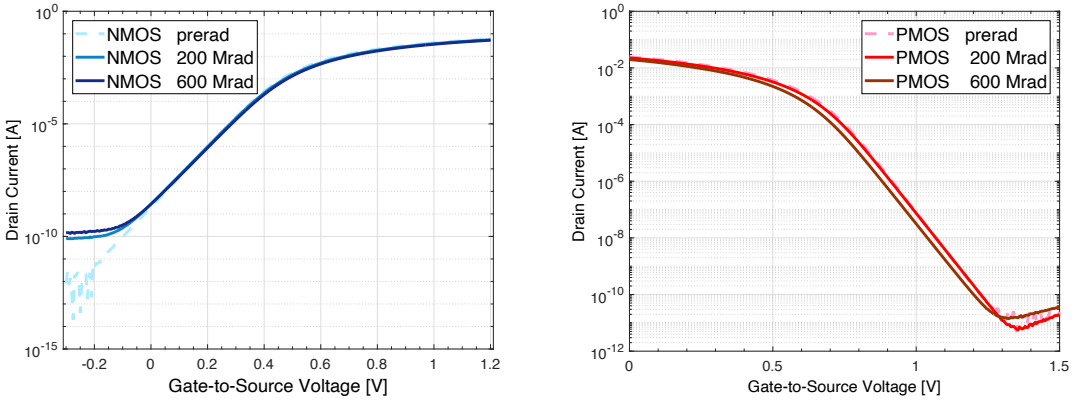
Figure 1.16: Transconductance g_m as a function of V_{GS} with V_{DS} as parameter.

Drain Current Characteristics

Figures 1.17a and 1.17b show the typical behaviour of the drain current as a function of gate-to-source voltage for an NMOS and a PMOS devices respectively, before and after irradiation at 200 Mrad and 600 Mrad.

A variation of the leakage current is observed. As predicted from the theory, such difference is more appreciable in NMOS devices.

Regarding current measurements, the OFF current (I_{off}) was measured at $V_{GS} = 0\,\text{V}$ and $|V_{DS}| = 1.2\,\text{V}$ for all devices before and after all irradiations. It is possible to observe that there is very little increase of this constant leakage current for NMOSFETs equivalent in the worst case to $\sim 30\,\text{nA}$, after both irradiations. Consinstently to 110 nm technology, for PMOS devices there is a very tiny decrease (less than 0.1 nA). Generally a higher TID for 65 nm technology devices seems to cause much smaller effects than the ones detected for 110 nm CMOS technology. Table 1.5



(a) N-channel with $W = 200\,\mu m$ and $L = 0.13\,\mu m$.

(b) P-channel with $W = 200\,\mu m$ and $L = 0.13\,\mu m$.

Figure 1.17: Drain current I_D with respect to V_{GS} for devices biased at $|V_{DS}| = 1.2\,V$ and $V_{BS} = 0\,V$, before and after irradiation up to 200 Mrad and 600 Mrad TID.

reports all measured I_{off} of 65 nm CMOS technology devices. One particular fact that can be observed from this table is that the two PMOS with $W/L = 600/0.350$ but with slightly different number of fingers show different ΔI_{off}. In particular, the 120 fingers device shows an I_{off} before irradiations and a $|\Delta I_{off}|$ higher than the 50 fingers ones. This fact can be ascribed to the larger number of external channels, due to the greater number of fingers.

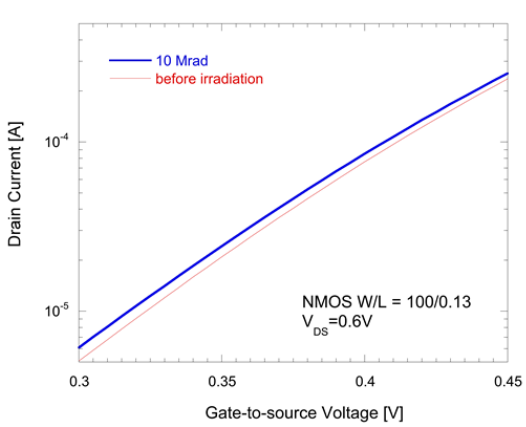
Generally, for NMOS devices, no sizable effects can be seen in devices with large W/L, except in the leakage current region. Comparing to a previous irradiation campaign [10], it is possible to see interesting effects that may be correlated with the behavior of noise in irradiated devices (see paragraph 1.5.2). In figures 1.18a and 1.18b $I_D - V_{GS}$ curves appear to shift in different directions, moving up at 10 Mrad, i.e. higher drain curretn at same V_{GS}, and then down at 200 Mrad and 600 Mrad, i.e. lower drain current at same V_{GS}.

This effect can be ascribed to the fact that at low TID, positive charge in STI oxides switches on lateral devices, increasing I_D (for the same V_{GS}). At higher doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge, switching off lateral parasitic transistors and reducing I_D (for the same V_{GS}), e.g. figure 1.19a and 1.19b shows the behaviour of NMOS with $W/L = 100/0.13$.

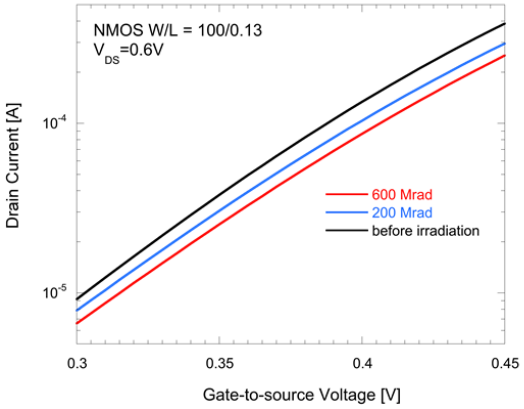
For what concernes PMOS devices, comparing results to previous irradiation tests at 5 Mrad [10], $I_D - V_{GS}$ curves appear to shift in the same direction (left) both at 5 Mrad (very slightly) and at 200 Mrad and 600 Mrad, see figure 1.20a and 1.20b. Figure 1.21 shows the drain current percentage variation of a PMOS with

W/L	NMOS I_{off} [A]			PMOS I_{off} [A]		
	Prerad	200 Mrad	600 Mrad	Prerad	200 Mrad	600 Mrad
0.12/0.065	$1.55 \cdot 10^{-10}$	$4.50 \cdot 10^{-9}$	$5.52 \cdot 10^{-9}$	-	-	-
0.24/0.065	-	-	-	$6.99 \cdot 10^{-11}$	$2.33 \cdot 10^{-9}$	$2.66 \cdot 10^{-9}$
0.24/0.065 EL	$2.02 \cdot 10^{-10}$	$4.45 \cdot 10^{-9}$	$5.42 \cdot 10^{-9}$	$5.01 \cdot 10^{-12}$	$7.89 \cdot 10^{-12}$	$2.14 \cdot 10^{-12}$
0.48/0.065	$5.78 \cdot 10^{-12}$	$2.10 \cdot 10^{-10}$	$2.57 \cdot 10^{-10}$	-	-	-
1/0.065	$3.12 \cdot 10^{-8}$	$5.5 \cdot 10^{-8}$	$3.48 \cdot 10^{-8}$	-	-	-
100/0.130	$9.17 \cdot 10^{-10}$	$1.35 \cdot 10^{-9}$	$1.32 \cdot 10^{-9}$	-	-	-
100/0.350	$2.36 \cdot 10^{-10}$	$3.52 \cdot 10^{-10}$	$3.70 \cdot 10^{-10}$	$5.31 \cdot 10^{-11}$	$3.57 \cdot 10^{-11}$	$2.32 \cdot 10^{-11}$
200/0.065	-	-	-	-	-	-
200/0.130	$1.97 \cdot 10^{-9}$	$2.74 \cdot 10^{-9}$	$2.72 \cdot 10^{-9}$	$1.96 \cdot 10^{-10}$	$2.10 \cdot 10^{-10}$	$1.01 \cdot 10^{-10}$
200/0.350	$6.46 \cdot 10^{-10}$	$4.99 \cdot 10^{-10}$	$6.03 \cdot 10^{-10}$	$9.46 \cdot 10^{-11}$	$9.25 \cdot 10^{-11}$	$5.61 \cdot 10^{-11}$
200/0.500	$1.30 \cdot 10^{-8}$	$1.89 \cdot 10^{-8}$	$2.04 \cdot 10^{-8}$	$6.46 \cdot 10^{-11}$	$7.12 \cdot 10^{-11}$	$62.56 \cdot 10^{-11}$
200/0.700	$5.30 \cdot 10^{-10}$	$4.73 \cdot 10^{-9}$	$6.00 \cdot 10^{-9}$	$5.44 \cdot 10^{-11}$	$5.28 \cdot 10^{-11}$	$2.59 \cdot 10^{-11}$
600/0.065	$1.51 \cdot 10^{-7}$	$1.80 \cdot 10^{-7}$	$1.59 \cdot 10^{-7}$	$6.02 \cdot 10^{-9}$	$4.48 \cdot 10^{-9}$	$4.58 \cdot 10^{-9}$
600/0.130	$5.94 \cdot 10^{-9}$	$8.92 \cdot 10^{-9}$	$8.63 \cdot 10^{-9}$	$5.76 \cdot 10^{-10}$	$6.39 \cdot 10^{-10}$	$4.80 \cdot 10^{-10}$
600/0.350 50 finger	-	-	-	$3.14 \cdot 10^{-10}$	$2.64 \cdot 10^{-10}$	$2.19 \cdot 10^{-10}$
600/0.350 120 finger	$1.55 \cdot 10^{-9}$	$2.37 \cdot 10^{-9}$	$2.17 \cdot 10^{-9}$	$3.48 \cdot 10^{-10}$	$2.79 \cdot 10^{-10}$	$2.35 \cdot 10^{-10}$
600/0.500	$1.36 \cdot 10^{-9}$	$1.89 \cdot 10^{-9}$	$1.89 \cdot 10^{-9}$	$2.70 \cdot 10^{-10}$	$2.17 \cdot 10^{-10}$	$1.74 \cdot 10^{-10}$
600/0.700	$1.19 \cdot 10^{-9}$	$1.70 \cdot 10^{-9}$	$1.57 \cdot 10^{-9}$	$2.13 \cdot 10^{-10}$	$1.71 \cdot 10^{-10}$	$1.55 \cdot 10^{-10}$

Table 1.5: I_{off} measurements of all 65 nm CMOS technology.

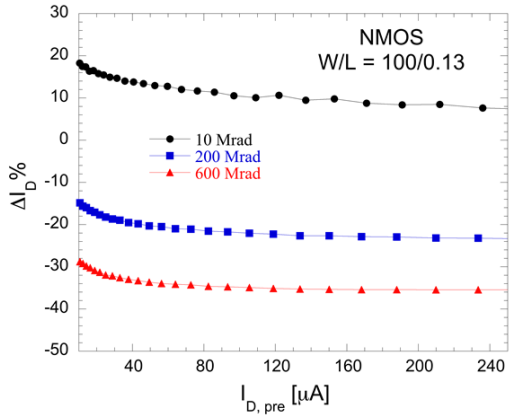


(a) Irradiation up to 10 Mrad.

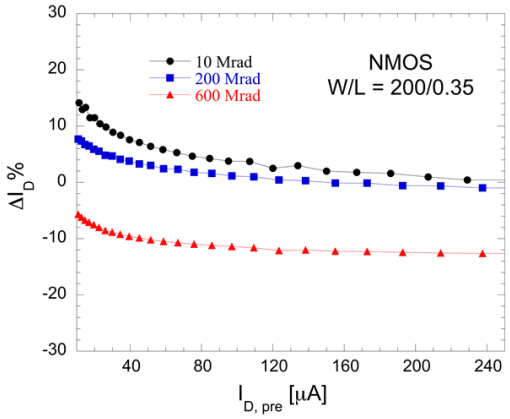


(b) Irradiation up to 200 Mrad and 600 Mrad.

Figure 1.18: Detail of I_D as a function of V_{GS} for NMOS with $W/L = 100/0.13$.



(a) NMOS with $W/L = 100/0.13$.

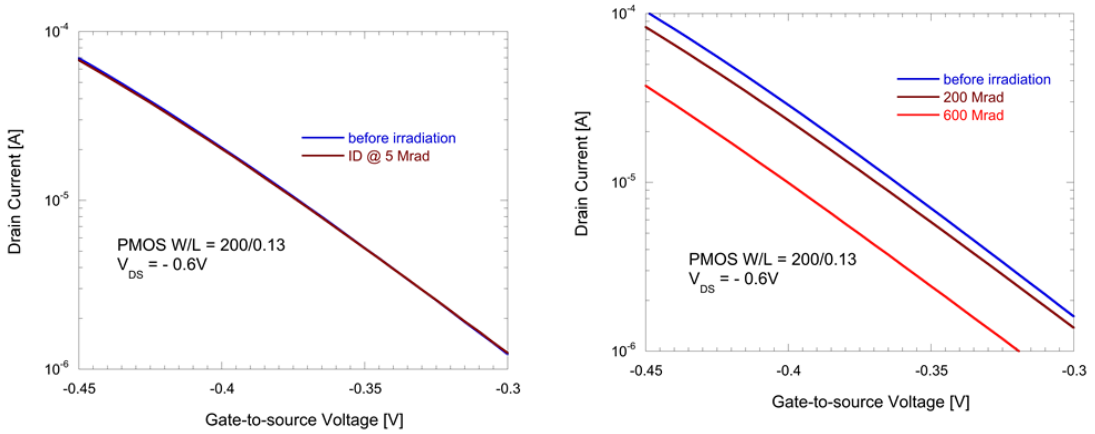


(b) NMOS with $W/L = 200/0.35$.

Figure 1.19: Detail of I_D as a function of V_{GS} for NMOS devices.

$W/L = 200/0.13$ for TID up to 600 Mrad. This behavior confirms that, unlike NMOS devices, trapped charge in the oxide region are not compensated by interface states, but they contribute in the same direction.

The ON current (I_{on}) was measured at $|V_{DS}| = |V_{GS}| = 1.2\,\text{V}$ for Core and ELT devices. This parameter was measured before and after irradiations. Table 1.6 reports averaged values of percentage variation of I_{on} current for both NMOS and PMOS with a channel width greater or lower than 1 µm. Such value was chosen because, for $W > 1\,\mu\text{m}$, I_{on} current devices seems to be less affected by ionizing radiation, i.e. the averaged decrease of I_{on} current is greater for $W \leq 1\,\mu\text{m}$ for both polarity.



(a) Irradiation up to 5 Mrad.

(b) Irradiation up to 200 Mrad and 600 Mrad.

Figure 1.20: Detail of I_D as a function of V_{GS} for PMOS with $W/L = 200/0.13$.

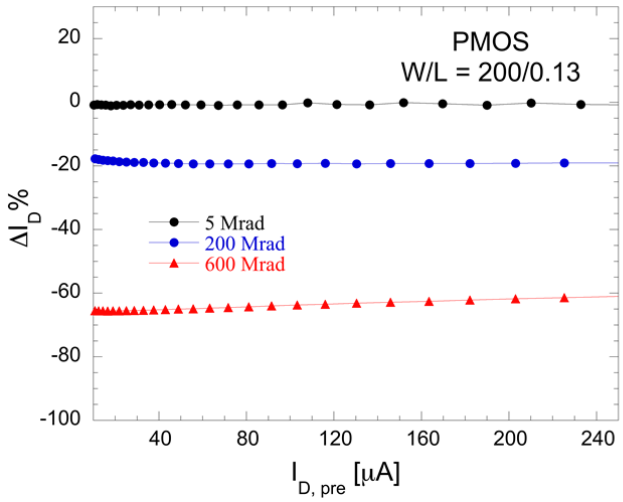


Figure 1.21: $\Delta I_D\%$ for PMOS $W/L = 200/0.13$ belonging to 65 nm technology at different TID.

W [µm]	NMOS TID		PMOS TID	
	200 Mrad	600 Mrad	200 Mrad	600 Mrad
$W \leq 1$	-15%	-20%	-25%	-43%
$W > 1$	-6%	-9%	-5%	-13%

Table 1.6: Averaged values of percentage variation of I_{on} current for both NMOS and PMOS with a channel width greater or lower than 1 µm.

Threshold Voltage

Threshold voltage (V_{Th}) was obtained with the quadratic extrapolation method from the $I_D - V_{GS}$ plot measured at $|V_{DS}| = 1.2$ V for Core and ELT devices [9]. The be-

havior of the drain current is confirmed by the trend of the radiation-induced threshold shift, which in NMOSFETs is negative at 10 Mrad and positive at 200 Mrad and 600 Mrad. Because of the effect of interface states, $I_D - V_{GS}$ curves are also stretched at high TID. For PMOSFETs the maximum $|\Delta V_{th}|$ is smaller than 40 mV and increases with the TID, see figure 1.22. For NMOSFETs at relatively low dose, i.e. 10 Mrad, the threshold voltage is lower the one extrapolated before irradiation, whereas for high dose, i.e. 200 Mrad and 600 Mrad, the threshold voltage is higher than the one extrapolated before irradiation. Such "change in direction" is another confermation to the fact that at higher doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge.

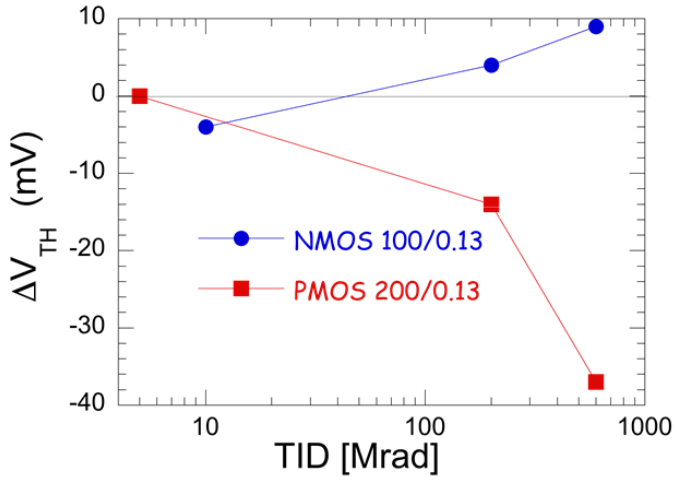


Figure 1.22: Threshold Voltage shift for NMOS with $W/L = 100/0.13$ and PMOS $W/L = 200/0.13$ belonging to 65 nm technology at different TID.

Transconductance

The value of the transconductance g_m was extracted from $I_D - V_{GS}$ curves and its behavior has been studied as a function of the gate-to-source voltage V_{GS} and of the drain current I_D before and after irradiations. No appreciable variations of the transconductance are detected. Figure 1.23 shows the transconductance g_m as a function of the drain current I_D, up to $I_D = 30$ mA, before and after exposure to X-rays, for PMOS and NMOS devices with $W/L = 100/0.35$ biased at $|V_{DS}| = 0.6$ V and $V_{BS} = 0$ V. As for the 110 nm technology such results was expected from the $I_D - V_{GS}$ curves.

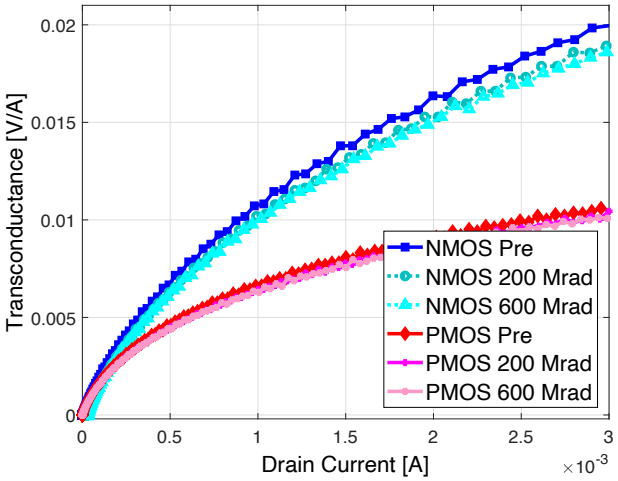


Figure 1.23: Transconductance g_m as a function of the drain current I_D, before and after irradiations up to 200 Mrad and 600 Mrad total dose, for PMOS and NMOS devices with $W/L = 100/0.35$ biased at $|V_{DS}| = 0.6\,\text{V}$ and $V_{BS} = 0\,\text{V}$.

1.5 Experimental Results - Noise Voltage Spectrum

1.5.1 110 nm technology

As already metioned in 1.1.5, Noise Voltage Spectrum of a MOSFET device can be modeled by the sum of two noise term: flicker or 1/f noise and white noise. Flicker noise is characterized by a power spectral density that is inversely proportional to frequency:

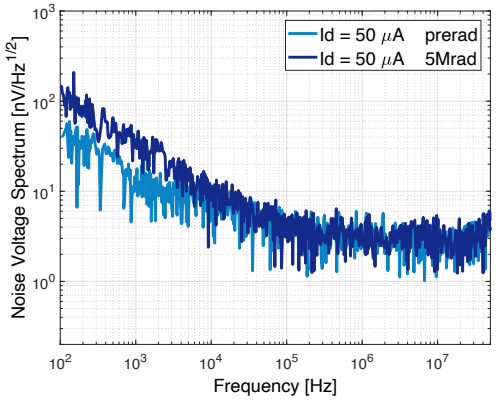
$$S^2_{1/f}(f) = \frac{K_f}{C_{OX}WL}\frac{1}{f^{\alpha_f}} \tag{1.19}$$

For the examined 110 nm technology, typical α_f values are 1.01 for the PMOS and 0.93 for the NMOS. Different profile of oxide traps interacting with carriers of different polarity might be the cause of this behavior ([11] [12]). Previous studies of the noise properties of scaled CMOS processes pointed out that α_f is independent of the device drain current and of the gate length and width ([13] [14]). The behavior of the 1/f and channel thermal noise components was monitored before and after irradiation.

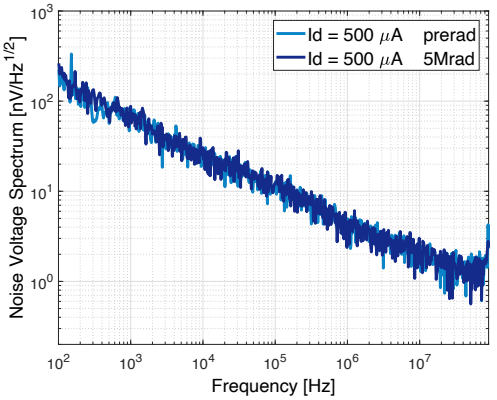
Effects on Noise Voltage Spectrum of 110 nm technology will be discussed in what follows.

Figures 1.24a and 1.24b show data for open layout NMOSFETs devices whereas Figure 1.25 shows data for an enclosed layout NMOS device. In agreement with the negligible post-irradiation change of the transconductance, channel thermal noise does not seem to be affected by ionizing radiation. The increase of 1/f noise is

small, too. In particular, both open layout and enclosed layout devices show a comparable slight rise in the 1/f noise. This little noise sensitivity is likely to be associated with the very thin gate oxide and correlated to the negligible threshold voltage shift. This change in the 1/f noise component becomes less important at higher I_D, in fact in Figure 1.24a, where the devices was operating at $I_D = 50\,\mu A$, it is possible to observe a larger increase of the flicker noise than the one detected in Figure 1.25, where the devices was operating at $I_D = 500\,\mu A$. This can be related to the larger impact of noise associated to the lateral parasitic transistors at small I_D density [15], in fact this effect is less evident in enclosed layout devices as represented in Figure 1.25.



(a) NMOS with $W/L = 600/0.72$ at $I_D = 50\,\mu A$.



(b) NMOS with $W/L = 600/0.12$ at $I_D = 500\,\mu A$.

Figure 1.24: Noise voltage spectra before and after exposure to X-rays (5 Mrad integrated dose) of 110 nm CMOS technology devices

As far as PMOSFETs are concerned, the behaviour after irradiation is slightly different. Although no changes either in white noise or in 1/f noise are detected, a Lorentzian noise component appears in the noise voltage spectrum. This can be modeled by an additional term in equation (1.12):

$$S_L^2 = \frac{A_L}{1 + (2\pi f)^2 \tau_L^2} \tag{1.20}$$

This Lorentzian term may arise from radiation-induced defects which act as traps for charge carriers in the device channel. In (1.20), A_L and τ_L are determined by the physical nature of the traps. The Lorentzian term has a constant amplitude A_L up to the frequency $f_L = 1/(2\pi\tau_L)$ and then falls off as $1/f^2$. This contribution is much more evident for bigger devices, in fact figures 1.26a and 1.26b represent PMOS devices with $W/L = 600/0.12$ and $W/L = 200/0.12$ respectively. Further studies are needed to investigate the reason of this behaviour.

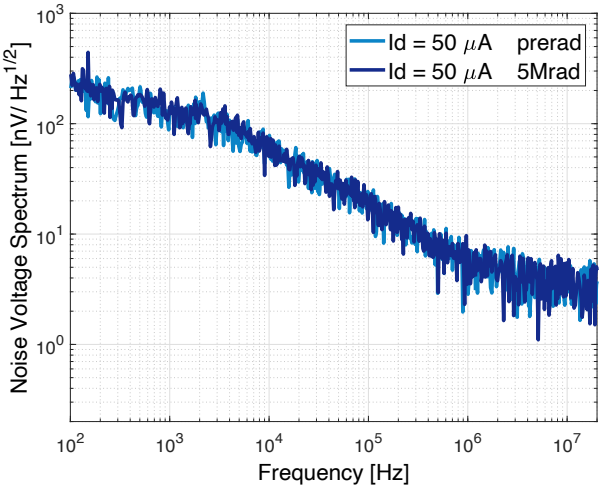
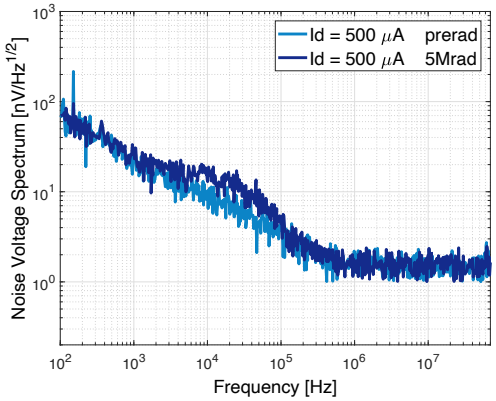
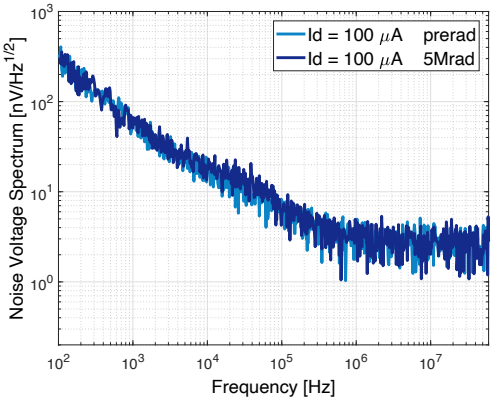


Figure 1.25: Noise voltage spectra before and after exposure to X-rays (5 Mrad integrated dose) of an NMOS with $W/L = 200/0.12$ EL belonging to the 110 nm technology at $I_D = 50\,\mu A$.



(a) PMOS with $W/L = 600/0.12$ at $I_D = 500\,\mu A$.



(b) PMOS with $W/L = 200/0.12$ at $I_D = 100\,\mu A$.

Figure 1.26: Noise voltage spectra before and after exposure to X-rays (5 Mrad integrated dose) of 110 nm CMOS technology devices

1.5.2 65 nm technology

For the examined 65 nm CMOS technology, typical α_f values are 0.88 and 1.19 for NMOS and PMOS respectively.

Regarding radiation effects on Noise Voltage Spectra of 65 nm technology devices, the following phenomena have been observed.

Figure 1.27 shows typical data for open layout NMOSFETs device operating at low current density. In agreement with the negligible post-irradiation change of the transconductance, channel thermal noise does not seem to be affected by ionizing radiation. The increase of 1/f noise is small, too. Consistently with 110 nm tech-

nology, this little noise sensitivity is likely to be associated with the very thin gate oxide.

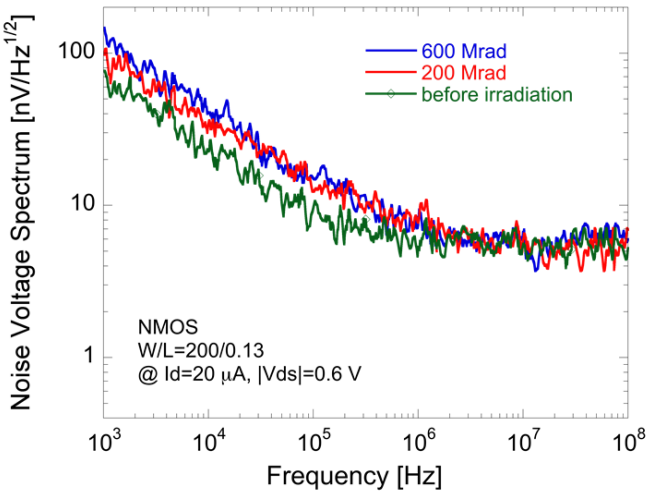
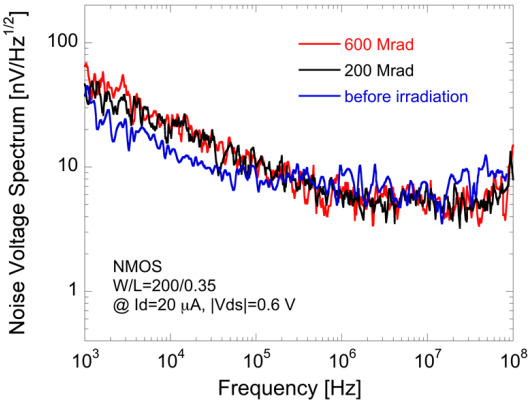
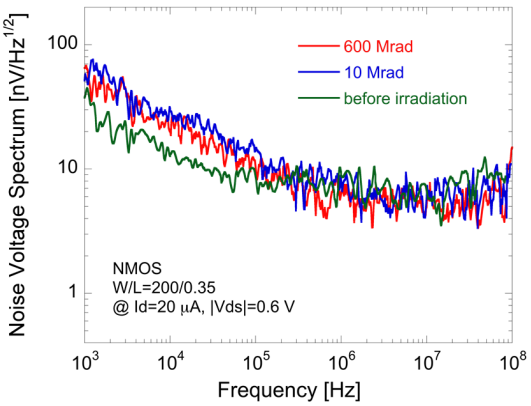


Figure 1.27: Noise voltage spectra before and after exposure to X-rays (200 and 600 Mrad integrated dose) of an NMOS with $W/L = 200/0.13$ belonging to the 65 nm technology at $I_D = 20\,\mu A$.

At 200 Mrad (and even 600 Mrad), at low I_D 1/f noise increase with respect to pre-irradiation values is smaller than the one detected in previous irradiation tests at 10 Mrad [10], as shown in figures 1.28a and 1.28b. Such effect can be correlated with the evolution of radiation effects at increasing TID and with the behavior of $I_D - V_{GS}$.



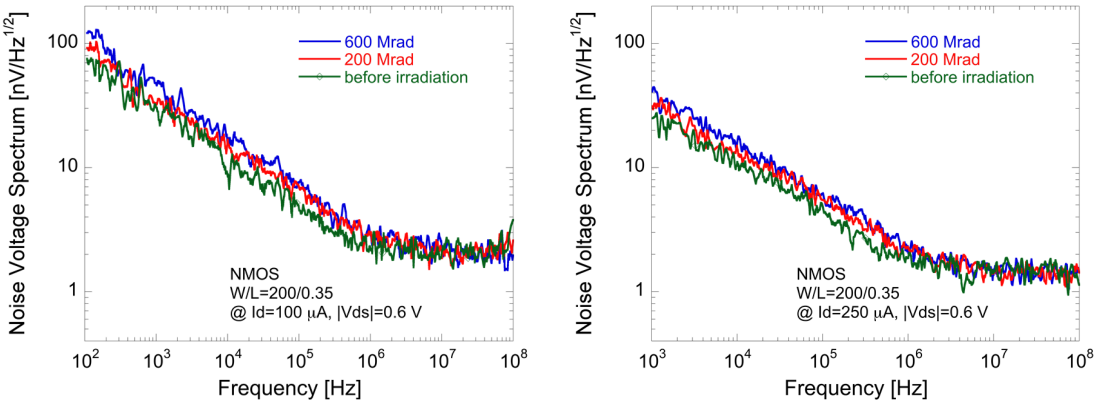
(a) Noise Voltage Spectrum before and after 200 Mrad and 600 Mrad of TID.



(b) Noise Voltage Spectrum before and after 10 Mrad and 600 Mrad of TID.

Figure 1.28: NMOS device with $W/L = 200/0.35$ belonging to 65 nm CMOS technology operating with $I_D = 20\,\mu A$.

The change in the 1/f noise component becomes less important at higher I_D, in fact in figure 1.27, where the device was operating at $I_D = 20\,\mu A$, it is possible to observe a larger increase of the flicker noise than the detected ones in figures 1.29a and 1.29b, where the device was operating at $I_D = 100\,\mu A$ and $I_D = 250\,\mu A$ respectively. Consistently with the 110 nm technology, this can be related to the larger impact of noise associated with the lateral parasitic transistors at small I_D density [15].



(a) $I_D = 100\,\mu A$. **(b)** $I_D = 250\,\mu A$.

Figure 1.29: Noise Voltage Spectrum before and after 200 and 600 Mrad of TID of NMOS device with $W/L = 200/0.35$ belonging to 65 nm CMOS technology.

The effect of 1/f noise increase can be nonnegligible. As already metioned in section 1.1.5, the gate referred noise voltage spectrum of a MOSFET device $S_e^2(f)$ can be modeled by the sum of two components, white noise $S_W^2(f)$ and 1/f noise $S_{1/f}^2(f)$, i.e. equation (1.12): $S_e^2(f) = S_W^2 + S_{1/f}^2(f)$. Figure 1.30 shows the ratio between $S_{1/f}^2(f)$ after and before the irradiation. It is possblie observe that at 600 Mrad the 1/f noise coefficient increases by about a factor 3 at low currents (70% increase of the contribution to the ENC of a detector readout channel). The lowering of 1/f noise contibution from 10 Mrad to higher doses can be explained by the fact that at very high doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge, switching off lateral parasitic transistors. Thus, noise contributions by these parasitic devices become less important. The 1/f noise increase from 200 Mrad to 600 Mrad can be explained by other effects, such as the increase of border traps in gate oxides or defects in spacer dielectrics.

For what concernes PMOSFET devices, figures 1.31a and 1.31b show the typical behavior before and after irradiation up to 200 Mrad to 600 Mrad. Again no effect is

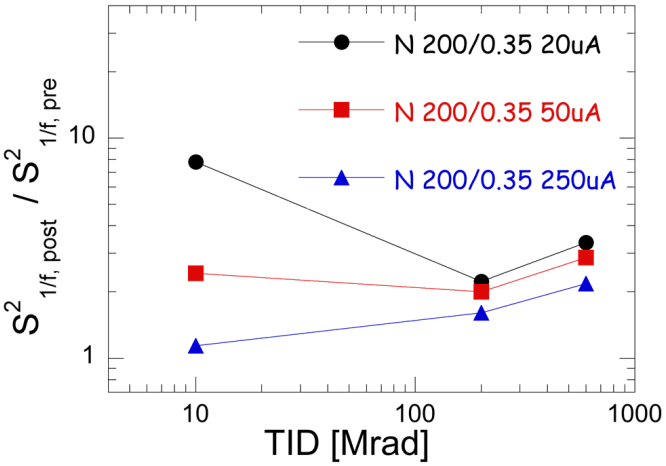
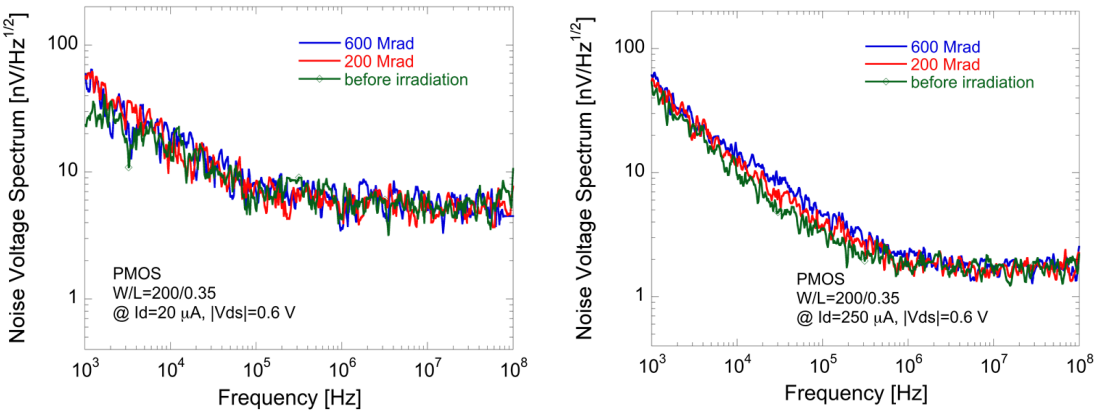


Figure 1.30: $S^2_{1/f,post}/S^2_{1/f,pre}$ with respect to TID of an NMOS with $W/L = 200/0.35$ belonging to the 65 nm technology at $I_D = 20, 50$ and $250\,\mu A$.

detected in the white noise region, whereas 1/f noise moderately increases. Unlike NMOS devices, lateral parasitic devices do not play a role here. Positive charge is accumulated both in oxides and at interface states, so there is no dependence on the drain current density.



(a) $I_D = 20\,\mu A$. **(b)** $I_D = 250\,\mu A$.

Figure 1.31: Noise Voltage Spectrum before and after 200 and 600 Mrad of TID of PMOS device with $W/L = 200/0.35$ belonging to 65 nm CMOS technology.

Like NMOS, also for PMOS the effect of 1/f noise increase can be nonnegligible. Figure 1.32 shows the ratio between $S^2_{1/f}(f)$ after and before the irradiation. It is possblie observe that at 600 Mrad the 1/f noise coefficient increases by about a factor 2 (40% increase of the contribution to the ENC of a detector readout channel). Unlike 110 nm technology no Lorentzian component is visible after irradiations.

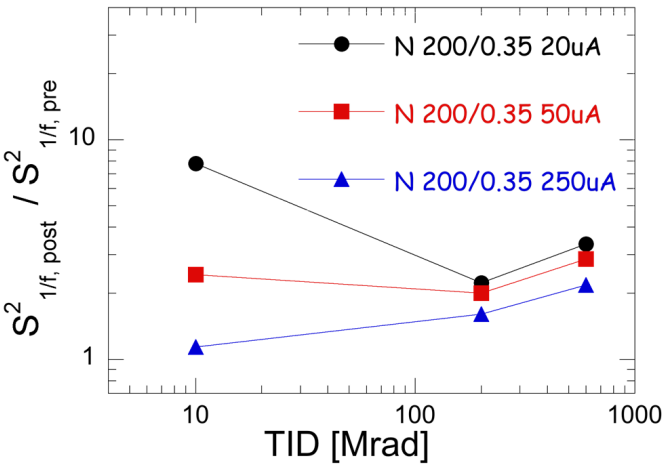


Figure 1.32: $S^2_{1/f,post}/S^2_{1/f,pre}$ with respect to TID of an PMOS with $W/L = 200/0.35$ belonging to the 65 nm technology at $I_D = 20, 50$ and $250\,\mu A$.

1.6 Discussion

A set of test devices in the 110 nm technology and in the 65 nm technology were irradiated up to 5 Mrad and 600 Mrad and their behavior after irradiation was studied, especially focusing on the noise performance.

It is possible to conclude that for what concernes 110 nm technology a large degree of tolerance up to Total Ionizing Dose of 5 Mrad is observed. This behaviour might be ascribed to their thin gate oxide. Little threshold voltage shift and negligible transconductance decrease were detected either for Core, Enclosed Layout and I/O devices. Despite there was almost no change in static characteristics, it is possible to observe a degradation of the low-frequency noise. In particular at 5 Mrad, PMOSFET devices show a Lorentzian noise term, instead NMOSFETs exhibit a moderate increase of 1/f noise at low current density. Overall, these result lead to the conclusion that this technology is suitable for the design of analog circuits with a good degree of radiation tolerance up to first step of 5 Mrad total dose. Further irradiation steps are programmed in order to study effects up to 10 Mrad and 50 Mrad TID.

On the other hand, 65 nm devices show a good degree of tolerance to ionizing radiation up to a total dose of 600 Mrad. Negligible transconductance increase was detected for all devices. A threshold voltage shift lesser than 40 mV is detected. With increasing TID, NMOS devices show $I_D - V_{GS}$ characteristic moving in different directions. This effect can be ascribed to the fact that at low TID, positive charge in STI oxides switches on lateral devices, increasing I_D for the same V_{GS} and reducing the threshold voltage value. At higher doses negative charge trapped in interface states at the STI oxides gradually compensates oxide-trapped positive charge, switching off lateral parasitic transistors and reducing I_D for the same V_{GS}, increasing the threshold voltage value. For both NMOSFET and PMOSFET no effect is detected in the white noise region. On the contrary, the effect of 1/f noise increase can be nonnegligible both for N-channel and P-channel devices. In particular, for what concerns NMOS devices, at 600 Mrad the 1/f noise coefficient increases by a factor 3 at low currents. Regarding PMOS devices, at 600 Mrad the 1/f noise coefficient increases by about a factor 2. Unlike 110 nm technology no Lorentzian component is visible after irradiations. Such results, in particular the flicker noise increase, can explain results obtained with chips designed in 65 nm CMOS technology in the frame of the RD53 and CHIPIX65 collaborations [16] [17]. A further irradiation step is programmed in order to study effects up to a Total Ionizing Dose of 1 Grad.

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