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## NANOELECTRONICS AND NANOLITHOGRAPHY

Jan VOVES

*Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Microelectronics,  
Technická 2, 166 27 Praha 6, Czech Republic, voves@feld.cvut.cz*

### Abstract

Currently optical lithography is the dominant exposure tool. The decrease of the critical dimensions is based on using radiation with a shorter wavelength. Extreme Ultra Violet lithography is the natural successor of conventional optical lithography. X-ray proximity lithography represents the last step in the decrease of photon wavelength for nanolithography purposes. Current e-beam lithography systems are mainly serial technologies, which are limited by the scanning speed of the e-beam in the pattern generation. Alternative techniques are developed for the mass production and for laboratory purpose as well. We present the Local Anodic Oxidation (LAO) by Atomic Force Microscope Ntegra NT-MDT. LAO is still attracting attention because of its relatively low cost and high resolution. The LAO can be applied to very thin semiconductor layers to define quantum point contacts, quantum wires, rings, dots and other devices. We report our results of LAO process on the thin GaMnAs layers prepared by low temperature MBE growth. We perform LAO in the AC mode with optimized parameters to construct a potential barriers in the thin GaMnAs layer patterned by the electron beam lithography.

### 1. INTRODUCTION

Nanotechnology is the manipulation or self assembly of individual atoms, molecules, or molecular clusters into structures to create materials and devices with new properties. Nanotechnology opens a completely new world of opportunities and solutions in all kinds of areas: the field of diagnostics and analytics, textile industry, energy sector, electronics and automotive industry. A key understanding of nanotechnology is that it offers not just better products, but improved means of production as well. That's the real meaning of nanotechnology, and why it is sometimes seen as *"the next industrial revolution"*.

In the field of electronics we can expect a huge improvements connected with the nanoelectronics. At the nano-level, operation at the rate of peta bytes per second becomes possible, resulting in systems a billion times more efficient than those of today. Nanostructured transistors will continue the trend in lower cost per transistor and use less energy, thereby improving the efficiency of computers by a factor of millions. Higher frequencies provide 10 times more bandwidth, with consequences in business, education, entertainment and defence. We can expect the expansion of small mass storage devices to multi-terabit capacities, 100 times better than today and integrated sensor systems that collect data utilizing minimal power, space and weight.

### 2. NANO-ELECTRONICS

The critical dimensions of the electron devices are fast streaming to the nanometric range, Therefore the new quantum effects appear in the nanoelectronic devices: discrete electron energy states in the nanometric quantum wells, electron tunneling through the thin potential barrier, electron wave function interference,

Cooper pair tunneling known as Josephson effects. These effects enable to develop the devices with a new functionality and performance. In other words we are entering the realm of quantum mechanics and it is different from the classical mechanics that we encounter in everyday life.

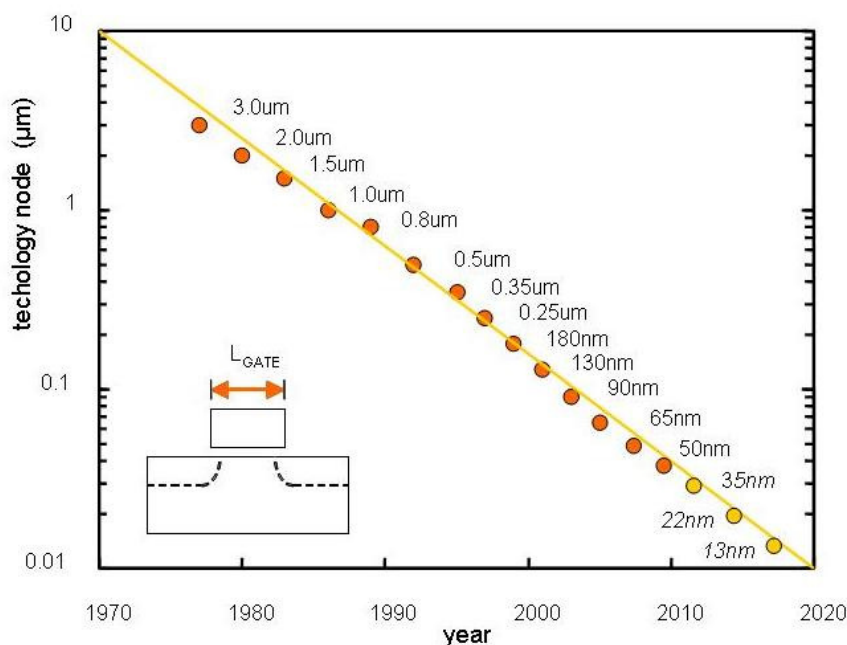


Fig. 1. MOSFET design gate length scaling.

Current status of the nanotechnology enables to emerge the *new nanoelectronic devices*. Most important and frequent is the advanced MOSFET with gate length down to 10 nm (Fig. 1.). Quantum effects appear fully in the so called low-dimensional structures using potential engineering by the semiconductor heterostructures. High Electron Mobility Transistor (HEMT) with the fast electron transport along the quantum well, Quantum Well (QW) Laser characterised by the low threshold current and Resonant Tunneling Diode (RTD) are the typical examples of the 2-dimensional

quantum devices. By the confining the electrons in the one more direction we get the quantum wire with 1D conduction. Such conditions we can expect in *carbon nanotubes*. Full confinement shows the quantum dot (QD) or "artificial atom". Transport through the quantum dot is strongly influenced by the tunneling and by the so called Coulomb blockade. These effects enable to realise the *Single Electron Transistor* (SET). Further progress we can expect from spin devices and from devices based on the self assembled organic and inorganic molecules (carbon nanotubes, graphene, fullerenes, DNA, peptides). *Molecular nanoelectronics* holds the promise of self-assembly of circuits, both on a massive scale and cheaply, using chemical or biological reactions. Self-assembling nanotube 'wires' just 2-nm wide and with 9-nm separation are already a reality. The combination of silicon structures and molecular electronics may open the way for solutions of truly impressive potential.

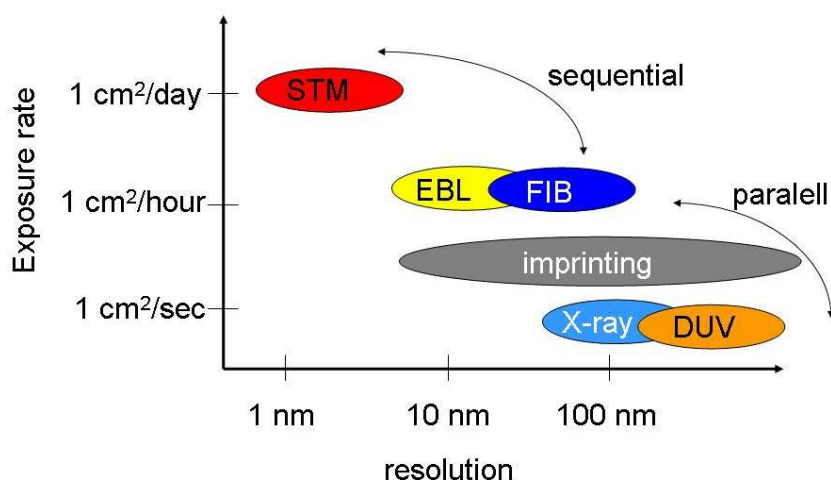
The development of novel devices at the nanometer scale with potential for large-scale integration and room temperature operation is a formidable task. Many of the difficulties and of the limits of candidate technologies for nanoelectronics and molecular electronics could be predicted, anticipated and, hopefully, solved if detailed modelling tools of realistic devices and structures were available. The same modelling tools could be used to design more robust devices, and to select molecules and device structures with potential for use in large-scale integrated circuits. All simulators integrated in the one complex package are named *Technology Computer Aided Design* (TCAD) tools. They include process, device and circuit simulation modules, as well as programs for parameter extraction and device modelling. Models originally developed for silicon technology were enhanced for other semiconductor materials including heterostructures. Device simulators give possibility to perform not only electrical analysis of the structure, but thermal and optical analysis as well. In this time, when the miniaturization of structures led to breakdown of the classical models,

the semi-classical and quantum models are taken in the account. The *nano-characterisation techniques* such as Atomic Force Microscopy (AFM), Scanning Tunneling Microscopy (STM) and Scanning Electron Microscopy (SEM) are necessary for the correct implementation of physical models into predictive simulation tools.

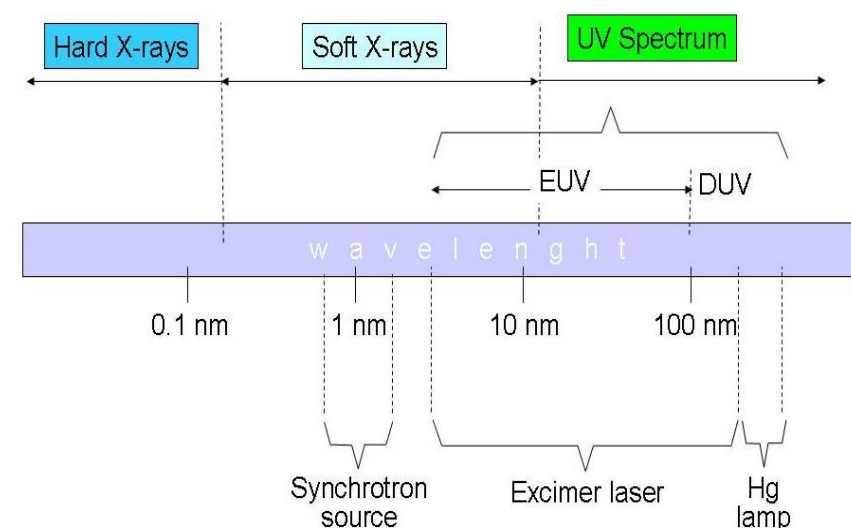
### 3. NANOLITHOGRAPHY

The “*top-down*” approach to lithography begins with a suitable starting material and then “sculpts” the functionality from the material. This technique is used by the semiconductor industry in forming devices out of an electronic substrate utilizing pattern formation and pattern transfer processes that have the requisite spatial resolution to achieve creation of structures at the nanoscale. Technology limits are moving to the subnanometric

range in the semiconductor epitaxy – such as Molecular Beam Epitaxy (MBE), Metallo-Organic Vapour Phase Epitaxy (MOVPE), Atomic Layer Epitaxy (ALE), defining vertical structure of devices. The horizontal structure is now defined by the *resolution of the lithography*, which is crucial (Fig. 2.). Currently optical lithography is the dominant exposure tool [1]. The decrease of the critical dimension is based on using light



**Fig. 2.** Lithography trade-off between resolution and exposure rate.



**Fig. 3.** Wavelength spectrum of exposure radiation sources.

with a shorter wavelength (Fig. 3.). It appears physically feasible to achieve optical lithography with sub 100 nm resolution. *Extreme Ultra Violet (EUV) lithography* is the natural successor of conventional optical lithography on its way towards smaller wavelengths (Fig. 4.). EUV resolution can be extended down to 40 nm. *X-ray proximity lithography*, using a typical wavelength of 1 nm, represents the last step in the decrease of photon wavelength for nanolithography purposes (Fig. 5.). Current e-beam lithography systems are mainly serial techno-

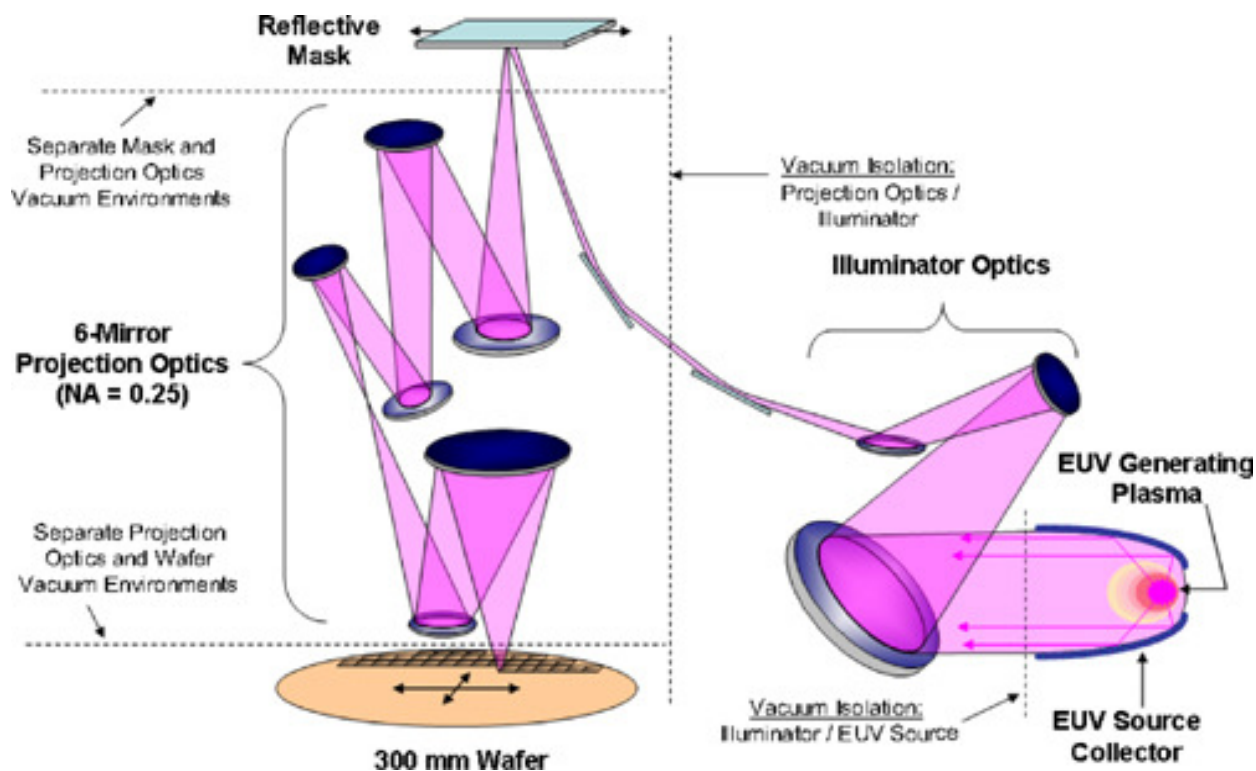


Fig. 4. Schematic of EUV lithography [2].

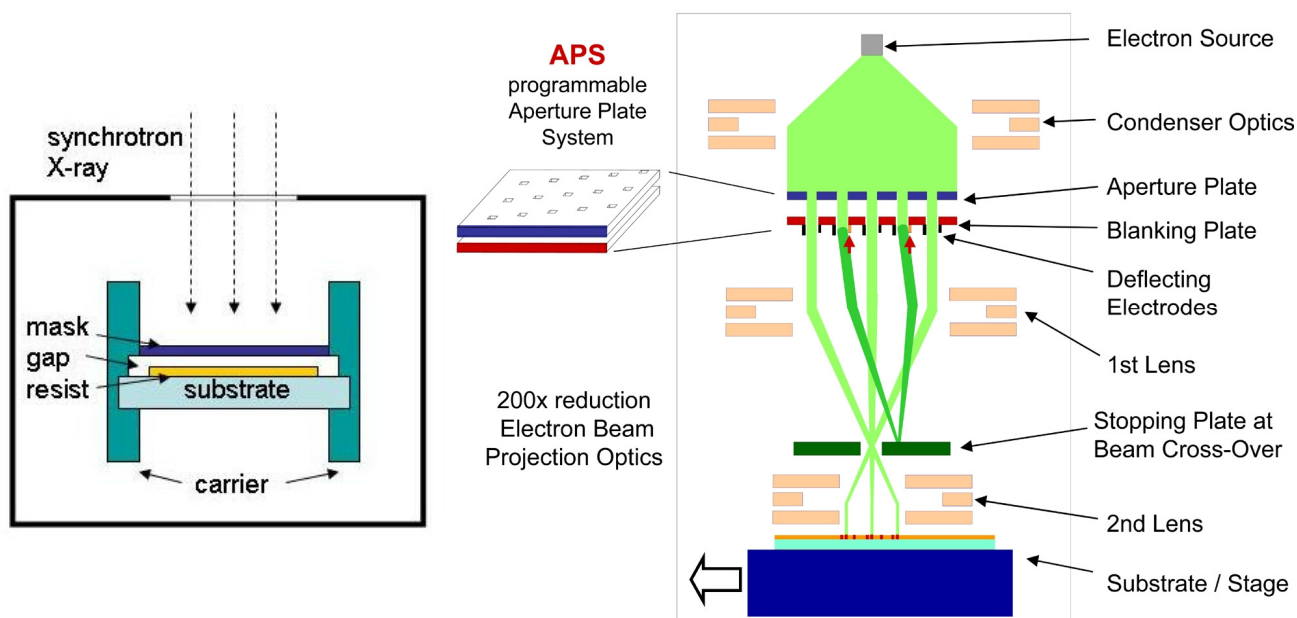
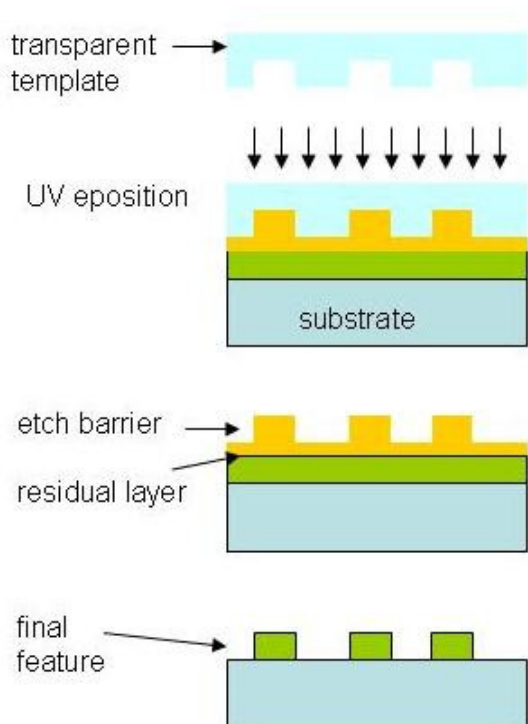


Fig. 5. Schematic of X-ray lithography.

Fig. 6. Schematic of electron projection lithography [3].



**Fig. 7.** Schematic of flash imprint lithography.

logies, which are limited by the scanning speed of the e-beam in the pattern generation. Electron-beam lithography (EBL) is the essential basis of nanostructure fabrication at present. Dimensions down to 30 nm are routinely produced in many research laboratories with high reproducibility. Resolutions down to 7 nm have been demonstrated. *Projection electron-beam lithography* approach combines the high resolution with the throughput of a parallel projection system (Fig. 6.). By the ion beam projection ions can also be used for resistless processes where ions directly modify the surface of a substrate.. There are two main strands to nanometer-scale printing. The first one relies on the moulding of a thin polymer layer by a stamp under controlled temperature and pressure (*imprinting*). The second one is based on the transfer of a monolayer of self assembled molecules from an elastomeric stamp to a substrate (*inking*). In step and flash

imprint lithography (Fig. 7) a transparent template is lowered onto a treated substrate and the gaps are filled with a low-viscosity UV-curable monomer. UV light shining

through the substrate causes the monomer to convert into a hardened etch barrier. Upon removal of the template, the etch barrier covers the substrate in a pattern of thick barriers separated by a thin residual layer. One etch removes the residual layer to expose areas of treated substrate; a subsequent etch transfers the pattern to the substrate.

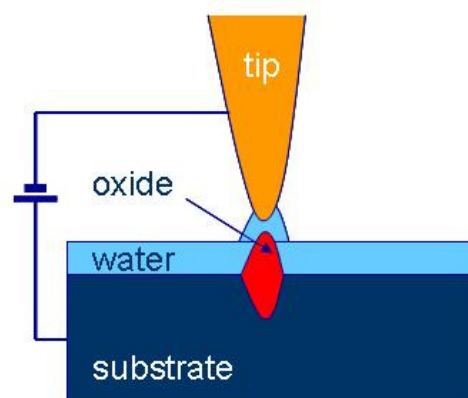
Further progress can be expected from the change of top-down defining of the structures to the self organisation of the matter called as *bottom-up approach*. This approach builds small structures from the atom, molecule, or single device level upward. At present, however, the top-down approach has substantially better development than the bottom-up approach. It is fair to assume that for the fabrication of structures with nanometer dimensions, the bottom-up approach will play an essential role in the near future. Effort in employing large arrays of *scanning probes* for the nanodevices fabrication is certainly promising. Probe tips can be used for the surface layer scratching or for the local anodic oxidation of the surface.

#### 4. LOCAL ANODIC OXIDATION

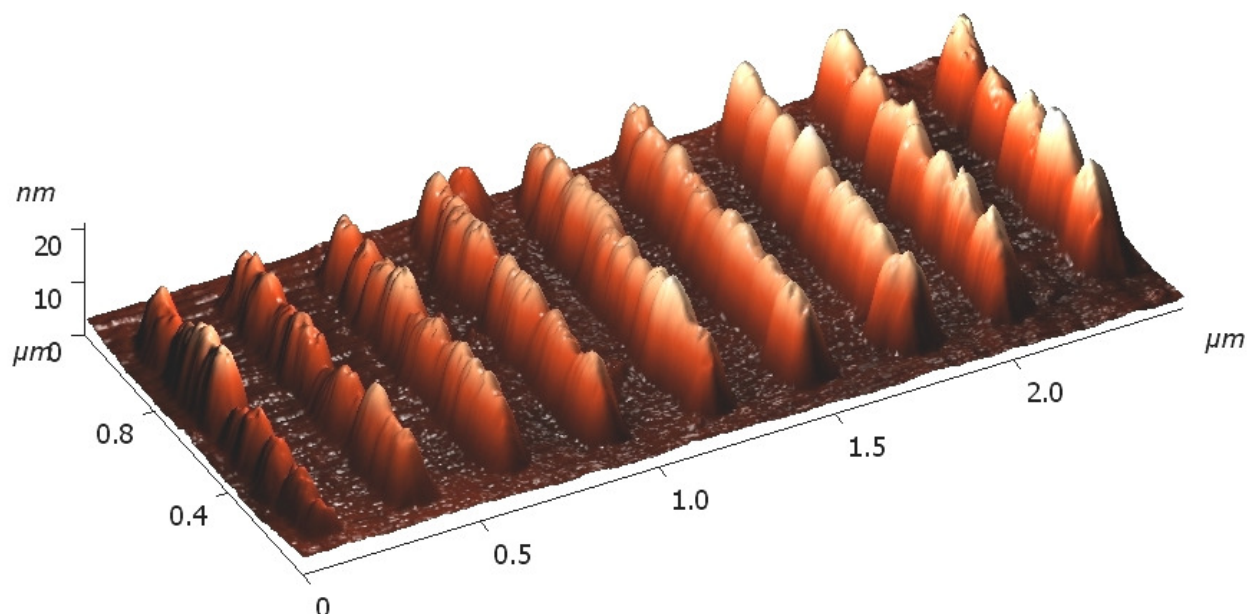
The local anodic oxidation (LAO) (Fig. 8.) performed by the conductive tip of an atomic force microscope (AFM) becomes attractive in the last years for the device patterning in the nanometer scale at laboratory conditions. Oxide lines produced by the constant negative voltage applied to the tip lack from poor homogeneity and reproducibility. Accumulation of ionic charges during the electro-chemical reaction limits the oxidation process. Modulated (AC) voltage instead of constant (DC) voltage applied between the tip and the sample was suggested to neutralize the reaction products and limit the lateral carrier diffusion. Modulation of the applied voltage enhances the aspect ratio of the oxide lines, which significantly strengthens the insulating properties of the lines. *AC mode oxidation process* is found to be more reliable and reproducible [4].



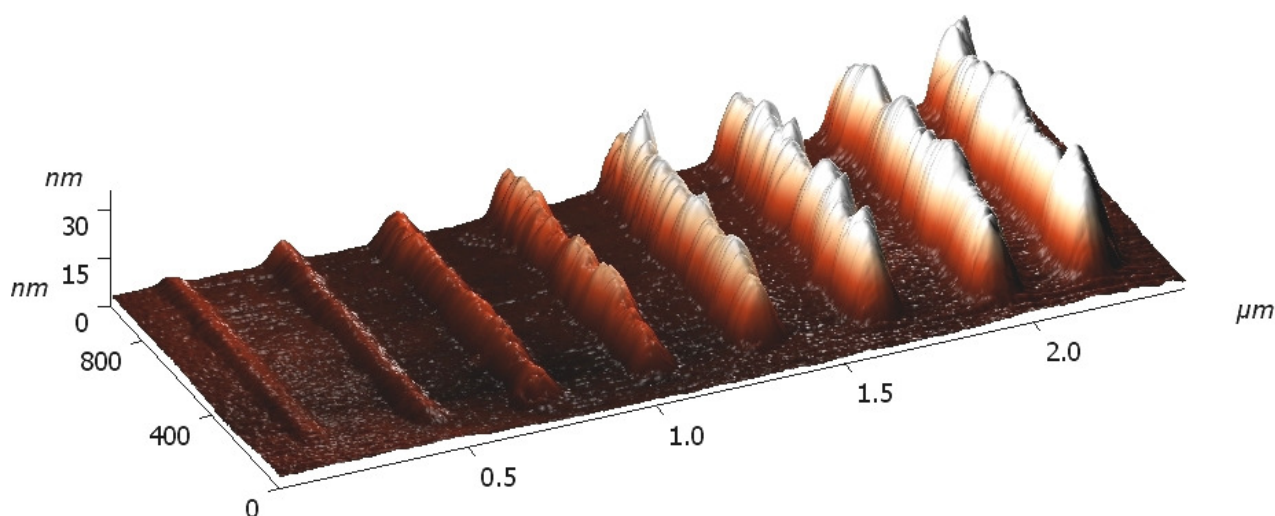
We report our results of LAO process on the thin GaMnAs layers prepared by low temperature MBE growth. The samples consist of GaAs buffer layer 200 nm thick followed by 5 nm GaAs and 10 nm GaMnAs layer. These structures were patterned by LAO in DC mode formerly [5]. We use the AFM microscope Ntegra NT-MDT placed in a sealed box with the controlled relative humidity (RH) in the range 50-80%. LAO in AC mode is performed by using a voltage pulse modulator, which provides positive and negative pulses depending on duty cycle of the modulation square signal from generator. An external power supply defines amplitudes of the modulated pulses  $V_{ox}$  and  $V_{res}$ . The external output of signal access module (NT-MDT SAM-01) is used to start and stop lithography (oxidation) process and modulated voltage is connected to an external input, which leads directly to an AFM-tip. Parameters to be set are modulation frequency, duty cycle defining oxidation  $t_{ox}$  and reset time  $t_{res}$ , negative voltage  $V_{ox}$  on the tip for oxidation and positive voltage  $V_{res}$  for eliminating accumulated space charge.



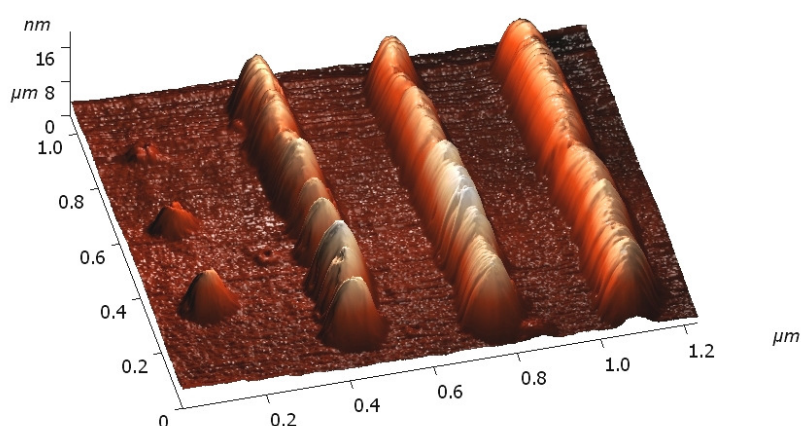
**Fig. 8.** Schematic of the local anodic oxidation by the AFM tip.



**Fig. 9.** Oxide lines for negative voltages  $V_{ox}$  applied on the tip from -10 V to -24 V. Temperature was 25 °C, velocity of the tip was 0.4 μm/s. Set point was 50 % from original value and RH = 65 %. Frequency was set up to 1 kHz, duty cycle to 50 % and  $V_{res} = 4$  V.



**Fig. 10.** Oxide lines for tip velocities: 0.1, 0.2, 0.3, 0.4, 0.5, 1, 1.5, 2 and 2.5  $\mu\text{m/s}$ .  $T = 25\text{ }^\circ\text{C}$ ,  $\text{RH} = 65\%$ . Set point was on 50 % of the original value. Duty cycle was 50 % and frequency 10 Hz. The voltages were:  $V_{\text{ox}} = -16\text{ V}$  and  $V_{\text{res}} = 4\text{ V}$  in the square pulse.



**Fig. 11.** Oxide lines for the frequency increasing by decades from 1 Hz to 1 kHz. Velocity of the tip was 0.4  $\mu\text{m/s}$ , set point was 50 % from the original.  $V_{\text{ox}} = -16\text{ V}$  and  $V_{\text{res}} = 4\text{ V}$ . Duty cycle was set up to 50 %,  $T = 25\text{ }^\circ\text{C}$  and  $\text{RH} = 60\%$ .

We analyzed the properties of LAO oxide lines for different negative voltages applied on the tip from -10 V to -24 V (Fig. 9). For voltage  $> -10\text{ V}$  oxidation did not start. The influence of the tip velocity in the range from 0.1 to 2.5  $\mu\text{m/s}$  is shown in Fig. 10. With increasing velocity the height of the oxide line increases. The reason of this behaviour is given probably by the less charge accumulation on the sample surface by higher velocities. Lines in the Fig. 11. are grown with different pulse frequencies in the range from 1 Hz to 1 kHz. Nonzero values of  $V_{\text{res}}$

improved homogeneity of lines and we observed no significant changes in the range 1 – 4 V. We used LAO in the AC mode with optimized parameters to construct constrictions and tunneling barriers in the thin GaMnAs stripes patterned by the electron beam lithography. We performed transport measurements in magnetic field with different polar orientations. Resulting data are analyzed with respect to the potential spintronic applications of ferromagnetic semiconductor structures.



## 7 CONCLUSION

The local anodic oxidation (LAO) by the atomic force microscope (AFM) in the AC mode could be a good alternative to standard lithographic techniques especially for the device patterning in the nanometer scale at laboratory conditions. In the combination with EBL the nanostructures with the resolution of a few tenths of nanometers could be prepared in a very fast and efficient way.

## ACKNOWLEDGEMENT

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