CEG 3156: High-Level Computer Systems Design (Winter 2024)
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Possible Solutions to Quiz #1: Arithmetic Circuits

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Instructions

This quiz will last 35 minutes. Please complete the following questions, and answer to the best of your ability. State any assumptions and acronyms that are utilized in the quiz, and do not forget to submit your answers on Brightspace.

Question I

This question deals with division circuitries. We have seen, in class, three different methodologies for the realization of unsigned division.

Part a

Explain, using a flow chart, one algorithm for the unsigned division of two 32-bit numbers. Draw its corresponding block diagram, using ALUs, registers, shift registers and a control block. Indicate the widths of all busses, as well as major status and control signals.

There are three different algorithms that were studied in class. We will show one here, but any of the three are valid solutions in this case. The algorithm we choose here is the simplest one, shown in the flowchart in figure 1, and the block diagram in figure 2.

Part b

State two drawbacks with your design, and provide a potential solution for each drawback.

Two possible drawbacks with our design are:

- Our ALU and divisor register are both 64-bit wide, due to the right shift of the 32-bit divisor. However, we can reduce both the ALU and divisor register widths to 32 bits by allowing the remainder register to shift to the left
- Our quotient register is a waste of a 32-bit register and its routing resources. We can eliminate it and store it in the left half of the remainder register. As we're shifting the remainder to the left, the quotient will be shifted within of the remainder register, with the final remainder remaining in the right half of the remainder register

Question II

Reviewing the circuit in Figure 3, provide the structural VHDL implementation of this 4-bit carry lookahead adder entity. Assume that you already have entities for both the Full Adder and the Carry Lookahead Logic.
This question has many potential answers in structural VHDL.

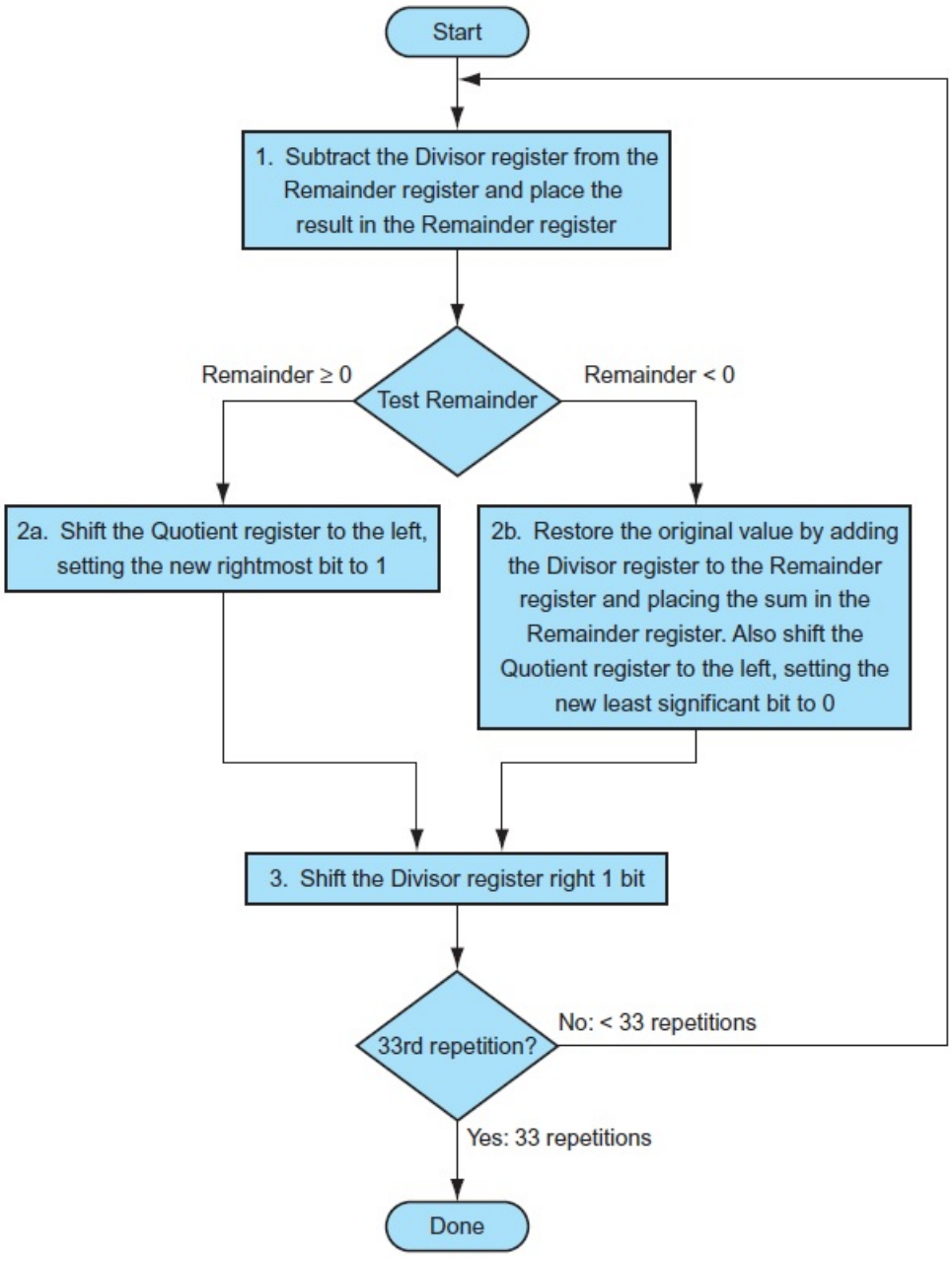

Figure 1: Possible flowchart of a divider

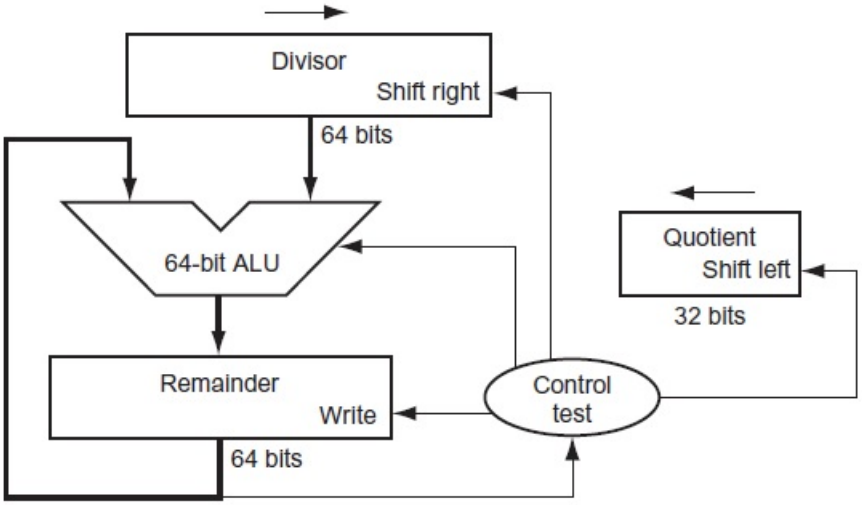

Figure 2: Possible realization of a divider

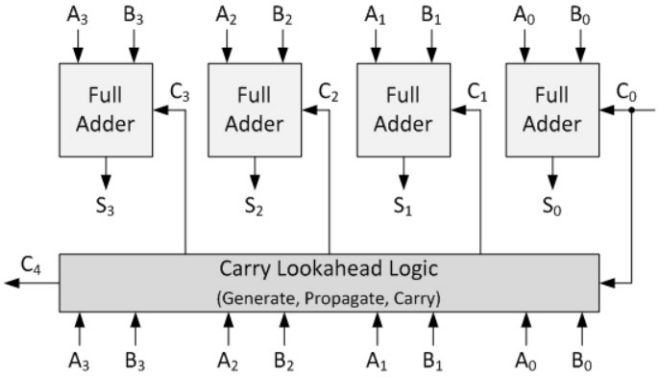

Figure 3: Possible implementation of a 4-bit carry lookahead adder