

CEG 3156: High-Level Computer Systems Design
(Winter 2024)

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Potential Solutions for Quiz #2: Pipelined
Processor

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Instructions

This quiz will last 35 minutes. Please complete the following question, and answer to the best of your ability. State any assumptions and acronyms that are utilized in the quiz, and do not forget to submit your quiz on Brightspace.

Question I

This question deals with pipelined processor design.

Solution

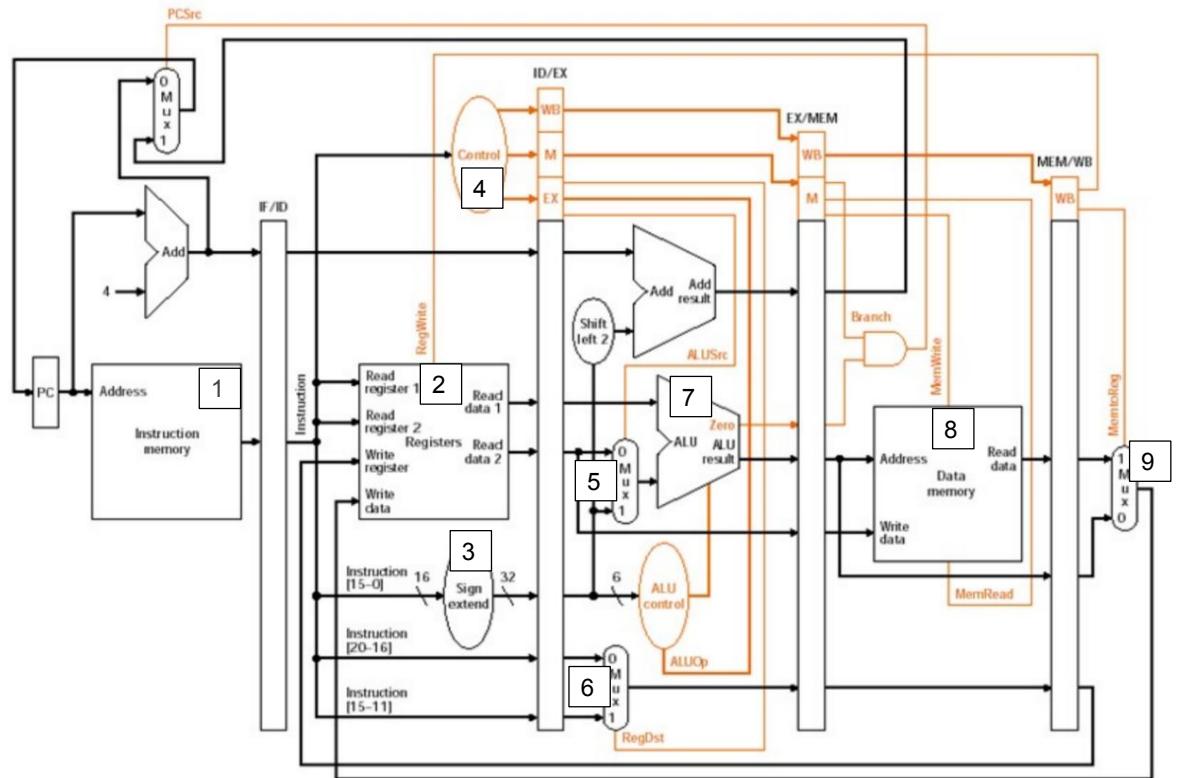
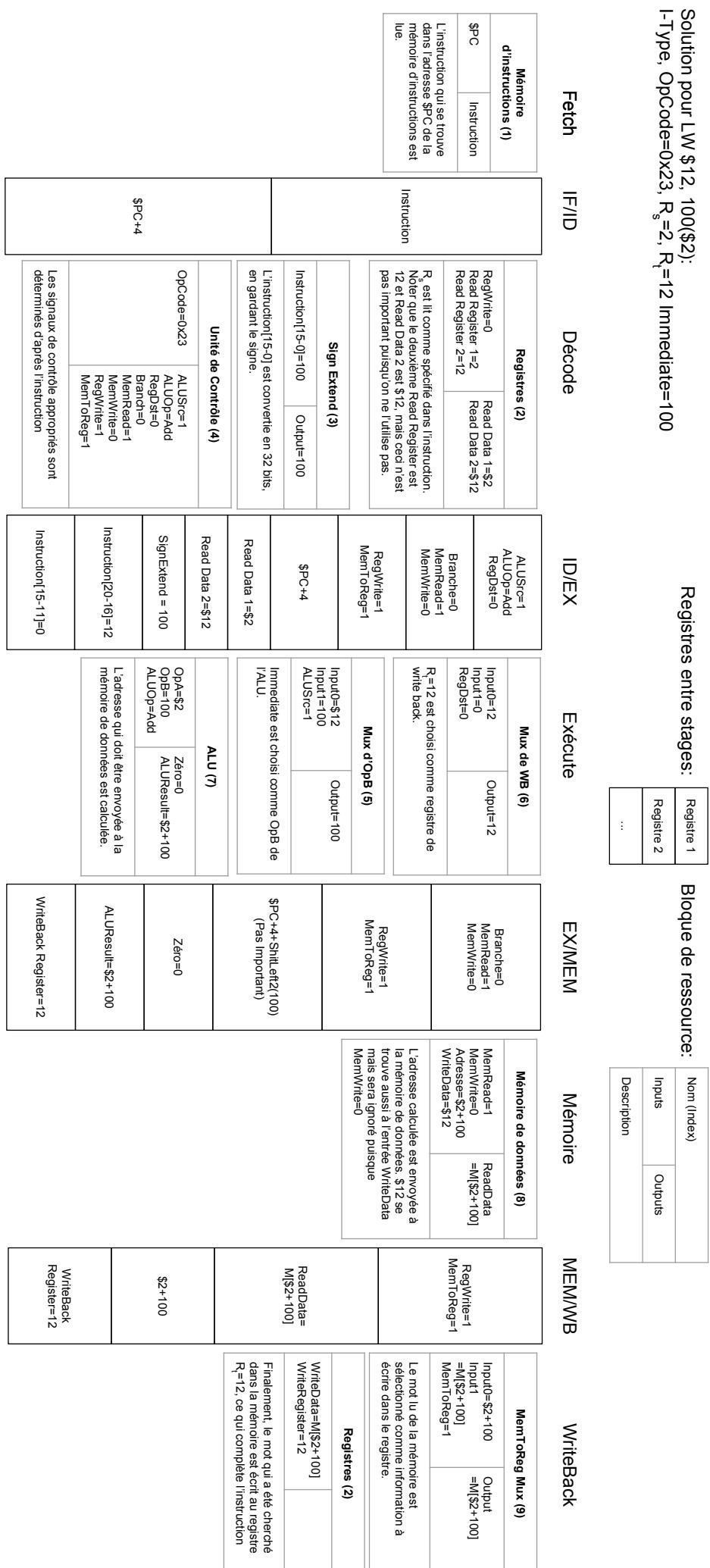


Figure 1: Datapath avec indexes

Solution pour LW \$12, 100(\$2):
I-Type, OpCode=0x23, R_s=2, R_t=12 Immediate=100



Solution pour instruction Add \$5, \$1, \$3:
R-Type, OpCode=0x00, R_s=5, R_t=1, R_d=3, Funct=0x20, Shamt=C

Registres entre stage:

Registre 1

Bloque de ressource:

Nom (Index)	
Inputs	Outputs
Description	

Nom (Index)

Mémoire d'instruction (1)		Registres (2)		Mux de WB (6)	
\$PC	Instruction	RegWrite=0 Read Register 1=5 Read Register 2=\$1	Read Data 1=\$5 Read Data 2=\$1	ALUOp=Funct RegDst=1	Input0=1 Input1=3 RegDst=1
	L'instruction qui se trouve dans l'adresse \$PC de la mémoire d'instructions est lue.	R _s et R _t sont lui, comme spécifié !		Branch=0 MemRead=0 MemWrite=0	
	Instruction	RegWrite=1		Branch=0 MemRead=0 MemWrite=0	
				R _t =3 est choisi comme registre de write back.	
					RegWrite=1 MemToReg=0

MémToReg	Mux (9)
Input0=\$5+\$1 Input1=M[\$5+\$1] MemToReg=1	Output=M[\$5+\$1]

La somme qui a été calculée à l'étape exécute est sélectionnée.