Exam 17 December 2008, questions

Digital Systems II (University of Ottawa)

Université d'Ottawa
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CEG3155/CEG3555 Digital Systems II

Name (surname, first name):_____

Student Number:_____

Examiners: Professor A. H. G. Al-Dhaher
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Final Examination, December 17, 2008 Time allowed: 3 hours

Note:

- This is a close-book examination and you are required to abide by the University's regulations regarding the conduct of exams
- Answer ALL questions.
- Use the provided space to answer the following questions. If more space is needed, use the back of the page.
- Read all the questions carefully before you start.

Good luck

Question	Points gained %	Percentage %
1		20
2		20
3		20
4		20
5		20
Total		**100**

Question 1 (20 marks)
Part A (10 marks):
Given the function:

$$f = w_1 \otimes w_2 \otimes w_3$$

(i) Write the truth table for this function.

(ii) Write the logic expression in sum of product form.

(iii) Implement this function in 4 – 1 multiplexer using the truth table method and draw the circuit.

(iv) Use Shannon's theorem to implement this function in 4- 1 multiplexer and use the same selection inputs you used in part (iii). Draw the circuit.

Question 1 part B (10 marks)

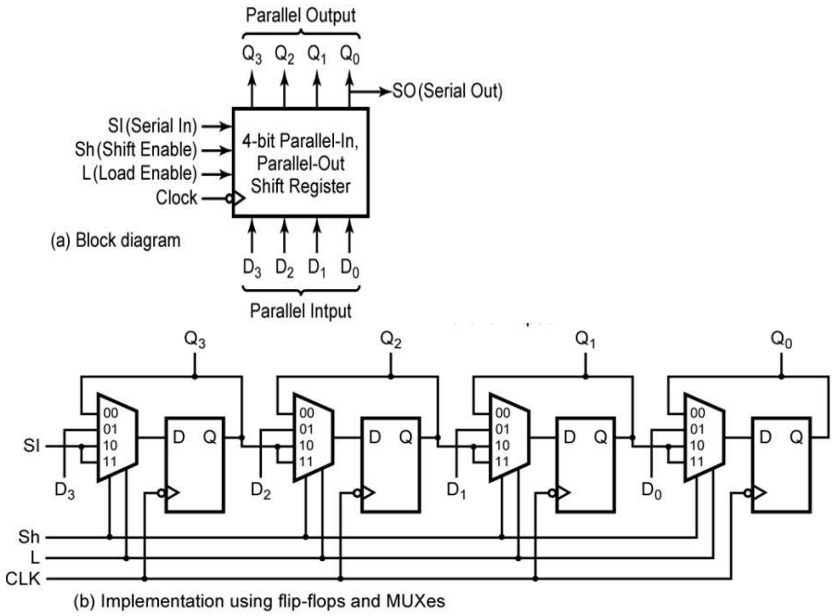
For the function of part A :

1. Write the logic expression of the function f in sum of minterms form and express the Boolean function in short notation using the Σ symbol, for example f (A, B, C) = Σ(1, 4, 5, 6, 7)

2. Write the VHDL code that represent the function using one selected signal assignment

Question 2 (20 marks)
Part A (10 marks)

The following figure shows a parallel-in parallel out right shift register, Part a is the block diagram and part b is the implementation using flip flops and multiplexers



Inputs		Next State				Action
Sh (Shift)	Ld (Load)	Q_3^+	Q_2^+	Q_1^+	Q_0^+	
0	0	Q_3	Q_2	Q_1	Q_0	no change
0	1	D_3	D_2	D_1	D_0	load
1	X	SI	Q_3	Q_2	Q_1	right shift

Show how to make the shift register reverse the order of its bits: i.e. $Q_3^+ = Q_0$, $Q_2^+ = Q_1$, $Q_1^+ = Q_2$, $Q_0^+ = Q_3$

1. Use external connections between the Q output and D inputs, what should the values of sh and L be for a reversal

2. Change the internal circuitry to allow bit reversal, so that the D inputs may be used for other purposes. Replace Sh and L with A and B and the register operate according to the following table:

Inputs A B	Next states $Q_3^+ Q_2^+ Q_1^+ Q_0^+$	Action
0 0	$Q_3 Q_2 Q_1 Q_0$	No
0 1	SI $Q_3 Q_2 Q_1$	Right shift
1 0	$D_3 D_2 D_1 D_0$	Load
1 1	$Q_0 Q_1 Q_2 Q_3$	Reverse bits

Question 2 Part B (10 marks)

Write VHDL code for an n-bit left-to-right shift register. Use GENERIC parameter N that sets the number of flip-flops.

Question 3 (20 marks):

Derive a 3-bit counter using T flip flops. The counting sequence is: 0, 4,2, 6, 1, 5, 3, 7, 0, 4 2, and so on. There is an input signal w, if w = 0 the counter stays in the same state and if w = 1 the counter will go to the next state.

(i) Show the state diagram of the counter
(ii) Show the state table of the counter
(iii) Show the transition table for the counter
(iv) Show the excitation table for the counter with T inputs
(v) Write the simplified (use k-map) logic expression for the T inputs
(vi) Draw the circuit diagram

Question 4 (20 marks):

For the following flow table:

Present State	**Next State**				Output z
	w_2w_1=00	**01**	**10**	**11**	
A	(A)	E	C	—	0
B	—	E	H	(B)	1
C	G	—	(C)	F	0
D	A	(D)	—	B	1
E	G	(E)	—	B	0
F	—	D	C	(F)	0
G	(G)	E	C	—	0
H	A	—	(H)	B	1

Part A (5 marks):

- Show the reduced table using the partitioning procedure
- Show the merger diagram for the table

Question 4 part B (5 marks)

- For the reduced table in part A, merge the compatible states
- Show the reduced flow table
- Show the relabeled flow table

Question 4 part C (10 marks)

- For the flow table in part B, show the initial transition diagram
- Modify the transition diagram to avoid any diagonals
- Show the final flow table, from the modified transition diagram
- Show the final excitation table, using a suitable state assignment.

Question 5 (20 marks):
Part A (10 marks):
All transitions between stable states in the following flow table have a Hamming distance of 2, since we are utilizing a one-hot state assignment for the table rows. We can add unstable states to try and reduce the Hamming distance by 1 for each transition from a stable state to another, passing through an unstable state. Your task is to determine the encodings of the unstable states, and the new values for the next state and output variables to reflect the addition of the unstable states. Complete the table below with your answers.

Present State	**Next State**				Output z
	w_2w_1=00	**01**	**10**	**11**	
A → 0001	(A)	(A)	C	B	0
B → 0010	—	A	D	(B)	1
C → 0100	A	D	(C)	(C)	0
D → 1000	A	(D)	(D)	B	1

Present State	**Next State**				Output z
	w_2w_1=00	**01**	**10**	**11**	
A → 0001	(A)	(A)			0
B → 0010	—			(B)	1
C → 0100			(C)	(C)	0
D → 1000		(D)	(D)		1
E → ____					
F → ____					
G → ____					
H → ____					
J → ____					

Question 5 part B (10 marks)

For the following logic circuit f(a, b, c, d), determine the static hazards. Redesign the circuit to be hazard-free and having the same output (i.e. *f*). Show the final circuit. Note that the apostrophe in the figure indicates the complemented form of the variable.