CEG 3156: Computer Systems Design (Winter 2024)
Prof. Rami Abielmona
Assignment #3: Processor Efficiency Schemes

14 February, 2024

Objective and Due Date

The objective of this assignment is to comprehend processor efficiency techniques in modern computer architectures. The due date of this assignment will be **Monday March 4, 2024 at 20:00**, to be submitted on Brightspace.

Question I

This question deals with multi-cycle processor implementation schemes.

Consider a change to the multiple-cycle implementation that alters the register file so that it has only one read port. Describe (via a diagram) any additional changes that will need to be made to the datapath in order to support this modification. Modify the finite state machine to indicate how the instructions will work, given your new datapath.

Question II

This question deals with simple pipelining techniques.

Part a

How could we modify the following code to make use of a delayed branch slot ?

```
Loop:   lw      $2, 100($3)
        addi    $3, $3, 4
        beq     $3, $4, Loop
```

Part b

For each pipeline register in Figure 4.46 on page 313, label each portion of the pipeline register with the name of the value that is loaded into the register. Determine the length of each field in bits. For example, the IF/ID pipeline register contains two fields, one of which is an instruction field that is 32 bits wide.

Question III

This question deals with processor architectures.

Pick a commercial or research processor out of the following architectural styles: CISC, RISC or VLIW. Discuss the following about your processor:

- Its history, including its founder/inventor, the year of invention and its respective place in its era;
- Its control logic implementation style;
- Its addressing modes and instruction types;
- Its instruction format;
- Its pipelining or parallelism (if any);
- Its associated compiler designs; and
- Its main applications.

Remember to relate, throughout your discussion, to the architectural style of your processor, and to emphasize its main design strengths. Do not exceed 1 type-written or 2 hand-written pages in your discussion.

Question IV

Research, then mathematically derive the *efficiency of an instruction pipeline* compared to execution without the pipeline. Assume that there are no branches in the program, and that we have a k-stage instruction pipeline and n instructions to process. Show your work, and state all your assumptions.