

Correction DGD 5 :

Correction 1 :

5-18 Binary up-down counter with enable E.

PS	mps	N.S	FF mps	
AB	EX	AB	J A K A	J B K B
00	00	00	0 X	0 X
00	01	00	0 X	0 X
00	10	11	1 X	1 X
00	11	01	0 X	1 X
01	00	01	0 X	X 0
01	01	01	0 X	X 0
01	00	00	0 X	X 1
01	11	10	1 X	X 1
10	00	10	X 0	0 X
10	01	10	X 0	0 X
10	10	01	X 1	1 X
10	11	11	X 0	1 X
11	00	11	X 0	X 0
11	01	11	X 0	X 0
11	10	00	X 0	X 1
111100		X 1	X 1	

AB      E<sup>2</sup>      00      01      11      10

JA =  $(Bx + B'x')E$

AB      E<sup>2</sup>      00      01      11      10

KA =  $(Bx + B'x')E$

AB      E<sup>2</sup>      00      01      11      10

JB = E

AB      E<sup>2</sup>      00      01      11      10

KB = E

**Correct 2 :**

Present State			Next State			D inputs		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$D_2$	$D_1$	$D_0$
0	0	0	0	1	0	0	1	0
0	0	1	x	x	x	x	x	x
0	1	0	1	0	1	1	0	1
0	1	1	0	0	0	0	0	0
1	0	0	0	1	1	0	1	1
1	0	1	1	1	1	1	1	1
1	1	0	x	x	x	x	x	x
1	1	1	1	0	0	1	0	0

- (ii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops, assume the next states of the unused combinations to be "don't care states"

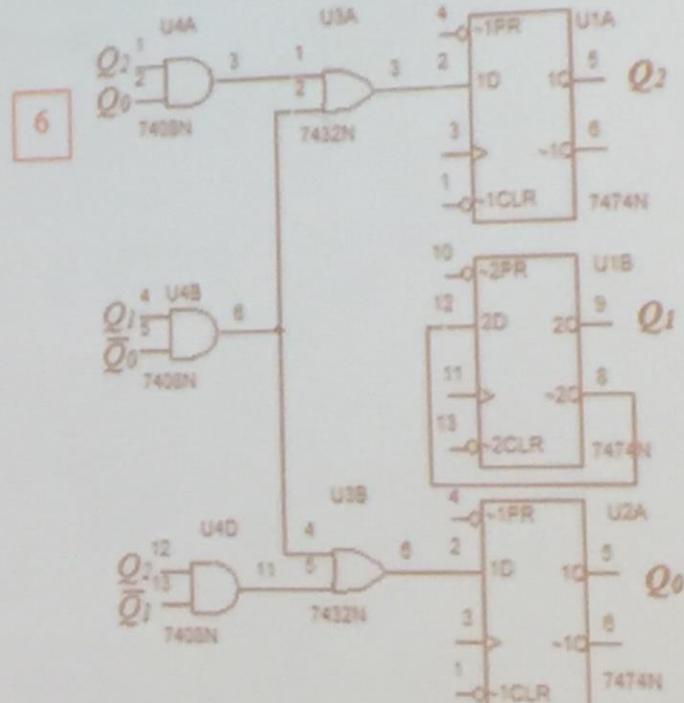
$D_2$

		D <sub>1</sub>				D <sub>0</sub>						D <sub>1</sub>			
		Q <sub>1</sub> Q <sub>0</sub>		00	01	11	10	Q <sub>1</sub> Q <sub>0</sub>		00	01	11	10		
		Q <sub>1</sub>		0	1	0	1	Q <sub>0</sub>		0	1	0	1		
		0	x	0	1	1	x	0	x	0	1	1	x		
		1	0	1	1	0	x	1	1	0	x	0	1		
2		$D_2 = Q_1 \cdot Q_0 + Q_1 \cdot \bar{Q}_0$						1	$D_1 = \bar{Q}_1$						

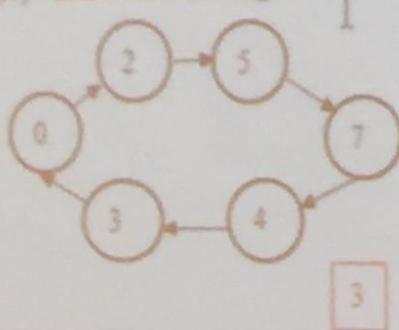
$D_1$

		D <sub>1</sub>				D <sub>0</sub>						D <sub>1</sub>			
		Q <sub>1</sub> Q <sub>0</sub>		00	01	11	10	Q <sub>1</sub> Q <sub>0</sub>		00	01	11	10		
		Q <sub>1</sub>		0	1	0	1	Q <sub>0</sub>		0	1	0	1		
		0	x	0	1	1	x	0	x	0	1	1	x		
		1	0	1	1	0	x	1	1	0	x	0	1		
2		$D_1 = Q_1 \cdot \bar{Q}_0 + Q_1 \cdot \bar{Q}_0$						1	$D_0 = Q_2 \cdot \bar{Q}_1 + Q_1 \cdot \bar{Q}_0$						

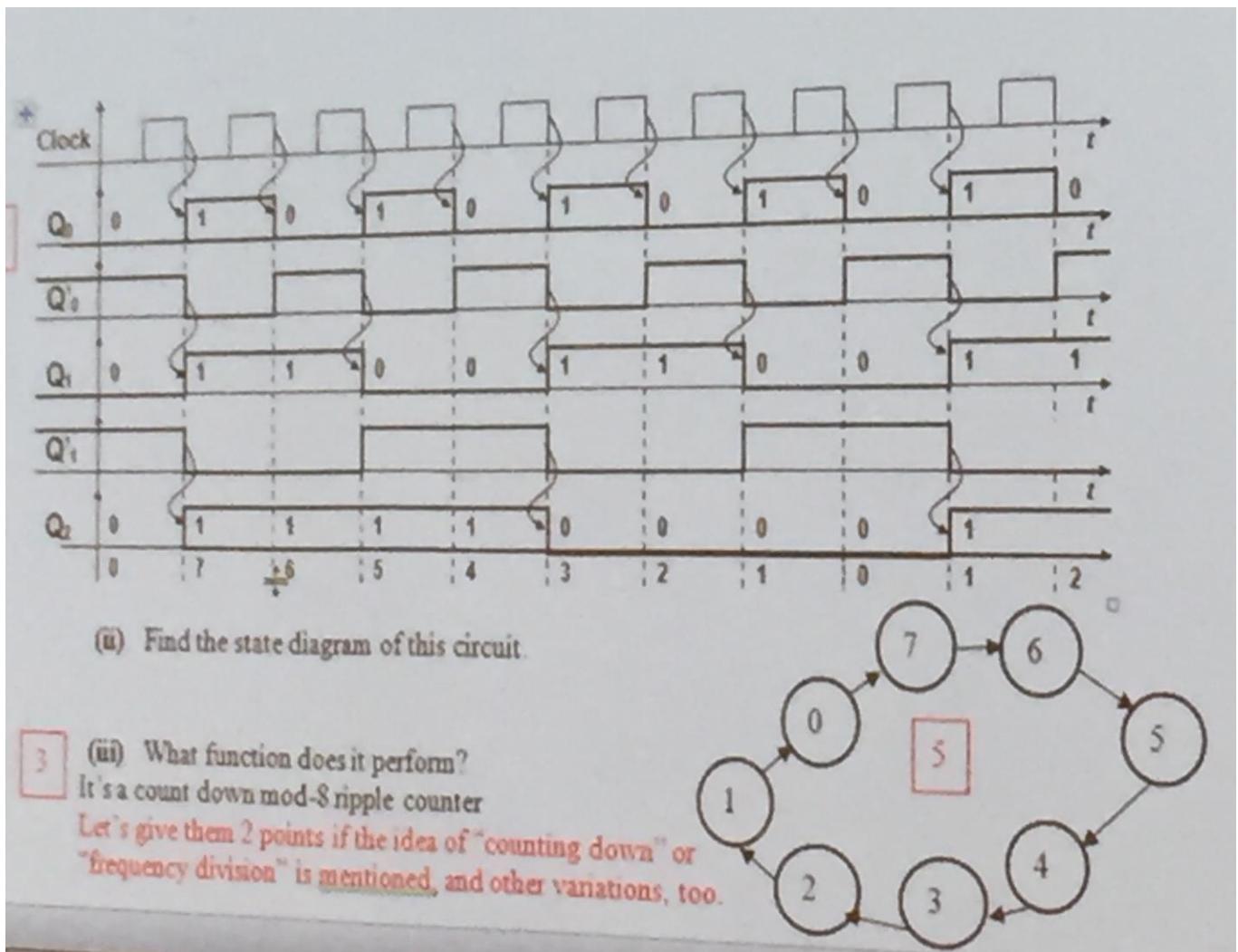
- (iii) Draw the logic diagram of the counter



- (iv) Draw the state diagram.



**Correction 3 :**



**Revision Bascule :**

### SR Latch :

S → Set  
R → Reset

Characteristic Equation:  
 $Q(t+1) = S + Q(t) \cdot \bar{R}$

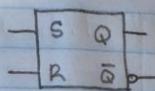
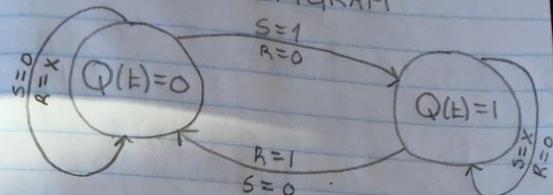
EXCITATION TABLE

$Q(t)$	$Q(t+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

BLOCK DIAGRAM →

		$Q(t+1)$	Function
0	0	$Q(t)$	Hold
0	1	0	Reset
1	0	1	Set
1	1	Ind	Forbidden (non sense)

STATE DIAGRAM



### JK Flip Flop :

Characteristic Equation:  
 $Q(t+1) = \bar{Q}(t) \cdot J + Q(t) \cdot K$

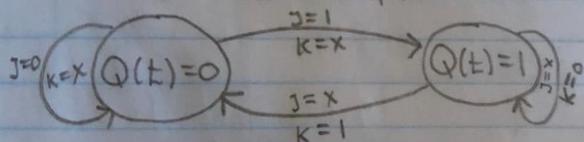
EXCITATION TABLE

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

CHARACTERISTIC TABLE

J	K	$Q(t+1)$	Function
0	0	$Q(t)$	Hold
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}(t)$	Toggle

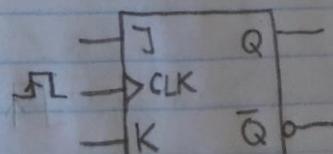
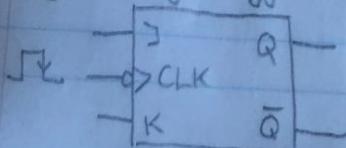
STATE DIAGRAM



BLOCK DIAGRAM → Positive Edge Triggered (rising edge)



Negative Edge Triggered (falling edge)

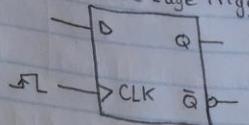


### D Flip Flop :

CHARACTERISTIC TABLE			Function	
En	D	Q(t)	Q(t+1)	
0	0	0	0	Reset
0	1	0	0	Reset
0	0	1	1	Set
1	0	1	1	Set
1	1	1	1	No change
0	X	Q(t)	Q(t)	

BLOCK DIAGRAM

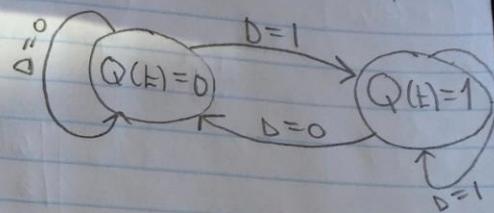
↓  
Positive Edge Triggered



EXCITATION TABLE

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

STATE DIAGRAM



Characteristic Equation :

$$Q(t+1) = D$$

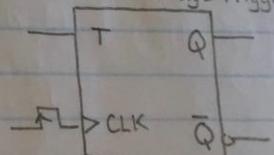
### T Flip Flop :

CHARACTERISTIC TABLE

T	Q(t)	Q(t+1)	Function
0	0	0	No change
0	1	1	No change
1	0	1	Toggle
1	1	0	Toggle

BLOCK DIAGRAM

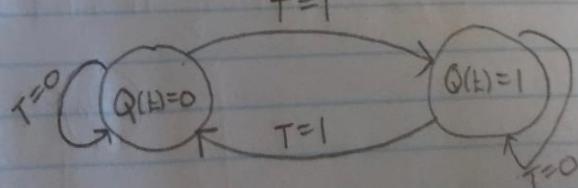
↓  
Positive Edge Triggered



Characteristic Equation:

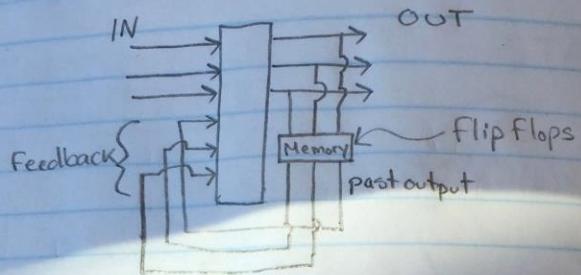
$$Q(t+1) = \bar{Q}(t) \cdot T + Q(t) \cdot \bar{T}$$

STATE DIAGRAM



## Sequential Circuits :

- output depends on the present input as well as the output of previous inputs
- Feedback signal + memory element present
- FlipFlops, counters , registers.



### Synchronous Sequential Circuit

The status of memory element is affected only at the active edge of clock if input is changed

Flip Flops are used

Clock present

### Asynchronous Sequential Circuit

The status of memory element will change anytime as soon as input is changed

Latches are used

No clock is present