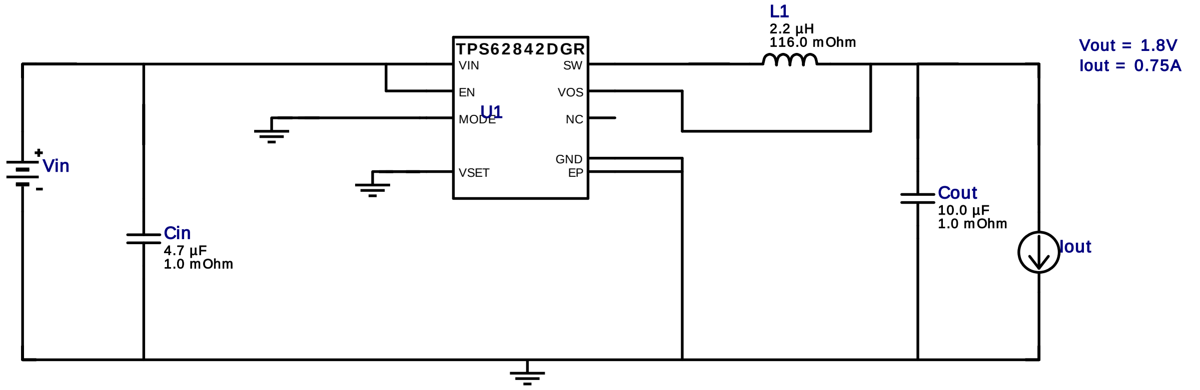
VinMin = 5.0V VinMax = 5.5V Vout = 1.8V Iout = 0.75A	Device = TPS62842DGRR Topology = Buck Created = 2025-12-16 19:04:45.546 BOM Cost = $0.91 BOM Count = 4 Total Pd = 0.28W

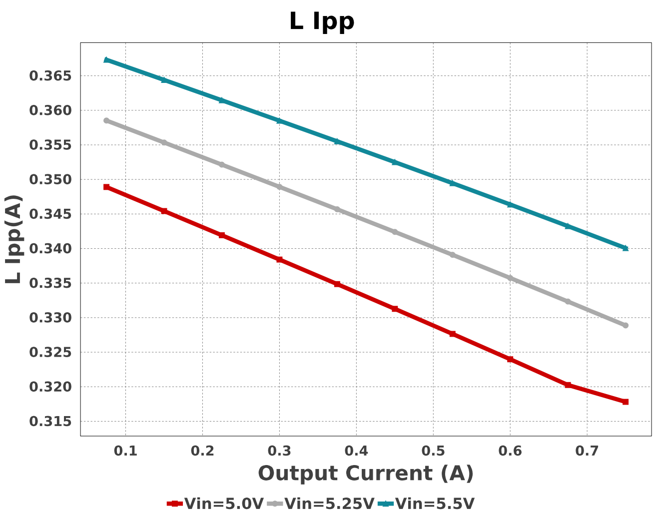
WEBENCH® Design Report

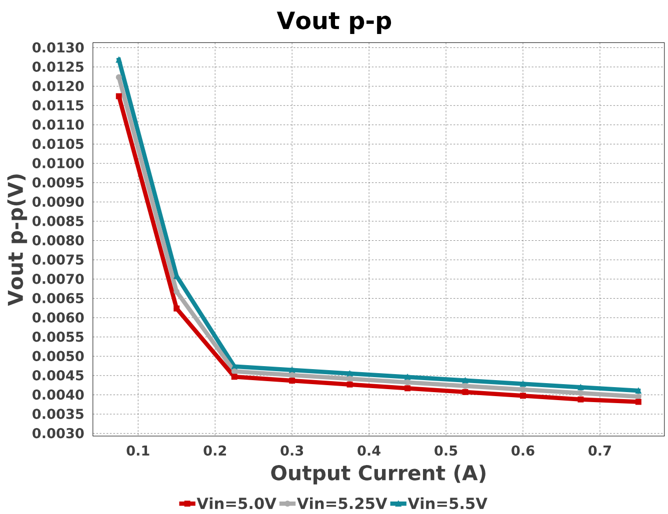
Design : 24 TPS62842DGRR
TPS62842DGRR 5V-5.5V to 1.80V @ 0.75A

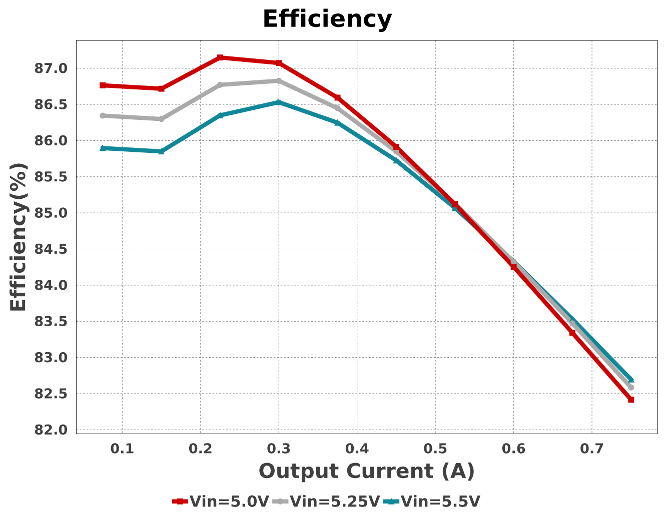


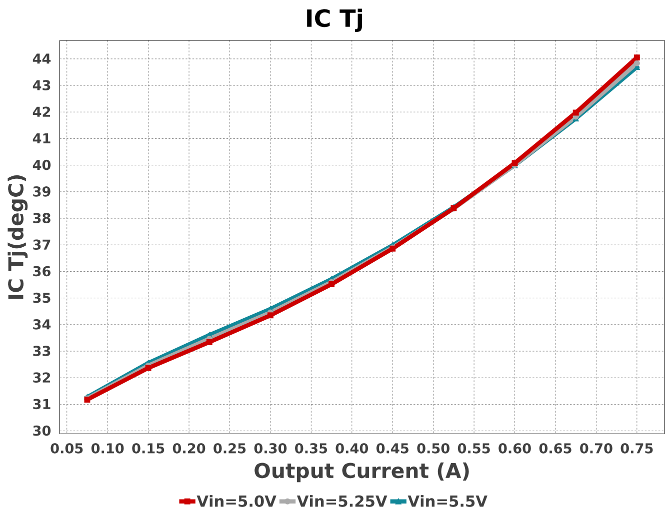
Electrical BOM

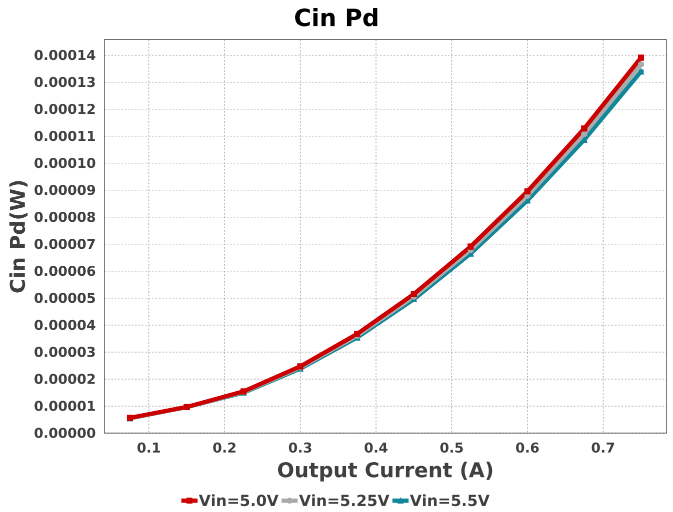
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cin	MuRata	GRM155R60J475ME87D Series= X5R	Cap= 4.7 uF ESR= 1.0 mOhm VDC= 6.3 V IRMS= 0.0 A	1	$0.01	0402_065 3 mm^2
Cout	MuRata	GRJ155R60J106ME11D Series= X5R	Cap= 10.0 uF ESR= 1.0 mOhm VDC= 6.3 V IRMS= 0.0 A	1	$0.02	0402_070 3 mm^2
L1	MuRata	DFE201612E-2R2M=P2	L= 2.2 µH 116.0 mOhm	1	$0.11	DFE201612E 8 mm^2
U1	Texas Instruments	TPS62842DGRR	Switcher	1	$0.77	DGR0008A 24 mm^2

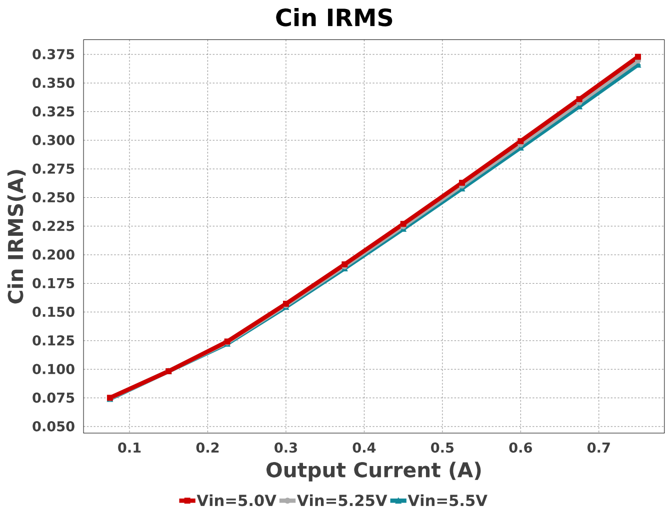


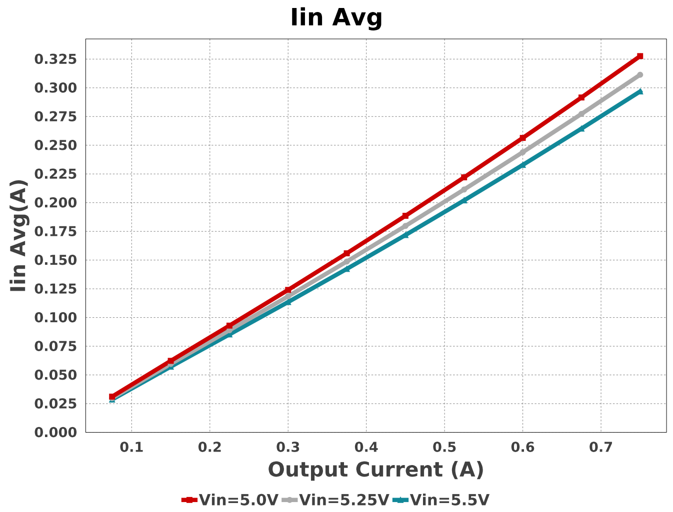


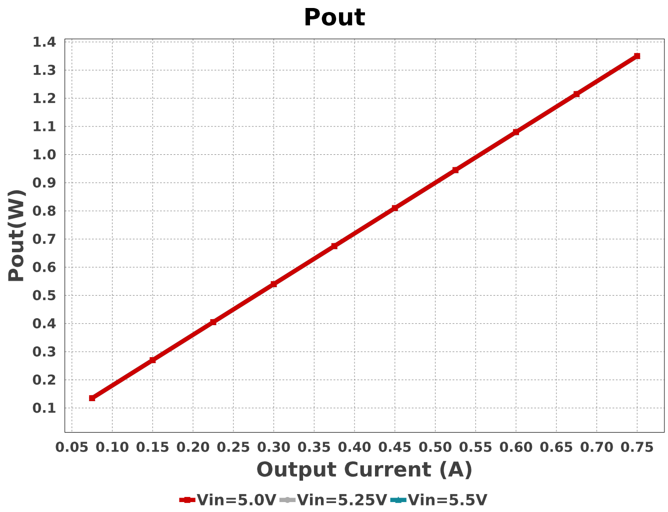

Efficiency
Efficiency(%)
Output Current (A)
Vin=5.0V Vin=5.25V Vin=5.5V


IC Tj
IC Tj(degC)
Output Current (A)
Vin=5.0V Vin=5.25V Vin=5.5V

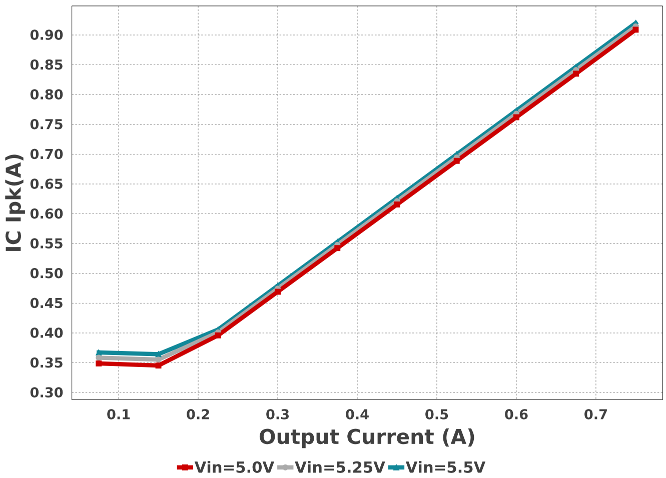

Cin Pd
Cin Pd(W)
Output Current (A)
Vin=5.0V Vin=5.25V Vin=5.5V


Cin IRMS
Cin IRMS(A)
Output Current (A)
Vin=5.0V Vin=5.25V Vin=5.5V

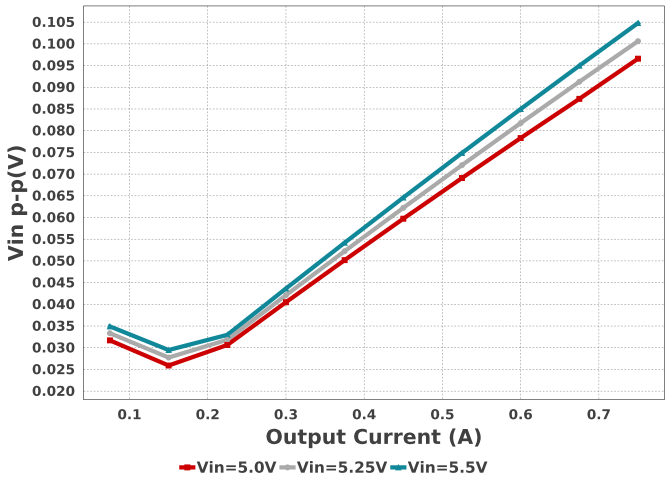

Iin Avg
Iin Avg(A)
Output Current (A)
Vin=5.0V Vin=5.25V Vin=5.5V


Pout
Pout(W)
Output Current (A)
Vin=5.0V Vin=5.25V Vin=5.5V

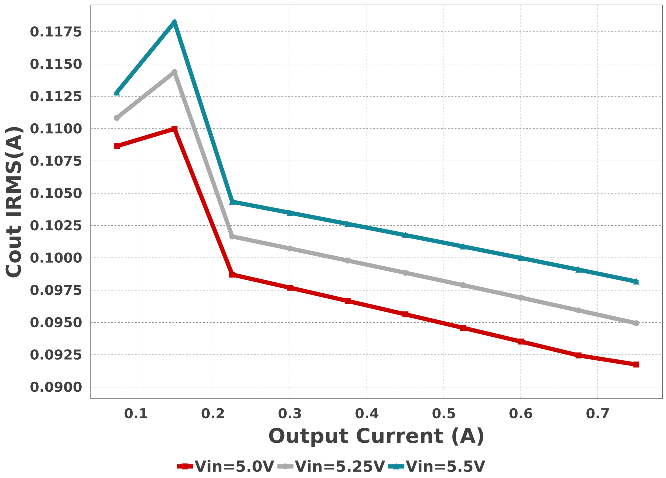
IC Ipk



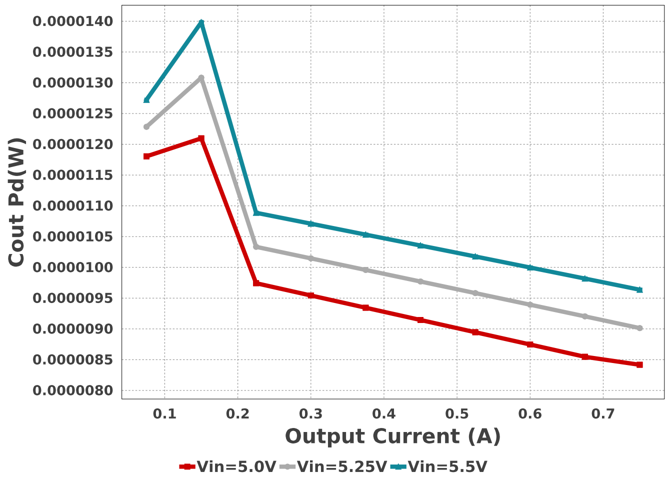
Vin p-p



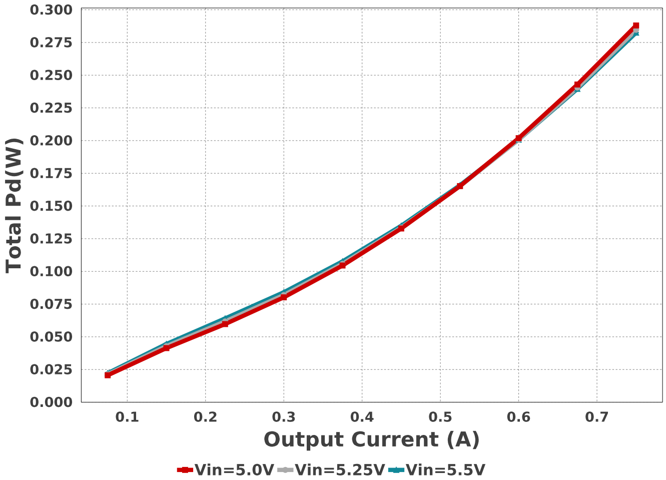
Cout IRMS



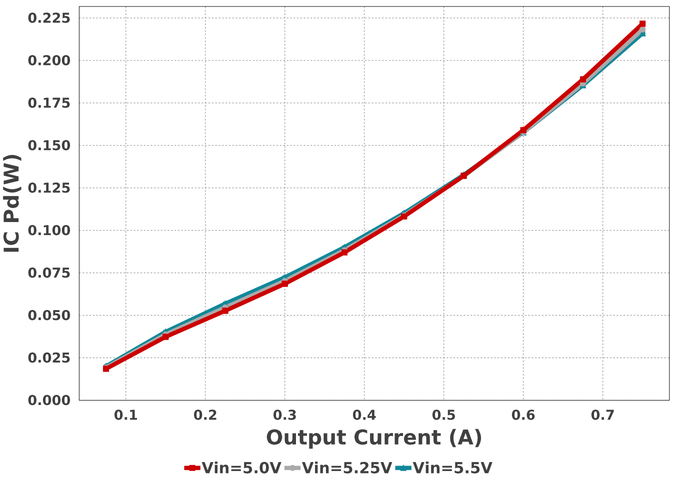
Cout Pd

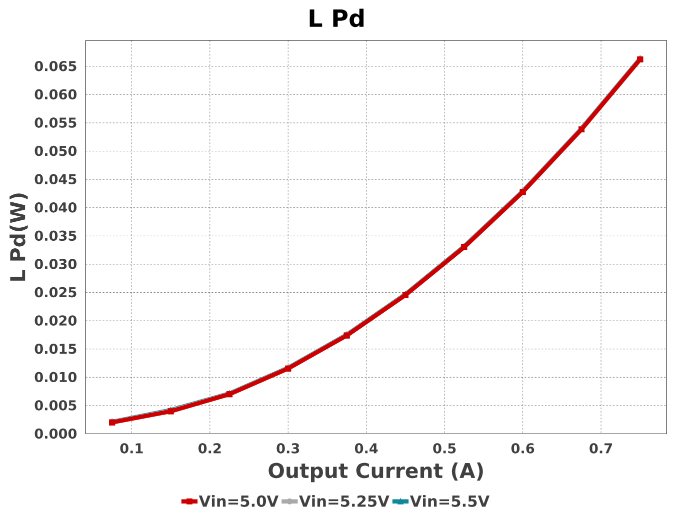


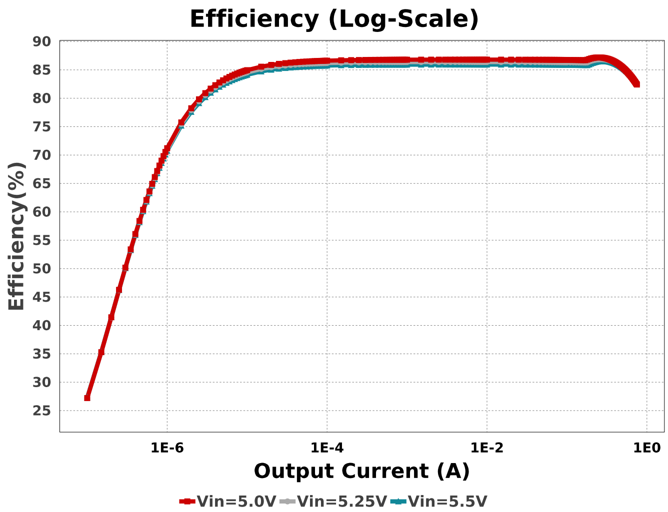
Total Pd



IC Pd







Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	365.998 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	133.95 µW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	98.168 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	9.637 µW	Capacitor	Output capacitor power dissipation
5.	IC Ipk	920.031 mA	IC	Peak switch current in IC
6.	IC Pd	216.0 mW	IC	IC power dissipation
7.	IC Tj	43.694 degC	IC	IC junction temperature
8.	ICThetaJA	63.4 degC/W	IC	IC junction-to-ambient thermal resistance
9.	Iin Avg	296.82 mA	IC	Average input current
10.	L Ipp	340.063 mA	Inductor	Peak-to-peak inductor ripple current
11.	L Pd	66.368 mW	Inductor	Inductor power dissipation
12.	Cin Pd	133.95 µW	Power	Input capacitor power dissipation
13.	Cout Pd	9.637 µW	Power	Output capacitor power dissipation
14.	IC Pd	216.0 mW	Power	IC power dissipation
15.	L Pd	66.368 mW	Power	Inductor power dissipation
16.	Total Pd	282.506 mW	Power	Total Power Dissipation
17.	BOM Count	4	System Information	Total Design BOM count
18.	Duty Cycle	36.54 %	System Information	Duty cycle
19.	Efficiency	82.695 %	System Information	Steady state efficiency
20.	FootPrint	37.0 mm^2	System Information	Total Foot Print Area of BOM components
21.	Frequency	1.66 MHz	System Information	Switching frequency
22.	Iout	750.0 mA	System Information	Iout operating point
23.	Mode	CCM	System Information	Conduction Mode
24.	Pout	1.35 W	System Information	Total output power
25.	Total BOM	$0.909	System Information	Total BOM Cost
26.	Vin	5.5 V	System Information	Vin operating point
27.	Vin p-p	104.79 mV	System Information	Peak-to-peak input voltage
28.	Vout	1.8 V	System Information	Operational Output Voltage
29.	Vout Tolerance	1.5 %	System Information	Vout Tolerance (full load)
30.	Vout p-p	4.108 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	750.0 m	Maximum Output Current
VinMax	5.5	Maximum input voltage
VinMin	5.0	Minimum input voltage
Vout	1.8	Output Voltage

Name	Value	Description
base_pn	TPS62842	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

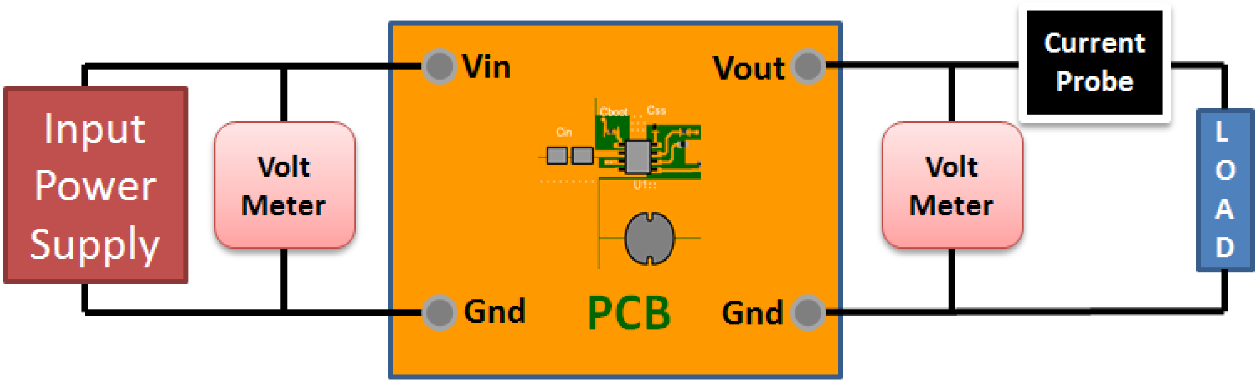
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 5.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : 49E76D69039D26F6[v1]

2. **TPS62842** Product Folder : http://www.ti.com/product/TPS62840 : contains the data sheet and other resources.

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