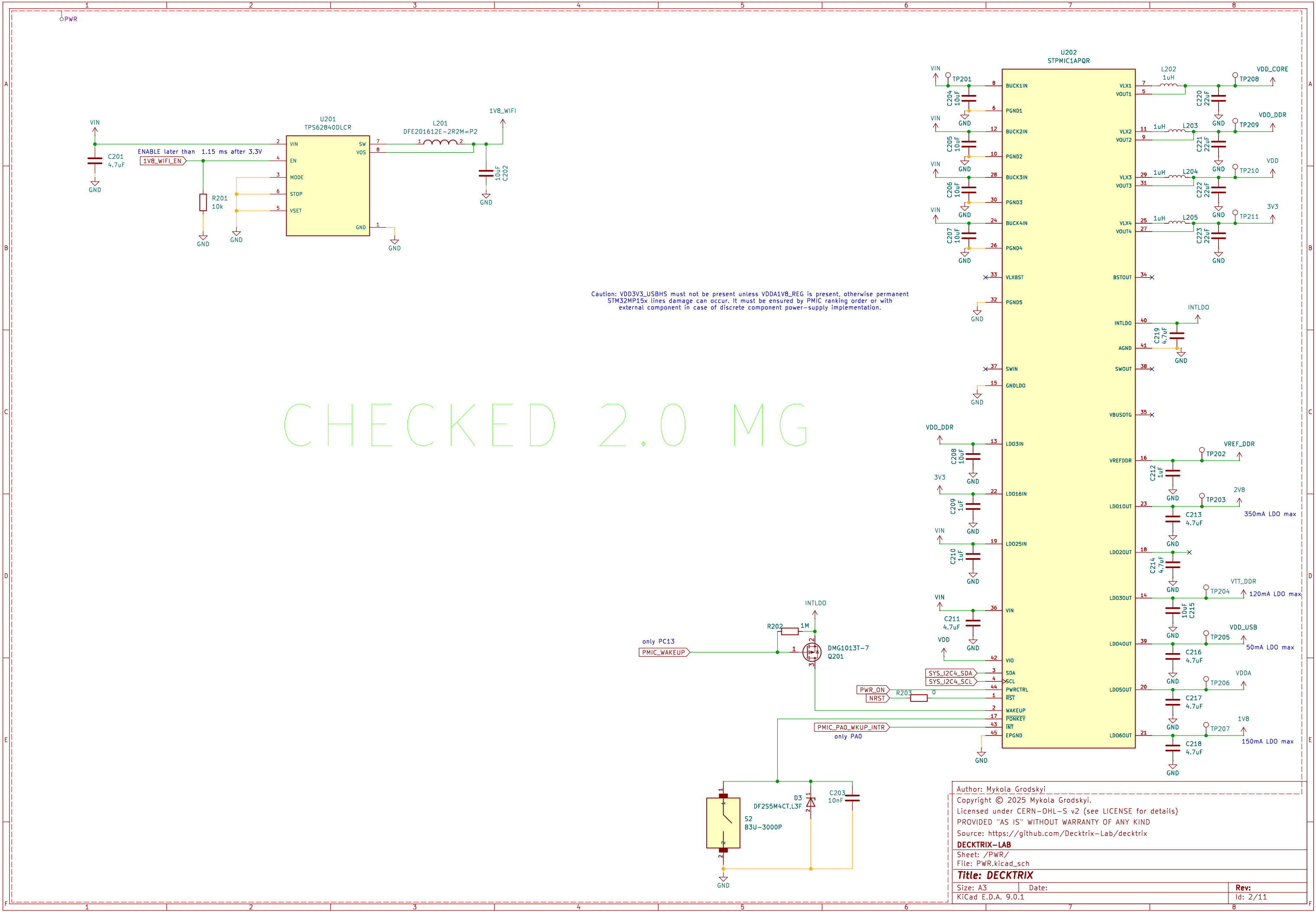
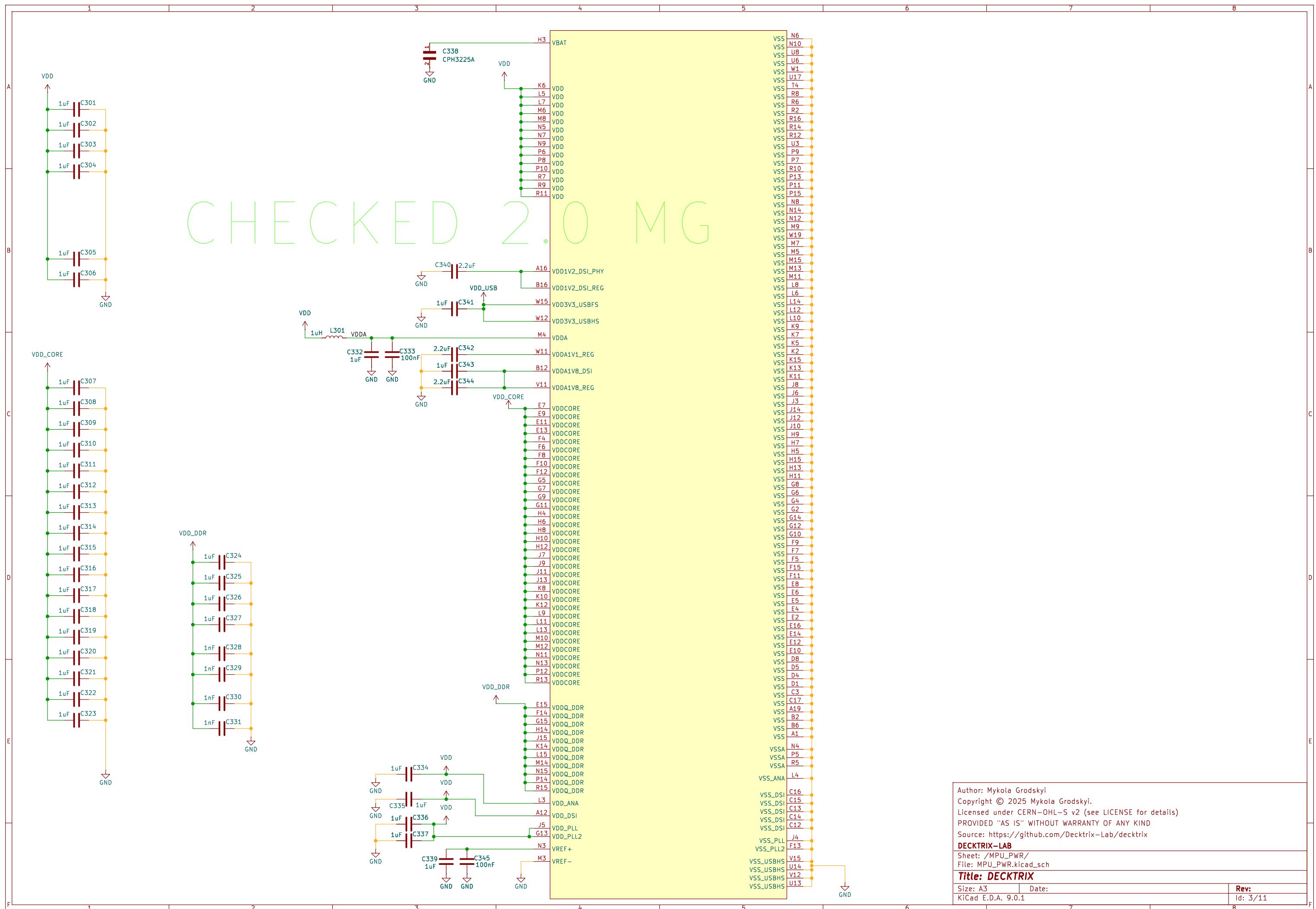
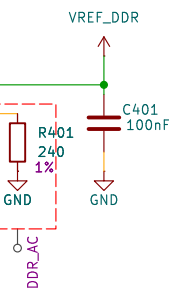
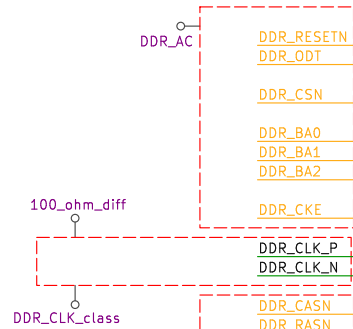
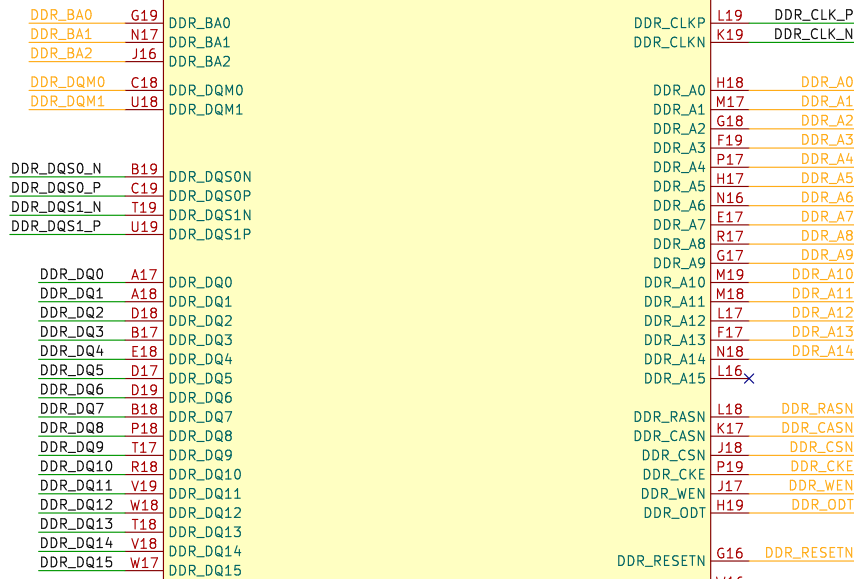


<b>DECKTRIX-LAB</b>		
Sheet: /		
File: MPU_MOD.kicad_sch		
<b>Title: DECKTRIX</b>		
Size: A3	Date:	<b>Rev:</b>
KiCad E.D.A. 9.0.1		Id: 1/11

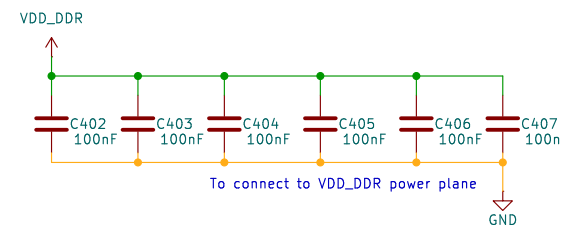
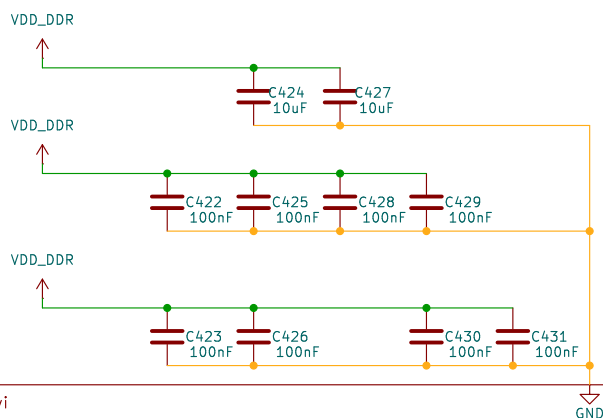
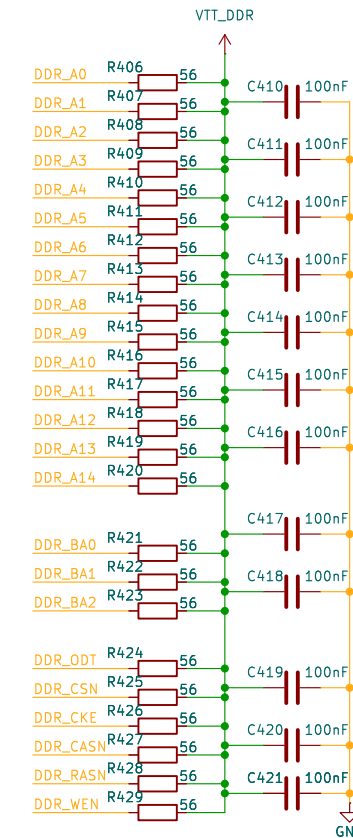
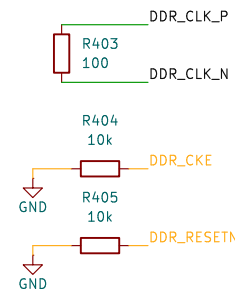
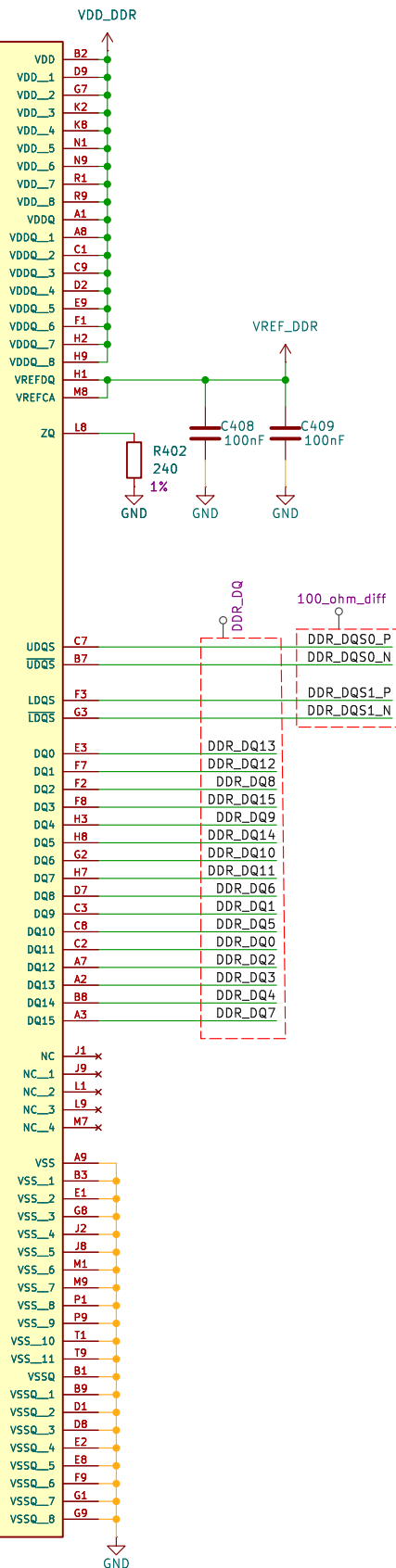


CHECKED 2.0 MG





U402  
MT41K256M16TW-107\_P  
P  
IPC-7351B  
1.20mm



55 Ohm impedance for  
single-end signals  
100 Ohm impedance for  
differential signals

Length of DQS\_N/DQS\_P must  
be from 0 to 590 mils (14.986  
mm) shorter than  
CLK\_N / CLK\_P length  
(CLK\_N/CLK\_P must be the  
longest traces).

• The PCB bottom layer must  
be used for A/C distribution to  
memory devices. The top  
layer is reserved for  
connections to the memory  
chip (stubs) and A/C bus  
crossing.

Length of A/C must be from  
0 to 40 mils (1.016 mm)  
shorter than CLK\_N / CLK\_P  
length

CLK\_N / CLK\_P maximum  
length 4.72 inch (12 cm)

CHECKED 2.0 MG

Author: Mykola Grodskiy  
Copyright © 2025 Mykola Grodskiy.  
Licensed under CERN-OHL-S v2 (see LICENSE for details)  
PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND  
Source: <https://github.com/Decktrix-Lab/decktrix>

DECKTRIX-LAB

Sheet: /DDR/  
File: DDR.kicad\_sch

Title: DECKTRIX

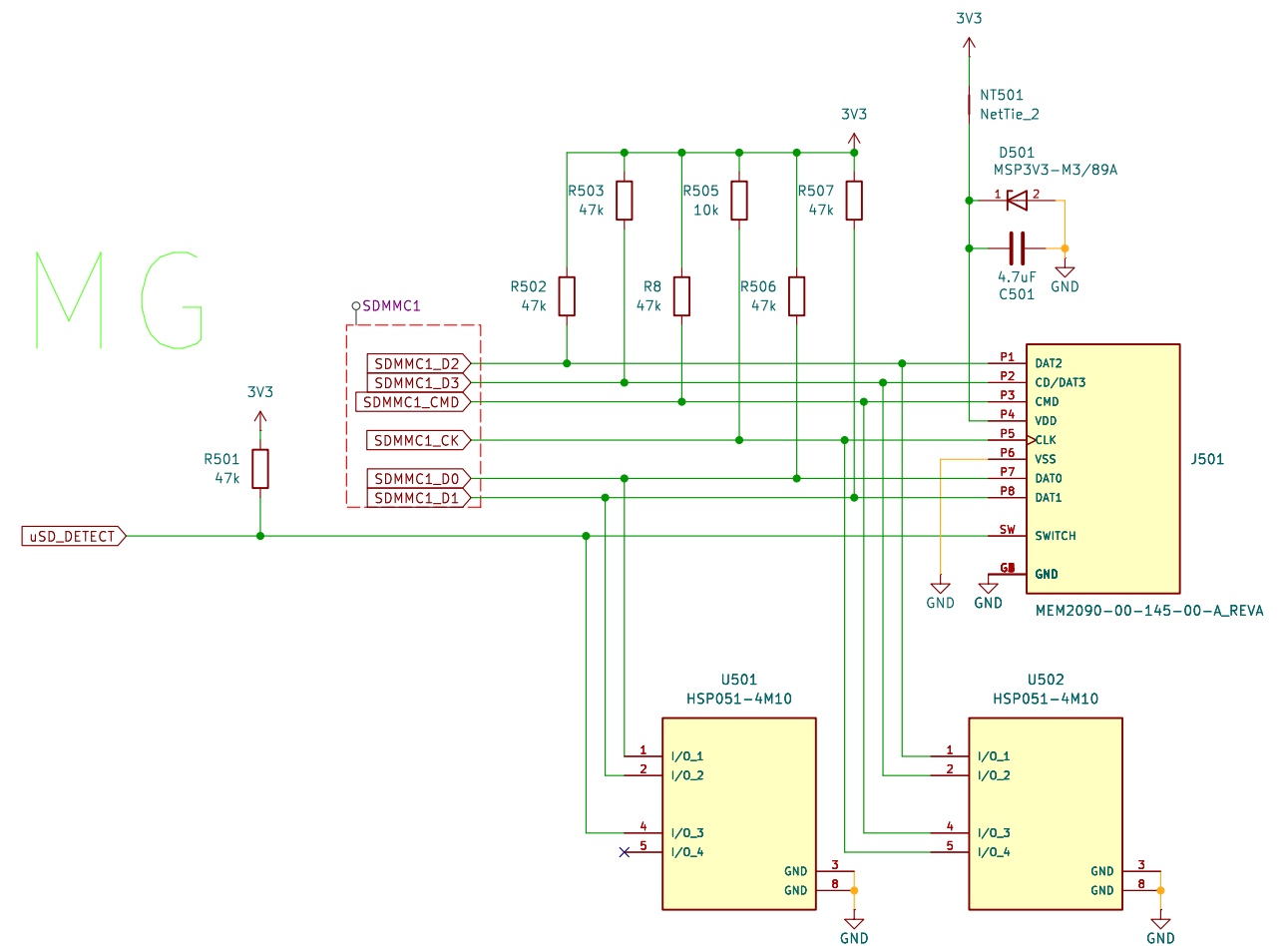
Size: A3

Date:

Rev:

KiCad E.D.A. 9.0.1

Id: 4/11



Author: Mykola Grodskyi  
Copyright © 2025 Mykola Grodskyi.  
Licensed under CERN-OHL-S v2 (see LICENSE for details)  
PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND  
Source: <https://github.com/Decktrix-Lab/decktrix>

**DECKTRIX-LAB**

Sheet: /FLASH\_SD/  
File: FLASH\_SD.kicad\_sch

**Title:** DECKTRIX

Size: A3

KiCad E.D.A. 9.0.1


Date:

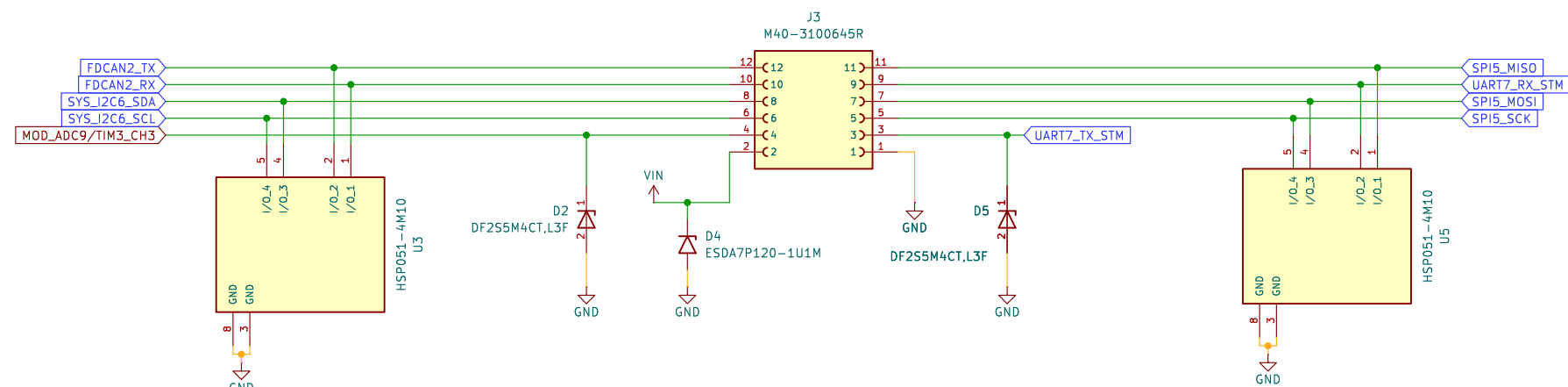
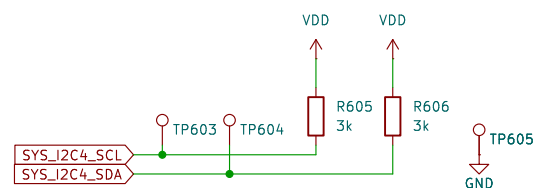
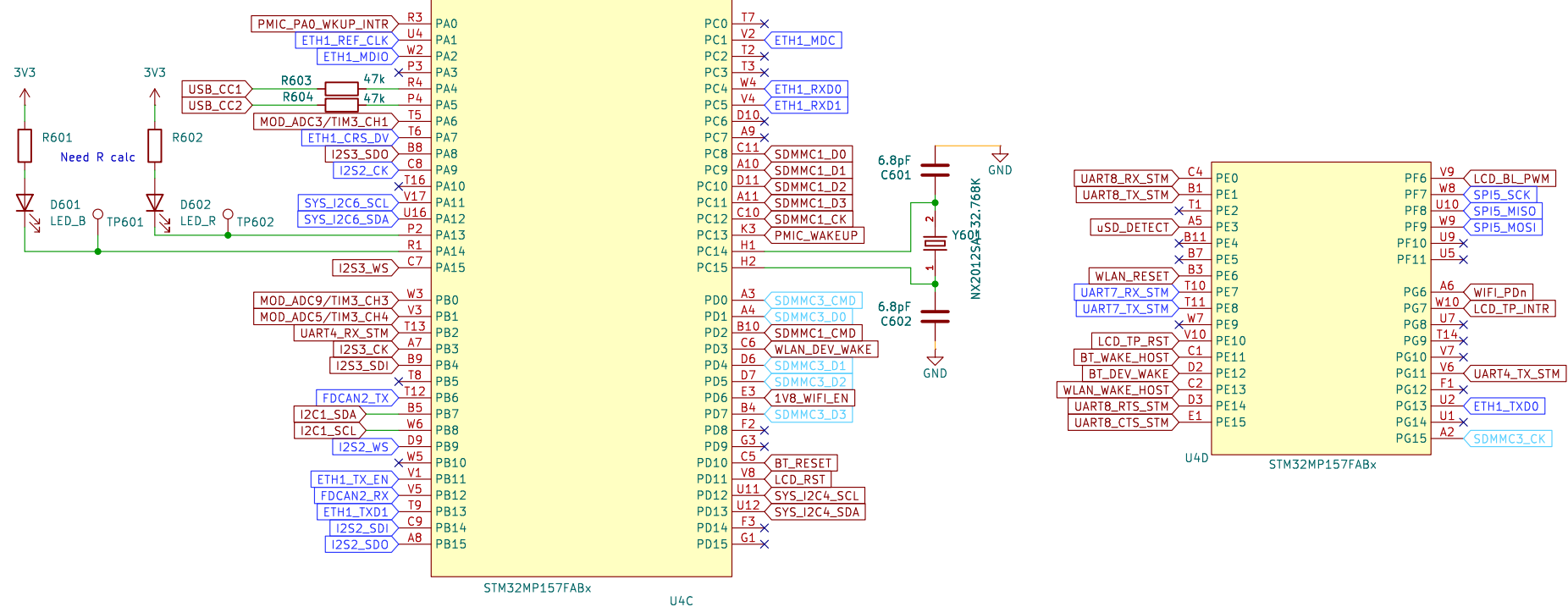
1

---

Rev:

5/11

---



SYS_I2C4_SDA	PD13	U12
SYS_I2C4_SCL	PB6	T12
SDMMC1_D0	PC8	C11
SDMMC1_D1	PC9	A10
SDMMC1_D2	PC10	D11
SDMMC1_D3	PC11	A11
SDMMC1_CK	PC12	C10
SDMMC1_CMD	PD2	B10
SDMMC2_D0	PB14	C9
SDMMC2_D1	PB15	A8
SDMMC2_D2	PB3	A7
SDMMC2_D3	PB4	B9
SDMMC2_D4	PA8	B8
SDMMC2_D5	PA9	C8
SDMMC2_D6	PE5	B7
SDMMC2_D7	PD3	C6
SDMMC2_CK	PE3	A5
SDMMC2_CMD	PG6	A6
SDMMC3_D0	PD1	A4
SDMMC3_D1	PD4	D6
SDMMC3_D2	PD5	D7
SDMMC3_D3	PD7	B4
SDMMC3_CK	PG15	A2
SDMMC3_CMD	PD0	A3
UART4_TX_STM	PG11	V6
UART4_RX_STM	PB2	T13
UART8_TX_STM	PE1	B1
UART8_RX_STM	PE0	C4
UART8_CTS_STM	PE15	F1
UART8_RTS_STM	PE14	D3
I2S2_SDI	PB14	T5
I2S2_CK	PA9	P4
I2S2_WS	PB9	R4
I2S2_SDO	PB15	T6
I2S3_SDI	PB4	T2
I2S3_CK	PB3	W5
I2S3_WS	PA15	V5
I2S3_SDO	PA8	B8
UART7_RX_STM	PE7	T10
UART7_TX_STM	PE8	T11
SYS_I2C6_SDA	PA12	U16
SYS_I2C6_SCL	PA11	V17
FDCAN2_RX	PB12	V5
FDCAN2_TX	PB6	T12

[illegible]

Author: Mykola Grodyski  
Copyright © 2025 Mykola Grodyski.  
Licensed under CERN-OHL-S v2 (see LICENSE for details)  
PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND  
Source: <https://github.com/Decktrix-Lab/decktrix>

DECKTRIX-LAB

Sheet: /IO\_Perph\_Conn/  
File: IO\_Perph\_Conn.kicad\_sch

**Title:** DECKTRIX

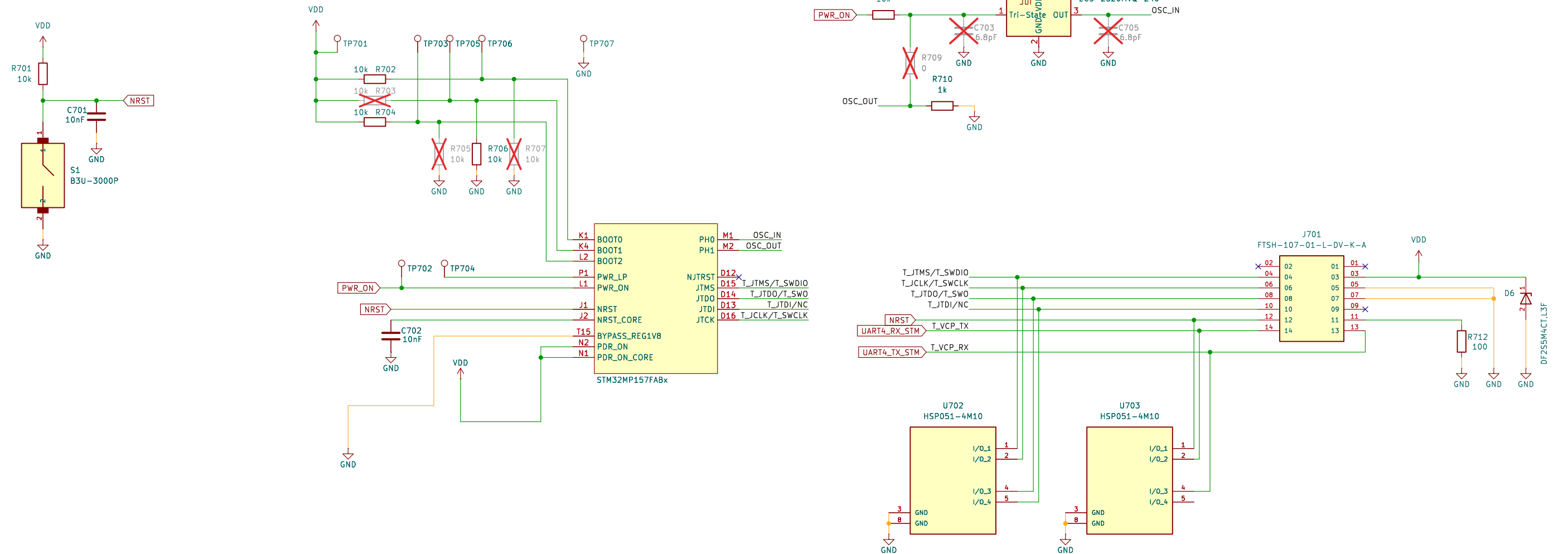
Size: A3

Date:

Rev:

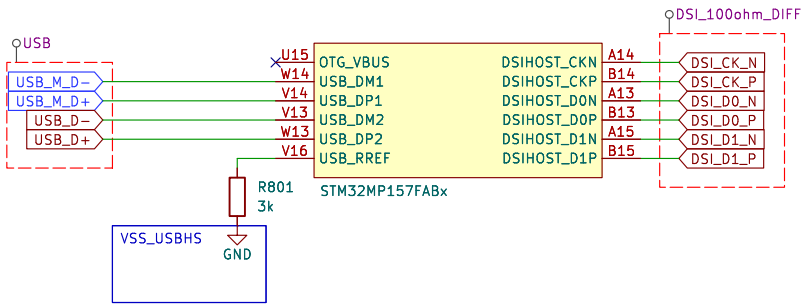
Id: 6/11

CHECKED 2.0 MG



Author: Mykola Grodskiy  
Copyright © 2025 Mykola Grodskiy.  
Licensed under CERN-OHL-S v2 (see LICENSE for details)  
PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND  
Source: <https://github.com/Decktrix-Lab/decktrix>  
**DECKTRIX-LAB**  
Sheet: /RCC\_BOOT\_RST\_DEBUG/  
File: RCC\_BOOT\_RST\_DEBUG.kicad\_sch  
**Title: DECKTRIX**  
Size: A3 Date: Rev:  
KiCad E.D.A. 9.0.1 Id: 7/11

CHECKED 2.0 MG









CHECKED 2.0 MG

