NOTES:

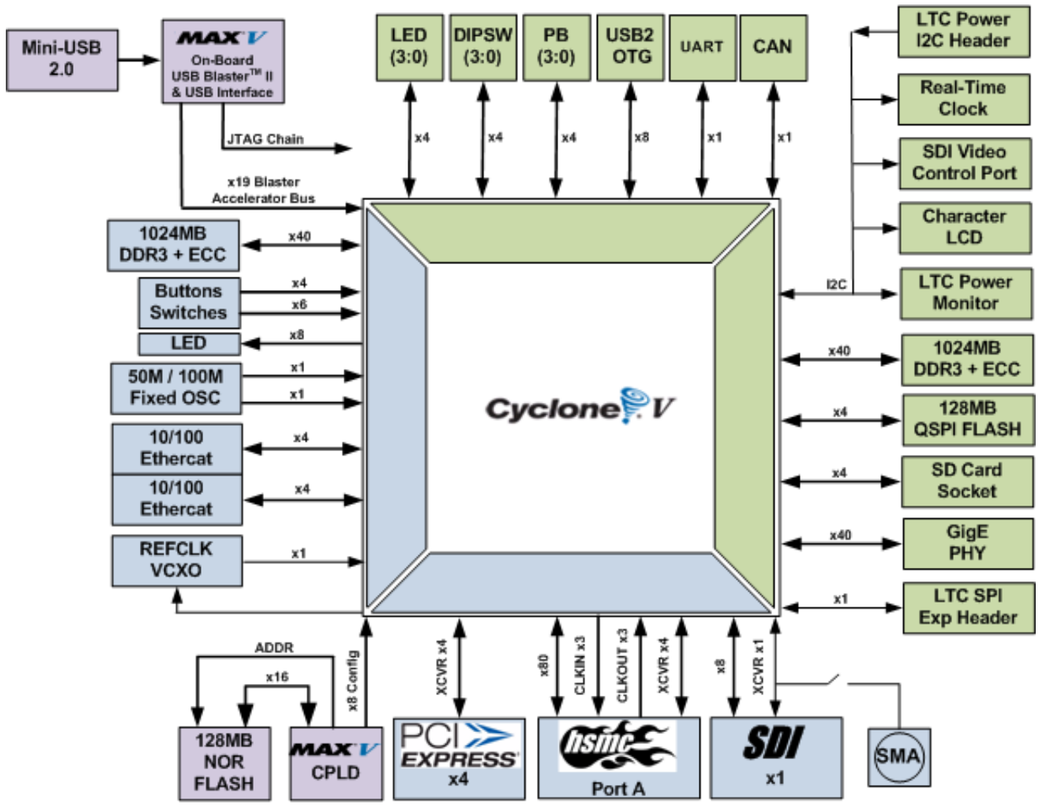
1. Project Drawing Numbers:

Raw PCB	100-0321003-D1
Gerber Files	110-0321003-D1
PCB Design Files	120-0321003-D1
Assembly Drawing	130-0321003-D1
Fab Drawing	140-0321003-D1
Schematic Drawing	150-0321003-D1
PCB Film	160-0321003-D1
Bill of Materials	170-0321003-D1
Schematic Design Files	180-0321003-D1
Functional Specification	210-0321003-D1
PCB Layout Guidelines	220-0321003-D1
Assembly Rework	320-0321003-D1

2. 1543 Parts, 88 Library Parts, 1330 Nets, 6643 Pins

Preliminary Schematic
DO NOT COPY

Cyclone V SoC FPGA Development Kit Board



REV	DATE	PAGES	DESCRIPTION
D1	07/29/2013	All	INITIAL REVISION A RELEASE

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diag, Rev. History	30	Power 3 - 1.5V FPGA
2	FPGA Package Top	31	Power 3 - 2.5V FPGA
3	PCI Express Edge Connector	32	Power 3 - 2.5V HPS
4	Cyclone V GX SoC Bank 3,4	33	Power 3 - 1.5V & 1.5V HPS
5	Cyclone V GX SoC Bank 5,6	34	Power 3 - 3.3V HPS
6	Cyclone V GX SoC Bank 7	35	Power 1.1V_HPS , 5.0V , 1.8V
7	Cyclone V GX SoC Bank 8	36	Power 4 - Linear Regulators
8	Cyclone V GX SoC Transceiver Banks	37	Power 6 - Power & Temp Monitor
9	Cyclone V GX SoC Clocks	38	CycloneV GX SOC Power
10	PLL	39	CycloneV GX SOC Ground
11	Cyclone V GX SoC Configuration	40	Decoupling
12	JTAG	41	Changes History
13	1024MB DDR3 (x32) - FPGA		
14	1024MB DDR3 (x32 + ECC) - HPS		
15	FLASH , EPCQ		
16	5M2210 System Controller		
17	HSMC PORT A		
18	10/100/1000 Ethernet - HPS		
19	10/100M Ethernet - FPGA		
20	SDI Cable Driver , SMA & SMB		
21	QSPI FLASH & RESET Circuit		
22	USB2.0 & Micro SD Card		
23	User I/O , RTC		
24	UART , CAN		
25	On - Board USB Blaster II		
26	FPGA Power Monitor		
27	HPS Power Monitor		
28	Power 1 - DC I/P & 12V , 3.3V O/P		
29	Power 2		

PCI EXPRESS®

ALTERA®

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone V SoC FPGA Development Kit Board

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

Date: Tuesday, October 15, 2013 Sheet 1 of 41

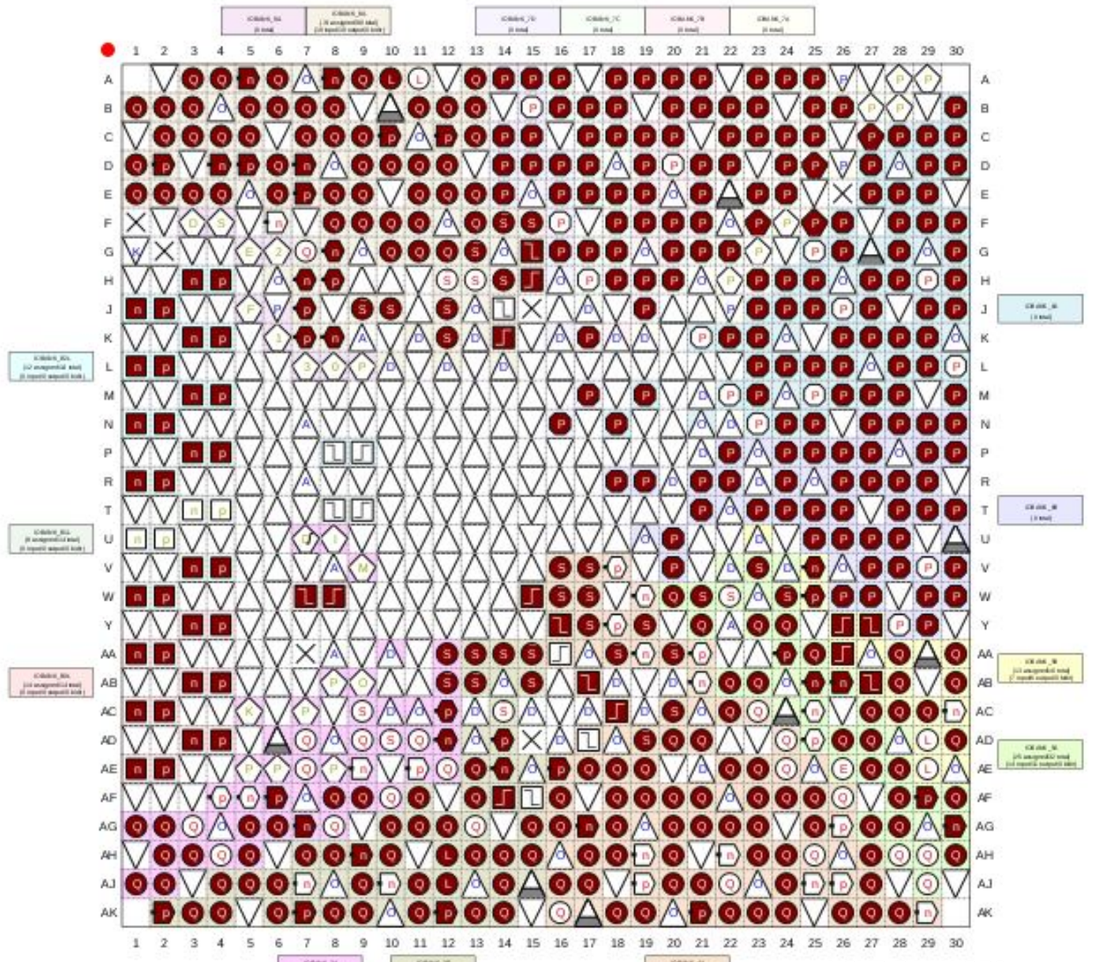
FPGA Package Top View

I/O Bank Usage

	I/O Bank	Usage	VCCIO Voltage	VREF Voltage	VCCPD Voltage
1	B2L	0 / 14 (0 %)	--	--	--
2	B1L	0 / 14 (0 %)	--	--	--
3	B0L	0 / 14 (0 %)	--	--	--
4	3A	28 / 32 (88 %)	2.5V	--	2.5V
5	3B	43 / 48 (90 %)	1.5V	0.75V	2.5V
6	4A	58 / 80 (73 %)	1.5V	0.75V	2.5V
7	5A	25 / 32 (78 %)	2.5V	--	2.5V
8	5B	13 / 16 (81 %)	2.5V	--	2.5V
9	6B	34 / 45 (76 %)	1.5V	0.75V	2.5V
10	6A	48 / 57 (84 %)	1.5V	0.75V	2.5V
11	7A	19 / 19 (100 %)	3.3V	--	3.3V
12	7B	20 / 22 (91 %)	3.3V	--	3.3V
13	7C	12 / 12 (100 %)	3.3V	--	3.3V
14	7D	12 / 14 (86 %)	3.3V	--	3.3V
15	8A	74 / 80 (93 %)	2.5V	--	2.5V

Top View - Wire Bond

Cyclone V - 5CSXFC6D6F31C7



XCVR BANK QR2

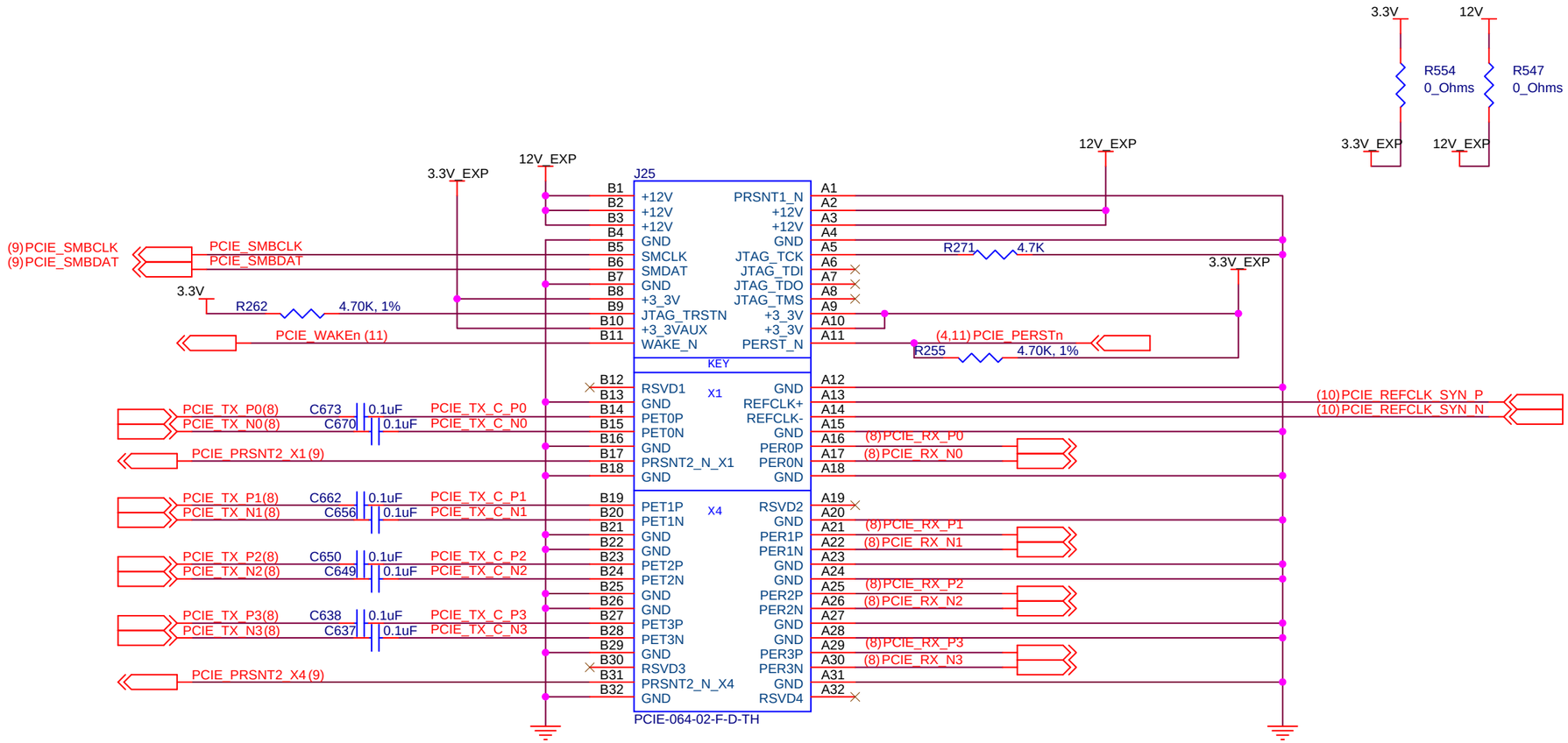
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

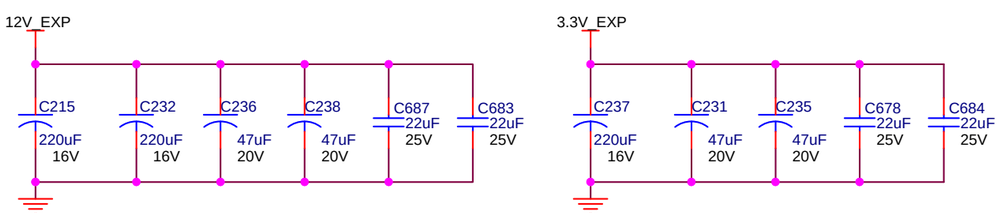
Title: Cyclone V SoC FPGA Development Kit Board

Size: B | Document Number: 150-0321003-D1 (6XX-44184R) | Rev: D1

Date: Tuesday, October 15, 2013 | Sheet 2 of 41

PCI Express Connector





Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title: Cyclone V SoC FPGA Development Kit Board		
Size: B	Document Number: 150-0321003-D1 (6XX-44184R)	Rev: D1
Date: Tuesday, October 15, 2013	Sheet 3 of 41	

Cyclone V GX SoC Bank 3 & 4

(5,19) ENET2_TX_D[3..0]

(5,19) ENET2_RX_D[3..0]

(19,21) ENET_DUAL_RESETn

U21A

CYCLONE V GX SoC BANK 3

Bank 3A
2.5 Volt

HSMA_D0	AF9	DIFFIO_TX_B8p,DQ1B	AG5	(19) P0TXERR	
HSMA_D1	AF8		AH5	(19) P1TXERR	
HSMA_D2	AG7	DIFFIO_TX_B9p,DQ2B	AJ1		
HSMA_D3	AG1	DIFFIO_TX_B9n	AJ2	HSMA_CLK_OUT_P1	
HSMA_SDA	AH2	DIFFIO_RX_B10p,DQ2B	AC12	HSMA_CLK_OUT_N1	
HSMA_SCL	AA12	DIFFIO_RX_B10n,DQ2B	AD12	HSMA_PRSNTn	
SDI_CLK148_UP (8)	AB12	DIFFIO_RX_B11p,DQS2B	AG2	HSMA_CLK_IN_P1	
SDI_CLK148_DN (8)	AF6	DIFFIO_RX_B11n,DQSn2B	AH3	HSMA_CLK_IN_N1	
PCIE_PERSTn	AG6	DIFFIO_TX_B12p			
		DIFFIO_TX_B12n,DQ2B			

		DIFFIO_TX_B13p,DQ2B			
		DIFFIO_TX_B13n,DQ2B			
		DIFFIO_RX_B14p,DQ2B			
		DIFFIO_RX_B14n,DQ2B			
		DIFFIO_RX_B15p			
		DIFFIO_RX_B15n			
		DIFFIO_TX_B16p,DQ2B			
		DIFFIO_TX_B16n,DQ2B			

Bank 3B
1.5 Volt

USER_DIPSW_FPGA0	AG10	DIFFIO_TX_B17p,DQ3B	DIFFIO_RX_B27p,DQS4B,B_CS#_0	AB15	DDR3_FPGA_CSn
USER_DIPSW_FPGA1	AH9	DIFFIO_TX_B17n	DIFFIO_RX_B27n,DQSn4B,B_CS#_1	AC14	
USER_DIPSW_FPGA2	AF11	DIFFIO_RX_B18p,DQ3B	DIFFIO_TX_B28p,B_A_12	AK7	DDR3_FPGA_A12
USER_DIPSW_FPGA3	AG11	DIFFIO_RX_B18n,DQ3B	DIFFIO_TX_B28n,DQ4B,B_A_13	AK8	DDR3_FPGA_A13
USER_PB_FPGA0	AA13	DIFFIO_RX_B19p,DQS3B	DIFFIO_TX_B29p,DQ4B,B_A_10	AJ9	DDR3_FPGA_A10
USER_PB_FPGA1	AB13	DIFFIO_RX_B19n,DQSn3B	DIFFIO_TX_B29n,DQ4B,B_A_11	AK9	DDR3_FPGA_A11
USER_LED_FPGA0	AK2	DIFFIO_TX_B20p	DIFFIO_RX_B30p,DQ4B,B_A_8	AH13	DDR3_FPGA_A8
USB_FULL	AK3	DIFFIO_RX_B20n,DQ3B	DIFFIO_RX_B30n,DQ4B,B_A_9	AH14	DDR3_FPGA_A9
USB_EMPTY	AJ4	DIFFIO_TX_B21p,DQ3B	DIFFIO_TX_B32p,DQ4B,B_CAS#	AH7	DDR3_FPGA_CASn
USB_SCL	AK4	DIFFIO_TX_B21n,DQ3B	DIFFIO_TX_B32n,DQ4B,B_RAS#	AH8	DDR3_FPGA_RASn
USB_SDA	AE13	DIFFIO_RX_B22p,DQ3B	DIFFIO_TX_B33p,DQ5B,B_BA_0	AH10	DDR3_FPGA_BA0
USB_B2_CLK	AF13	DIFFIO_RX_B22n,DQ3B	DIFFIO_TX_B33n,GND	AJ10	
USB_RESETn	AD14	DIFFIO_RX_B23p	DIFFIO_RX_B34p,DQ5B,B_BA_1	AJ11	DDR3_FPGA_BA1
USB_OEn	AE14	DIFFIO_RX_B23n	DIFFIO_RX_B34n,DQ5B,B_BA_2	AK11	DDR3_FPGA_BA2
USB_RDn	AJ5	DIFFIO_TX_B24p,DQ3B	DIFFIO_RX_B35p,DQS5B,B_CK	AA14	DDR3_FPGA_CLK_P
USB_WRn	AK6	DIFFIO_TX_B24n,DQ3B	DIFFIO_RX_B35n,DQSn5B,B_CK#	AA15	DDR3_FPGA_CLK_N
DDR3_FPGA_WEn	AJ6	DIFFIO_TX_B25p,DQ4B,B_WE#	DIFFIO_TX_B36p,B_A_6	AK12	DDR3_FPGA_A6
	AJ7	DIFFIO_TX_B25n,GND	DIFFIO_TX_B36n,DQ5B,B_A_7	AK13	DDR3_FPGA_A7
DDR3_FPGA_A14	AG12	DIFFIO_RX_B26p,DQ4B,B_A_14	DIFFIO_RX_B38p,DQ5B,B_A_4	AG15	DDR3_FPGA_A4
	AG13	DIFFIO_RX_B26n,DQ4B,B_A_15	DIFFIO_RX_B38n,DQ5B,B_A_5	AH15	DDR3_FPGA_A5
			DIFFIO_TX_B40p,DQ5B,B_A_0	AJ14	DDR3_FPGA_A0
			DIFFIO_TX_B40n,DQ5B,B_A_1	AK14	DDR3_FPGA_A1

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

U21B

CYCLONE V GX SoC BANK 4

Bank 4A
1.5 Volt

DDR3_FPGA_DQ2	AG16	DIFFIO_TX_B41p,DQ6B,B_DQ_2	RZQ_0,DIFFIO_TX_B41n	AG17	RZQIN_1_5V
DDR3_FPGA_DQ1	AE17	DIFFIO_RX_B42p,DQ6B,B_DQ_1			
DDR3_FPGA_DQ0	AF18	DIFFIO_RX_B42n,DQ6B,B_DQ_0	DIFFIO_RX_B62p,DQ8B,B_DQ_21	AF20	DDR3_FPGA_DQ21
DDR3_FPGA_DQS_P0	V16	DIFFIO_RX_B43p,DQS6B,B_DQS_0	DIFFIO_RX_B62n,DQ8B,B_DQ_20	AF21	DDR3_FPGA_DQ20
DDR3_FPGA_DQS_N0	W16	DIFFIO_RX_B43n,DQSn6B,B_DQS#_0	DIFFIO_RX_B63p,GND	Y18	
DDR3_FPGA_ODT	AE16	DIFFIO_TX_B44p,B_ODT_0	DIFFIO_RX_B63n,GND	AA19	
DDR3_FPGA_DQ3	AF16	DIFFIO_TX_B44n,DQ6B,B_DQ_3	DIFFIO_TX_B64p,DQ8B,B_DM_2	AK23	DDR3_FPGA_DM2
DDR3_FPGA_DQ6	AJ16	DIFFIO_TX_B45p,DQ6B,B_DQ_6	DIFFIO_TX_B64n,DQ8B,B_DQ_23	AK24	DDR3_FPGA_DQ23
	AK16	DIFFIO_TX_B45n,DQ6B,B_ODT_1	DIFFIO_TX_B65p,DQ9B,B_DQ_26	AJ24	DDR3_FPGA_DQ26
DDR3_FPGA_DQ5	AG21	DIFFIO_TX_B46p,DQ6B,B_DQ_5	DIFFIO_TX_B65n,GND	AJ25	
DDR3_FPGA_DQ4	AH20	DIFFIO_RX_B46n,DQ6B,B_DQ_4	DIFFIO_RX_B66p,DQ9B,B_DQ_25	AF23	DDR3_FPGA_DQ25
DDR3_FPGA_DM0	AH17	DIFFIO_TX_B48p,DQ6B,B_DM_0	DIFFIO_RX_B66n,DQ9B,B_DQ_24	AF24	DDR3_FPGA_DQ24
DDR3_FPGA_DQ7	AH18	DIFFIO_TX_B48n,DQ6B,B_DQ_7	DIFFIO_RX_B67p,DQS9B,B_DQS_3	AC20	DDR3_FPGA_DQS_P3
DDR3_FPGA_DQ10	AG18	DIFFIO_TX_B49p,DQ7B,B_DQ_10	DIFFIO_RX_B67n,DQSn9B,B_DQS#_3	AD19	DDR3_FPGA_DQS_N3
	AH19	DIFFIO_TX_B49n,GND	DIFFIO_TX_B68p,GND	AJ26	
DDR3_FPGA_DQ9	AJ17	DIFFIO_RX_B50p,DQ7B,B_DQ_9	DIFFIO_TX_B68n,DQ9B,B_DQ_27	AK26	DDR3_FPGA_DQ27
DDR3_FPGA_DQ8	AK18	DIFFIO_RX_B50n,DQ7B,B_DQ_8	DIFFIO_TX_B69p,DQ9B,B_DQ_30	AG25	DDR3_FPGA_DQ30
DDR3_FPGA_DQS_P1	V17	DIFFIO_RX_B51p,DQS7B,B_DQS_1	DIFFIO_TX_B69n,DQ9B,GND	AH25	
DDR3_FPGA_DQS_N1	W17	DIFFIO_RX_B51n,DQSn7B,B_DQS#_1	DIFFIO_RX_B70p,DQ9B,B_DQ_29	AE22	DDR3_FPGA_DQ29
	AJ19	DIFFIO_TX_B52p,B_CKE_1	DIFFIO_RX_B70n,DQ9B,B_DQ_28	AE23	DDR3_FPGA_DQ28
DDR3_FPGA_DQ11	AK19	DIFFIO_TX_B52n,DQ7B,B_DQ_11	DIFFIO_RX_B71p,GND	V18	
DDR3_FPGA_DQ14	AJ20	DIFFIO_TX_B53p,DQ7B,B_DQ_14	DIFFIO_RX_B71n,GND	W19	
DDR3_FPGA_CKE	AJ21	DIFFIO_TX_B53n,DQ7B,B_CKE_0	DIFFIO_TX_B72p,DQ9B,B_DM_3	AJ27	DDR3_FPGA_DM3
DDR3_FPGA_DQ13	AF19	DIFFIO_RX_B54p,DQ7B,B_DQ_13	DIFFIO_TX_B72n,DQ9B,B_DQ_31	AK27	DDR3_FPGA_DQ31
DDR3_FPGA_DQ12	AG20	DIFFIO_RX_B54n,DQ7B,B_DQ_12	DIFFIO_TX_B73p,DQ10B,B_DQ_34	AK28	USB_B2_DATA0
DDR3_FPGA_DM1	AG23	DIFFIO_TX_B56p,DQ7B,B_DM_1	DIFFIO_TX_B73n,GND	AK29	
DDR3_FPGA_DQ15	AH24	DIFFIO_TX_B56n,DQ7B,B_DQ_15	DIFFIO_RX_B74p,DQ10B,B_DQ_33	AD20	USB_B2_DATA1
DDR3_FPGA_DQ18	AG22	DIFFIO_TX_B57p,DQ8B,B_DQ_18	DIFFIO_RX_B74n,DQ10B,B_DQ_32	AD21	USB_B2_DATA2
	AH22	DIFFIO_TX_B57n,GND	DIFFIO_RX_B75p,DQS10B,B_DQS_4	Y19	USB_B2_DATA3
DDR3_FPGA_DQ17	AE18	DIFFIO_RX_B58p,DQ8B,B_DQ_17	DIFFIO_RX_B75n,DQSn10B,B_DQS#_4	AA20	USB_B2_DATA4
DDR3_FPGA_DQ16	AE19	DIFFIO_RX_B58n,DQ8B,B_DQ_16	DIFFIO_TX_B76p,GND	AG26	
DDR3_FPGA_DQS_P2	Y17	DIFFIO_RX_B59p,DQS8B,B_DQS_2	DIFFIO_TX_B76n,DQ10B,B_DQ_35	AH27	USB_B2_DATA5
DDR3_FPGA_DQS_N2	AA18	DIFFIO_RX_B59n,DQSn8B,B_DQS#_2	DIFFIO_TX_B77p,DQ10B,B_DQ_38	AF25	USB_B2_DATA6
DDR3_FPGA_RESETn	AK21	DIFFIO_TX_B60p,B_RESET#	DIFFIO_TX_B77n,DQ10B,GND	AF26	
DDR3_FPGA_DQ19	AK22	DIFFIO_TX_B60n,DQ8B,B_DQ_19	DIFFIO_RX_B78p,DQ10B,B_DQ_37	AC22	USB_B2_DATA7
DDR3_FPGA_DQ22	AH23	DIFFIO_TX_B61p,DQ8B,B_DQ_22	DIFFIO_RX_B78n,DQ10B,B_DQ_36	AC23	
	AJ22	DIFFIO_TX_B61n,DQ8B,GND	DIFFIO_RX_B79p,GND	AA21	
			DIFFIO_RX_B79n,GND	AB21	
			DIFFIO_TX_B80p,DQ10B,B_DM_4	AD24	
			DIFFIO_TX_B80n,DQ10B,B_DQ_39	AE24	

100, 1%
R449

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

HSMC LVCMOS INTERFACE

LVCMOS Only

(17) HSMA_CLK_OUT_P1
(17) HSMA_CLK_OUT_N1
(17) HSMA_CLK_IN_P1
(17) HSMA_CLK_IN_N1

(16,17,23) HSMA_PRSNTn

(17) HSMA_D[3:0]
(17) HSMA_SDA
(17) HSMA_SCL

USER_DIPSW_FPGA[3:0] (23)
USER_PB_FPGA[1:0] (23)
USER_LED_FPGA[3:0] (9,23)

USB_B2_DATA[7:0]
USB_B2_DATA[7:0] (25)

USB_FULL
USB_EMPTY
USB_SCL
USB_SDA
USB_B2_CLK
USB_RESETn
USB_OEn
USB_RDn
USB_WRn

USB_FULL (25)
USB_EMPTY (25)
USB_SCL (25)
USB_SDA (25)
USB_B2_CLK (16,25)
USB_RESETn (25)
USB_OEn (25)
USB_RDn (25)
USB_WRn (25)

(13) DDR3_FPGA_CKE
(13) DDR3_FPGA_CLK_P
(13) DDR3_FPGA_CLK_N
→ DDR3_FPGA_CKE, DDR3_FPGA_CLK_P, DDR3_FPGA_CLK_N

(13) DDR3_FPGA_DM0
(13) DDR3_FPGA_DM1
(13) DDR3_FPGA_DM2
(13) DDR3_FPGA_DM3
→ DDR3_FPGA_DM0, DDR3_FPGA_DM1, DDR3_FPGA_DM2, DDR3_FPGA_DM3

(13) DDR3_FPGA_CSn
(13) DDR3_FPGA_WEn
(13) DDR3_FPGA_RASn
(13) DDR3_FPGA_CASn
→ DDR3_FPGA_CSn, DDR3_FPGA_WEn, DDR3_FPGA_RASn, DDR3_FPGA_CASn

(13) DDR3_FPGA_BA0
(13) DDR3_FPGA_BA1
(13) DDR3_FPGA_BA2
(13) DDR3_FPGA_RESETn
(13) DDR3_FPGA_ODT
→ DDR3_FPGA_BA0, DDR3_FPGA_BA1, DDR3_FPGA_BA2, DDR3_FPGA_RESETn, DDR3_FPGA_ODT

DDR3_FPGA_BA[2:0] (13)
DDR3_FPGA_DM[3:0] (13)
DDR3_FPGA_DQS_P[3:0] (13)
DDR3_FPGA_DQS_N[3:0] (13)
DDR3_FPGA_DQ[31:0] (13)
DDR3_FPGA_A[14:0] (9,13)

PCIE INTERFACE

(3,11) PCIE_PERSTn

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone V SoC FPGA Development Kit Board

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

Date: Tuesday, October 15, 2013 Sheet 4 of 41

Cyclone V GX SoC Bank 5 & 6

U21C — CYCLONE V GX SoC BANK 5

Bank 5A — 2.5 Volt

ENET1_TX_D0	W20	DIFFIO_RX_R4p,DQ1R	
ENET1_TX_D1	Y21	DIFFIO_RX_R4n,DQ1R	
ENET1_TX_D2	AA25	DIFFIO_TX_R7p,DQ1R	
ENET1_TX_D3	AB26	DIFFIO_TX_R7n	
ENET1_TX_EN (19)	AB22	DIFFIO_RX_R8p,DQ1R	
ENET1_RX_D0	AB23	DIFFIO_RX_R8n,DQ1R	
ENET1_RX_D1	AA24	DIFFIO_RX_R9p	
ENET1_RX_D2	AB25	DIFFIO_RX_R9n	
ENET1_RX_D3	AE27	DIFFIO_TX_R10p,DQ2R	
ENET1_RX_ERROR (19)	AE28	DIFFIO_TX_R10n,DQ2R	
ENET1_RX_DV (19)	Y23	DIFFIO_RX_R11p,DQ2R	
ENET1_RX_CLK (19)	Y24	DIFFIO_RX_R11n,DQ2R	
		RZQ_1,DIFFIO_TX_R1p,DQ1R	
		DIFFIO_TX_R12p,DQ2R	
		DIFFIO_TX_R12n,DQ2R	
		DIFFIO_RX_R13p,DQS2R	
		DIFFIO_RX_R13n,DQSn2R	
		DIFFIO_TX_R14p	
		DIFFIO_TX_R14n,DQ2R	
		DIFFIO_RX_R15p,DQ2R	
		DIFFIO_RX_R15n,DQ2R	
		DIFFIO_TX_R16p,DQ2R	
		DIFFIO_TX_R16n	

Bank 5B — 2.5 Volt

ENET1_TX_CLK_FB (19)	W25	DIFFIO_RX_R17p
ENET2_RX_ERROR (19)	V25	DIFFIO_RX_R17n
ENET2_RX_DV (19)	AC28	DIFFIO_TX_R18p,DQ3R
SDI_TX_SD_HDn (20)	AC29	DIFFIO_TX_R18n,DQ3R
SDI_RSTI (20)	AB30	DIFFIO_RX_R19p,DQ3R
SDI_TX_EN (16,20)	AA30	DIFFIO_RX_R19n,DQ3R
SDI_RX_BYPASS (16,20)	AB28	DIFFIO_TX_R20p,DQ3R
SDI_RX_EN (16,20)	AA28	DIFFIO_TX_R20n,DQ3R
SDI_FAULT (20)	AD30	DIFFIO_TX_R24p,DQ3R
	AC30	RZQ_2,DIFFIO_TX_R24n

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

	AG27	ENET2_TX_D0
	AG28	ENET2_TX_D1
	AF28	ENET2_TX_D2
	V23	ENET2_TX_D3
(19) ENET2_TX_EN	W24	
ENET2_RX_D0	AF29	
ENET2_RX_D1	AF30	
ENET2_RX_D2	AD26	
ENET2_RX_D3	AC27	
(19) ENET2_RX_CLK	AH30	
ENET2_TX_CLK_FB (19)	AG30	

100, 1% — R410

U21D — CYCLONE V GX SoC BANK 6

Bank 6A — 1.5 Volt

HPS_RZQ_0	D27			K28	DDR3_HPS_DM0
HPS_DDR,HPS_A_0	F26	DDR3_HPS_A0	HPS_DDR,HPS_DM_0	N18	DDR3_HPS_DQS_P0
HPS_DDR,HPS_A_1	G30	DDR3_HPS_A1	HPS_DDR,HPS_DQS_0	M19	DDR3_HPS_DQS_N0
HPS_DDR,HPS_A_2	F28	DDR3_HPS_A2	HPS_DDR,HPS_DQS#_0	K23	DDR3_HPS_DQ0
HPS_DDR,HPS_A_3	F30	DDR3_HPS_A3	HPS_DDR,HPS_DQ_0	K22	DDR3_HPS_DQ1
HPS_DDR,HPS_A_4	J25	DDR3_HPS_A4	HPS_DDR,HPS_DQ_1	H30	DDR3_HPS_DQ2
HPS_DDR,HPS_A_5	J27	DDR3_HPS_A5	HPS_DDR,HPS_DQ_2	G28	DDR3_HPS_DQ3
HPS_DDR,HPS_A_6	F29	DDR3_HPS_A6	HPS_DDR,HPS_DQ_3	L25	DDR3_HPS_DQ4
HPS_DDR,HPS_A_7	E28	DDR3_HPS_A7	HPS_DDR,HPS_DQ_4	L24	DDR3_HPS_DQ5
HPS_DDR,HPS_A_8	H27	DDR3_HPS_A8	HPS_DDR,HPS_DQ_5	J30	DDR3_HPS_DQ6
HPS_DDR,HPS_A_9	G26	DDR3_HPS_A9	HPS_DDR,HPS_DQ_6	J29	DDR3_HPS_DQ7
HPS_DDR,HPS_A_10	D29	DDR3_HPS_A10	HPS_DDR,HPS_DQ_7		
HPS_DDR,HPS_A_11	C30	DDR3_HPS_A11		M28	DDR3_HPS_DM1
HPS_DDR,HPS_A_12	B30	DDR3_HPS_A12	HPS_DDR,HPS_DM_1	N25	DDR3_HPS_DQS_P1
HPS_DDR,HPS_A_13	C29	DDR3_HPS_A13	HPS_DDR,HPS_DQS_1	N24	DDR3_HPS_DQS_N1
HPS_DDR,HPS_A_14	H25	DDR3_HPS_A14	HPS_DDR,HPS_DQS#_1	K26	DDR3_HPS_DQ8
HPS_DDR,HPS_A_15	G25		HPS_DDR,HPS_DQ_8	L26	DDR3_HPS_DQ9
			HPS_DDR,HPS_DQ_9	K29	DDR3_HPS_DQ10
HPS_DDR,HPS_CK	M23	DDR3_HPS_CLK_P	HPS_DDR,HPS_DQ_10	K27	DDR3_HPS_DQ11
HPS_DDR,HPS_CK#	L23	DDR3_HPS_CLK_N	HPS_DDR,HPS_DQ_11	M26	DDR3_HPS_DQ12
HPS_DDR,HPS_CKE_0	L29	DDR3_HPS_CKE	HPS_DDR,HPS_DQ_12	M27	DDR3_HPS_DQ13
HPS_DDR,HPS_CKE_1	L30		HPS_DDR,HPS_DQ_13	L28	DDR3_HPS_DQ14
HPS_DDR,HPS_BA_0	E29	DDR3_HPS_BA0	HPS_DDR,HPS_DQ_14	M30	DDR3_HPS_DQ15
HPS_DDR,HPS_BA_1	J24	DDR3_HPS_BA1	HPS_DDR,HPS_DQ_15		
HPS_DDR,HPS_BA_2	J23	DDR3_HPS_BA2		M25	
HPS_DDR,HPS_RAS#	D30	DDR3_HPS_RASn	HPS_GI14	J26	
HPS_DDR,HPS_CAS#	E27	DDR3_HPS_CASn	HPS_GI13	M22	
HPS_DDR,HPS_WE#	C28	DDR3_HPS_WEn	HPS_GI11	N23	
HPS_DDR,HPS_CS#_0	H24	DDR3_HPS_CSn	HPS_GI12		
HPS_DDR,HPS_CS#_1	K21				
HPS_DDR,HPS_ODT_0	H28	DDR3_HPS_ODT			
HPS_DDR,HPS_ODT_1	H29				

Bank 6B — 1.5 Volt

HPS_DDR,HPS_DM_2	R28	DDR3_HPS_DM2	HPS_DDR,HPS_DM_4	W27	DDR3_HPS_DM4
HPS_DDR,HPS_DQS_2	R19	DDR3_HPS_DQS_P2	HPS_DDR,HPS_DQS_4	T24	DDR3_HPS_DQS_P4
HPS_DDR,HPS_DQS#_2	R18	DDR3_HPS_DQS_N2	HPS_DDR,HPS_DQS#_4	T23	DDR3_HPS_DQS_N4
HPS_DDR,HPS_DQ_16	U26	DDR3_HPS_DQ16	HPS_DDR,HPS_DQ_32	W26	DDR3_HPS_DQ32
HPS_DDR,HPS_DQ_17	T26	DDR3_HPS_DQ17	HPS_DDR,HPS_DQ_33	R24	DDR3_HPS_DQ33
HPS_DDR,HPS_DQ_18	N29	DDR3_HPS_DQ18	HPS_DDR,HPS_DQ_34	U27	DDR3_HPS_DQ34
HPS_DDR,HPS_DQ_19	N28	DDR3_HPS_DQ19	HPS_DDR,HPS_DQ_35	V28	DDR3_HPS_DQ35
HPS_DDR,HPS_DQ_20	P26	DDR3_HPS_DQ20	HPS_DDR,HPS_DQ_36	T25	DDR3_HPS_DQ36
HPS_DDR,HPS_DQ_21	P27	DDR3_HPS_DQ21	HPS_DDR,HPS_DQ_37	U25	DDR3_HPS_DQ37
HPS_DDR,HPS_DQ_22	N27	DDR3_HPS_DQ22	HPS_DDR,HPS_DQ_38	V27	DDR3_HPS_DQ38
HPS_DDR,HPS_DQ_23	R29	DDR3_HPS_DQ23	HPS_DDR,HPS_DQ_39	Y29	DDR3_HPS_DQ39
HPS_DDR,HPS_DM_3	W30	DDR3_HPS_DM3		N30	USER_DIPSW_HPS0
HPS_DDR,HPS_DQS_3	R22	DDR3_HPS_DQS_P3	HPS_GI10	P29	USER_DIPSW_HPS1
HPS_DDR,HPS_DQS#_3	R21	DDR3_HPS_DQS_N3	HPS_GI9	P22	USER_DIPSW_HPS2
HPS_DDR,HPS_DQ_24	P24	DDR3_HPS_DQ24	HPS_GI8	V20	USER_DIPSW_HPS3
HPS_DDR,HPS_DQ_25	P25	DDR3_HPS_DQ25	HPS_GI7	T30	USER_PB_HPS0
HPS_DDR,HPS_DQ_26	T29	DDR3_HPS_DQ26	HPS_GI6	U28	USER_PB_HPS1
HPS_DDR,HPS_DQ_27	T28	DDR3_HPS_DQ27	HPS_GI5	T21	USER_PB_HPS2
HPS_DDR,HPS_DQ_28	R27	DDR3_HPS_DQ28	HPS_GI4	U20	USER_PB_HPS3
HPS_DDR,HPS_DQ_29	R26	DDR3_HPS_DQ29	HPS_GI3	V29	
HPS_DDR,HPS_DQ_30	V30	DDR3_HPS_DQ30	HPS_GI2	Y28	
HPS_DDR,HPS_DQ_31	W29	DDR3_HPS_DQ31	HPS_GI1		
			HPS_DDR,HPS_RESET#	P30	DDR3_HPS_RESETn

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

(23) USER_DIPSW_HPS[3:0]

(23) USER_PB_HPS[3:0]

(4,7,17) HSMA_CLK_OUT_P[2:1]
(4,7,17) HSMA_CLK_OUT_N[2:1]
(7,17) HSMA_TX_D_P[16:0]
(7,17) HSMA_TX_D_N[16:0]
(7,17) HSMA_RX_D_P[16:0]
(7,17) HSMA_RX_D_N[16:0]

Si571 VCXO

(4,8) SDI_CLK148_DN

ENET1_TX_D[3..0] (19)
ENET1_RX_D[3..0] (19)
ENET2_TX_D[3..0] (19)
ENET2_RX_D[3..0] (19)

(14) DDR3_HPS_CLK_P → DDR3_HPS_CLK_P
(14) DDR3_HPS_CLK_N → DDR3_HPS_CLK_N
(14) DDR3_HPS_CKE → DDR3_HPS_CKE
(14) DDR3_HPS_BA0 → DDR3_HPS_BA0
(14) DDR3_HPS_BA1 → DDR3_HPS_BA1
(14) DDR3_HPS_BA2 → DDR3_HPS_BA2
(14) DDR3_HPS_RASn → DDR3_HPS_RASn
(14) DDR3_HPS_CASn → DDR3_HPS_CASn
(14) DDR3_HPS_WEn → DDR3_HPS_WEn
(14) DDR3_HPS_CSn → DDR3_HPS_CSn
(14) DDR3_HPS_ODT → DDR3_HPS_ODT
(14) DDR3_HPS_RESETn → DDR3_HPS_RESETn

DDR3_HPS_BA[2:0] (14)
DDR3_HPS_DM[4:0] (14)
DDR3_HPS_DQS_P[4:0] (14)
DDR3_HPS_DQS_N[4:0] (14)
DDR3_HPS_DQ[39:0] (14)
DDR3_HPS_A[14:0] (14)

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone V SoC FPGA Development Kit Board

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

Date: Tuesday, October 15, 2013 Sheet 5 of 41

Cyclone V GX SoC Bank 7

U21E

CYCLONE V GX SoC BANK 7

HPS_nRST			Bank 7A		
HPS_nPOR			CAN0_TX,UART0_TX,SPIM1_SS0,HPS_GPIO66	D24	(24) UART_TX
HPS_TDO			CAN0_RX,UART0_RX,SPIM1_MISO,HPS_GPIO65	E24	(24) UART_RX
VCC_HPS			I2C0_SCL,UART1_TX,SPIM1_MOSI,HPS_GPIO64	B22	(18,27) I2C_SCL_HPS
HPS_TMS			I2C0_SDA,UART1_RX,SPIM1_CLK,HPS_GPIO63	C23	(18,27) I2C_SDA_HPS
HPS_TCK			UART0_TX,CAN0_TX,SPIM1_SS1,HPS_GPIO62	G22	(24) CAN_0_TX
HPS_TRST			UART0_RX,CAN0_RX,SPIM0_SS1,HPS_GPIO61	B22	(24) CAN_0_RX
HPS_TDI			SPIM0_SS0,CAN1_TX,UART1_RTS,BOOTSEL0,HPS_GPIO60	H20	SPI_CSn
HPS_PORSEL			SPIM0_MISO,CAN1_RX,UART1_CTS,HPS_GPIO59	B23	SPI_MISO
HPS_CLK1			SPIM0_MOSI,I2C1_SCL,UART0_RTS,HPS_GPIO58	C22	SPI_MOSI
HPS_CLK2			SPIM0_CLK,I2C1_SDA,UART0_CTS,HPS_GPIO57	A23	SPI_SCK
			TRACE_D7,SPIS1_MISO,I2C0_SCL,HPS_GPIO56	E23	R377 22 TRACE_DATA7
TRACE_CLK,HPS_GPIO48			TRACE_D6,SPIS1_SS0,I2C0_SDA,HPS_GPIO55	C24	R376 22 TRACE_DATA6
TRACE_D0,SPIS0_CLK,UART0_RX,HPS_GPIO49			TRACE_D5,SPIS1_MOSI,CAN1_TX,HPS_GPIO54	G21	R396 22 TRACE_DATA5
TRACE_D1,SPIS0_MOSI,UART0_TX,HPS_GPIO50			TRACE_D4,SPIS1_CLK,CAN1_RX,HPS_GPIO53	A24	R395 22 TRACE_DATA4
TRACE_D2,SPIS0_MISO,I2C1_SDA,HPS_GPIO51			TRACE_D3,SPIS0_SS0,I2C1_SCL,HPS_GPIO52	H23	R394 22 TRACE_DATA3
NAND_DQ6,RGMII1_RXD1,USB1_D7,HPS_GPIO25			Bank 7B	NAND_ALE,RGMII1_TX_CLK,QSPI_SS3,HPS_GPIO14	H19 ENET_HPS_GTX_CLK
NAND_DQ5,RGMII1_RX_CLK,USB1_D6,HPS_GPIO24				NAND_DQ7,RGMII1_RXD2,HPS_GPIO26	B18 ENET_HPS_RXD2
NAND_DQ4,RGMII1_TX_CTL,USB1_D5,HPS_GPIO23				NAND_WP,RGMII1_RXD3,QSPI_SS2,HPS_GPIO27	D21 ENET_HPS_RXD3
NAND_DQ3,RGMII1_RX_CTL,USB1_D4,HPS_GPIO22				NAND_WE,QSPI_SS1,BOOTSEL2,HPS_GPIO28	D20 BOOTSEL2
NAND_DQ2,RGMII1_MDC,I2C3_SCL,HPS_GPIO21				QSPI_IO0,USB1_CLK,HPS_GPIO29	C20 (21) QSPI_IO0
NAND_DQ1,RGMII1_MDIO,I2C3_SDA,HPS_GPIO20				QSPI_IO1,USB1_STP,HPS_GPIO30	H18 (21) QSPI_IO1
NAND_DQ0,RGMII1_RXD0,HPS_GPIO19				QSPI_IO2,USB1_DIR,HPS_GPIO31	A19 (21) QSPI_IO2
NAND_RB,RGMII1_TXD3,USB1_D3,HPS_GPIO18				QSPI_IO3,USB1_NXT,HPS_GPIO32	E19 (21) QSPI_IO3
NAND_RE,RGMII1_TXD2,USB1_D2,HPS_GPIO17				QSPI_SS0,BOOTSEL1,HPS_GPIO33	A18 (21) QSPI_SS0
NAND_CLE,RGMII1_TXD1,USB1_D1,HPS_GPIO16				QSPI_CLK,HPS_GPIO34	D19 (21) QSPI_CLK
NAND_CE,RGMII1_TXD0,USB1_D0,HPS_GPIO15				QSPI_SS1,HPS_GPIO35	C19 ENET_HPS_INTn
SDMMC_D3,USB0_NXT,HPS_GPIO47			Bank 7C	SDMMC_CMD,USB0_D0,HPS_GPIO36	F18 SD_CMD
SDMMC_D2,USB0_DIR,HPS_GPIO46				SDMMC_PWREN,USB0_D1,HPS_GPIO37	B17 SD_PWREN
SDMMC_CLK,USB0_STP,HPS_GPIO45				SDMMC_D0,USB0_D2,HPS_GPIO38	G18 SD_DAT0
SDMMC_CLK_IN,USB0_CLK,HPS_GPIO44				SDMMC_D1,USB0_D3,HPS_GPIO39	C17 SD_DAT1
SDMMC_D7,USB0_D7,HPS_GPIO43				SDMMC_D4,USB0_D4,HPS_GPIO40	H17
SDMMC_D6,USB0_D6,HPS_GPIO42				SDMMC_D5,USB0_D5,HPS_GPIO41	C18 USER_LED_HPS3
RGMII0_MDC ,USB1_D6,I2C2_SCL,HPS_GPIO7			Bank 7D	RGMII0_RXD0,USB1_D4,HPS_GPIO5	A15 USB_DATA4
RGMII0_MDIO,USB1_D5,I2C2_SDA,HPS_GPIO6				RGMII0_TXD3,USB1_D3,HPS_GPIO4	D14 USB_DATA3
RGMII0_RX_CTL,USB1_D7,HPS_GPIO8				RGMII0_TXD2,USB1_D2,HPS_GPIO3	D16 USB_DATA2
RGMII0_RX_CLK,USB1_CLK,HPS_GPIO10				RGMII0_TXD1,USB1_D1,HPS_GPIO2	G16 USB_DATA1
RGMII0_RXD3,USB1_NXT,HPS_GPIO13				RGMII0_TXD0,USB1_D0,HPS_GPIO1	E16 USB_DATA0
RGMII0_RXD2,USB1_DIR,HPS_GPIO12				RGMII0_TX_CLK,HPS_GPIO0	F16 CODEC_SEL
RGMII0_RXD1,USB1_STP,HPS_GPIO11				RGMII0_TX_CTL,HPS_GPIO9	B15

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

2.5V_HPS
3.3V
R393 4.70K, 1%
R392 4.70K, 1%
2.5V_HPS
MICTOR_RSTn C27
HPS_RESETn F23
JTAG_HPS_TDO (12) B28
HPS_EN_2.5V G23
JTAG_HPS_TMS (12) A29
JTAG_HPS_TCK (12) H22
JTAG_HPS_TRST A28
JTAG_HPS_TDI (12) B27
F24
CLK_OSC1 (10) D25
CLK_OSC2 (10) F25
R693 38.3
C784 22pF
TRACE_CLK_MIC R391 0 B26
TRACE_DATA0 R375 22 B25
TRACE_DATA1 R373 22 C25
TRACE_DATA2 R374 22 A25
HEADER, 1x3-PIN
J26
1 10.0K R239 3.3V
2 UART_TX CLKSEL0
3 1.00k R240
J27
1 10.0K R241 3.3V
2 CAN_0_TX CLKSEL1
3 1.00k R242
HEADER, 1x3-PIN
ENET_HPS_RXD1 B20
ENET_HPS_RX_CLK G20
ENET_HPS_TX_EN A20
ENET_HPS_RX_DV K17
ENET_HPS_MDC B21
ENET_HPS_MDIO E21
ENET_HPS_RXD0 A21
ENET_HPS_TXD3 F19
ENET_HPS_TXD2 F21
ENET_HPS_TXD1 J19
ENET_HPS_TXD0 F20
(22) SD_CD_DAT3
(22) SD_DAT2
(22) SD_CLK
SD_CD_DAT3 B16
SD_DAT2 D17
SD_CLK A16
USER_LED_HPS0 E17
USER_LED_HPS1 E18
USER_LED_HPS2 G17
(22) USB_DATA6
(22) USB_DATA5
(22) USB_DATA7
(22) USB_CLK
(22) USB_NXT
(22) USB_DIR
(22) USB_STP
USB_DATA6 D15
USB_DATA5 C14
USB_DATA7 M17
USB_CLK N16
USB_NXT A14
USB_DIR E14
USB_STP C15

3.3V
R3 4.70K, 1% JTAG_MICTOR_TMS
R4 4.70K, 1% JTAG_MICTOR_TDI
9V_VPP
J32
HDR 2X7, VT, THM, 2mm
3.3V
3.3V
R258 0
SCK_SCL
CSn
MISO
MOSI_SDA
I2C_SDA_HPS R260 0
I2C_SCL_HPS R259 0
XJ4
881545-2
J16
CON2
JTAG_MIC_SEL
R125 4.70K, 1%
2.5V_REG_HPS
Logic 0 = pin 10 <--> pin 9 (TRST from JTAG)
Logic 1 = pin 10 <--> pin 2 (TRST from MICTOR)
U57
JTAG_MIC_SEL
MICTOR_TRST
IN1
NO1
GND
NO2
IN2
COM1
NC1
V+
NC2
COM2
MICTR_TRST
R318 0
JTAG_HPS_TRST
(12,16) JTAG_TRST
2.5V_REG_HPS
C244 0.1uF
Logic 0 = pin 6 <--> pin 7 (Bypass)
Logic 1 = pin 6 <--> pin 4 (Enable)
TS5A23157
Manufacturer = Texas Instruments
PART_NUMBER = TS5A23157DGSR

(12,16,21) MICTOR_RSTn
(12) JTAG_MICTOR_TDI
(12) JTAG_MICTOR_TCK
(12) JTAG_MICTOR_TMS
(12) JTAG_MICTOR_TDO
R310 10.0K
MICTOR_RSTn
JTAG_MICTOR_TDI
JTAG_MICTOR_TCK
JTAG_MICTOR_TMS
JTAG_MICTOR_TDO
MICTOR_TRST
J4
Mictor38P
TRACE_CLK_MIC
R338 10.0K
R33 0_Ohms DNI
MICTOR_PWR1
MICTOR_PWR2
R32
TRACE_DATA7
TRACE_DATA6
TRACE_DATA5
TRACE_DATA4
TRACE_DATA3
TRACE_DATA2
TRACE_DATA1
TRACE_DATA0
R327 10K
R328 10K
R330 10K
R331 10K
MIC_34
MIC_36
3.3V
C25 0.1uF
C24 0.001uf
MIC_34 R329 DNI
MIC_36 R332 DNI

Micro SD / USB INTERFACE
USB_DATA[7..0]
USB_DATA[7..0] (22)
ETHERNET INTERFACE
ENET_HPS_TXD[3..0]
ENET_HPS_TXD[3..0] (18)
ENET_HPS_GTX_CLK
ENET_HPS_TX_EN
ENET_HPS_MDC
ENET_HPS_RESETn
ENET_HPS_GTX_CLK(18)
ENET_HPS_TX_EN(18)
ENET_HPS_MDC (18)
ENET_HPS_RESETn (18,21)
ENET_HPS_RXD[3..0]
ENET_HPS_RXD[3..0] (18)
ENET_HPS_RX_CLK
ENET_HPS_RX_DV
ENET_HPS_MDIO
ENET_HPS_INTn
ENET_HPS_RX_CLK (18)
ENET_HPS_RX_DV (18)
ENET_HPS_MDIO (18)
ENET_HPS_INTn (18)
HPS_RESETn
HPS_RESETn (16,21)
USER_LED_HPS[3..0]
USER_LED_HPS[3..0] (23)
HEADER, 1x3-PIN
3.3V
R243 10.0K
SPI_CSn
R244 1.00k
J28
BOOTSEL0
HEADER, 1x3-PIN
3.3V
R245 10.0K
QSPI_SS0
R246 1.00k
J29
BOOTSEL1
HEADER, 1x3-PIN
3.3V
R247 10.0K
BOOTSEL2
R248 1.00k
J30
BOOTSEL2
HEADER, 1x3-PIN

U54
IDTQS3VH257
Manufacturer = IDT
PART_NUMBER = QS3VH257PAG
3.3V
C685 2.2uF
C686 0.1uF
VCC
I0A
I1A
I0B
I1B
I0C
I1C
I0D
I1D
GND
YA
YB
YC
YD
S
E
SPI_MISO
MISO
SPI_MOSI
MOSI_SDA
I2C_SDA_HPS
I2C_SCL_HPS
SPI_SCK
SCK_SCL
SPI_CSn
CSn
CODEC_SEL
XJ3
881545-2
R266 10.0K
J31
CON2

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121			
Title: Cyclone V SoC FPGA Development Kit Board			
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Size: B	Document Number: 150-0321003-D1 (6XX-44184R)		Rev: D1
Date: Tuesday, October 15, 2013	Sheet 6 of 41		

Cyclone V GX SoC Bank 8

(4,17) HSMA_D[3:0]
(17) HSMA_TX_D_P[16:0]
(17) HSMA_TX_D_N[16:0]
(17) HSMA_RX_D_P[16:0]
(17) HSMA_RX_D_N[16:0]
(4,17) HSMA_CLK_OUT_P[2:1]
(4,17) HSMA_CLK_OUT_N[2:1]
(4,9,17) HSMA_CLK_IN_P[2:1]
(4,9,17) HSMA_CLK_IN_N[2:1]

U21F

CYCLONE V GX SoC BANK 8

Bank 8A
2.5 Volt

HSMA_TX_D_P15	B13	DIFFIO_TX_T2p,DQ1T	
HSMA_TX_D_N15	A13	DIFFIO_TX_T2n,DQ1T	
HSMA_RX_D_P15	C13	DIFFIO_RX_T3p,DQ1T	
HSMA_RX_D_N15	B12	DIFFIO_RX_T3n,DQ1T	
HSMA_RX_D_P16	F15	DIFFIO_RX_T5p,DQS1T	
HSMA_RX_D_N16	F14	DIFFIO_RX_T5n,DQSn1T	
HSMA_TX_D_P16	C12	DIFFIO_TX_T6p	
HSMA_TX_D_N16	B11	DIFFIO_TX_T6n,DQ1T	
HSMA_RX_D_P12	D11	DIFFIO_RX_T7p,DQ1T	
HSMA_RX_D_N12	D10	DIFFIO_RX_T7n,DQ1T	
HSMA_TX_D_P12	A9	DIFFIO_TX_T8p,DQ1T	
HSMA_TX_D_N12	A8	DIFFIO_TX_T8n	
HSMA_TX_D_P11	C7	DIFFIO_TX_T10p,DQ2T	
HSMA_TX_D_N11	B7	DIFFIO_TX_T10n,DQ2T	
HSMA_RX_D_P11	E9	DIFFIO_RX_T11p,DQ2T	
HSMA_RX_D_N11	D9	DIFFIO_RX_T11n,DQ2T	
HSMA_TX_D_P13	C8	DIFFIO_TX_T12p,DQ2T	
HSMA_TX_D_N13	B8	DIFFIO_TX_T12n,DQ2T	
HSMA_RX_D_P0	H14	DIFFIO_RX_T13p,DQS2T	
HSMA_RX_D_N0	G13	DIFFIO_RX_T13n,DQSn2T	
HSMA_TX_D_P14	C10	DIFFIO_TX_T14p	
HSMA_TX_D_N14	C9	DIFFIO_TX_T14n,DQ2T	
HSMA_RX_D_P14	F13	DIFFIO_RX_T15p,DQ2T	
HSMA_RX_D_N14	E13	DIFFIO_RX_T15n,DQ2T	
HSMA_TX_D_P10	A6	DIFFIO_TX_T16p,DQ2T	
HSMA_TX_D_N10	A5	DIFFIO_TX_T16n	
HSMA_RX_D_P6	H8	DIFFIO_RX_T17p	
HSMA_RX_D_N6	G8	DIFFIO_RX_T17n	
HSMA_TX_D_P8	A4	DIFFIO_TX_T18p,DQ3T	
HSMA_TX_D_N8	A3	DIFFIO_TX_T18n,DQ3T	
HSMA_RX_D_P13	E12	DIFFIO_RX_T19p,DQ3T	
HSMA_RX_D_N13	D12	DIFFIO_RX_T19n,DQ3T	
HSMA_TX_D_P1	D6	DIFFIO_TX_T20p,DQ3T	
HSMA_TX_D_N1	C5	DIFFIO_TX_T20n,DQ3T	
ENET_FPGA_MDIO (19)	H13	DIFFIO_RX_T21p,DQS3T	
ENET_FPGA_MDC (19)	H12	DIFFIO_RX_T21n,DQSn3T	
HSMA_TX_D_P9	D5	DIFFIO_TX_T22p	
HSMA_TX_D_N9	C4	DIFFIO_TX_T22n,DQ3T	

DIFFIO_RX_T23p,DQ3T	F11	HSMA_RX_D_P9	
DIFFIO_RX_T23n,DQ3T	E11	HSMA_RX_D_N9	
DIFFIO_RX_T24p,DQ3T	E8	HSMA_TX_D_P0	
DIFFIO_TX_T24n	D7	HSMA_TX_D_N0	
DIFFIO_RX_T25p	J7	HSMA_RX_D_P5	
DIFFIO_RX_T25n	H7	HSMA_RX_D_N5	
DIFFIO_TX_T26p,DQ4T	B2	HSMA_TX_D_P6	
DIFFIO_TX_T26n,DQ4T	B1	HSMA_TX_D_N6	
DIFFIO_RX_T27p,DQ4T	B6	HSMA_RX_D_P10	
DIFFIO_RX_T27n,DQ4T	B5	HSMA_RX_D_N10	
DIFFIO_TX_T28p,DQ4T	C3	HSMA_TX_D_P7	
DIFFIO_TX_T28n,DQ4T	B3	HSMA_TX_D_N7	
DIFFIO_RX_T29p,DQS4T	K12	HSMA_RX_D_P1	
DIFFIO_RX_T29n,DQSn4T	J12	HSMA_RX_D_N1	
DIFFIO_TX_T30p	D2	HSMA_TX_D_P5	
DIFFIO_TX_T30n,DQ4T	C2	HSMA_TX_D_N5	
DIFFIO_RX_T31p,DQ4T	G12	HSMA_RX_D_P4	
DIFFIO_RX_T31n,DQ4T	G11	HSMA_RX_D_N4	
DIFFIO_TX_T32p,DQ4T	E4	HSMA_TX_D_P2	
DIFFIO_TX_T32n	D4	HSMA_TX_D_N2	
DIFFIO_RX_T33p	K7	HSMA_RX_D_P3	
DIFFIO_RX_T33n	K8	HSMA_RX_D_N3	
DIFFIO_TX_T34p,DQ5T	E3	HSMA_TX_D_P3	
DIFFIO_TX_T34n,DQ5T	E2	HSMA_TX_D_N3	
DIFFIO_RX_T35p,DQ5T	G10	HSMA_RX_D_P7	
DIFFIO_RX_T35n,DQ5T	F10	HSMA_RX_D_N7	
DIFFIO_TX_T36p,DQ5T	E1	HSMA_TX_D_P4	
DIFFIO_TX_T36n,DQ5T	D1	HSMA_TX_D_N4	
DIFFIO_RX_T37p,DQS5T	J10	HSMA_RX_D_P2	
DIFFIO_RX_T37n,DQSn5T	J9	HSMA_RX_D_N2	
DIFFIO_TX_T38p	E7	HSMA_CLK_OUT_P2	
DIFFIO_TX_T38n,DQ5T	E6	HSMA_CLK_OUT_N2	
DIFFIO_RX_T39p,DQ5T	F9	HSMA_RX_D_P8	
DIFFIO_RX_T39n,DQ5T	F8	HSMA_RX_D_N8	
DIFFIO_TX_T40p,DQ5T	G7	I2C_SCL_FPGA	(16,20,26) I2C_SCL
DIFFIO_TX_T40n	F6	I2C_SDA_FPGA	(16,20,26) I2C_SDA

5CSXFC6D_F896

R427
R426

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121	
Title	Cyclone V SoC FPGA Development Kit Board
Size: B	Document Number: 150-0321003-D1 (6XX-44184R) Rev: D1
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Cyclone V GX SoC Transceivers and Power

U21M

Cyclone V GX SoC Transceiver

GXB_L0

PCIE_RX_P0 (3)	AE2	GXB_RX_L0p,GXB_REFCLK_L0p	GXB_TX_L0p AD4 (3) PCIE_TX_P0
PCIE_RX_N0 (3)	AE1	GXB_RX_L0n,GXB_REFCLK_L0n	GXB_TX_L0n AD3 (3) PCIE_TX_N0
PCIE_RX_P1 (3)	AC2	GXB_RX_L1p,GXB_REFCLK_L1p	GXB_TX_L1p AB4 (3) PCIE_TX_P1
PCIE_RX_N1 (3)	AC1	GXB_RX_L1n,GXB_REFCLK_L1n	GXB_TX_L1n AB3 (3) PCIE_TX_N1
PCIE_RX_P2 (3)	AA2	GXB_RX_L2p,GXB_REFCLK_L2p	GXB_TX_L2p Y4 (3) PCIE_TX_P2
PCIE_RX_N2 (3)	AA1	GXB_RX_L2n,GXB_REFCLK_L2n	GXB_TX_L2n Y3 (3) PCIE_TX_N2
PCIE_REFCLK_QL0_P (10)	W8	REFCLK0Lp	
PCIE_REFCLK_QL0_N (10)	W7	REFCLK0Ln	

CMU PLL (PCIe)

GXB_L1

PCIE_RX_P3 (3)	W2	GXB_RX_L3p,GXB_REFCLK_L3p	GXB_TX_L3p V4 (3) PCIE_TX_P3
PCIE_RX_N3 (3)	W1	GXB_RX_L3n,GXB_REFCLK_L3n	GXB_TX_L3n V3 (3) PCIE_TX_N3
	U2	GXB_RX_L4p,GXB_REFCLK_L4p	GXB_TX_L4p T4 GXB_TX_L4_P
	U1	GXB_RX_L4n,GXB_REFCLK_L4n	GXB_TX_L4n T3 GXB_TX_L4_N
HSMA_RX_P0 (17)	R2	GXB_RX_L5p,GXB_REFCLK_L5p	GXB_TX_L5p P4 (17) HSMA_TX_P0
HSMA_RX_N0 (17)	R1	GXB_RX_L5n,GXB_REFCLK_L5n	GXB_TX_L5n P3 (17) HSMA_TX_N0
CLK_148_P	T9	REFCLK1Lp	
CLK_148_N	T8	REFCLK1Ln	

GXB_L2

HSMA_RX_P1 (17)	N2	GXB_RX_L6p,GXB_REFCLK_L6p	GXB_TX_L6p M4 (17) HSMA_TX_P1
HSMA_RX_N1 (17)	N1	GXB_RX_L6n,GXB_REFCLK_L6n	GXB_TX_L6n M3 (17) HSMA_TX_N1
HSMA_RX_P2 (17)	L2	GXB_RX_L7p,GXB_REFCLK_L7p	GXB_TX_L7p K4 (17) HSMA_TX_P2
HSMA_RX_N2 (17)	L1	GXB_RX_L7n,GXB_REFCLK_L7n	GXB_TX_L7n K3 (17) HSMA_TX_P3
HSMA_RX_P3 (17)	J2	GXB_RX_L8p,GXB_REFCLK_L8p	GXB_TX_L8p H4 (17) HSMA_TX_N3
HSMA_RX_N3 (17)	J1	GXB_RX_L8n,GXB_REFCLK_L8n	GXB_TX_L8n H3
REFCLK_QL2_P (10)	P9	REFCLK2Lp	
REFCLK_QL2_N (10)	P8	REFCLK2Ln	
		RREF_TL	G1 XCVR_RREF_TL

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

R413 2.00K 1%

CAD Note:
Place resistor near RREF_TL pins.
Route away frm aggressor

(20) SDI_RX_P
(20) SDI_RX_N
SDI_RX_P
SDI_RX_N
R137 0
R135 0
GXB_RX_L4_P
GXB_RX_L4_N

CAD Note:
Overlap R137 & R138
Overlap R135 & R136

R138 DNI
R136 DNI

SMA Connector Interface

J19
1 OPTION_SMA_XCVR_RX_P
J18
1 OPTION_SMA_XCVR_RX_N

CAD Note:
Place resistors & capacitors near SMA connectors

R62 DNI
R60 DNI
R61 0
R63 0
SDI_TX_P
SDI_TX_N
(20) SDI_TX_P
(20) SDI_TX_N

CAD Note:
Overlap R22 & R27
Overlap R24 & R19

SMA Connector Interface

OPTION_SMA_XCVR_TX_P 1 J10
OPTION_SMA_XCVR_TX_N 1 J11

CAD Note:
Place resistors & capacitors near SMA connectors

SDI Reference Clocks

2.5V_REG_HPS
C62 0.1uF
C66 10uF
R54 DNI
From MAXV
X3
SI571_EN (16) 2 OE
I2C_SDA_MAX (10,16) 7 SDA
I2C_SCL_MAX (10,16) 8 SCL
3 GND
VDD 6
CLK+ 4 CLK_148_CP C64 0.1uF CLK_148_P
CLK- 5 CLK_148_CN C65 0.1uF CLK_148_N
VC 1 SI571_VCONTROL
Si571
LVDS
SDI_CLK148_UP (4) R58 4.99K C53 1000pF
From FPGA
SDI_CLK148_DN (4) R59 4.99K R57 180K C50 0.1uF

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121	
Title	Cyclone V SoC FPGA Development Kit Board
Size B	Document Number 150-0321003-D1 (6XX-44184R) Rev D1
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Cyclone V GX SoC Clocks

HSMA_CLK_IN_P2 — R412 100, 1% — HSMA_CLK_IN_N2

U21N

Cyclone V GX SoC Clocks

1.5 Volt
Bank 3B

(10) CLK_BOT1		AF15	CLK0n,FPLL_BL_FBn,DIFFIO_RX_B31n
CLK_BOT1 — R453 0 — R456 DNI		AF14	CLK0p,FPLL_BL_FBp,DIFFIO_RX_B31p
			FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB,DIFFIO_TX_B37p,DQ5B,B_A_2 — AH12 DDR3_FPGA_A2
			FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn,DIFFIO_TX_B37n,DQ5B,B_A_3 — AJ12 DDR3_FPGA_A3
USER_LED_FPGA[3:0] (4,23)	USER_LED_FPGA1	Y16	CLK1n,DIFFIO_RX_B39n
	USER_LED_FPGA2	W15	CLK1p,DIFFIO_RX_B39p

(4,13) DDR3_FPGA_A[14:0]

1.5 Volt
Bank 4A

	USER_LED_FPGA3	AB17	CLK2n,DIFFIO_RX_B47n
CLK_ENET_FPGA_PHY (10)	CLK_ENET_FPGA_PHY	AA16	CLK2p,DIFFIO_RX_B47p
(10) CLK_50M_FPGA		AD17	CLK3n,DIFFIO_RX_B55n
	CLK_50M_FPGA	AC18	CLK3p,DIFFIO_RX_B55p

2.5 Volt
Bank 5B

(10) CLK_TOP1	CLK_TOP1	AA26	CLK5p,DIFFIO_RX_R21p,DQS3R
(10) CLK_100M_FPGA	CLK_100M_FPGA	AB27	CLK5n,DIFFIO_RX_R21n,DQSn3R
			FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB,DIFFIO_TX_R22p — AE29 PCIE_SMBCLK — PCIE_SMBCLK — PCIE_SMBCLK (3)
(10) CLK_ENET_FPGA_P	CLK_ENET_FPGA_P	Y26	CLK4p,FPLL_BR_FBp,DIFFIO_RX_R23p,DQ3R
(10) CLK_ENET_FPGA_N	CLK_ENET_FPGA_N	Y27	CLK4n,FPLL_BR_FBn,DIFFIO_RX_R23n,DQ3R
			FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn,DIFFIO_TX_R22n,DQ3R — AD29 (3) PCIE_PRSNT2_X1

2.5 Volt
Bank 8A

(17) HSMA_CLK_IN_P2	HSMA_CLK_IN_P2	H15	CLK7p,DIFFIO_RX_T1p
(17) HSMA_CLK_IN_N2	HSMA_CLK_IN_N2	G15	CLK7n,DIFFIO_RX_T1n
			FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn,DIFFIO_TX_T4n,DQ1T — A10 HSMA_CLK_OUT0 — (17) HSMA_CLK_OUT0
(17) HSMA_CLK_IN0	HSMA_CLK_IN0	K14	CLK6p,FPLL_TL_FBp,DIFFIO_RX_T9p
(3) PCIE_SMBDAT	PCIE_SMBDAT	J14	CLK6n,FPLL_TL_FBn,DIFFIO_RX_T9n
			FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB,DIFFIO_TX_T4p,DQ1T — A11 (3) PCIE_PRSNT2_X4

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121		
Title: Cyclone V SoC FPGA Development Kit Board		
Size: B	Document Number: 150-0321003-D1 (6XX-44184R)	Rev: D1
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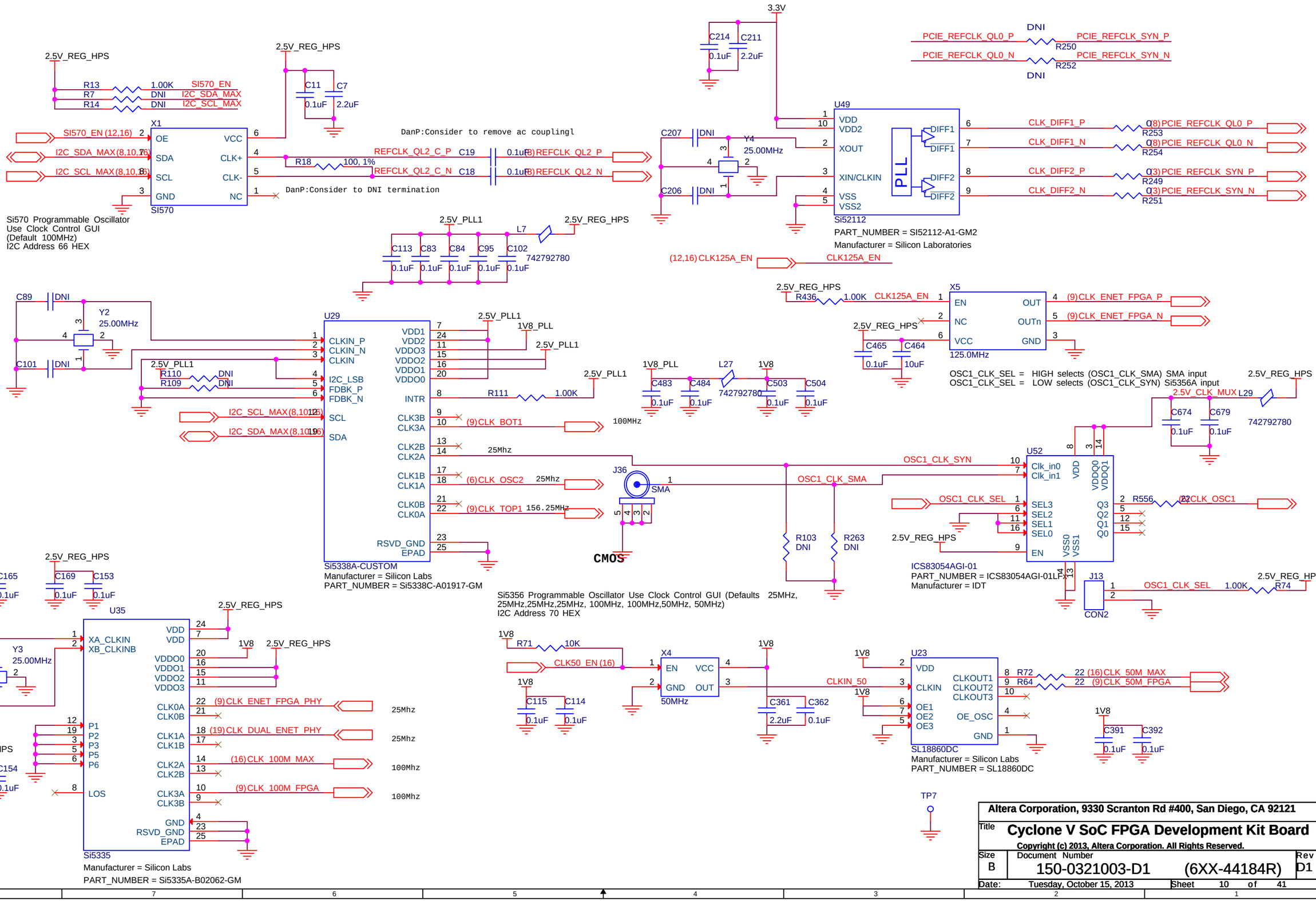
PLL



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121	
Title	Cyclone V SoC FPGA Development Kit Board
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Size: B	Document Number: 150-0321003-D1 (6XX-44184R) Rev: D1
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Cyclone V GX SoC Configuration

FPGA_DCLK — R433 DNI — C463 DNI

R432 DNI

U21G

Cyclone V GX SoC Configuration

Bank 3A — 2.5V BANK

JTAG_FPGA_TMS(12)	V9	TMS
JTAG_MUX_TCK(12,16,17)	AC5	TCK
JTAG_FPGA_TDI(12)	U8	TDI
JTAG_FPGA_TDO(12)	AB9	TDO
	AD7	CLKUSR,DIFFIO_RX_B5p,DQ1B
FPGA_DCLK (15,16)	U7	DCLK
FPGA_CONFIG_D0	AE6	AS_DATA0,ASDO,DATA0
FPGA_CONFIG_D1	AE5	AS_DATA1,DATA1
FPGA_CONFIG_D2	AE8	AS_DATA2,DATA2
FPGA_CONFIG_D3	AC7	AS_DATA3,DATA3
FPGA_CONFIG_D4	AB8	nCSO,DATA4
FPGA_CONFIG_D5	AE9	DATA5,DIFFIO_TX_B2n
FPGA_CONFIG_D6	AE12	DATA6,DIFFIO_RX_B1n,DQ1B
FPGA_CONFIG_D7	AD9	DATA7,DIFFIO_TX_B2p,DQ1B
FPGA_CONFIG_D8	AD11	DATA8,DIFFIO_RX_B1p,DQ1B
FPGA_CONFIG_D9	AF10	DATA9,DIFFIO_TX_B4n,DQ1B
FPGA_CONFIG_D10	AD10	DATA10,DIFFIO_RX_B3n,DQSn1B
FPGA_CONFIG_D11	AE11	DATA11,DIFFIO_TX_B4p
FPGA_CONFIG_D12	AC9	DATA12,DIFFIO_RX_B3p,DQS1B
FPGA_CONFIG_D13	AH4	DATA13,DIFFIO_TX_B6n,DQ1B
FPGA_CONFIG_D14	AE7	DATA14,DIFFIO_RX_B5n,DQ1B
FPGA_CONFIG_D15	AG3	DATA15,DIFFIO_TX_B6p,DQ1B

FPGA_CONFIG_D[15:0] (15,16)

	AG8	PR_READY,DIFFIO_TX_B8n,DQ1B
	AF5	PR_DONE,DIFFIO_RX_B7n
	AF4	PR_ERROR,DIFFIO_RX_B7p

Bank 5A — 2.5V BANK

	AH28	PR_REQUEST,DIFFIO_TX_R1n,DQ1R
	AH29	CvP_CONFDONE,DIFFIO_TX_R3n,DQ1R
	AC25	CRC_ERROR,DIFFIO_RX_R2n
CPU_RESETn (16,23)	AD27	DEV_CLRn,DIFFIO_TX_R5n,DQ1R
(16) MAX_FPGA_MOSI — MAX_FPGA_MOSI	AE26	DEV_OE,DIFFIO_TX_R5p
	W21	nPERSTL0,DIFFIO_RX_R6p,DQS1R
	W22	nPERSTR0,DIFFIO_RX_R6n,DQSn1R
(16) MAX_FPGA_MISO — MAX_FPGA_MISO	AD25	INIT_DONE,DIFFIO_RX_R2p
	AJ29	nCEO,DIFFIO_TX_R3p,DQ1R

Bank 9A — 2.5V BANK

FPGA_nCONFIG (16)	J5	nCONFIG
FPGA_nSTATUS(16)	F4	nSTATUS
FPGA_CONF_DONE (16)	F3	CONF_DONE
	G5	nCE
	L9	MSEL4
	L7	MSEL3
	G6	MSEL2
	K6	MSEL1
	L8	MSEL0

5CSXFC6D_F896
Manufacturer = Altera Corp
PART_NUMBER = 5CGXFC7D7F31C8NES

MAX_FPGA_SSEL — MAX_FPGA_SSEL(16)

MAX_FPGA_SCK — MAX_FPGA_SCK(16)

(16) MSEL4, (16) MSEL3, (16) MSEL2, (16) MSEL1, (16) MSEL0

(16) FPGA_PR_READY, (16) FPGA_PR_DONE, (16) FPGA_PR_ERROR

(16) FPGA_PR_REQUEST, (16) FPGA_CvP_CONFDONE

(3) PCIE_WAKEn, (3,4) PCIE_PERSTn

2.5V_REG_FPGA

R459 10K, R457 10K, R458 10K, R248 10K

2.5V_REG_FPGA

R397 10K FPGA_nSTATUS

R411 10K FPGA_CONF_DONE

R415 10K FPGA_nCONFIG

R414 10K JTAG_FPGA_TDI

USER I/O INTERFACES

SW3 — TDA06H0SB1

1	12	MSEL0	R306	1.00k	2.5V_REG_FPGA
2	11	MSEL1	R305	1.00k	
3	10	MSEL2	R304	1.00k	
4	9	MSEL3	R303	1.00k	
5	8	MSEL4	R302	1.00k	
6	7				

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone V SoC FPGA Development Kit Board

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

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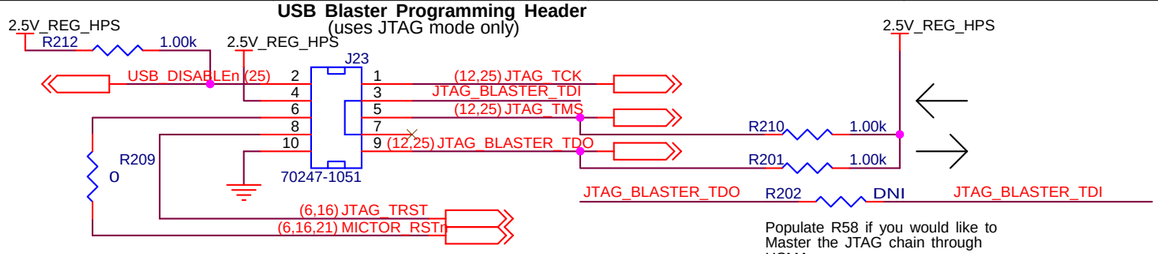
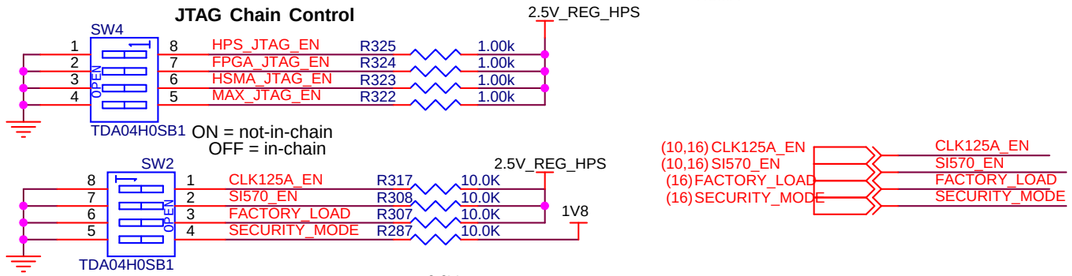
JTAG

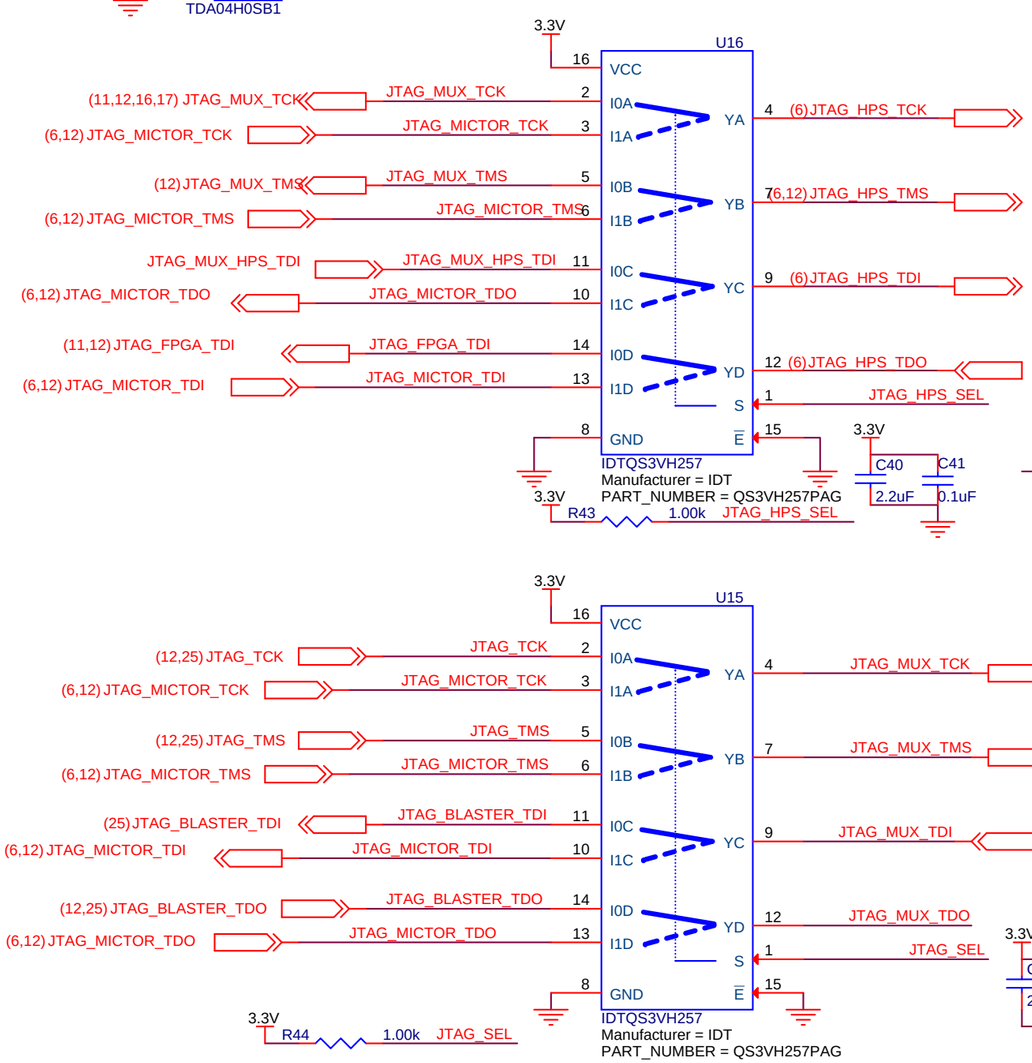
USB Blaster Programming Header
(uses JTAG mode only)



Populate R58 if you would like to Master the JTAG chain through HSMA

JTAG Chain Control





TS5A23157 Switch Functions

When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

Logic 0 = pin 10 <--> pin 9 (HPS Bypass)
Logic 1 = pin 10 <--> pin 2 (HPS Enable)

Logic 0 = pin 6 <--> pin 7 (HPS Bypass)
Logic 1 = pin 6 <--> pin 4 (HPS Enable)

Logic 0 = pin 10 <--> pin 9 (FPGA Bypass)
Logic 1 = pin 10 <--> pin 2 (FPGA Enable)

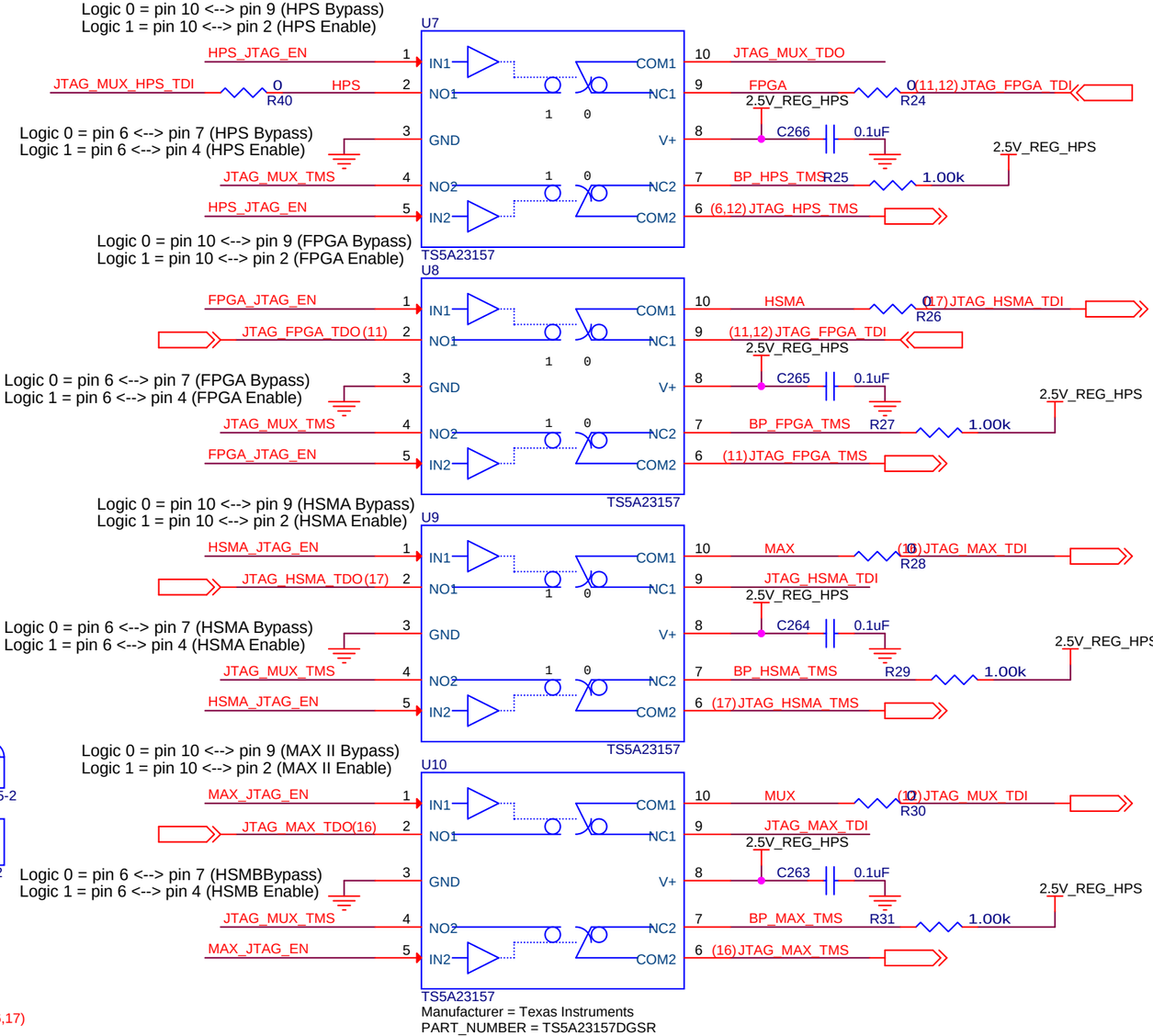
Logic 0 = pin 6 <--> pin 7 (FPGA Bypass)
Logic 1 = pin 6 <--> pin 4 (FPGA Enable)

Logic 0 = pin 10 <--> pin 9 (HSMA Bypass)
Logic 1 = pin 10 <--> pin 2 (HSMA Enable)

Logic 0 = pin 6 <--> pin 7 (HSMA Bypass)
Logic 1 = pin 6 <--> pin 4 (HSMA Enable)

Logic 0 = pin 10 <--> pin 9 (MAX II Bypass)
Logic 1 = pin 10 <--> pin 2 (MAX II Enable)

Logic 0 = pin 6 <--> pin 7 (HSMBBypass)
Logic 1 = pin 6 <--> pin 4 (HSMB Enable)



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Cyclone V SoC FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

Date: Tuesday, October 15, 2013 Sheet 12 of 41

1024MB DDR3 (x32) - FPGA

DDR3_FPGA_CLK_P — 100, 1% — R469 — DDR3_FPGA_CLK_N

DDR3_FPGA_BA[2:0] (4)
DDR3_FPGA_DM[3:0] (4)
DDR3_FPGA_DQS_P[3:0] (4)
DDR3_FPGA_DQS_N[3:0] (4)
DDR3_FPGA_DQ[31:0] (4)
DDR3_FPGA_A[14:0] (4,9)

VTT_FPGA_DDR3 — CN6 — 0.1uF
VTT_FPGA_DDR3 — CN4 — 0.1uF
VTT_FPGA_DDR3 — CN5 — 0.1uF

V31	DDR3_FPGA_A11	RN4A	1	16	51
V30	DDR3_FPGA_A1	RN4D	4	13	51
V32	DDR3_FPGA_BA1	RN4G	7	10	51
V28	DDR3_FPGA_A9	RN5B	2	15	51
V10	DDR3_FPGA_ODT	RN5E	5	12	51
V31	DDR3_FPGA_A14	RN5H	8	9	51
V16	DDR3_FPGA_BA2	RN6C	3	14	51
V24	DDR3_FPGA_A5	RN6F	6	11	51
V2	DDR3_FPGA_CKE	R472		4.70K, 1%	

VTT_FPGA_DDR3

V38	DDR3_FPGA_A8	RN4B	2	15	51
V33	DDR3_FPGA_A4	RN4E	5	12	51
V19	DDR3_FPGA_A10	RN4H	8	9	51
V36	DDR3_FPGA_A13	RN5C	3	14	51
V12	DDR3_FPGA_CASn	RN5F	6	11	51
V15	DDR3_FPGA_CSn	RN6A	1	16	51
V23	DDR3_FPGA_A3	RN6D	4	13	51
		RN6G	7	10	51
	DDR3_FPGA_RESETn	2.00K		R497	

VTT_FPGA_DDR3 — 1.5V_REG_FPGA

V34	DDR3_FPGA_A6	RN4C	3	14	51
V29	DDR3_FPGA_A12	RN4F	6	11	51
V25	DDR3_FPGA_A7	RN5A	1	16	51
V17	DDR3_FPGA_WEn	RN5D	4	13	51
V11	DDR3_FPGA_RASn	RN5G	7	10	51
V16	DDR3_FPGA_BA0	RN6B	2	15	51
V26	DDR3_FPGA_A0	RN6E	5	12	51
V27	DDR3_FPGA_A2	RN6H	8	9	51

U37
MT41K256M16HA-125:E
Manufacturer = Micron
PART_NUMBER = MT41K256M16HA-125:E

DDR3_FPGA_A0	N3	A0		E3	DDR3_FPGA_DQ16
DDR3_FPGA_A1	P7	A1	DQ0	F7	DDR3_FPGA_DQ21
DDR3_FPGA_A2	P3	A2	DQ1	F2	DDR3_FPGA_DQ17
DDR3_FPGA_A3	N2	A3	DQ2	F8	DDR3_FPGA_DQ19
DDR3_FPGA_A4	P8	A4	DQ3	H3	DDR3_FPGA_DQ20
DDR3_FPGA_A5	P2	A5	DQ4	H8	DDR3_FPGA_DQ18
DDR3_FPGA_A6	R8	A6	DQ5	G2	DDR3_FPGA_DQ22
DDR3_FPGA_A7	R2	A7	DQ6	H7	DDR3_FPGA_DQ23
DDR3_FPGA_A8	T8	A8	DQ7	D7	DDR3_FPGA_DQ24
DDR3_FPGA_A9	R3	A9	DQ8	C3	DDR3_FPGA_DQ26
DDR3_FPGA_A10	L7	A10/AP	DQ9	C8	DDR3_FPGA_DQ25
DDR3_FPGA_A11	R7	A11	DQ10	C2	DDR3_FPGA_DQ27
DDR3_FPGA_A12	N7	A12/BCn	DQ11	A7	DDR3_FPGA_DQ29
DDR3_FPGA_A13	T3	A13	DQ12	A2	DDR3_FPGA_DQ30
DDR3_FPGA_A14	T7	A14	DQ13	B8	DDR3_FPGA_DQ28
			DQ14	A3	DDR3_FPGA_DQ31
DDR3_FPGA_CKE	K9	CKE	DQ15		
DDR3_FPGA_CLK_P	J7	CK_P		F3	DDR3_FPGA_DQS_P2
DDR3_FPGA_CLK_N	K7	CK_N	LDQS_P	G3	DDR3_FPGA_DQS_N2
			LDQS_N	C7	DDR3_FPGA_DQS_P3
DDR3_FPGA_DM2	E7	LDM	UDQS_P	B7	DDR3_FPGA_DQS_N3
DDR3_FPGA_DM3	D3	UDM	UDQS_N		
DDR3_FPGA_CSn	L2	CS		J1	
DDR3_FPGA_WEn	L3	WE	NC1	J9	
DDR3_FPGA_RASn	J3	RAS	NC2	L1	
DDR3_FPGA_CASn	K3	CAS	NC3	L9	
			NC4	M7	
DDR3_FPGA_BA0	M2	BA0	NC5		
DDR3_FPGA_BA1	N8	BA1			
DDR3_FPGA_BA2	M3	BA2			
DDR3_FPGA_RESETn	T2	RESETn			
DDR3_FPGA_ODT	K1	ODT			
DDR3_FPGA_ZQ1	L8	ZQ			
			VSSQ	B1	
VREF_FPGA_DDR3	H1	VREFDQ	VSSQ	B9	
	M8	VREFCA	VSSQ	D1	
			VSSQ	D8	
	B2	VDD	VSSQ	E2	
	D9	VDD	VSSQ	E8	
	G7	VDD	VSSQ	F9	
	K2	VDD	VSSQ	G1	
	K8	VDD	VSSQ	G9	
	N1	VDD			
	N9	VDD	VSS	J2	
	R1	VDD	VSS	J8	
	R9	VDD	VSS	A9	
1.5V_REG_FPGA			VSS	M1	
	A1	VDDQ	VSS	M9	
	A8	VDDQ	VSS	B3	
	C1	VDDQ	VSS	P1	
	C9	VDDQ	VSS	P9	
	D2	VDDQ	VSS	E1	
	E9	VDDQ	VSS	T1	
	F1	VDDQ	VSS	T9	
	H2	VDDQ	VSS	G8	
	H9	VDDQ			

R473 240 — C590 0.1uF

U38
DDR3 Device
MT41K256M16HA-125:E
Manufacturer = Micron
PART_NUMBER = MT41K256M16HA-125:E

DDR3_FPGA_A0	N3	A0		E3	DDR3_FPGA_DQ0
DDR3_FPGA_A1	P7	A1	DQ0	F7	DDR3_FPGA_DQ1
DDR3_FPGA_A2	P3	A2	DQ1	F2	DDR3_FPGA_DQ2
DDR3_FPGA_A3	N2	A3	DQ2	F8	DDR3_FPGA_DQ3
DDR3_FPGA_A4	P8	A4	DQ3	H3	DDR3_FPGA_DQ4
DDR3_FPGA_A5	P2	A5	DQ4	H8	DDR3_FPGA_DQ5
DDR3_FPGA_A6	R8	A6	DQ5	G2	DDR3_FPGA_DQ6
DDR3_FPGA_A7	R2	A7	DQ6	H7	DDR3_FPGA_DQ7
DDR3_FPGA_A8	T8	A8	DQ7	D7	DDR3_FPGA_DQ8
DDR3_FPGA_A9	R3	A9	DQ8	C3	DDR3_FPGA_DQ9
DDR3_FPGA_A10	L7	A10/AP	DQ9	C8	DDR3_FPGA_DQ10
DDR3_FPGA_A11	R7	A11	DQ10	C2	DDR3_FPGA_DQ11
DDR3_FPGA_A12	N7	A12/BCn	DQ11	A7	DDR3_FPGA_DQ12
DDR3_FPGA_A13	T3	A13	DQ12	A2	DDR3_FPGA_DQ13
DDR3_FPGA_A14	T7	A14	DQ13	B8	DDR3_FPGA_DQ14
			DQ14	A3	DDR3_FPGA_DQ15
DDR3_FPGA_CKE	K9	CKE	DQ15		
DDR3_FPGA_CLK_P	J7	CK_P		F3	DDR3_FPGA_DQS_P0
DDR3_FPGA_CLK_N	K7	CK_N	LDQS_P	G3	DDR3_FPGA_DQS_N0
			LDQS_N	C7	DDR3_FPGA_DQS_P1
DDR3_FPGA_DM0	E7	LDM	UDQS_P	B7	DDR3_FPGA_DQS_N1
DDR3_FPGA_DM1	D3	UDM	UDQS_N		
DDR3_FPGA_CSn	L2	CS		J1	
DDR3_FPGA_WEn	L3	WE	NC1	J9	
DDR3_FPGA_RASn	J3	RAS	NC2	L1	
DDR3_FPGA_CASn	K3	CAS	NC3	L9	
			NC4	M7	
DDR3_FPGA_BA0	M2	BA0	NC5		
DDR3_FPGA_BA1	N8	BA1			
DDR3_FPGA_BA2	M3	BA2			
DDR3_FPGA_RESETn	T2	RESETn			
DDR3_FPGA_ODT	K1	ODT			
DDR3_FPGA_ZQ	L8	ZQ			
			VSSQ	B1	
VREF_FPGA_DDR3	H1	VREFDQ	VSSQ	B9	
	M8	VREFCA	VSSQ	D1	
			VSSQ	D8	
	B2	VDD	VSSQ	E2	
	D9	VDD	VSSQ	E8	
	G7	VDD	VSSQ	F9	
	K2	VDD	VSSQ	G1	
	K8	VDD	VSSQ	G9	
	N1	VDD			
	N9	VDD	VSS	J2	
	R1	VDD	VSS	J8	
	R9	VDD	VSS	A9	
1.5V_REG_FPGA			VSS	M1	
	A1	VDDQ	VSS	M9	
	A8	VDDQ	VSS	B3	
	C1	VDDQ	VSS	P1	
	C9	VDDQ	VSS	P9	
	D2	VDDQ	VSS	E1	
	E9	VDDQ	VSS	T1	
	F1	VDDQ	VSS	T9	
	H2	VDDQ	VSS	G8	
	H9	VDDQ			

R471 240 — C586 0.1uF

(4) DDR3_FPGA_CKE
(4) DDR3_FPGA_CLK_P
(4) DDR3_FPGA_CLK_N
(4) DDR3_FPGA_DM2
(4) DDR3_FPGA_DM3
(4) DDR3_FPGA_CSn
(4) DDR3_FPGA_WEn
(4) DDR3_FPGA_RASn
(4) DDR3_FPGA_CASn
(4) DDR3_FPGA_BA0
(4) DDR3_FPGA_BA1
(4) DDR3_FPGA_BA2
(4) DDR3_FPGA_RESETn
(4) DDR3_FPGA_ODT
(4) DDR3_FPGA_DM0
(4) DDR3_FPGA_DM1

1.5V_REG_FPGA

C568	C602	C572	C585	C601	C571	C598	C569	C589	C583	C597	C570	C574	C587
2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	2.2nF	3.3nF	3.3nF	4.7nF	4.7nF	4.7nF

1.5V_REG_FPGA

C600	C599	C603	C577	C596	C576	C579	C575	C578	C588	C584
0.01uF	0.01uF	0.01uF	0.1uF	0.1uF	0.1uF	0.1uF	0.47uF	0.47uF	0.47uF	0.47uF

ALTERA

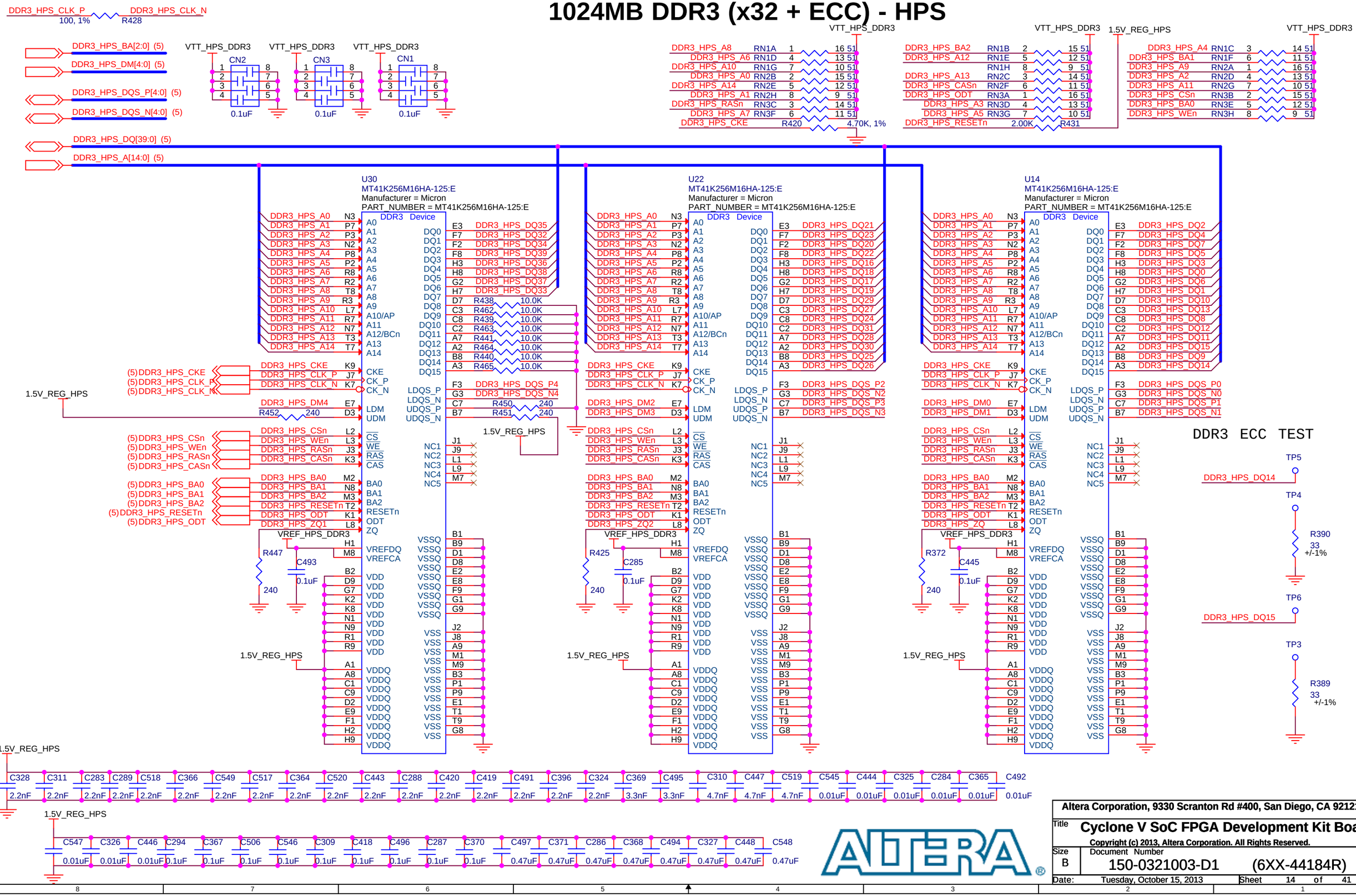
Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone V SoC FPGA Development Kit Board

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

Date: Tuesday, October 15, 2013 — Sheet 13 of 41

1024MB DDR3 (x32 + ECC) - HPS



FLASH, EPCQ

EPCQ

3.3V

C316 0.1uF

C315 0.1uF

U20

NC01 NC02 NC03 NC04 NC05 NC06 NC07 NC08

VCC 2

GND 10

DATA0 15 FPGA_AS_DATA0

DATA1 8 FPGA_AS_DATA1

DATA2 9 FPGA_AS_DATA2

DATA3 1 FPGA_AS_DATA3

DCLK 16 (11,16) FPGA_DCLK

nCS 7 FPGA_nCSO

EPCQ256
Manufacturer = Altera
PART_NUMBER = EPCQ256SI16N

5.0V

C30 0.1uF

C31 0.1uF

U13

NC 1 | VCC 24

FPGA_AS_DATA0 2 A0 | B0 22 FPGA_CONFIG_D0 — FPGA_CONFIG_D0 (11,16)

FPGA_AS_DATA1 3 A1 | B1 21 FPGA_CONFIG_D1 — FPGA_CONFIG_D1 (11,16)

FPGA_AS_DATA2 4 A2 | B2 20 FPGA_CONFIG_D2 — FPGA_CONFIG_D2 (11,16)

FPGA_AS_DATA3 5 A3 | B3 19 FPGA_CONFIG_D3 — FPGA_CONFIG_D3 (11,16)

FPGA_nCSO 6 A4 | B4 18 FPGA_CONFIG_D4 — FPGA_CONFIG_D4 (11,16)

7 A5 | B5 17

8 A6 | B6 16

9 A7 | B7 15

10 A8 | B8 14

11 A9 | B9 13

BE 23 | GND 12

IDTQS3861
Manufacturer = IDT
PART_NUMBER = IDTQS3861QG

MAX_AS_CONF(16)

FM BUS

FM_D[15:0] (16)

FM_A[26:1] (16)

NOR PARALLEL FLASH

FLASH 512Mb (32M X 16)

U6

PC28FxxxP30B85
FLASH

FM_A1 A1 | FM_A2 B1 | FM_A3 C1 | FM_A4 D1 | FM_A5 D2 | FM_A6 A2 | FM_A7 C2 | FM_A8 A3 | FM_A9 B3 | FM_A10 C3 | FM_A11 D3 | FM_A12 C4 | FM_A13 A5 | FM_A14 B5 | FM_A15 C5 | FM_A16 D7 | FM_A17 D8 | FM_A18 A7 | FM_A19 B7 | FM_A20 C7 | FM_A21 C8 | FM_A22 A8 | G1 | H8 | B6 | B8

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22

NC(64M)/A23
NC(64M,128M)/A24
NC/A25(512M)
NC/A26(1G)

FLASH_CLK (16) E6 CLK

FLASH_RESETn (16) D4 RESET#

FLASH_CEn0 (16) B4 CE#

FLASH_OEn (16) F8 OE#

FLASH_WEn (16) G8 WE#

FLASH_ADVn (16) F6 ADV#

FLASH_WPn C6 WP#

VPP A4

VCC A6 | VCC H3

VCCQ D5 | VCCQ D6 | VCCQ G4

D0 F2 FM_D0 | D1 E2 FM_D1 | D2 G3 FM_D2 | D3 E4 FM_D3 | D4 E5 FM_D4 | D5 G5 FM_D5 | D6 G6 FM_D6 | D7 H7 FM_D7

D8 E1 FM_D8 | D9 E3 FM_D9 | D10 F3 FM_D10 | D11 F4 FM_D11 | D12 F5 FM_D12 | D13 H5 FM_D13 | D14 G7 FM_D14 | D15 E7 FM_D15

WAIT F7 (16) FLASH_RDYBSYn

GND B2 | GND H2 | GND H4 | GND H6 | GND

RFU0 H1 | RFU1 G2 | RFU2 F1 | RFU3 E8

1V8 1V8 1V8

PC28F512P30BF
Manufacturer = Micron
PART_NUMBER = PC28F512P30BFA

XJ1

881545-2

J5

1 2

CON2

9V_VPP

VPP

12V

U4

VIN 1 | VOUT 5

ADJ/BYPASS 4

SHDN 3 | GND 2

4.7K R335

LT1761_CSENSE

R333 36K

R334 5.62k

C22 4.7uF

C17 4.7uF

LT1761
PART_NUMBER = LT1761ES5-SD#PBF
Manufacturer = Linear Technology

VPP D13 1V8

CMDSH-3

1V8

R363 10K FLASH_WPn

R336 10K FLASH_WEn

R326 10K FLASH_RDYBSYn

R362 10K FLASH_RESETn

1V8 C246 0.1uF

1V8 C247 0.1uF | C257 0.1uF | C253 0.1uF | C268 0.1uF | C267 0.1uF

- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Cyclone V SoC FPGA Development Kit Board

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

Date: Tuesday, October 15, 2013 Sheet 15 of 41

5M2210 System Controller

U19A — MAX V BANK1

FPGA_CONFIG_D0	D3	DIFFIO_L1P	DIFFIO_L13P	J4	FPGA_nSTATUS
FPGA_CONFIG_D1	C2	DIFFIO_L1N	DIFFIO_L13N	K1	FPGA_CONF_DONE
FPGA_CONFIG_D2	C3	DIFFIO_L2P	DIFFIO_L14P	J3	FPGA_DCLK
FPGA_CONFIG_D3	E3	DIFFIO_L2N	DIFFIO_L14N	K2	
FPGA_CONFIG_D4	D2	DIFFIO_L3P	DIFFIO_L15P	K5	
FPGA_CONFIG_D5	E4	DIFFIO_L3N	DIFFIO_L15N	L1	
FPGA_CONFIG_D6	D1	DIFFIO_L4P	DIFFIO_L16P	L2	0 R552 (12) JTAG_TRST
FPGA_CONFIG_D7	E5	DIFFIO_L4N	DIFFIO_L16N	K3	0 R546 (21) MICTOR_RSTn
FPGA_CONFIG_D8	F3	DIFFIO_L5P	DIFFIO_L17P	M1	I2C_SCL_MAX
FPGA_CONFIG_D9	E1	DIFFIO_L5N	DIFFIO_L17N	M2	I2C_SDA_MAX
FPGA_CONFIG_D10	F4	DIFFIO_L6P	DIFFIO_L18P	L4	
FPGA_CONFIG_D11	F2	DIFFIO_L6N	DIFFIO_L18N	L3	
FPGA_CONFIG_D12	F1	DIFFIO_L7P	DIFFIO_L19P	N1	FPGA_nCONFIG
FPGA_CONFIG_D13	F6	DIFFIO_L7N	DIFFIO_L19N	M4	
FPGA_CONFIG_D14	G2	DIFFIO_L8P	DIFFIO_L20P	N2	
FPGA_CONFIG_D15	G3	DIFFIO_L8N	DIFFIO_L20N	M3	
MAX_FPGA_MOSI	G1	DIFFIO_L9P	DIFFIO_L21P	N3	FPGA_CvP_CONFDONE
MAX_FPGA_MISO	G4	DIFFIO_L9N	DIFFIO_L21N	P2	FPGA_PR_ERROR
MAX_AS_CONF	H2	DIFFIO_L10P			
MAX_FPGA_SSEL	G5	DIFFIO_L10N	IOB1_1	E2	FPGA_PR_READY
MAX_FPGA_SCK	H3	DIFFIO_L11P	IOB1_2	F5	FPGA_PR_REQUEST
	J1	DIFFIO_L11N	IOB1_3	H1	FPGA_PR_DONE
	H4	DIFFIO_L12P	IOB1_4	K4	
	J2	DIFFIO_L12N	IOB1_5	L5	M570_PCIE_JTAG_EN
USB_B2_CLK	H5	IOB1/CLK0	TCK	P3	(11,12,17) JTAG_MUX_TCK
CLK_100M_MAX	J5	IOB1/CLK1	TDI	L6	(12) JTAG_MAX_TDI
			TDO	M5	(12) JTAG_MAX_TDO
			TMS	N4	(12) JTAG_MAX_TMS

5M2210ZF256
Manufacturer = Altera Corporation
PART_NUMBER = 5M2210ZF256C4N

U19B — MAX V BANK2

SI571_EN	D4	DIFFIO_T1P	DIFFIO_T13P	E10	(26) OVERTEMP
	B1	DIFFIO_T1N	DIFFIO_T13N	A11	(22) USB_RESET
	C5	DIFFIO_T2P	DIFFIO_T14P	B11	HPS_RESETn
	C4	DIFFIO_T2N	DIFFIO_T14N	A12	
	B4	DIFFIO_T3P	DIFFIO_T15P	E11	MAX_CONF_DONE
	D6	DIFFIO_T3N	DIFFIO_T15N	B12	
	E6	DIFFIO_T4P	DIFFIO_T16P	C11	QSPI_RESETn
	B5	DIFFIO_T4N	DIFFIO_T16N	B13	PGM_SEL
	A5	DIFFIO_T5P	DIFFIO_T17P	D12	PGM_CONFIG
	D7	DIFFIO_T5N	DIFFIO_T17N	B14	PGM_LED0
	B6	DIFFIO_T6P	DIFFIO_T18P	C13	PGM_LED1
	E7	DIFFIO_T6N	DIFFIO_T18N	B16	PGM_LED2
	C8	DIFFIO_T7P			
	B7	DIFFIO_T7N			
	D8	DIFFIO_T8P	IOB2_6	A13	CLK_SEL
	A7	DIFFIO_T8N	IOB2_7	A15	
HSMA_PRSNTn	B8	DIFFIO_T9P	IOB2_8	A2	FACTORY_LOAD
	A8	DIFFIO_T9N	IOB2_9	A4	MAX_ERROR
	A9	DIFFIO_T10P	IOB2_10	A6	MAX_LOAD
CLK50_EN	E9	DIFFIO_T10N	IOB2_11	B10	MSEL0
CLK125A_EN	B9	DIFFIO_T11P	IOB2_12	B3	MSEL1
	D9	DIFFIO_T11N	IOB2_13	C10	MSEL2
Si570_EN	A10	DIFFIO_T12P	IOB2_14	C12	MSEL3
	C9	DIFFIO_T12N	IOB2_15	C6	MSEL4
			IOB2_16	C7	PCIE_JTAG_EN
			IOB2_17	D10	CPU_RESETn
			IOB2_18	D11	SDI_TX_EN
			IOB2_19	D5	SDI_RX_BYPASS
			IOB2_20	E8	SDI_RX_EN

5M2210ZF256
Manufacturer = Altera Corporation
PART_NUMBER = 5M2210ZF256C4N

U19C — MAX V BANK3

FM_A0	E14	DIFFIO_R1P	DIFFIO_R13P	J14	FM_D0
FM_A1	C14	DIFFIO_R1N	DIFFIO_R13N	J15	FM_D1
FM_A2	C15	DIFFIO_R2P	DIFFIO_R14P	K16	FM_D2
FM_A3	E13	DIFFIO_R2N	DIFFIO_R14N	K13	FM_D3
FM_A4	E12	DIFFIO_R3P	DIFFIO_R15P	K15	FM_D4
FM_A5	D15	DIFFIO_R3N	DIFFIO_R15N	K14	FM_D5
FM_A6	F14	DIFFIO_R4P	DIFFIO_R16P	L16	FM_D6
FM_A7	D16	DIFFIO_R4N	DIFFIO_R16N	L11	FM_D7
FM_A8	F13	DIFFIO_R5P	DIFFIO_R17P	L15	FM_D8
FM_A9	E15	DIFFIO_R5N	DIFFIO_R17N	L12	FM_D9
FM_A10	E16	DIFFIO_R6P	DIFFIO_R18P	M16	FM_D10
FM_A11	F15	DIFFIO_R6N	DIFFIO_R18N	L13	FM_D11
FM_A12	G14	DIFFIO_R7P	DIFFIO_R19P	M15	FM_D12
FM_A13	F16	DIFFIO_R7N	DIFFIO_R19N	L14	FM_D13
FM_A14	G13	DIFFIO_R8P	DIFFIO_R20P	N16	FM_D14
FM_A15	G15	DIFFIO_R8N	DIFFIO_R20N	M13	FM_D15
FM_A16	G12	DIFFIO_R9P	DIFFIO_R21P	N15	FLASH_WEn
FM_A17	G16	DIFFIO_R9N	DIFFIO_R21N	N14	FLASH_CEn0
FM_A18	H14	DIFFIO_R10P	DIFFIO_R22P	P15	FLASH_OEn
FM_A19	H15	DIFFIO_R10N	DIFFIO_R22N	P14	FLASH_RDYBSYn
FM_A20	H13	DIFFIO_R11P			
FM_A21	H16	DIFFIO_R11N	IOB3_21	D13	FLASH_RESETn
FM_A22	J13	DIFFIO_R12P	IOB3_22	D14	FLASH_CLK
FM_A23	J16	DIFFIO_R12N	IOB3_23	F11	FLASH_ADVn
			IOB3_24	F12	
			IOB3_25	K12	FM_A24
			IOB3_26	M14	FM_A25
CLK_50M_MAX	J12	IOB3/CLK2	IOB3_27	N13	FM_A26
	H12	IOB3/CLK3			

5M2210ZF256
Manufacturer = Altera Corporation
PART_NUMBER = 5M2210ZF256C4N

U19D — MAX V BANK4

	R1	DIFFIO_B1P	DIFFIO_B14P	M10	
	P4	DIFFIO_B1N	DIFFIO_B14N	R10	
	T2	DIFFIO_B2P	DIFFIO_B15P	N10	
	P5	DIFFIO_B2N	DIFFIO_B15N	T11	
	R3	DIFFIO_B3P	DIFFIO_B16P	P10	
	N5	DIFFIO_B3N	DIFFIO_B16N	P11	
	P6	DIFFIO_B4P	DIFFIO_B17P	T12	
	N6	DIFFIO_B4N	DIFFIO_B17N	N11	
	R5	DIFFIO_B5P	DIFFIO_B19P	T13	EXTRA_SIG1
	M6	DIFFIO_B5N	DIFFIO_B19N	R13	
	T5	DIFFIO_B6P	DIFFIO_B18P	R12	SECURITY_MODE
	P7	DIFFIO_B6N	DIFFIO_B18N	P11	M570_CLOCK
	R6	DIFFIO_B7P	DIFFIO_B20P	N12	FACTORY_STATUS
	N7	DIFFIO_B7N	DIFFIO_B20N	R14	FACTORY_REQUEST
	M7	DIFFIO_B8P	DIFFIO_B21P	P12	
	R7	DIFFIO_B8N	DIFFIO_B21N	T15	EXTRA_SIG2
USB_CFG2	P8	DIFFIO_B9P	DIFFIO_B22P	R16	(25) TRST
USB_CFG3	T7	DIFFIO_B9N	DIFFIO_B22N	P13	(25) RST
USB_CFG4	N8	DIFFIO_B10P	IOB4_28	M11	
USB_CFG5	R8	DIFFIO_B10N	IOB4_29	M12	
USB_CFG6	T8	DIFFIO_B11P	IOB4_30	N9	
USB_CFG7	T9	DIFFIO_B11N	IOB4_31	R4	USB_CFG0
USB_CFG8	R9	DIFFIO_B12P	IOB4_32	T10	USB_CFG11
USB_CFG9	P9	DIFFIO_B12N	IOB4_33	T4	USB_CFG1
MAX_RESETn	M9	DIFFIO_B13N/DEV_CLRn			
USB_CFG10	M8	DIFFIO_B13P/DEV_OE			

5M2210ZF256
Manufacturer = Altera Corporation
PART_NUMBER = 5M2210ZF256C4N

U19E — MAX V Power

F7	GNDINT	VCCINT	F10	1V8
G6	GNDINT	VCCINT	G11	
H7	GNDINT	VCCINT	H10	
H9	GNDINT	VCCINT	H8	
J10	GNDINT	VCCINT	J7	
J8	GNDINT	VCCINT	J9	
K11	GNDINT	VCCINT	K6	
L10	GNDINT	VCCINT	L7	
A1	GNDIO	VCCIO1	C1	2.5V_REG_HPS
A16	GNDIO	VCCIO1	H6	
B15	GNDIO	VCCIO1	J6	
B2	GNDIO	VCCIO1	P1	
G10	GNDIO			
G7	GNDIO	VCCIO2	A14	
G8	GNDIO	VCCIO2	A3	
G9	GNDIO	VCCIO2	F8	
K10	GNDIO	VCCIO2	F9	
K7	GNDIO			1V8
K8	GNDIO	VCCIO3	C16	
K9	GNDIO	VCCIO3	H11	
R15	GNDIO	VCCIO3	J11	
R2	GNDIO	VCCIO3	P16	
T1	GNDIO			1.5V_REG_HPS
T16	GNDIO	VCCIO4	L8	
T6	GNDIO	VCCIO4	L9	
		VCCIO4	T14	
		VCCIO4	T3	

5M2210ZF256
Manufacturer = Altera Corporation
PART_NUMBER = 5M2210ZF256C4N

Connections

- (11,15) FPGA_CONFIG_D[15:0]
- (11) FPGA_nSTATUS
- (11) FPGA_CONF_DONE
- (11,15) FPGA_DCLK
- (11) FPGA_nCONFIG
- (11) FPGA_PR_DONE
- (11) FPGA_PR_REQUEST
- (11) FPGA_PR_READY
- (11) FPGA_PR_ERROR
- (11) FPGA_CvP_CONFDONE
- HPS_RESETn (6,21)
- QSPI_RESETn (21)
- MAX_FPGA_SSEL
- MAX_FPGA_SCK
- MAX_FPGA_SSEL(11)
- MAX_FPGA_SCK(11)
- (5,20) SDI_TX_EN
- (5,20) SDI_RX_BYPASS
- (5,20) SDI_RX_EN
- (10) CLK_50M_MAX
- (10) CLK_100M_MAX
- (15,16) MAX_AS_CONF
- I2C_SCL_MAX — R424 — (7,20,26) I2C_SCL
- I2C_SDA_MAX — R423 — (7,20,26) I2C_SDA
- 2.5V_REG_HPS — R419 10K I2C_SCL_MAX — R418 10K I2C_SDA_MAX
- (8,10) I2C_SCL_MAX
- (8,10) I2C_SDA_MAX
- (15) FM_D[15:0]
- (15) FM_A[26:0]
- (15) FLASH_WEn
- (15) FLASH_CEn0
- (15) FLASH_OEn
- (15) FLASH_RDYBSYn
- (15) FLASH_RESETn
- (15) FLASH_CLK
- (15) FLASH_ADVn
- (10,12) CLK125A_EN
- (10) CLK50_EN
- (10,12) Si570_EN
- (8) Si571_EN
- (11) MSEL0
- (11) MSEL1
- (11) MSEL2
- (11) MSEL3
- (11) MSEL4
- (4,17,23) HSMA_PRSNTn
- MAX_FPGA_MOSI — MAX_FPGA_MOSI(11)
- MAX_FPGA_MISO — MAX_FPGA_MISO(11)
- (11,23) CPU_RESETn
- (15,16) MAX_AS_CONF

ON-BOARD USB BLASTER II

- USB_CFG[11:0] — USB_CFG[11:0] (25)
- EXTRA_SIG[2:0] — EXTRA_SIG[2:0] (25)
- (4,25) USB_B2_CLK
- PCIE_JTAG_EN
- (25) M570_PCIE_JTAG_EN
- (25) M570_CLOCK
- (25) FACTORY_STATUS
- (25) FACTORY_REQUEST

MAXV DIPSWITCH

- CLK_SEL
- (12) FACTORY_LOAD
- (12) SECURITY_MODE

PUSH BUTTON INTERFACE

- PGM_SEL — PGM_SEL(23)
- PGM_CONFIG — PGM_CONFIG (23)
- MAX_RESETn — MAX_RESETn(23)

LED INTERFACE

- PGM_LED[2:0] — PGM_LED[2:0] (23)
- MAX_ERROR — MAX_ERROR (23)
- MAX_LOAD — MAX_LOAD(23)
- MAX_CONF_DONE — MAX_CONF_DONE (23)

VCCINT

1V8: C345 C322 C320 C304 C319 C318 C321 C337 — 0.1uF

2.5V VCCIO

2.5V_REG_HPS: C346 C305 C281 C282 C306 C323 — 0.1uF

1.5V VCCIO

1V8: C291 C394 C317 — 0.1uF
1.5V_REG_HPS: C395 C336 C393 — 0.1uF

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HSMC Port A

J12

BANK 1

BANK 2

BANK 3

A

ASP-122953-01

HSMA_TX_P3(8)
HSMA_TX_N3(8)
HSMA_TX_P2(8)
HSMA_TX_N2(8)
HSMA_TX_P1(8)
HSMA_TX_N1(8)
HSMA_TX_P0(8)
HSMA_TX_N0(8)
HSMA_SDA(4)
JTAG_MUX_TCK(11,12,16)
JTAG_HSMA_TDO(12)
HSMA_CLK_OUT0(9)

R694
38.3
C785
22pF

HSMA_RX_P3(8)
HSMA_RX_N3(8)
HSMA_RX_P2(8)
HSMA_RX_N2(8)
HSMA_RX_P1(8)
HSMA_RX_N1(8)
HSMA_RX_P0(8)
HSMA_RX_N0(8)
HSMA_SCL(4)
JTAG_HSMA_TMS(12)
JTAG_HSMA_TDI(12)
HSMA_CLK_IN0(9)

HSMA_D[3:0](4)
HSMA_TX_D_P[16:0](7)
HSMA_TX_D_N[16:0](7)
HSMA_RX_D_P[16:0](7)
HSMA_RX_D_N[16:0](7)
HSMA_CLK_OUT_P[2:1](4,7)
HSMA_CLK_OUT_N[2:1](4,7)
HSMA_CLK_IN_P[2:1](4,9)
HSMA_CLK_IN_N[2:1](4,9)
HSMA_PRSNTn(4,16,23)

12V
C335
22uF
25V

3.3V
C482
22uF
25V

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10/100/1000 Ethernet - HPS

ETHERNET INTERFACE

ENET_HPS_TXD[3..0] — ENET_HPS_TXD[3..0] (6)
ENET_HPS_GTX_CLK — ENET_HPS_GTX_CLK(6)
ENET_HPS_TX_EN — ENET_HPS_TX_EN(6)
ENET_HPS_MDC — ENET_HPS_MDC (6,18)
ENET_HPS_RESETn — ENET_HPS_RESETn (18,21)
ENET_HPS_RXD[3..0] — ENET_HPS_RXD[3..0] (6)
ENET_HPS_RX_CLK — ENET_HPS_RX_CLK (6)
ENET_HPS_RX_DV — ENET_HPS_RX_DV (6)
ENET_HPS_MDIO — ENET_HPS_MDIO (6,18)
ENET_HPS_INTn — ENET_HPS_INTn (6,18)

ENET_HPS_LED2_LINK

J2
13 YK Yellow
14 YA — R1 220 — 3.3V_REG_HPS
18 GND_TAB
19 GND_TAB
Orange
15 OK
17 GK Green
16 GOA
ENET_L829-1J1T-43

TD0_P 11 — MDI_HPS_P0 2
CT0 12 — CT0
TD0_N 10 — MDI_HPS_N0 3
TD1_P 4 — MDI_HPS_P1 5
CT1 6 — CT1
TD1_N 5 — MDI_HPS_N1 6
TD2_P 3 — MDI_HPS_P2 7
CT2 1 — CT2
TD2_N 2 — MDI_HPS_P3 10
MDI_HPS_N3 11
TD3_P 8
CT3 7 — CT3
TD3_N 9

R50 4.99K — ENET_HPS_RSET 48
3.3V_REG_HPS — R2 220
ENET_HPS_LED1_LINK 17
ENET_HPS_LED2_LINK 15

C49 DNI — Y1 25.00MHz — C48 DNI
3 — 4 — 2 — 1
46 XI
45 XO

ENET_HPS_LED1_LINK

U11A
ENET_HPS_MDC 36 — MDC
ENET_HPS_MDIO 37 — MDIO
ENET_HPS_RESETn 42 — RESET_N
ENET_HPS_INTn 38 — INT_N

MDI INTERFACE
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D

RX_CLK_PHYAD2 35 — ENET_HPS_RX_CLK
GTX_CLK 24 — ENET_HPS_GTX_CLK
TX_EN 25 — ENET_HPS_TX_EN
RX_DV_CLK125_EN 33 — ENET_HPS_RX_DV
TXD3 22 — ENET_HPS_TXD3
TXD2 21 — ENET_HPS_TXD2
TXD1 20 — ENET_HPS_TXD1
TXD0 19 — ENET_HPS_TXD0
RXD0_MODE0 32 — ENET_HPS_RXD0
RXD1_MODE1 31 — ENET_HPS_RXD1
RXD2_MODE2 28 — ENET_HPS_RXD2
RXD3_MODE3 27 — ENET_HPS_RXD3
ISET
CLK125_NDO_LED_MODE 41 — CLK125_NDO_LED_MODE
LED1_PHYAD0
LED2_PHYAD1
XI
XO

KSZ9021RN
Manufacturer = Micrel
PART_NUMBER = KSZ9021RN

2.5V_REG_HPS — U28 — 2.5V_REG_HPS
1 A0 — VCC 8
2 A1 — WP 7
3 A2 — SCL 6 — (23,27) I2C_SCL_HPS
4 GND — SDA 5 — (23,27) I2C_SDA_HPS
24LC32A
PART_NUMBER = 24LC32A-I/SN
Manufacturer = Microchip Technology Inc.

3.3V_REG_HPS — C21 10uF — C27 10uF

3.3V_REG_HPS — L1 3A, 30 Ohm FB — 3.3V_AVDDH
C26 22uF — C23 2.2uF — C28 0.1uF

1.2V_AVDLL_PLL
L4 3A, 30 Ohm FB — 1.2V_AVDDL
C59 22uF — C61 2.2uF — C60 0.1uF
L3 3A, 30 Ohm FB — 1.2V_DVDDL
C56 22uF — C55 2.2uF — C57 0.1uF

3.3V_REG_HPS — L24 3A, 30 Ohm FB — 3.3V_DVDDH
C262 22uF — C261 2.2uF — C270 0.1uF

C16 0.01uF — CT0
C15 0.01uF — CT1
C13 0.01uF — CT2
C14 0.01uF — CT3

U11B
3.3V_AVDDH — 47 AVDDH, 12 AVDDH, 1 AVDDH
3.3V_DVDDH — 40 DVDDH, 16 DVDDH, 34 DVDDH
49 P_GND, 13 VSS_PS, 29 VSS
AVDDL_PLL 44 — 1.2V_AVDDL_PLL
LDO_O 43
AVDDL 9, AVDDL 4 — 1.2V_AVDDL
DVDDL 18, DVDDL 14, DVDDL 39, DVDDL 30, DVDDL 26, DVDDL 23 — 1.2V_DVDDL
KSZ9021RN
Manufacturer = Micrel
PART_NUMBER = KSZ9021RN

Place near KSZ9021RN PHY

1.2V AVDLL_PLL

2.5V_REG_HPS — C52 10uF
U18
1 IN1 — BST 5 — 5.0V — C47 1uF — 1.2V_AVDLL_PLL
2 IN2 — OUT2 10
4 SW — OUT1 9
6 SHDN — ADJ 8 — R56 2.00K — R55 1.00K
GND GND — PG 7
2.5V_REG_HPS — R46 10.0K
LTC3026
3 — 11
C45 22uF — C46 2.2uF

3.3V
R340 DNI — ENET_HPS_LED2_LINK — R342 1.00k
R339 DNI — ENET_HPS_LED1_LINK — R341 1.00k
R347 4.70K, 1% — ENET_HPS_RXD3 — R348 DNI
R364 4.70K, 1% — ENET_HPS_RXD2 — R366 DNI
R365 4.70K, 1% — ENET_HPS_RXD1 — R367 DNI
R368 4.70K, 1% — ENET_HPS_RXD0 — R370 DNI
R369 DNI — ENET_HPS_RX_DV — R371 4.70K, 1%
R378 4.70K, 1% — ENET_HPS_RX_CLK — R379 DNI
R406 4.70K, 1% — CLK125_NDO_LED_MODE — R407 DNI
BOOT-STRAPS

3.3V_REG_HPS
R47 4.70K, 1% — (6,18) ENET_HPS_MDIO
R42 4.70K, 1% — (6,18) ENET_HPS_MDC
R48 4.70K, 1% — (6,18) ENET_HPS_INTn
R49 4.70K, 1% — (18,21) ENET_HPS_RESETn

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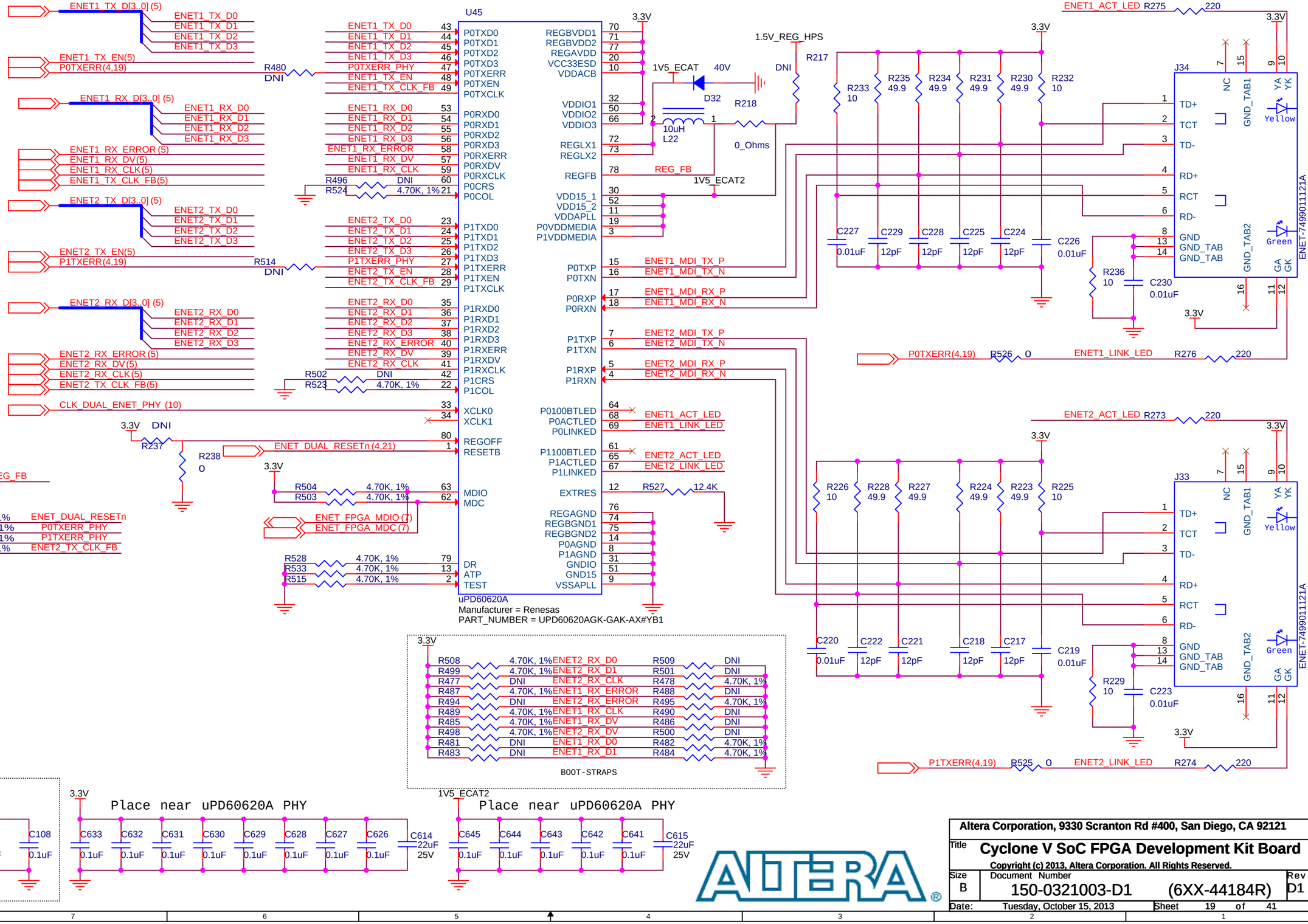
10/100M Ethernet - FPGA



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Title: **Cyclone V SoC FPGA Development Kit Board**

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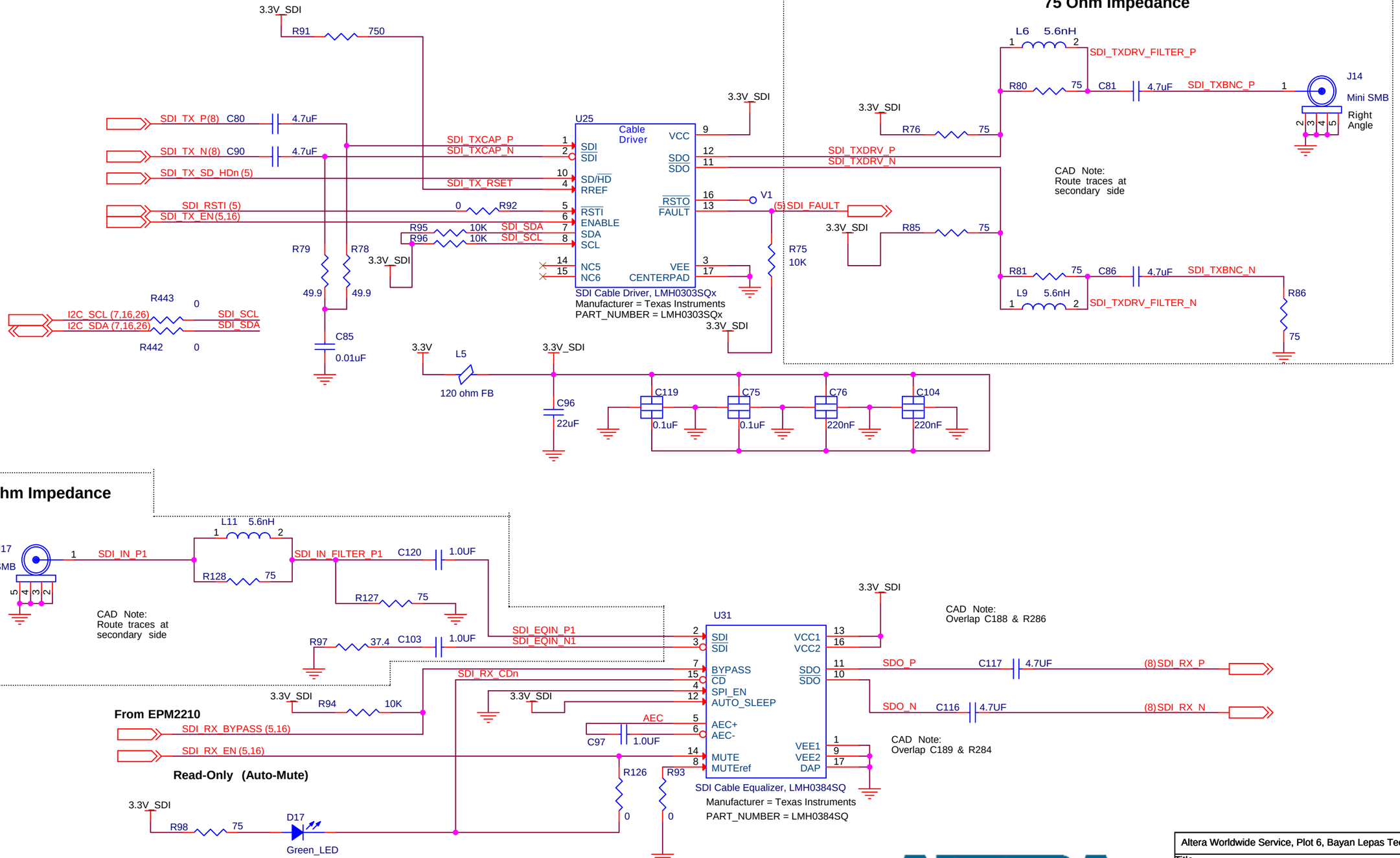
SDI Cable Driver, Equalizer, SMA Option and SMB



Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

Title: **Cyclone V SoC FPGA Development Kit Board**

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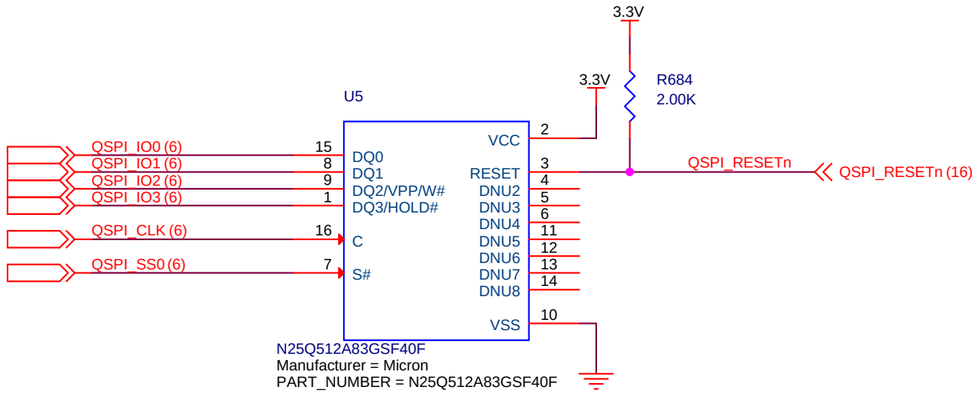
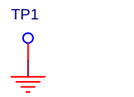
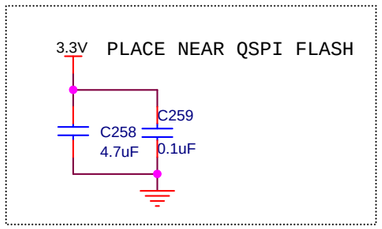
QSPI Flash & Reset Circuit

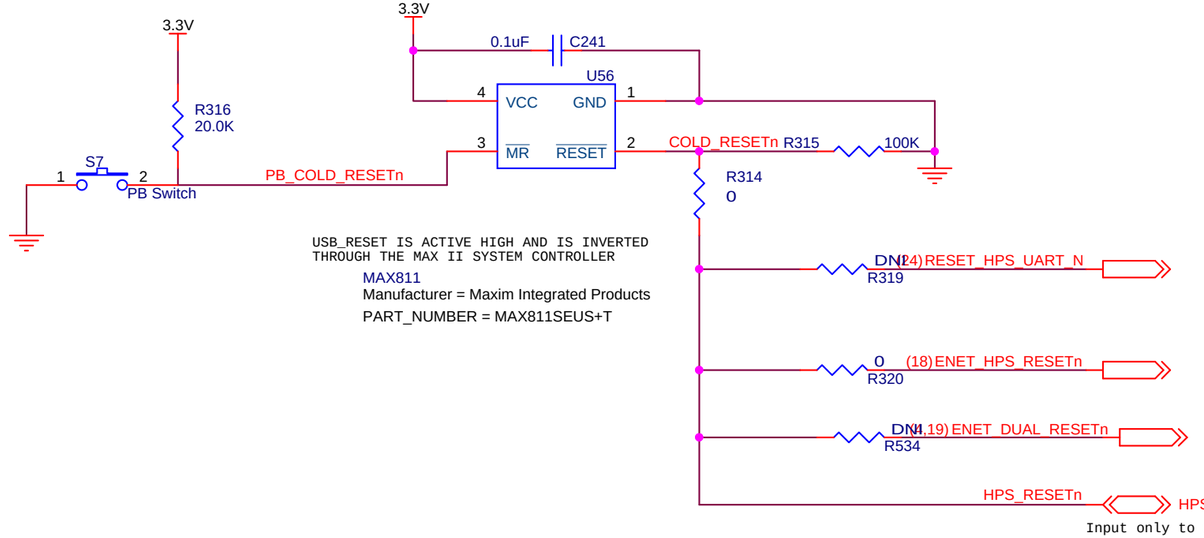
QSPI FLASH

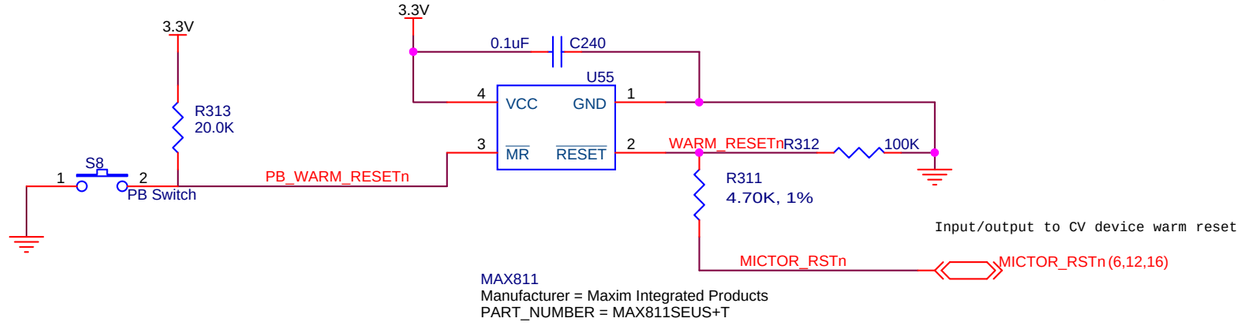






RESET CIRUIT





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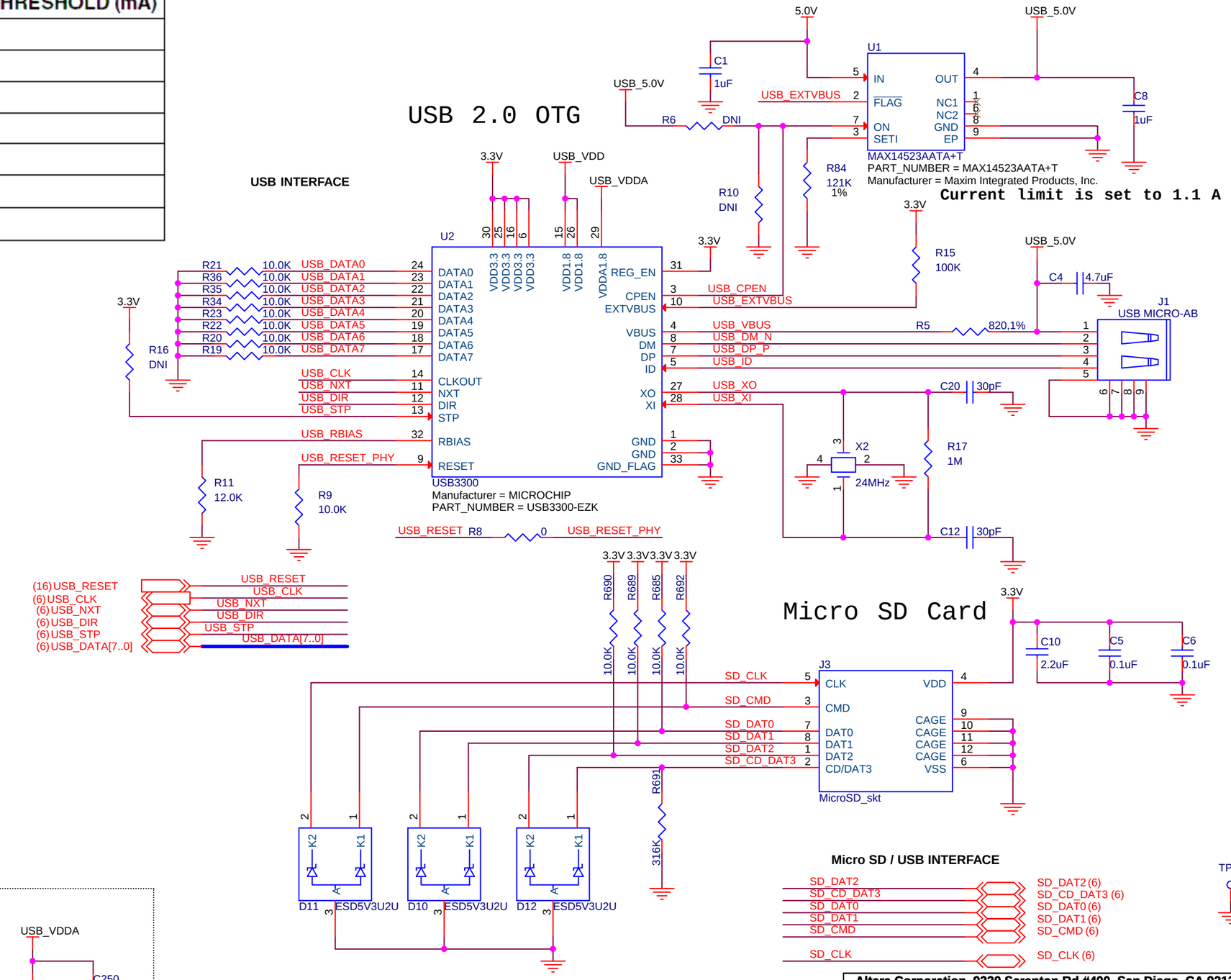
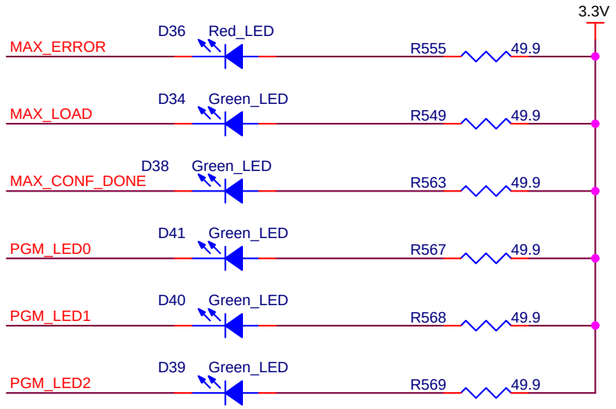
USB 2.0 OTG , Micro SD Card

R_{SETI} (kΩ)	TYPICAL CURRENT LIMIT/THRESHOLD (mA)
91.78	1500
121	1145
221	632
301	466
422	333
563.12	250
∞ (Open)	0



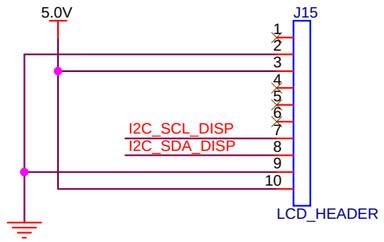
User I/O, RTC

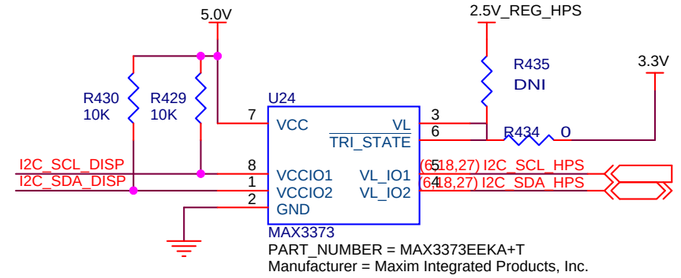


B1
2x16 LCD I2C
I2C ADDRESS: 0x50

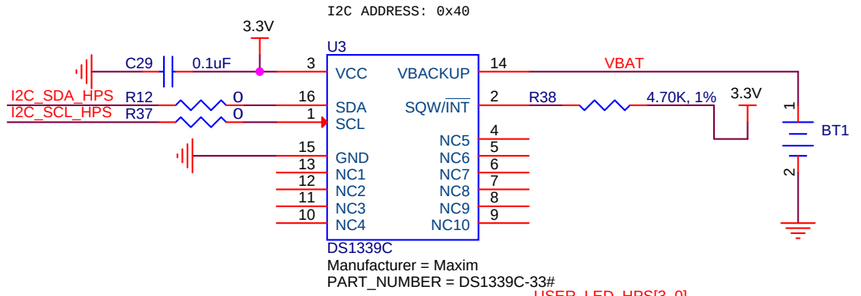
B2
HEADER 3X1

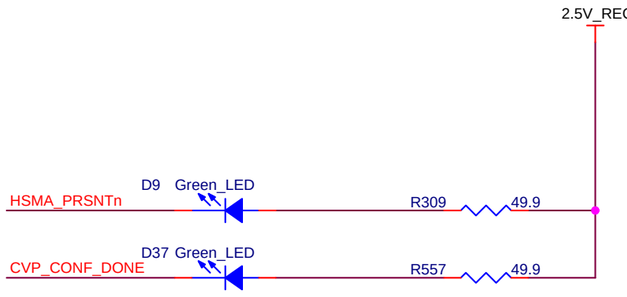
B4
HEADER 6X1

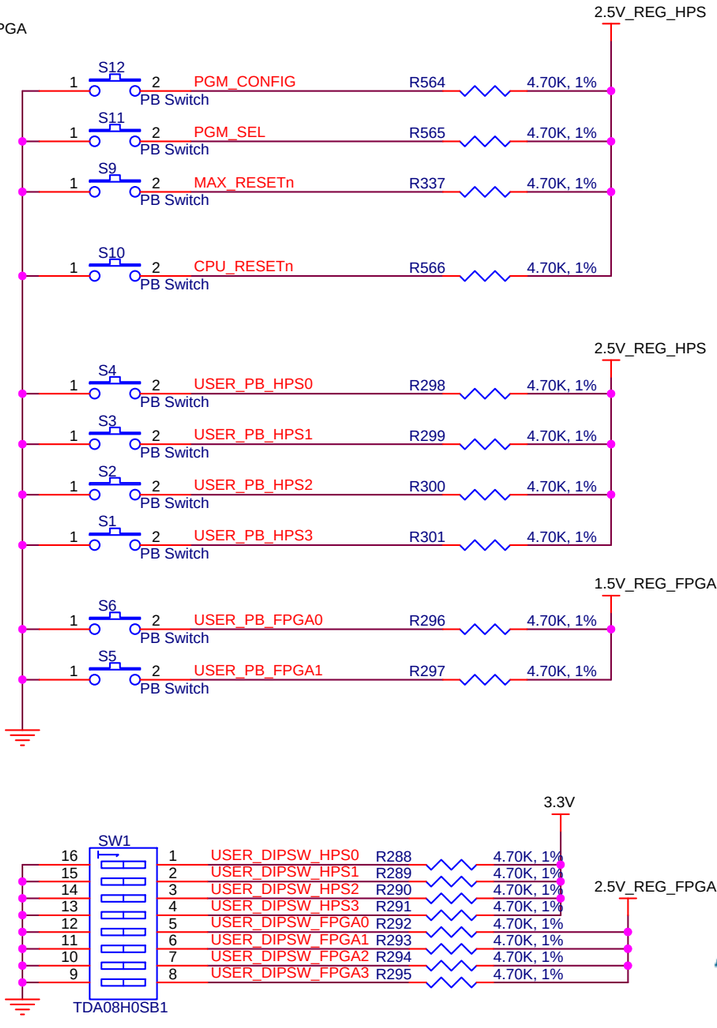


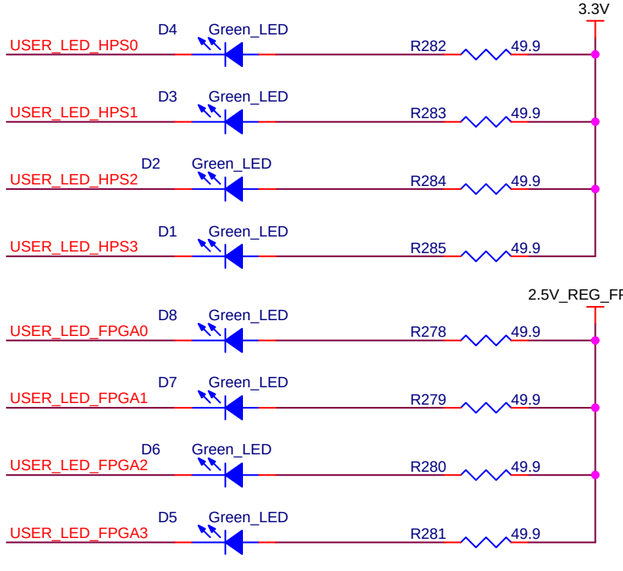


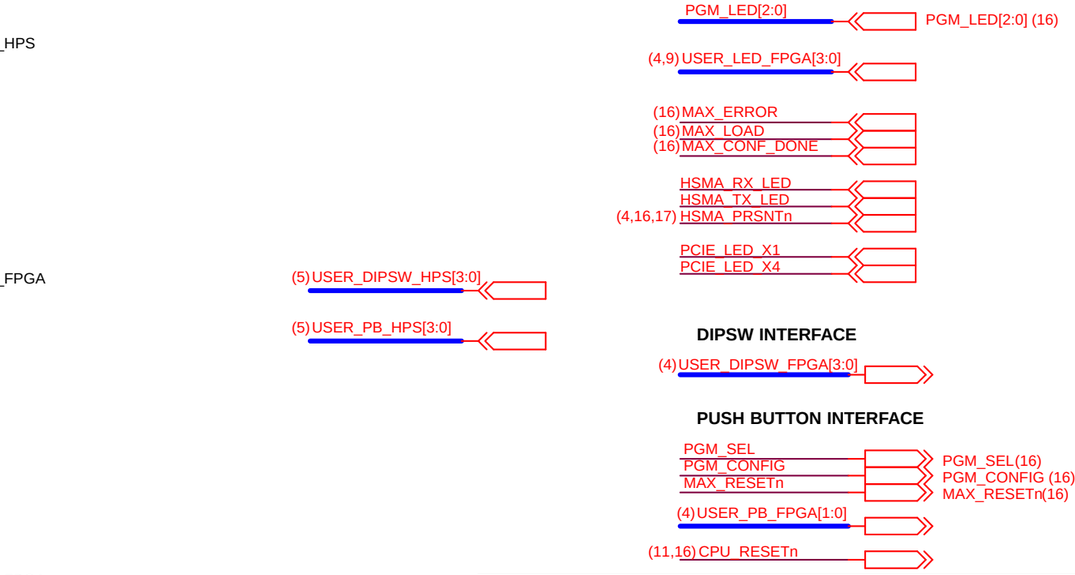
I2C ADDRESS: 0x40











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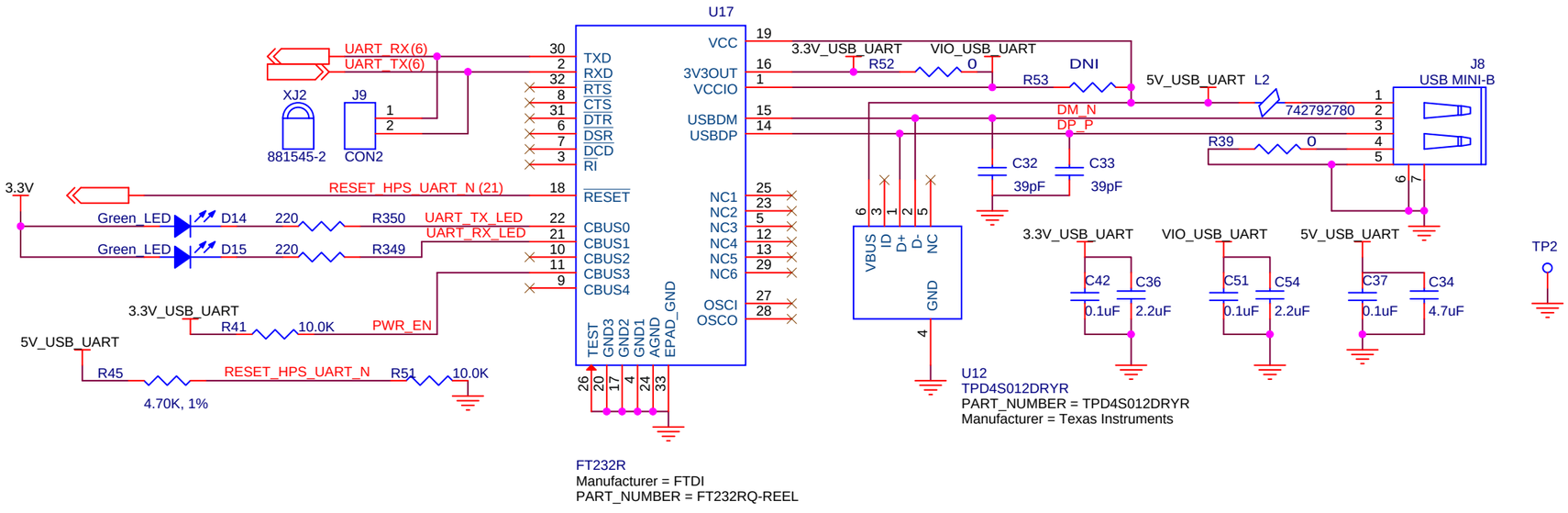
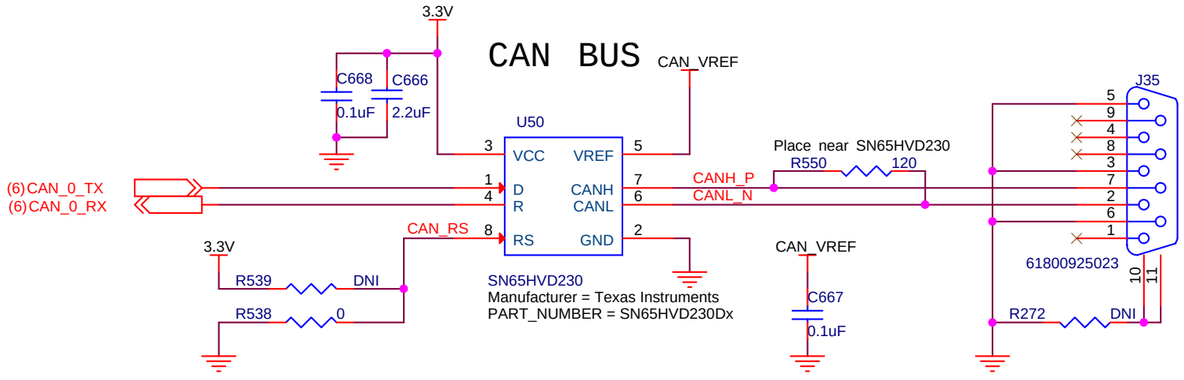
UART, CAN

UART





Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Cyclone V SoC FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0321003-D1 (6XX-44184R)	D1

Date: Tuesday, October 15, 2013 Sheet 24 of 41

On-Board USB Blaster II

J37
USB MINI-B
1 VBUS_5V
2 FX2_D_N
3 FX2_D_P
4 R265 DNI
5
7 6

U53
TPD2EUSB30
Manufacturer = Texas Instruments
PART_NUMBER = TPD2EUSB30DRxx
3 GND
D+ 1
D- 2
1M R277
4.7nF C239

Y5
24.00MHz
C233 12pF
C234 12pF

FX2_SDA R531 0 MAX_SDA
C216 0.1uF
U48
GND VCC
RESET MR
100K R216 FX2_RESETn
MAX811
Manufacturer = Maxim Integrated Products
PART_NUMBER = MAX811SEUS+T

U51
AVCC AVCC VCC VCC VCC VCC VCC VCC
DMINUS DPLUS
IFCLK XTALIN XTALOUT
RESERVED
AGND AGND GND GND GND GND GND GND
RESET SCL SDA WAKEUP CTL0 CTL1 CTL2 RDY0 RDY1 CLKOUT
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7
USB_B2_CLK
24M_XTALIN
24M_XTALOUT
FX2_RESETn FX2_SCL FX2_SDA FX2_WAKEUP FX2_FLAGA FX2_FLAGB FX2_FLAGC FX2_SLRDn FX2_SLWRn
FX2_PA1 FX2_PA2 FX2_PA3 FX2_PA4 FX2_PA5 FX2_PA6 FX2_PA7
FX2_PB0 FX2_PB1 FX2_PB2 FX2_PB3 FX2_PB4 FX2_PB5 FX2_PB6 FX2_PB7
FX2_PD0 FX2_PD1 FX2_PD2 FX2_PD3 FX2_PD4 FX2_PD5 FX2_PD6 FX2_PD7
CY7C68013A_VFBGA
Manufacturer = Cypress
PART_NUMBER = CY7C68013A-56BAXC

3.3V
R553 2.00K
R551 2.00K

VBUS_5V R561 10.0K FX2_WAKEUP
R562 20.0K C681 0.1uF

3.3V
PLACE NEAR CY7C68013A
C677 C675 C672 C682 C669 C671 C676 C680
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

1V8
D30 JTAG_RX RESn_JTAG_RX R518 56.2 Green_LED
D31 JTAG_TX RESn_JTAG_TX R517 56.2 Green_LED
D29 SC_RX RESn_SC_RX R519 56.2 Green_LED
D28 SC_TX RESn_SC_TX R520 56.2 Green_LED

1.5V_REG_HPS
R544 1.00k USB_SCL
R542 1.00k USB_SDA
R545 1.00k USB_FULL
R543 1.00k USB_EMPTY
R541 1.00k FACTORY_REQUEST

3.3V
J38
R286 1.00K C_USB_MAX_TCK
R321 1.00K C_USB_MAX_TDO
C_USB_MAX_TMS
C_USB_MAX_TDI
DNI

U47B
MAX II BANK 1
FX2_PA2 B1
FX2_FLAGC C1
FX2_PA7 C2
FX2_FLAGA D1
FX2_PA3 D2
FX2_PA4 D3
EXTRA_SIG0 E3
FX2_PB4 F1
FX2_PA6 F2
FX2_PB2 F3
FX2_FLAGB G1
FX2_PB0 G2
FX2_PA1 G3
USB_DISABLEn H4
FX2_PB6 H7
IO_B1_B1 IO_B1_C1 IO_B1_C2 IO_B1_D1 IO_B1_D2 IO_B1_D3 IO_B1_E3 IO_B1_F1 IO_B1_F2 IO_B1_F3 IO_B1_G1 IO_B1_G2 IO_B1_G3 IO_B1_H1 IO_B1_H4 IO_B1_H7
IO_B1_H8 IO_B1_J3 IO_B1_J4 IO_B1_J5 IO_B1_J6 IO_B1_J8 IO_B1_J9 IO_B1_K1 IO_B1_K2 IO_B1_K3 IO_B1_K4 IO_B1_K5 IO_B1_K6 IO_B1_K7 IO_B1_K8 IO_B1_K10
H8 FX2_PB1
J3 FX2_PB3
J4 FX2_SCL
J5 FX2_PD6
J6 FX2_PD4
J8
J9 FX2_SLWRn
K1 FX2_SLRDn
K2 FX2_PD7
K3 FX2_PD5
K4 FX2_PA5
K5 C_JTAG_TDO
K6 C_JTAG_TMS
K7 C_JTAG_TDI
K8 C_JTAG_TCK
K10
EPM570GF100
PART_NUMBER = EPM570GF100C5N
Manufacturer = Altera Corporation

U47D
MAX II CONFIGURATION
IO1/DEV_OE IO1/DEV_CLRn
TDI TCK TMS TDO
IO1/GCLK0p IO1/GCLK1p IO2/GCLK2p IO2/GCLK3p
MAX_SDA J7
C_USB_MAX_TDI H2
C_USB_MAX_TCK H3
C_USB_MAX_TMS J1
C_USB_MAX_TDO J2
K9 FX2_RESETn
E2 USB_B2_CLK
E1 FX2_PB7
F8 USB_CFG7
E10 M570_CLOCK
EPM570GF100
PART_NUMBER = EPM570GF100C5N
Manufacturer = Altera Corporation

U47C
MAX II BANK 2
JTAG_TX A1
JTAG_RX A2
FACTORY_REQUEST A3
USB_CFG5 A4
USB_RESETn A7
USB_OEn B8
USB_RDn D10
USB_WRn D9
FACTORY_STATUS A9
SC_RX A10
SC_TX B2
USB_CFG4 B3
EXTRA_SIG1 B4
USB_CFG6 B5
USB_B2_DATA0 B9
USB_B2_DATA1 C9
USB_B2_DATA2 C8
USB_B2_DATA3 B7
USB_B2_DATA4 C7
IO_B2_A1 IO_B2_A2 IO_B2_A3 IO_B2_A4 IO_B2_A7 IO_B2_B8 IO_B2_D10 IO_B2_D9 IO_B2_A9 IO_B2_A10 IO_B2_B2 IO_B2_B3 IO_B2_B4 IO_B2_B5 IO_B2_B9 IO_B2_C9 IO_B2_C8 IO_B2_B7 IO_B2_C7
IO_B2_C3 IO_B2_C4 IO_B2_A6 IO_B2_F10 IO_B2_F9 IO_B2_B10 IO_B2_E8 IO_B2_C10 IO_B2_D8 IO_B2_B6 IO_B2_E9 IO_B2_A8 IO_B2_A5 IO_B2_G8 IO_B2_G9 IO_B2_G10 IO_B2_H9 IO_B2_H10 IO_B2_J10
C3 USB_CFG3
C4 M570_PCIE_JTAG_EN
A6 USB_B2_DATA7
F10 USB_B2_DATA5
F9 USB_B2_DATA6
B10 RST
E8 USB_CFG8
C10 TRST
D8 USB_FULL
B6 USB_EMPTY
E9 USB_CFG11
A8 USB_SCL
A5 USB_SDA
G8 EXTRA_SIG2
G9 USB_CFG10
G10 USB_CFG0
H9 USB_CFG1
H10 USB_CFG2
J10 USB_CFG9
V39 V43 V42
EPM570GF100
PART_NUMBER = EPM570GF100C5N
Manufacturer = Altera Corporation

(16)TRST
(16)RST

C_JTAG_TCK 0 R529 JTAG_TCK
C_JTAG_TMS 0 R530 JTAG_TMS
C_JTAG_TDI 0 R535 JTAG_BLASTER_TDI
C_JTAG_TDO 0 R536 JTAG_BLASTER_TDO

2.5V_REG_HPS
R211 DNI JTAG_BLASTER_TDI

FPGA USB INTERFACE

USB_B2_DATA[7:0] — USB_B2_DATA[7:0] (4)
USB_ADDR[1:0] — USB_ADDR[1:0]
USB_FULL — USB_FULL (4)
USB_EMPTY — USB_EMPTY (4)
USB_SCL — USB_SCL (4)
USB_SDA — USB_SDA (4)
USB_B2_CLK — USB_B2_CLK (4,16)
USB_RESETn — USB_RESETn (4)
USB_OEn — USB_OEn (4)
USB_RDn — USB_RDn (4)
USB_WRn — USB_WRn (4)
M570_PCIE_JTAG_EN — M570_PCIE_JTAG_EN (16)

MAX V USB INTERFACE

USB_CFG[11:0] — USB_CFG[11:0] (16)
EXTRA_SIG[2:0] — EXTRA_SIG[2:0] (16)
USB_DISABLEn — USB_DISABLEn (12)
M570_CLOCK — M570_CLOCK (16)
FACTORY_STATUS — FACTORY_STATUS (16)
FACTORY_REQUEST — FACTORY_REQUEST (16)

C_USB_MAX_TCK R560 0 FX2_PD0
C_USB_MAX_TDI R558 0 FX2_PD2
C_USB_MAX_TDO R537 0 FX2_PD3
C_USB_MAX_TMS R559 0 FX2_PD1

JTAG INTERFACE

JTAG_TCK — JTAG_TCK (12)
JTAG_TMS — JTAG_TMS (12)
JTAG_BLASTER_TDI — JTAG_BLASTER_TDI (12)
JTAG_BLASTER_TDO — JTAG_BLASTER_TDO (12)

U47A
MAX II POWER
GNDINT GNDINT GNDINT GNDINT
GNDIO GNDIO GNDIO GNDIO GNDIO GNDIO GNDIO
VCCINT VCCINT VCCINT VCCINT
VCCIO1 VCCIO1 VCCIO1 VCCIO2 VCCIO2 VCCIO2
C5 E6 F5 H5 D5 D7 E5 F6 G5 G7
C6 E7 F4 H6 E4 G4 G6 D4 D6 F7
1V8
3.3V
1.5V_REG_HPS
EPM570GF100
PART_NUMBER = EPM570GF100C5N
Manufacturer = Altera Corporation

PLACE NEAR MAX II (U14)
3.3V: C647 0.1uF, C648 0.1uF
1.5V_REG_HPS: C653 0.1uF, C655 0.1uF
1V8: C654 0.1uF, C661 0.1uF

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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FPGA Power Monitor

V48 RSNS SNS SENSE_PAD — 1.1V_VCC_N (1) → 1.1V_VCC (2)
V49 RSNS SNS SENSE_PAD — 1.1V_VCC_P (1) → 1.1V_REG_VCC (2)
V45 RSNS SNS SENSE_PAD — 1.5V_FPGA_N (1) → 1.5V_FPGA (2)
V44 RSNS SNS SENSE_PAD — 1.5V_FPGA_P (1) → 1.5V_REG_FPGA (2)
V41 RSNS SNS SENSE_PAD — 2.5V_FPGA_N (1) → 2.5V_FPGA (2)
V40 RSNS SNS SENSE_PAD — 2.5V_FPGA_P (1) → 2.5V_REG_FPGA (2)

12V
J21 (22_23_2021): 1, 2 — TSENSE_FAN_CNTL
Q1 FDV305N — (16) OVERTEMP
B3 FAN_2pin_Conn

3.3V_PM_FPGA
R417 10K SCL_PM
R416 10K SDA_PM
SCL_PM → (7,16,20) I2C_SCL
SDA_PM → (7,16,20) I2C_SDA

R88/R87 1K, C92 0.1uF, C93 0.1uF
R83/R82 1K, C87 0.1uF, C88 0.1uF
R77/R73 1K, C77 0.1uF, C82 0.1uF
R70/R69 1K, C72 0.1uF, C73 0.1uF
R68/R67 1K, C70 0.1uF, C71 0.1uF
R66/R65 1K, C68 0.1uF, C69 0.1uF

2.5V_FPGA_V_P
2.5V_FPGA_V_N
2.5V_FPGA_I_P
2.5V_FPGA_I_N
1.5V_FPGA_V_P
1.5V_FPGA_V_N
1.5V_FPGA_I_P
1.5V_FPGA_I_N
1.1V_VCC_V_P
1.1V_VCC_V_N
1.1V_VCC_I_P
1.1V_VCC_I_N

12V

U26 LTC2978

14	VIN_SNS	VIN_EN	12
36	VSENSEP0	REFP	34
37	VSENSEM0	REFM	35
42	VSENSEP1	NC	13
43	VSENSEM1		
46	VSENSEP2	VDACP0	39
47	VSENSEM2	VDACM0	38
48	VSENSEP3	VDACP1	40
49	VSENSEM3	VDACM1	41
52	VSENSEP4	VDACP2	44
53	VSENSEM4	VDACM2	45
62	VSENSEP5	VDACP3	50
63	VSENSEM5	VDACM3	51
64	VSENSEP6	VDACP4	55
1	VSENSEM6	VDACM4	54
2	VSENSEP7	VDACP5	56
3	VSENSEM7	VDACM5	57
		VDACP6	59
		VDACM6	58
		VDACP7	60
		VDACM7	61
SCL_PM 28	SCL	VOUT_EN0	4
SDA_PM 27	SDA	VOUT_EN1	5
PM2_ASEL0 32	ASEL0	VOUT_EN2	6
PM2_ASEL1 33	ASEL1	VOUT_EN3	7
PM_CNTL0 30	CONTROL0	VOUT_EN4	8
PM_CNTL1 31	CONTROL1	VOUT_EN5	9
PM_RSTn 22	WDI/RESET	VOUT_EN6	10
		VOUT_EN7	11
PM2_FAULTB00 23	FAULTB00		
PM2_FAULTB01 24	FAULTB01		
PM2_FAULTB10 25	FAULTB10		
PM2_FAULTB11 26	FAULTB11		
PM_SHARE_CLK 21	SHARE_CLK	ALERTB	29
		PWRGD	20
		VPWR	15
		VDD25	18
19	WP	VDD33_OUT	16
65	E-PAD	VDD33_IN	17

GND pad

Manufacturer = Linear Technology
PART_NUMBER = LTC2978CUP#PBF

2.5V_FPGA_VDACP0
2.5V_FPGA_VDACP2
1.5V_FPGA_VDACP4
1.1V_FPGA_VDACP4

2.5V_FPGA_RUN → 2.5V_FPGA_RUN (31)
1.5V_FPGA_RUN → 1.5V_FPGA_RUN (30)
1.1V_FPGA_RUN → 1.1V_FPGA_RUN (29)

PM_ALERTB
PM_PWRGD

C481 0.1uf
C91 0.1uf, C98 0.1uf, C99 0.1uf
3.3V_PM_FPGA

R422
R421

2.5V_FPGA_VDACP0 → 2.5V_FPGA_VDACP0 (31)
1.5V_FPGA_VDACP2 → 1.5V_FPGA_VDACP2 (30)
1.1V_FPGA_VDACP4 → 1.1V_FPGA_VDACP4 (29)

SCL_PM → SCL_PM (27)
SDA_PM → SDA_PM (27)

PM_SHARE_CLK → PM_SHARE_CLK (27)
PM_CNTL0 → PM_CNTL0 (27)
PM_CNTL1 → PM_CNTL1 (27)
PM_RSTn → PM_RSTn (27)

PM_ALERTB → PM_ALERTB (27)
PM_PWRGD → PM_PWRGD (27)

PM2_FAULTB00 → PM2_FAULTB00
PM2_FAULTB01 → PM2_FAULTB01
PM2_FAULTB10 → PM2_FAULTB10
PM2_FAULTB11 → PM2_FAULTB11

3.3V_PM_FPGA
R107 10K, R106 10K, R105 10K, R104 10K, R108 10K
PM2_ASEL0
PM2_FAULTB00
PM2_FAULTB01
PM2_FAULTB10
PM2_FAULTB11

PM2_ASEL0
PM2_ASEL1

LTC2978
Address Select
PWRMON2 = 7'h5D

Altera Corporation, 101 Innovation Drive, San Jose, CA

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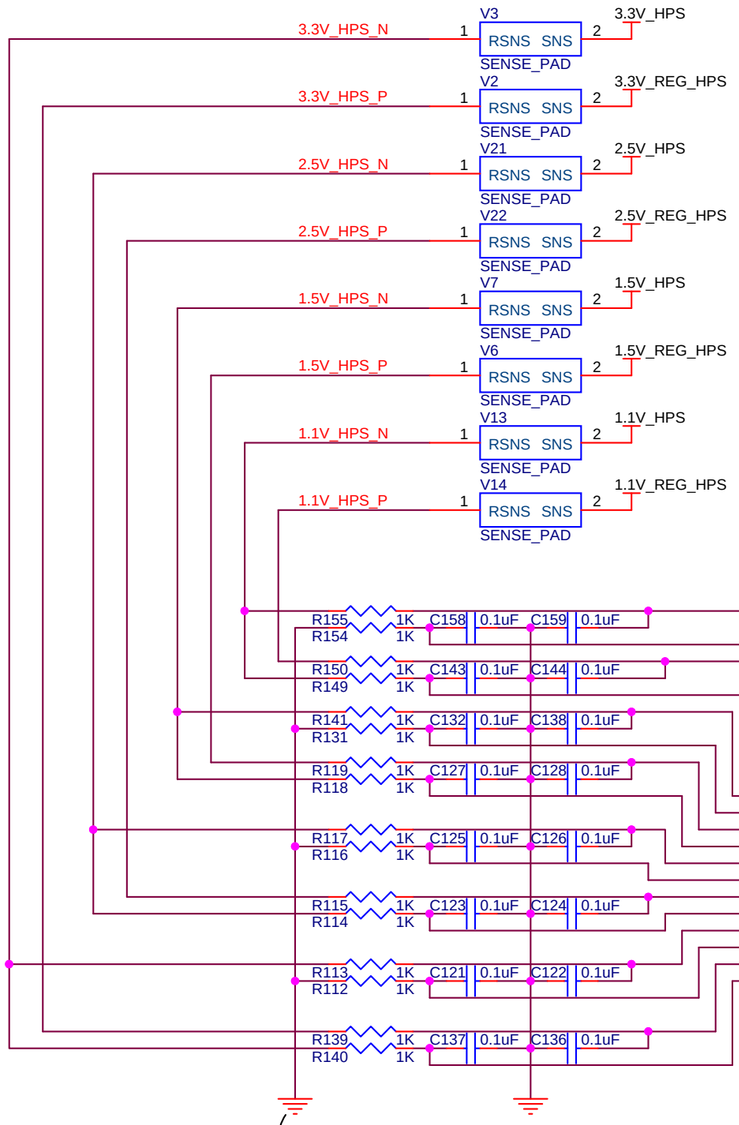
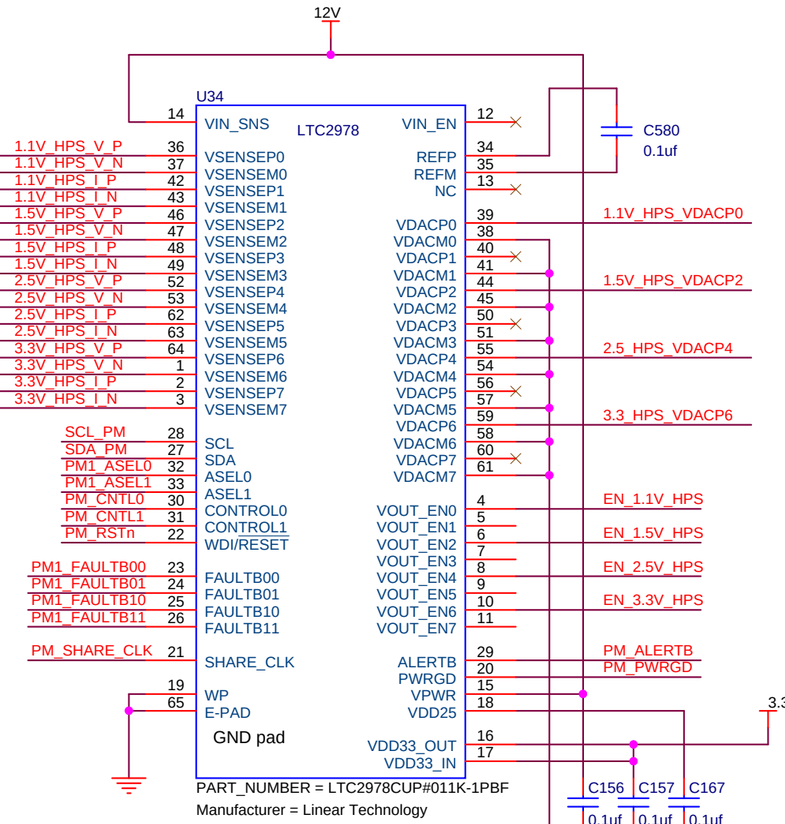
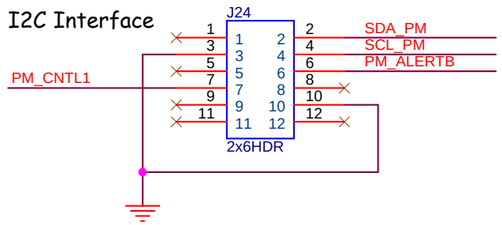
HPS Power Monitor

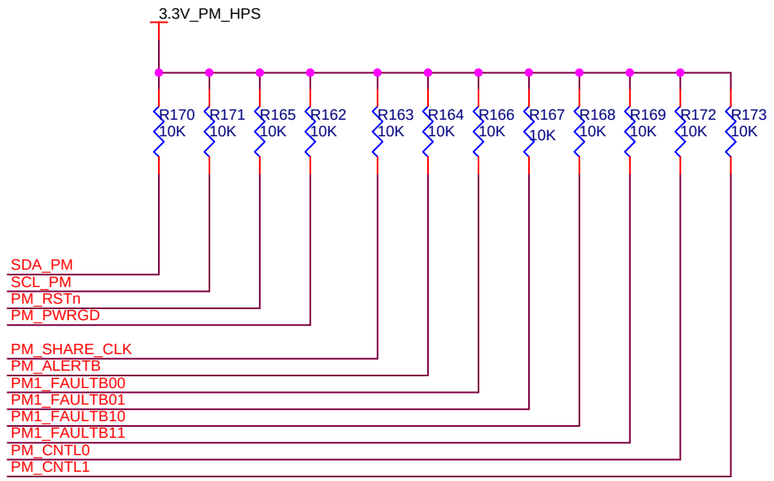


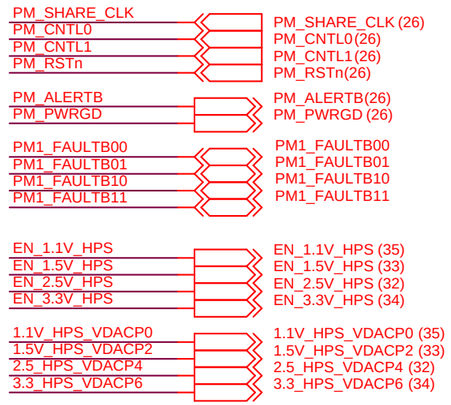
these GND connections to each VSENSEMx pin needs to be placed close to a GND pin of the BGA!

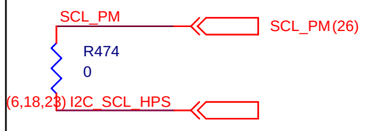


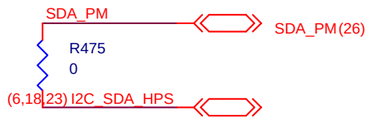
PART_NUMBER = LTC2978CUP#011K-1PBF
Manufacturer = Linear Technology

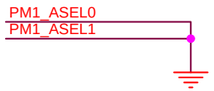












LTC2978
Address Select
PWRMON1 = 7'h5C

Altera Corporation, 101 Innovation Drive, San Jose, CA

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Power 1 - DC Input & 12V, 3.3V Output

DC_INPUT
J22
CONN JACK PWR
19V
DC Input
U44
FDMC8878
U60
LTC4357
GATE
IN
NC
OUT
VDD
GND
EP_GND
D27
MMBD1205
12V_ATX
U41
FDMC8878
J20
ATX-POWER_4P
COM
+12V
U59
LTC4357
DC_IN
C175 47uF 35V
C196 47uF 35V
C176 22uF 25V
C197 22uF 25V
C187 4.7uF
R178 20.0K
R179 20.0K
C179 1000pF
C194 1000pF
C186 82pF
C180 22pF
C185 22pF
R180 169.0K
C192 100pF
R198 57.6K
R192 52.3K
U43
LTC3855EUJ
Manufacturer = Linear Technology
Manufacturer Part Num = LTC3855EUJ#PBF
VIN
INTVCC
EXTVCC
RUN1
ITEMP1
ILIM1
ITH1
TK/SS1
RUN2
ITEMP2
ILIM2
ITH2
TK/SS2
FREQ
MODE/PLLIN
PHSASMD
CLKOUT
SGND1
SGND2
PGND1
PGND2
NC
gnd-pad
DIFFOUT
DIFFP
DIFFN
INTVCC_1
3.3V_SHDNn
12V_SHDNn
3.3V
TG1
BOOST1
SW1
BG1
VFB1
SENSE1+
SENSE1-
PGOOD1
TG2
BOOST2
SW2
BG2
VFB2
SENSE2+
SENSE2-
PGOOD2
LTC3855_S1P
LTC3855_S1N
LTC3855_S2P
LTC3855_S2N
PG_12V
D24
CMDSH-3
D26
C181 0.1uF
C195 0.1uF
C193 0.1uF
C174 0.1uF
C166 22uF 25V
C210 22uF 25V
RJK0305DPB
RJK0301DPB
Q3
Q4
Q5
Q6
drain-tab
L14 1.5uH
L23 0.68uH
V9
V8
V46
V47
SNS
RSNS
SENSE_PAD
R177 3.09K
R470 4.02K
R205 11.5K
DIFFOUT
R193 2.55K
R256 215.0K
R257 11.3K
R199 3.92K
DNI
R200
R206 100K
3.3V
C564 100uF 6.3v
C540 330uF 10V
C664 68uF 25V
C665 68uF 25V
C663 68uF 25V
12V_REG
Q7
FDMC8878
U62
LTC4357
Q8
FDMC8878
U63
LTC4357
5.0V
R548 1.00k
POWER LED
D35
BLUE LED
SW5
SW SLIDE-4P2T
R268 100K
R270 100K
R267 20.0K
R261 100K
R264 100K
R269 20.0K

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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Power 2

1.1V_VCC — L10 — 1.1V_VCCEL

3A, 30 Ohm FB

1.1V_REG_VCC — R461 0.001 CSNL1206 — 1.1V_VCC

TP16 12V — R667 0.003 WSL0805 — TP18 12V_VCC1V1

C768 22uF 1206 | C692 22uF 1206 | C769 22uF 1206

C696 47uF 1206 | C697 47uF 1206 | C706 47uF 1206 | C774 100uF 1206

U72 EN23F0QI

46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25		
PGND1	PGND2	PGND3	PGND4	PGND5	PGND6	PGND7	NC28	NC27	NC26	NC25	VOUT11	VOUT10	VOUT9	VOUT8	VOUT7	VOUT6	VOUT5	VOUT4	VOUT3	VOUT2	VOUT1		
93	PGND																					NC24	24
47	PVIN17																					NC23	23
48	PVIN16																					NC22	22
49	PVIN15																					NC21	21
50	PVIN14																					NC20	20
51	PVIN13																					NC19	19
52	PVIN12																					NC18	18
53	PVIN11																					NC17	17
54	PVIN10																					NC16	16
55	PVIN9																					NC15	15
56	PVIN8																					NC14	14
57	PVIN7																					NC13	13
58	PVIN6																					NC12	12
59	PVIN5																					NC11	11
60	PVIN4																					NC10	10
61	PVIN3																					NC9	9
62	PVIN2																					NC8	8
63	PVIN1																					NC7	7
64	AVINO																					NC6	6
65	PG																					NC5	5
66	BTMP																					NC4	4
67	VDDB																					NC3	3
68	BGND																					NC2	2
69	S_IN																					NC1	1
70	S_OUT																						
71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92		
POK	ENABLE	AVIN	AGND	M/S	VFB	EAIN	SS	RCLX	FQADJ	NC29	CGND	NC30	NC31	NC32	NC33	NC34	NC35	NC36	NC37	NC38	NC39		

PART_NUMBER = EN23F0QI
Manufacturer = Enpirion
QFN-92

1uF 0402 C775 — 1.1V_VCC_AVINO — C776 0.1uF 0402 — R661 0402 4.75K — C777 0.47uF 0603

100K R587 0402 — 3.3V — 1.1V_VCC_AVINO — 200K R662 0402 — 47nF C694 0402 — 1.5K R663 0402

3.3V — R648 10K 0402 — R589 0 0402 — (26) 1.1V_FPGA_RUN

C778 1uF 0402 — 100K R588 0402 — RCLX

1.1V_REG_VCC — V51 RSNS SNS SENSE_PAD — R675 10 0402 — R676 10 0402 — V52 RSNS SNS SENSE_PAD — 1.1V_VCC

C781 0402 0.1uF

R677 2.21K 1% 0402 — R678 2.21K 1% 0402

R680 365K 1% 0402

U73 IN+ IN- V- OUT V+ — AD8638ARJZ-REEL7 — Analog Devices — AD8638ARJZ_SOT235

12V — C782 0.1uF 0402

R681 0402 365K 1%

RCLX

U75 OUT VCC- IN- VCC+ IN+ — Manufacturer = STmicro — PART_NUMBER = TS391ILT — TS391ILT_SOT23

12V — R679 4.99K 0402

U74 CATHODE ANODE REF — LM431SCCMFX — PART_NUMBER = LM431SCCMFX — Manufacturer = Fairchild Semiconductor — LM431S_SOT23

R590 0402 DNI — V50 RSNS SNS SENSE_PAD — 1.1V_VCC

1.1V_REG_VCC — 200K R664 0402 — 0 R665 0603

15K R666 0201 — 27pF C779 0402

Place this SENSE PAD close to SOC

R590 and R665 resistors should be close to each other

1.21M R183 0402 — 1.1V_FPGA_VDACP4 (26)

R595 240K 0402

TP14 — Test_Pad_SMT

Over Current Protection	
Current	Resistor Value Rin
15A	2.21K

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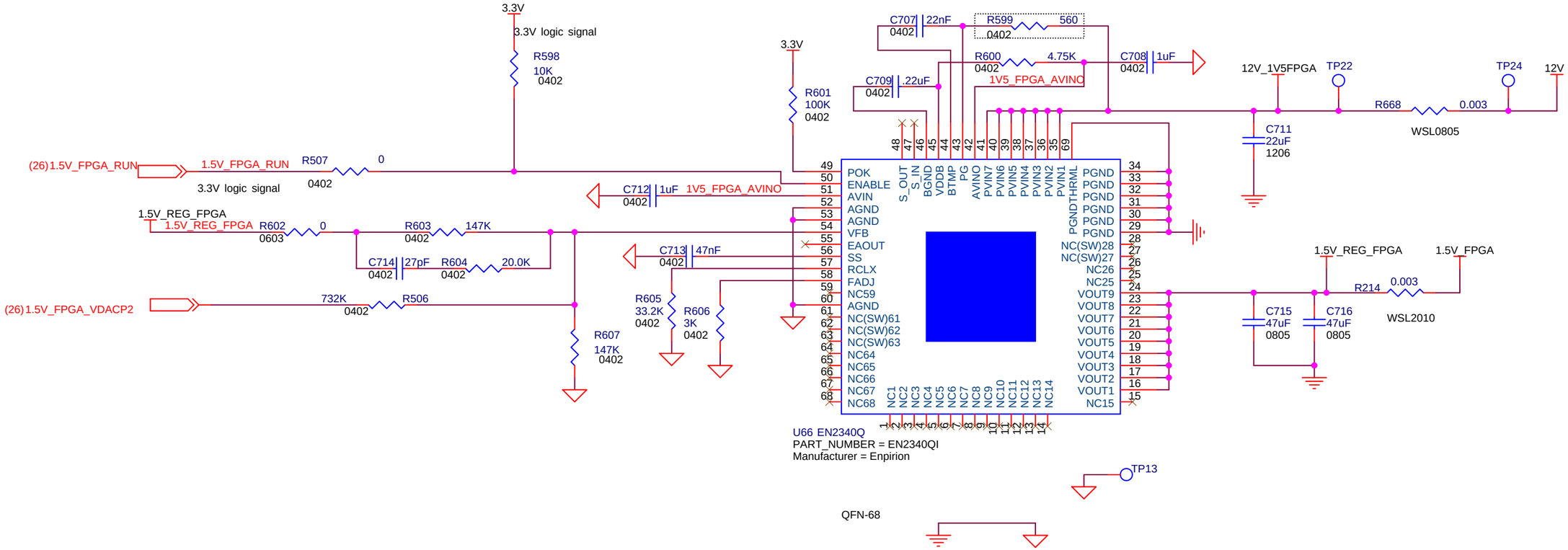
Power 3 - 1.5V FPGA



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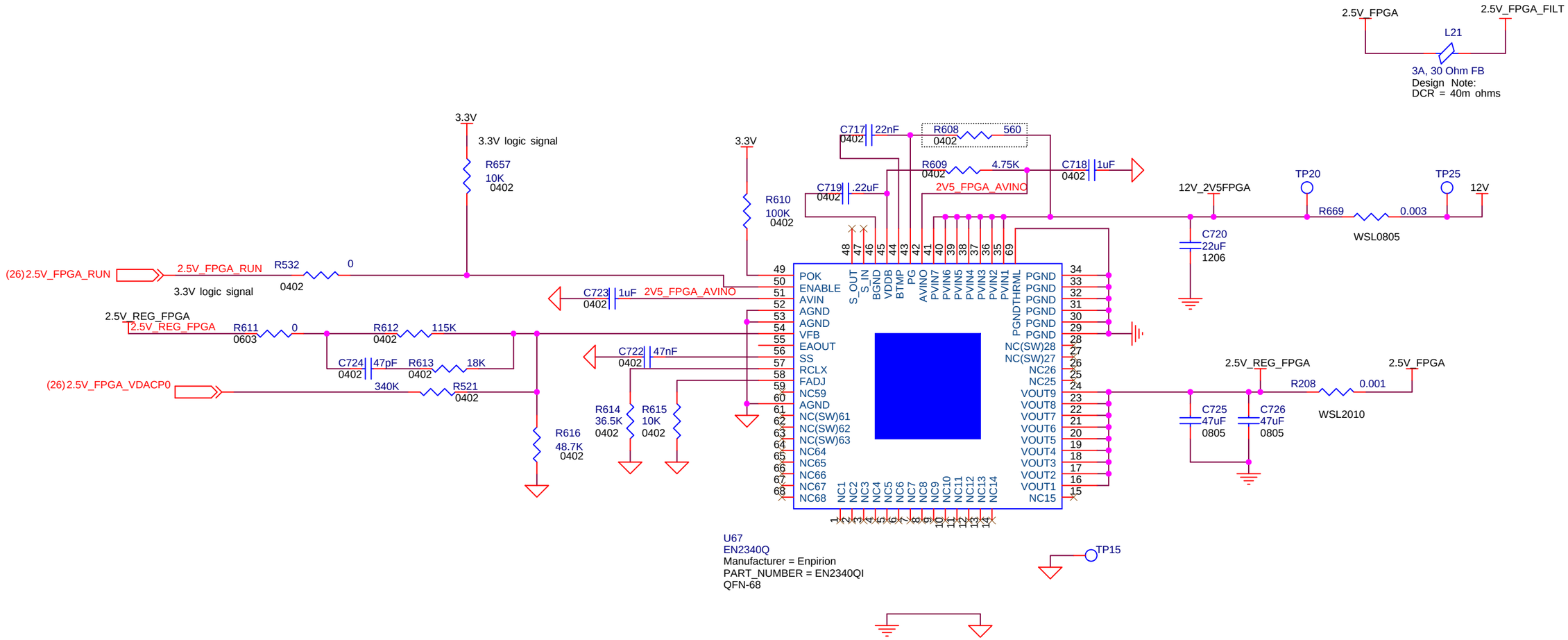
Power 3 - 2.5V FPGA



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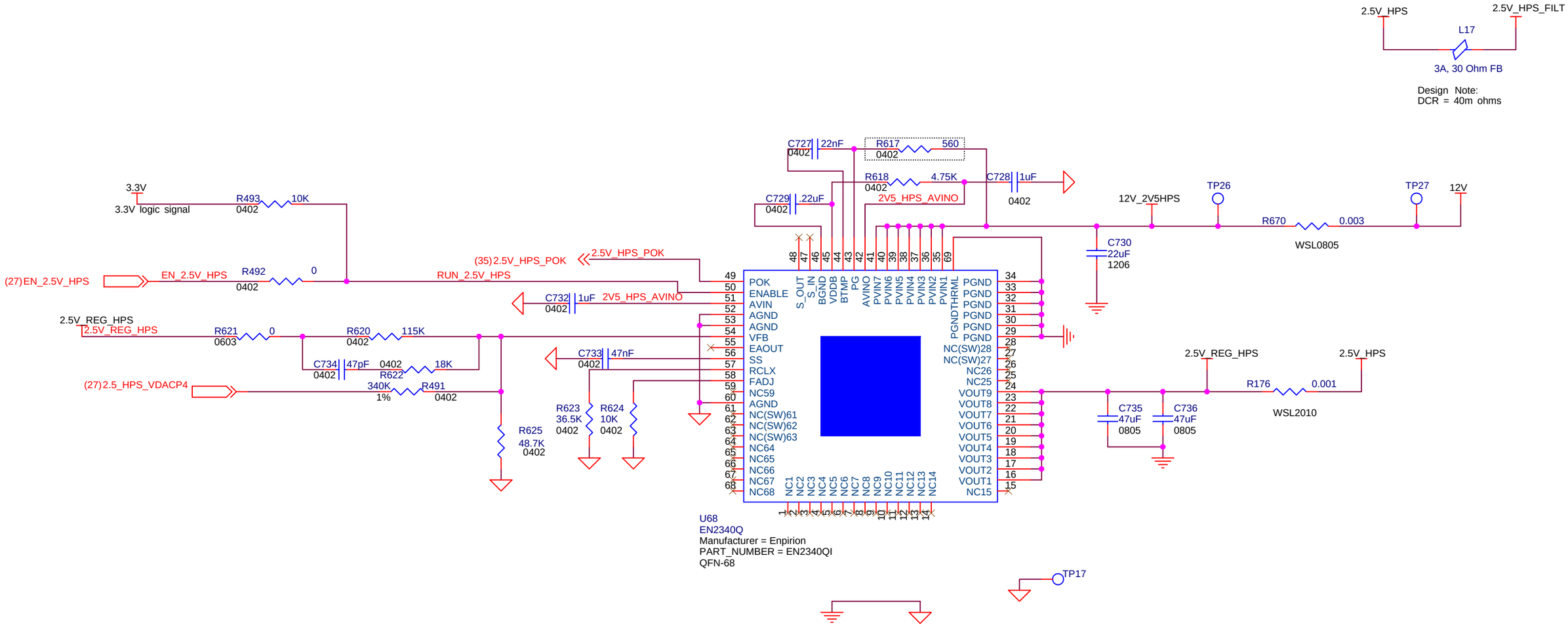
Power 3 - 2.5V HPS



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Title: **Cyclone V SoC FPGA Development Kit Board**

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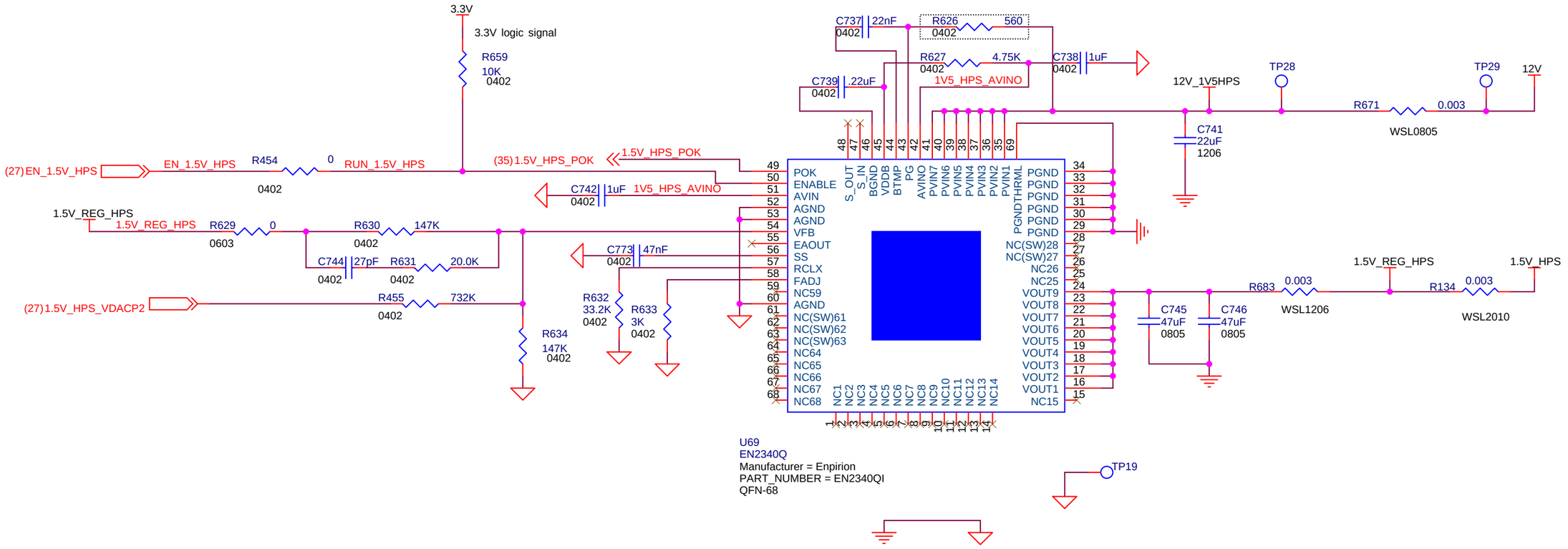
Power 3 - 1.5V & 1.5V HPS



Size	Document Number	Rev
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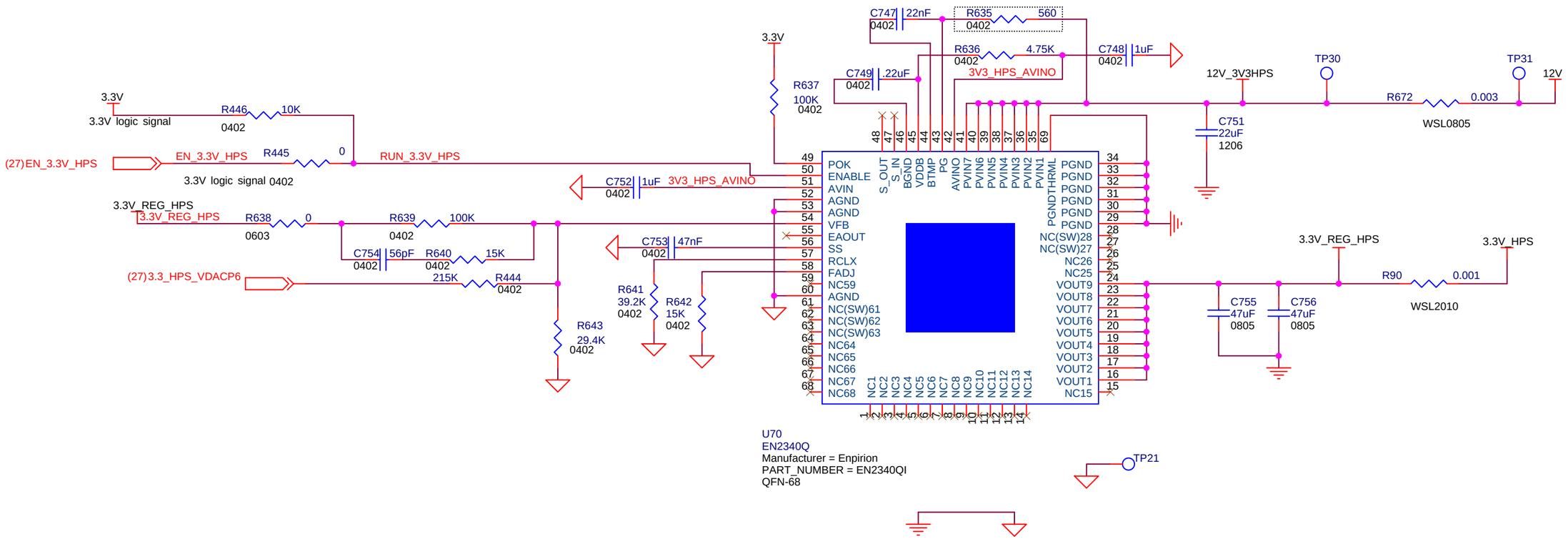
Power 3 - 3.3V HPS



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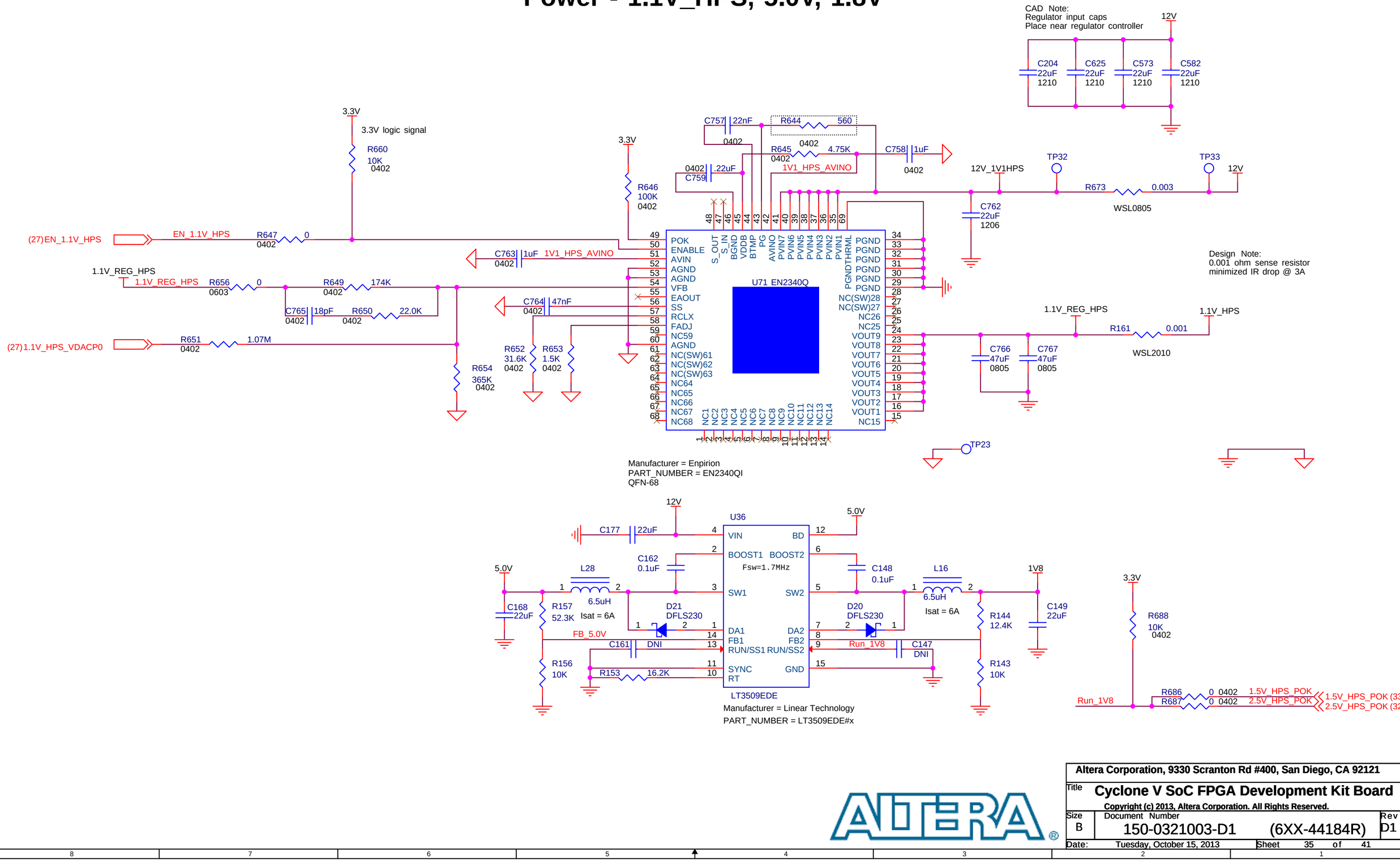
Power - 1.1V_HPS, 5.0V, 1.8V



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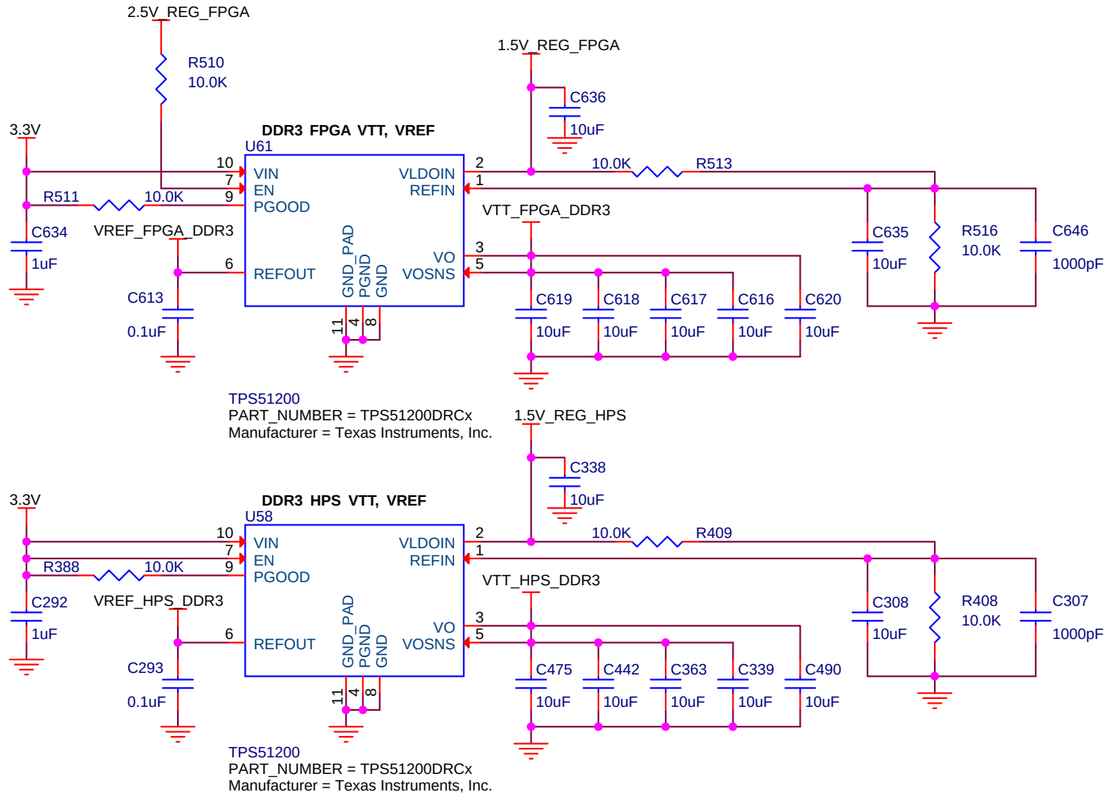
Power 4 - Linear Regulators



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Power 6 - Power & Temperature Monitor

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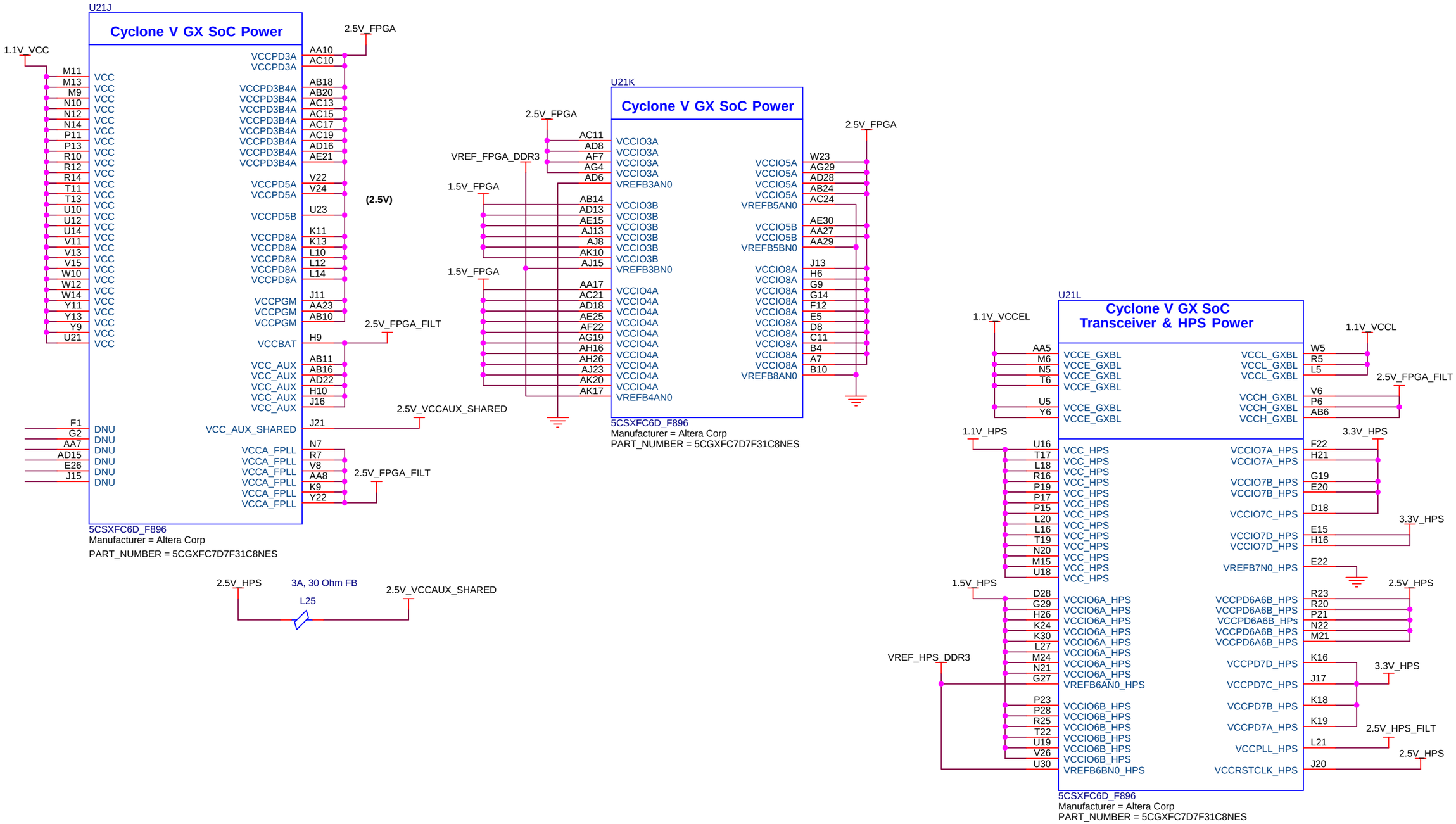
Power 7 - Cyclone V GX SoC Power



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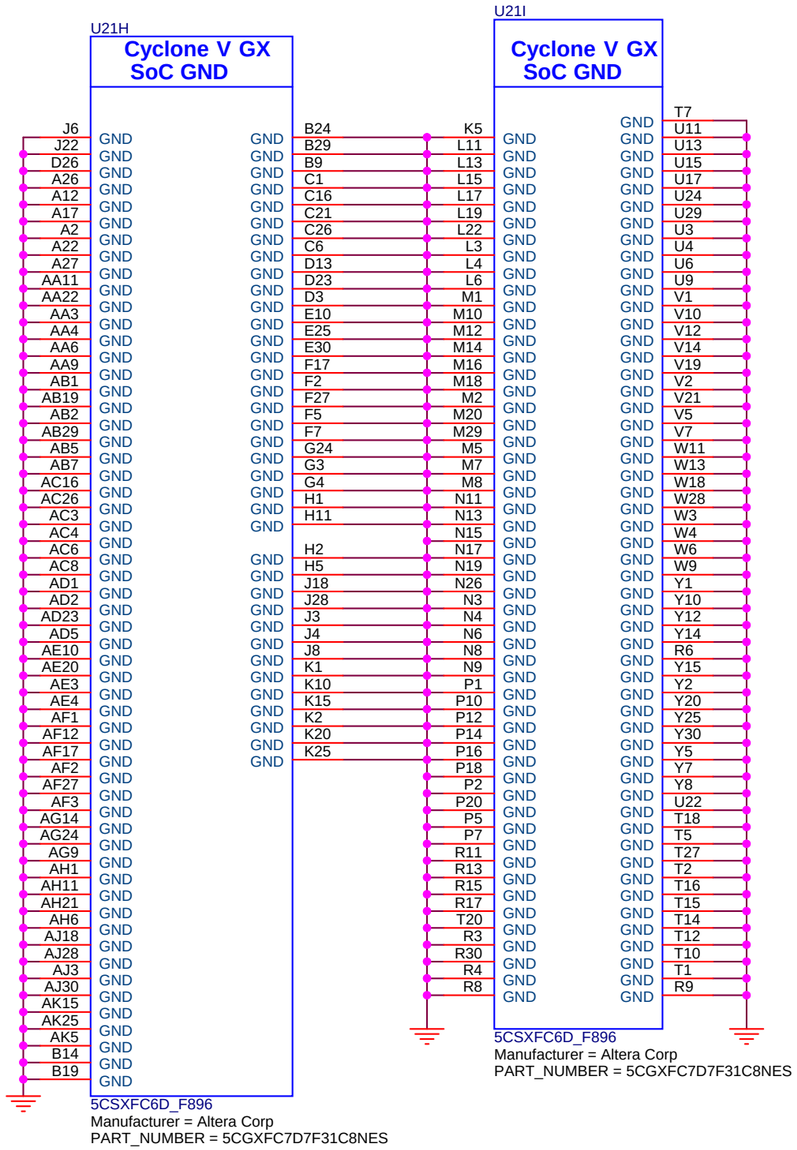
Power 8 - Cyclone V GX SoC Ground



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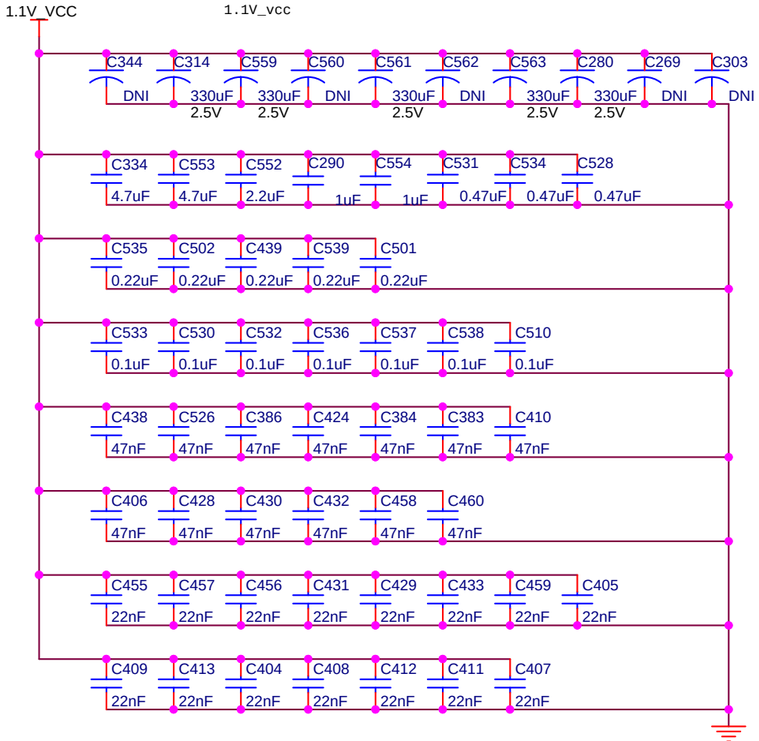
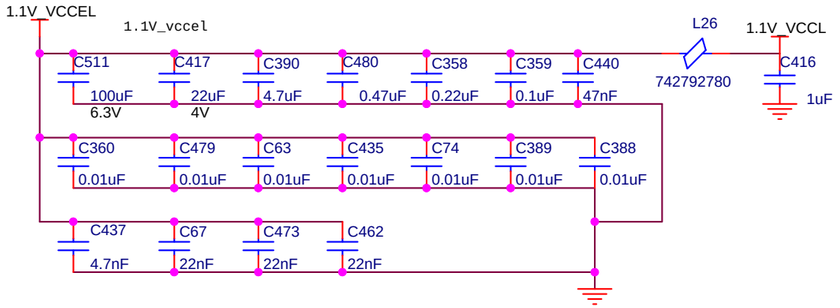
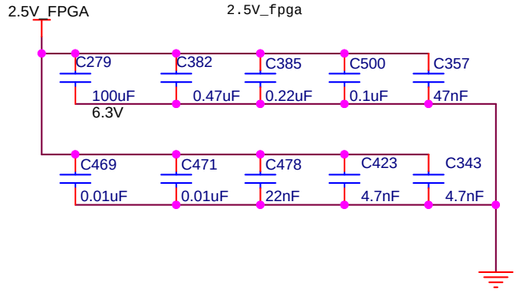
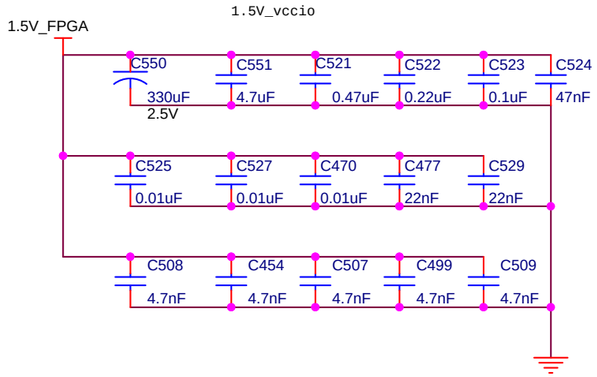
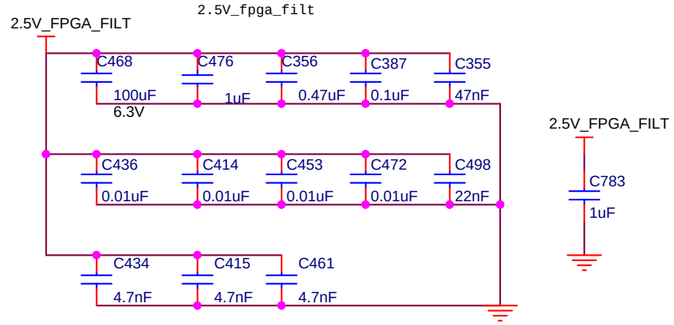
Decoupling

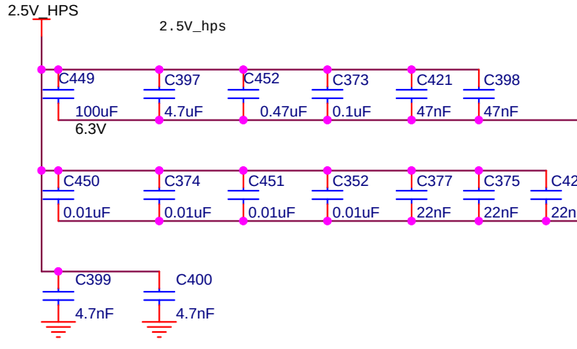


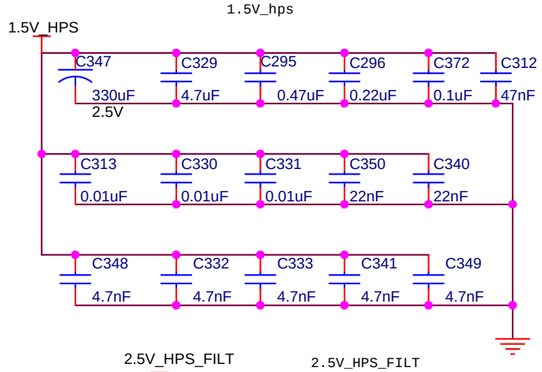


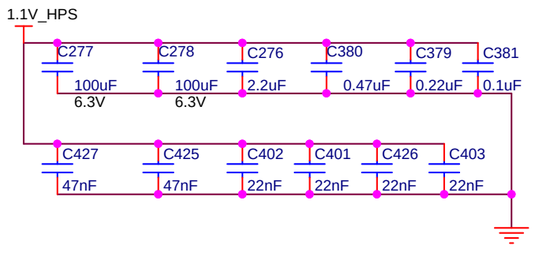


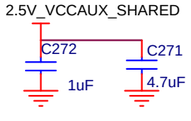


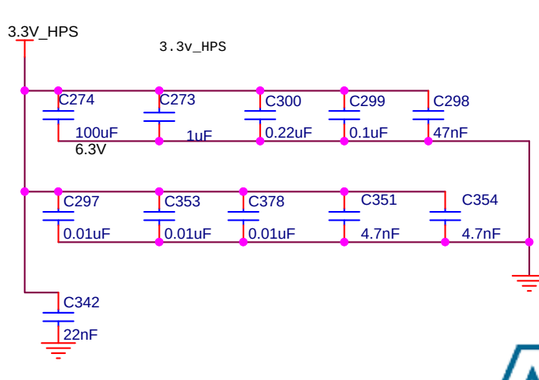


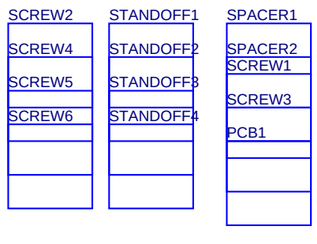


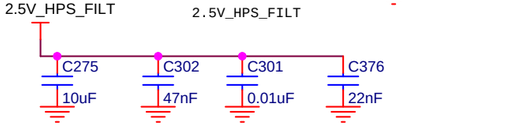












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REV	DATE	PAGES	DESCRIPTION
D1	06/28/2013	29-35	Initial version with Enpirion Power Supply
	07/01/2013	30-35	Input cap configuration is changed from 2 x 1206 caps to 1 x 1206 cap
	07/01/2013	30-35	Output cap configuration is changed from 2 x 1206 caps to 2 x 0805 caps
	07/01/2013	29-35	Input sense resistor 1206 size is added
	07/01/2013	29	0 ohm resistor DNL is added for current sensing option at load,OCP circuit is added
	07/03/2013	29-35	Added SMT testpoints at 0 ohm resistor at input rails
	07/03/2013	6	U21.F16 is connected to CODEC_SEL, R32 marked DNL
	07/03/2013	14	R390 and R391 changed to 1K
	07/03/2013	19	R479,R512,R515 changed to 4.7K 1% with load option. R480, R512,R276,R274 marked as DNL.
	07/03/2013	19	R522 is added with 4.7K DNL on RNET2_TX_CLK_FB net. R526,RR525 is changed to 0 Ohm load.
	07/03/2013	21	U5 is changed to N25Q512A83GSF40F. R319 is marked as DNL, R311 is changed to 4.7K
	07/03/2013	22	U1 is cahnged to MAX14523B. Changed C1 to 1uF,C8 to 1uF. C9,C243,C242,C2,C3 were removed.
	07/03/2013	22	J1 change to Micro AB USB type connector.
	07/03/2013	27	Netnames were corrected as per correct power rail name.
	07/10/2013	21	Warm_Reset signal is connected to U5 pin3.
	07/10/2013	6	J32 pin 10 is conncted to 3.3V from 5V
	07/10/2013	35	PIN 9 of U36 pulled to 2.5V HPS.
	07/16/2013	21,16	Connected QSPI reset signal on pin 3 of U5 to pin C11 of the MAX V system controller U19
	07/23/2013	19	R522,R274,R276 is changed to Load from DNL.U45 changed to UPD60620AGK-GAK-AX#YB1
	07/26/2013	30-35	560 Ohm resistors from PG to PVIN on the EN2340 parts are made Install
	07/26/2013	30-35	All the input sense resistors are changed to 0805 size.
	07/26/2013	14,21	R389,R390 changed to 33 ohms. Added 2K pull up on QSPI_RESET signal.
	07/26/2013	22	Added 10K pull up in SD_DAT0,
	07/26/2013	23	R425 is changed to DNI and R434 is changed to 0 ohm load.
	07/26/2013	38	VCC_AUX pins connected to 2.5V FPGA_FILT from 2.5V HPS_FILT
	07/26/2013	40	1uF 0402 cap is added on 2.5V_FPGA_FILT net
	08/01/2013	40	Added 10K pullup on SD_DAT0,SD_DAT1,SD_DAT2,SD_CMD. 316K pull down on SD_DAT3.
	08/06/2013	6,17	Added RC termination on JTAG_MUX_TCK and JTAG_HPS_TCK
	08/07/2013	12	Removed DNI resistors from JTAG chain - R343R344,R345,R346,R351,R352,R353,R354,R355, R356,R357,R358,R359,R360,R361,R380,R381,R382,R383,R384,R385,R386,R387,R398,R399 ,R400,R401,R402,R403,R404,R405.

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