Digital Systems I

Computer Assignment #2

Basic Switch and Gate Structures in SystemVerilog

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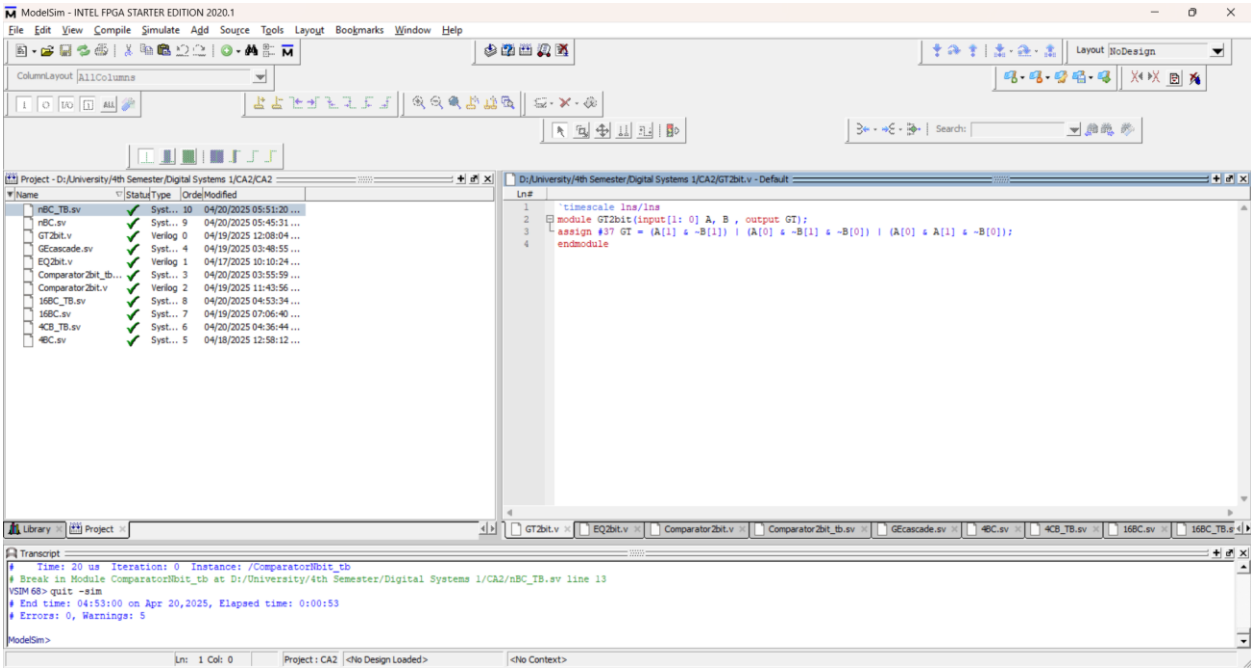
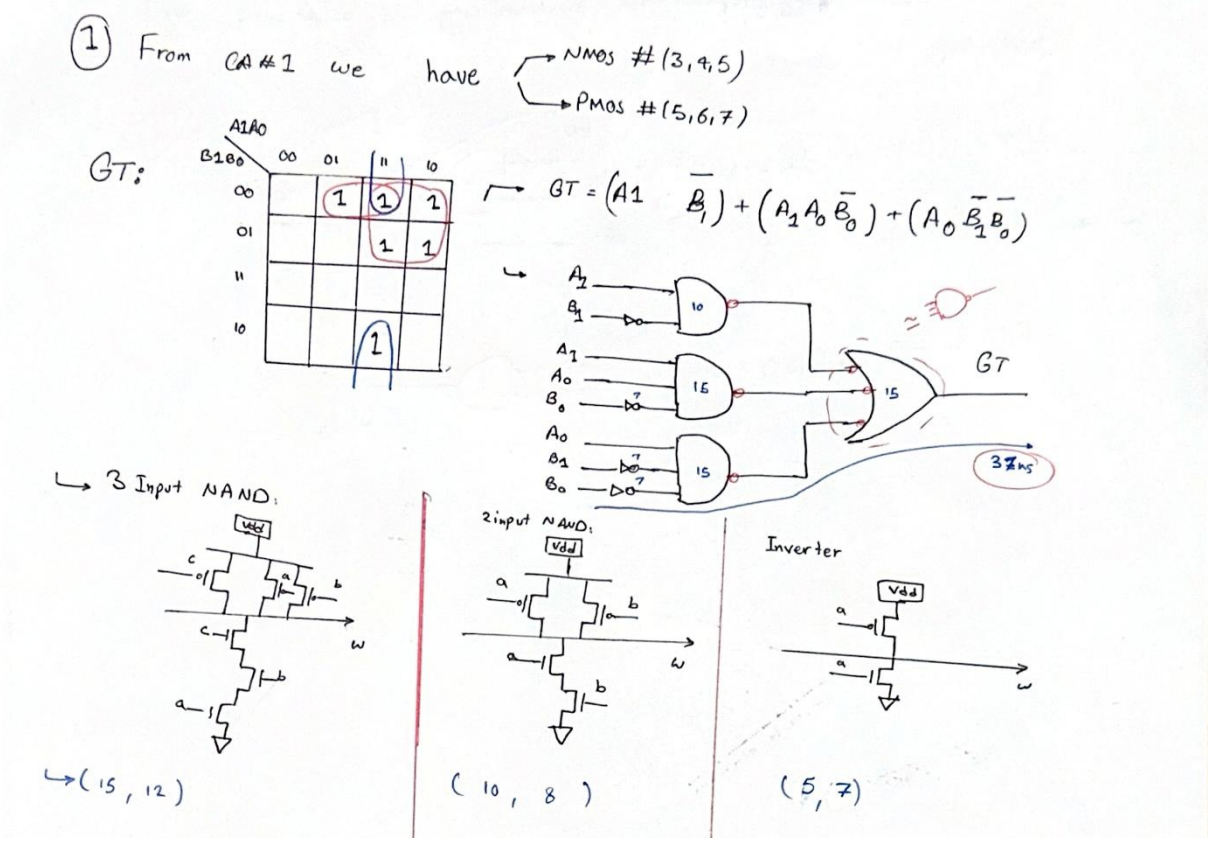
Introduction

This is an image of the project that I have created in ModelSim for the simulation of my circuit.



Question 1

Calculating gates delay on paper

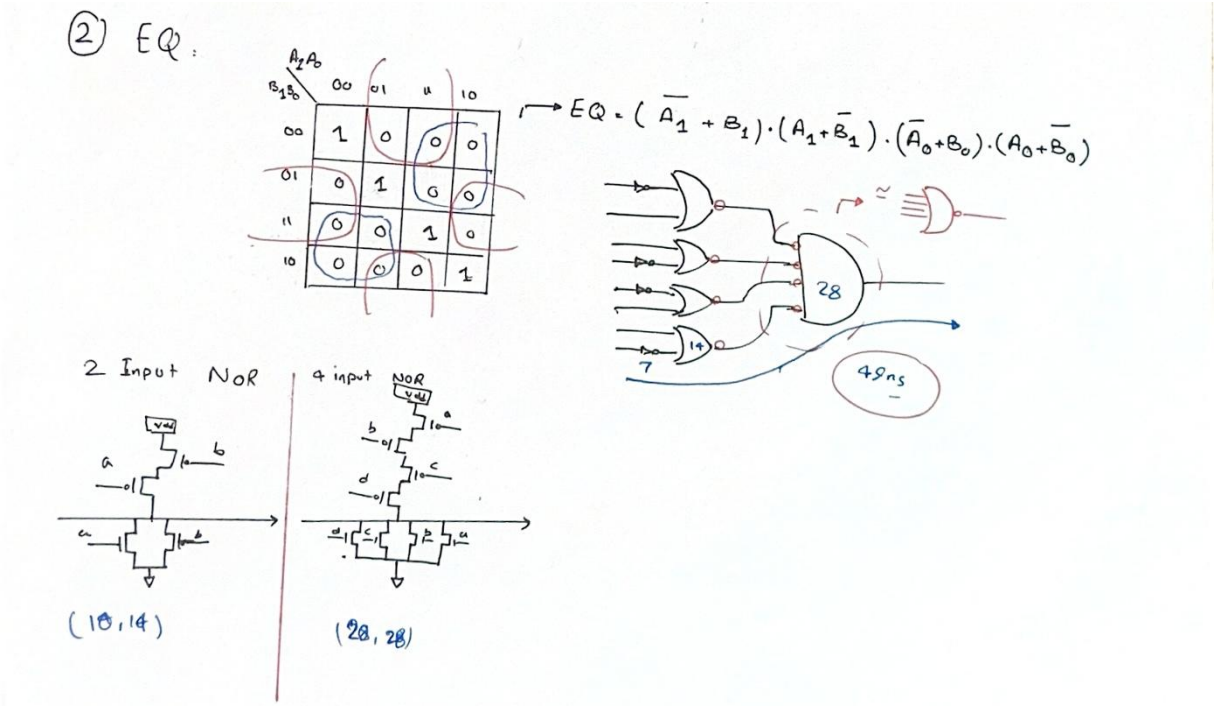


Code

```
`timescale 1ns/1ns
module GT2bit(input[1: 0] A, B , output GT);
assign #37 GT = (A[1] & ~B[1]) | (A[0] & ~B[1] & ~B[0]) | (A[0] & A[1] & ~B[0]);
endmodule
```

Question 2

Calculating gates delay on paper



Code

```
1   `timescale 1ns/1ns
2   module EQ2bit(input[1: 0] A, B , output EQ);
3   assign #49 EQ = (~A[1] | B[1]) & (A[1] | ~B[1]) & (~A[0] | B[0]) & (A[0] | ~B[0]);
4   endmodule
```

Question 3

For this part, because I have used GT2bit and EQ2bit modules, I expect 49ns delay as my 2-bit comparator's worst-case delay. Because it is between these 2 modules and EQ2bit has higher delay (49 > 37).

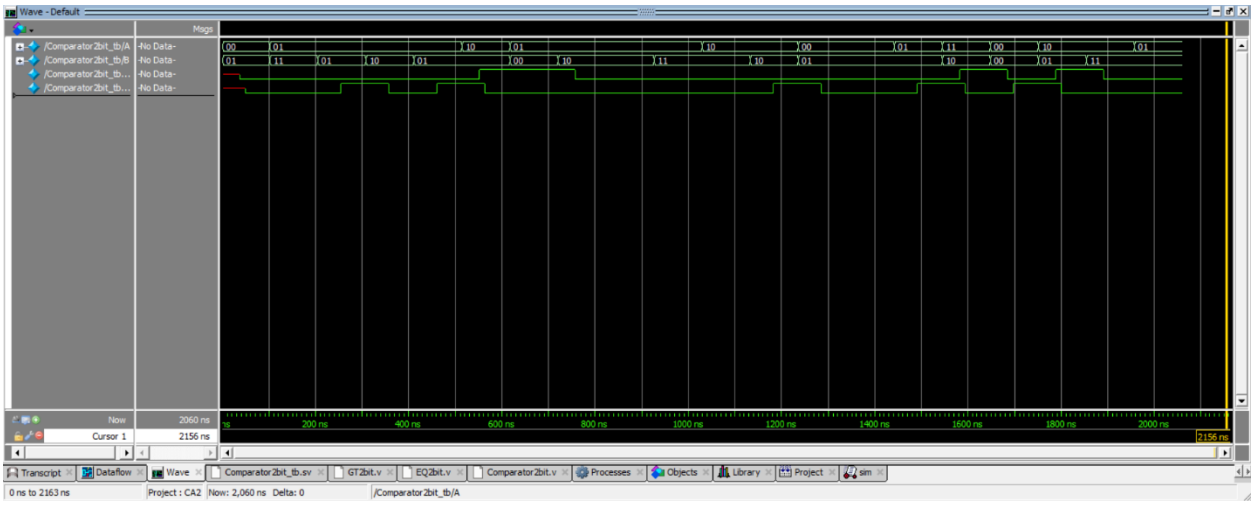
Code

```
`timescale 1ns/1ns
module Comparator2bit(input  [1:0] A, B, output GT, EQ);
    GT2bit gt(.A(A), .B(B), .GT(GT));
    EQ2bit eq(.A(A), .B(B), .EQ(EQ));
endmodule
```

Testbench

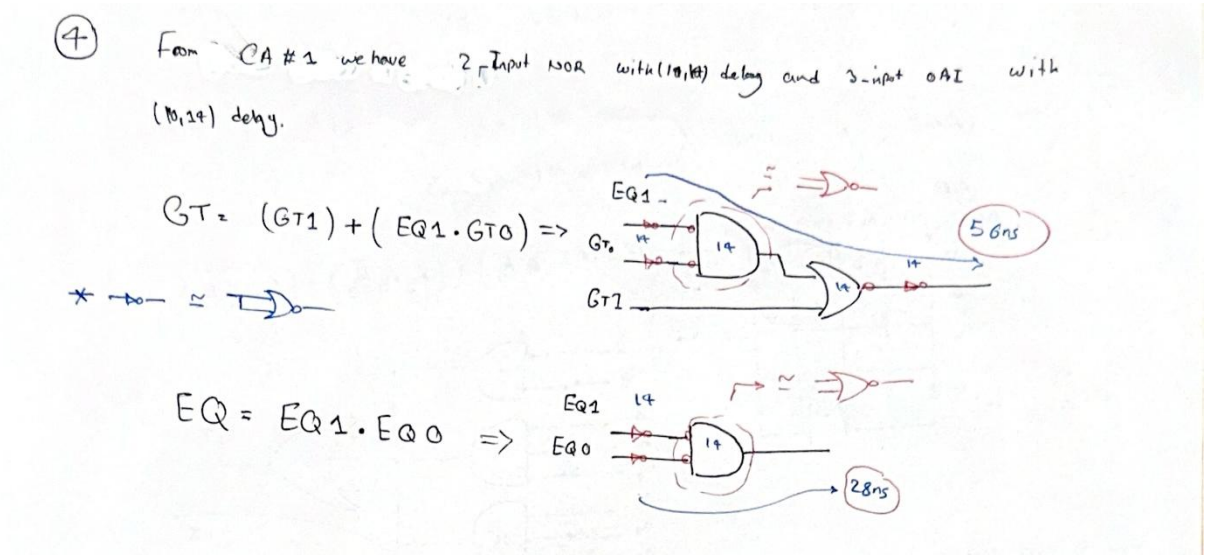
```
`timescale 1ns/1ns
module Comparator2bit_tb();
  logic [1:0] A, B;
  logic GT, EQ;
  Comparator2bit uut(.A(A), .B(B), .GT(GT), .EQ(EQ));
  initial begin
    repeat (20) begin
      A = $random() % 4;
      B = $random() % 4;
      #103;
    end
    $stop;
  end
endmodule
```

Output



Question 4

Building circuit on paper



Code

```
1   `timescale 1ns/1ns
2   module GEcascade(input GT1, GT0, EQ1, EQ0, output logic GT, EQ);
3       assign #56 GT = (EQ1 & GT0) | GT1;
4       assign #28 EQ = EQ1 & EQ0;
5   endmodule
```

Question 5

For this part, because I have used Comparator2bit and GEcascade modules, I expect 105ns delay as my 4-bit comparator's worst-case delay. Because GEcascade needs the output of 2-bit Comparators so it is 49 + 56 = 105. GEcascade's delay is 56ns because of the expressions and circuits that I explained and drew in Question 4.

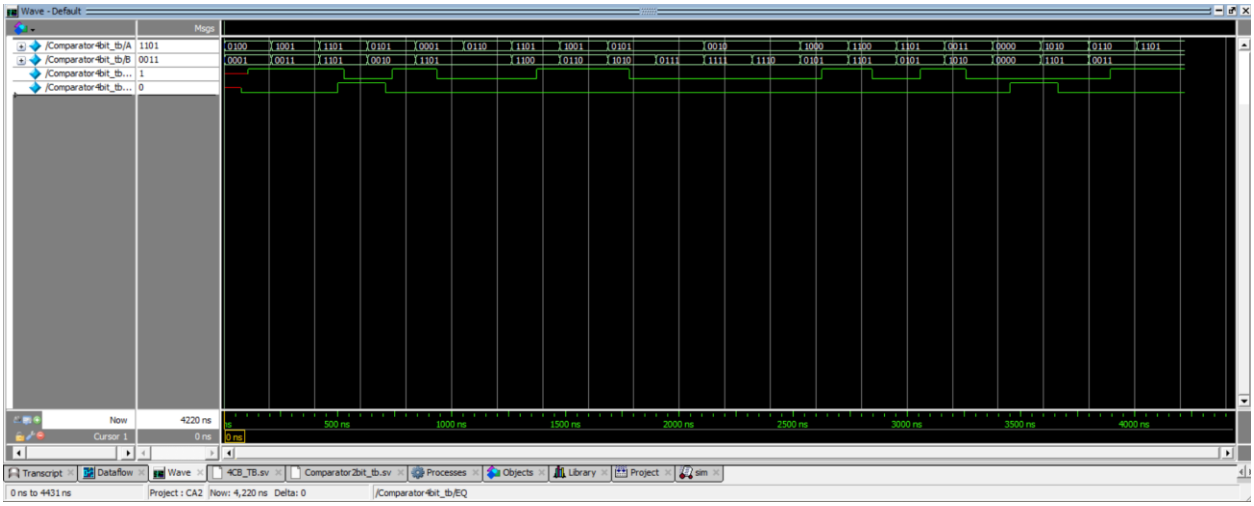
Code

```
1  `timescale 1ns/1ns
2  module Comparator4bit (input  [3:0] A, B, output GT, EQ);
3     wire GT1, EQ1, GT0, EQ0;
4     Comparator2bit hi (.A(A[3:2]), .B(B[3:2]), .GT(GT1), .EQ(EQ1));
5     Comparator2bit lo (.A(A[1:0]), .B(B[1:0]), .GT(GT0), .EQ(EQ0));
6     GEcascade ge(.GT1(GT1), .EQ1(EQ1), .GT0(GT0), .EQ0(EQ0), .GT(GT), .EQ(EQ));
7  endmodule
```

Testbench

```
1  `timescale 1ns/1ns
2  module Comparator4bit_tb;
3    logic [3:0] A, B;
4    logic GT, EQ;
5    Comparator4bit uut(.A(A), .B(B), .GT(GT), .EQ(EQ));
6    initial begin
7      repeat (20) begin
8        A = $random() % 16;
9        B = $random() % 16;
10       #211;
11     end
12     $stop;
13   end
14 endmodule
```

Output


Wave - Default
Msgs
/Comparator4bit_tb/A
/Comparator4bit_tb/B
/Comparator4bit_tb...
/Comparator4bit_tb...
1101
0011
1
0
Now
4220 ns
Cursor 1
0 ns
500 ns
1000 ns
1500 ns
2000 ns
2500 ns
3000 ns
3500 ns
4000 ns
Transcript
Dataflow
Wave
4CB_TB.sv
Comparator2bit_tb.sv
Processes
Objects
Library
Project
sim
0 ns to 4431 ns
Project : CA2
Now: 4,220 ns Delta: 0
/Comparator4bit_tb/EQ

Question 6

As I explained my idea about last part, I expect 56 + 105 = 161ns delay for 8-bit comparator and 161+56 = 217ns delay for 16-bit comparator.

Code

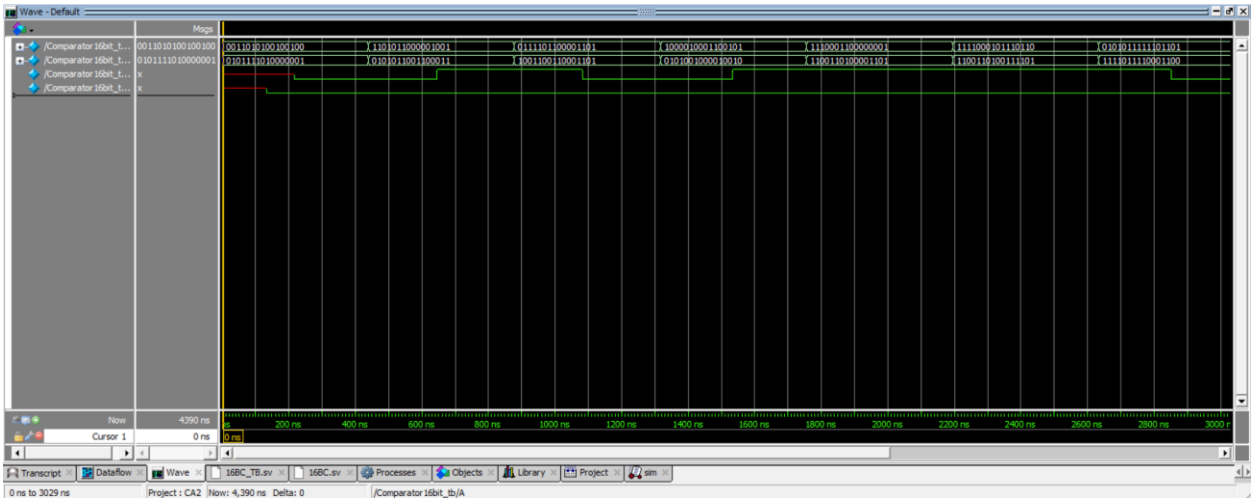
```
`timescale 1ns/1ns
module Comparator8bit(input[7:0] A, B, output GT, EQ);
   wire GT1, EQ1, GT0, EQ0;
   Comparator4bit hi (.A(A[7:4]), .B(B[7:4]), .GT(GT1), .EQ(EQ1));
   Comparator4bit lo (.A(A[3:0]), .B(B[3:0]), .GT(GT0), .EQ(EQ0));
   GEcascade ge(.GT1(GT1), .EQ1(EQ1), .GT0(GT0), .EQ0(EQ0), .GT(GT), .EQ(EQ));
endmodule

module Comparator16bit(input[15:0] A, B, output GT, EQ);
   wire GT1, EQ1, GT0, EQ0;
   Comparator8bit hi (.A(A[15:8]), .B(B[15:8]), .GT(GT1), .EQ(EQ1));
   Comparator8bit lo (.A(A[7:0]), .B(B[7:0]), .GT(GT0), .EQ(EQ0));
   GEcascade ge(.GT1(GT1), .EQ1(EQ1), .GT0(GT0), .EQ0(EQ0), .GT(GT), .EQ(EQ));
endmodule
```

Testbench

```
`timescale 1ns/1ns
module Comparator16bit_tb;
  logic [15:0] A, B;
  logic GT, EQ;
  Comparator16bit uut(.A(A), .B(B), .GT(GT), .EQ(EQ));
  initial begin
    repeat (10) begin
      A = $random() % (2**16);
      B = $random() % (2**16);
      #439;
    end
    $stop;
  end
endmodule
```

Output


Wave - Default
Msgs
/Comparator 16bit_t...
/Comparator 16bit_t...
/Comparator 16bit_t...
/Comparator 16bit_t...
Now
4390 ns
Cursor 1
0 ns
200 ns
400 ns
600 ns
800 ns
1000 ns
1200 ns
1400 ns
1600 ns
1800 ns
2000 ns
2200 ns
2400 ns
2600 ns
2800 ns
Transcript
Dataflow
Wave
16BC_TB.sv
16BC.sv
Processes
Objects
Library
Project
sim
0 ns to 3029 ns
Project : CA2
Now: 4,390 ns
Delta: 0
/Comparator 16bit_tb/A

Question 7

In general, the delay for each n-bit comparator was 56*n+49. For each testbench, I chose the nearest to twice that delay. But here is kind of different because now we have a for loop. So here we have a 2-bit comparator and a GEcascade that iterates for n/2 times. So now I expect 105(n/2) for each one as worst-case delay. For example we have about 840ns delay for 16-bit comparator.

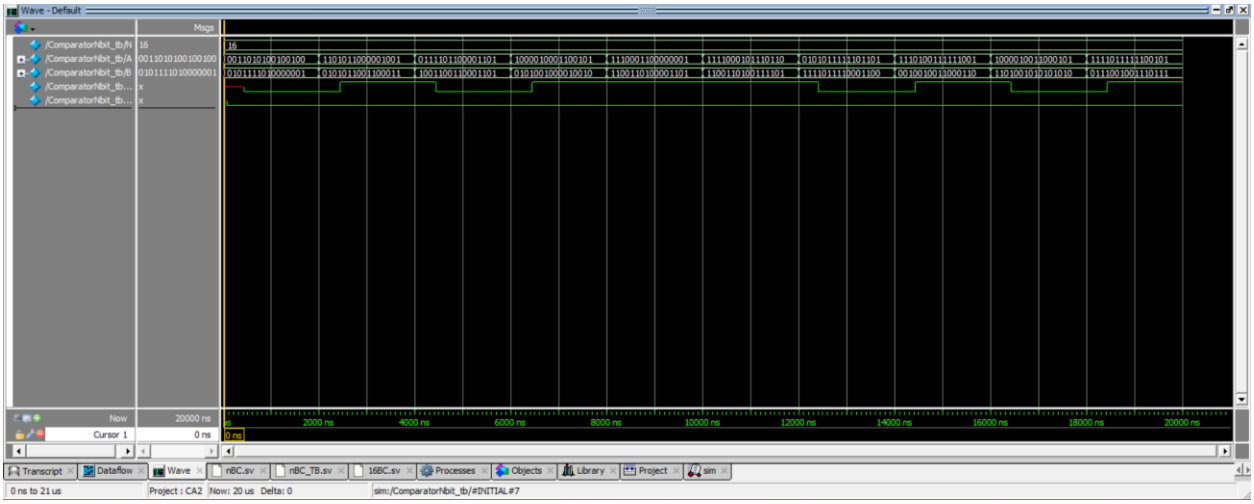
Code

```
1   `timescale 1ns/1ns
2   module ComparatorNbit #(parameter N = 16) (input [N-1:0] A, B, output GT, EQ);
3       logic [N/2-1:0] gt, eq;
4       assign gt[0] = 0;
5       assign eq[0] = 1;
6       genvar i;
7       generate
8           for (i = 0; i < N/2; i++) begin
9               logic gti, eqi;
10              Comparator2bit c2 (.A(A[N - 2*i - 1 -: 2]), .B(B[N - 2*i - 1 -: 2]), .GT(gti
                ), .EQ(eqi));
11              GEcascade ge (.GT1(gt[i]), .EQ1(eq[i]), .GT0(gti), .EQ0(eqi), .GT(gt[i+1]), .
                EQ(eq[i+1]));
12          end
13      endgenerate
14      assign GT = gt[N/2-1];
15      assign EQ = eq[N/2-1];
16  endmodule
```

Testbench

```
1   `timescale 1ns/1ns
2   module ComparatorNbit_tb();
3     parameter N = 16;
4     logic [N-1:0] A, B;
5     logic GT, EQ;
6     ComparatorNbit #(N) uut(.A(A), .B(B), .GT(GT), .EQ(EQ));
7     initial begin
8       repeat (10) begin
9         A = $random() % (2**N);
10        B = $random() % (2**N);
11        #2000;
12      end
13      $stop;
14    end
15  endmodule
```

Output


Wave - Default
Msgs
/ComparatorNbit_tb/N
/ComparatorNbit_tb/A
/ComparatorNbit_tb/B
/ComparatorNbit_tb...
/ComparatorNbit_tb...
16
0011010100100100
0101111010000001
x
x
Now
20000 ns
Cursor 1
0 ns
2000 ns
4000 ns
6000 ns
8000 ns
10000 ns
12000 ns
14000 ns
16000 ns
18000 ns
20000 ns
Transcript
Dataflow
Wave
nBC.sv
nBC_TB.sv
16BC.sv
Processes
Objects
Library
Project
sim
0 ns to 21 us
Project : CA2
Now: 20 us Delta: 0
sim:/ComparatorNbit_tb/#INITIAL#7