Digital Systems I – CA1

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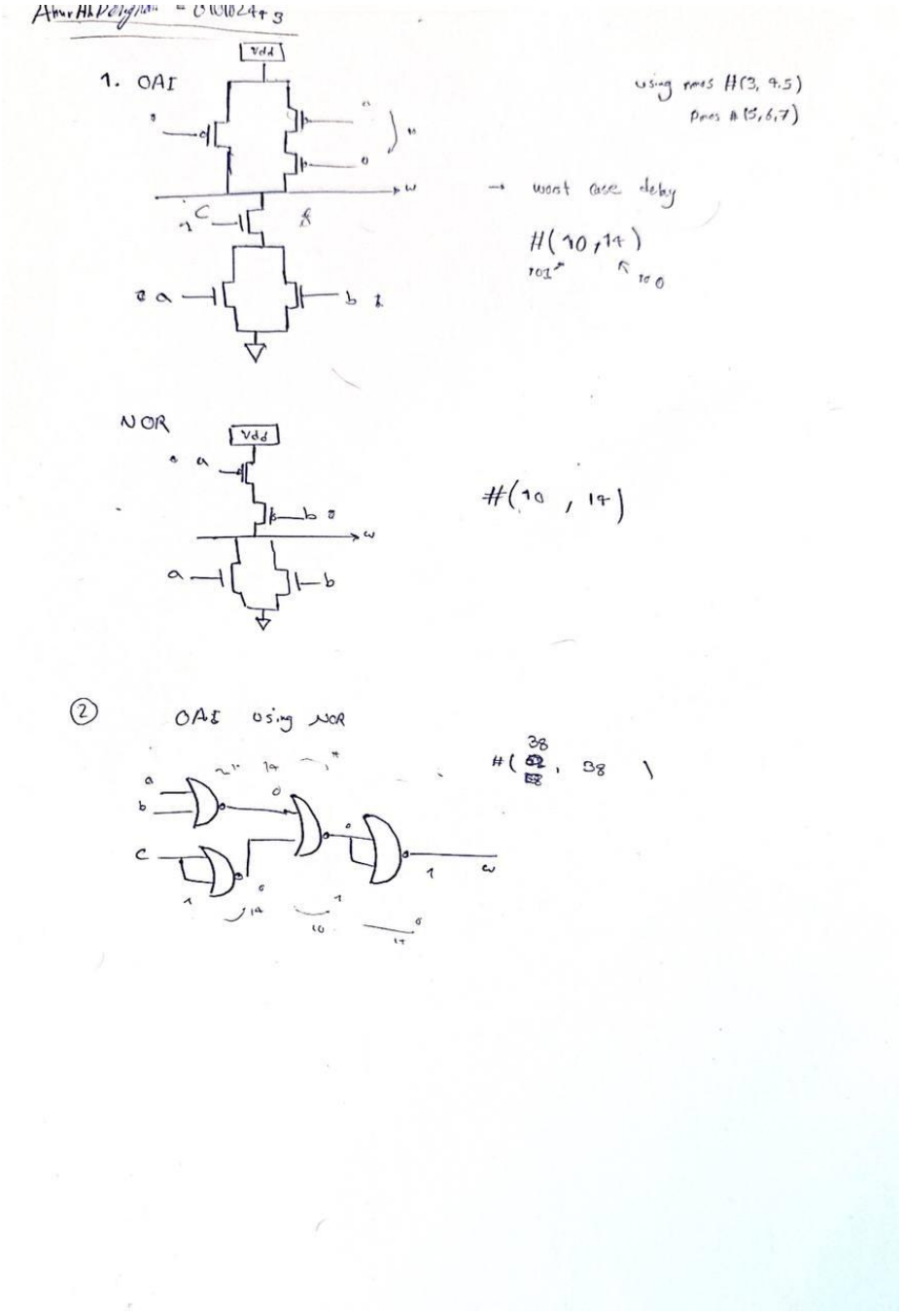
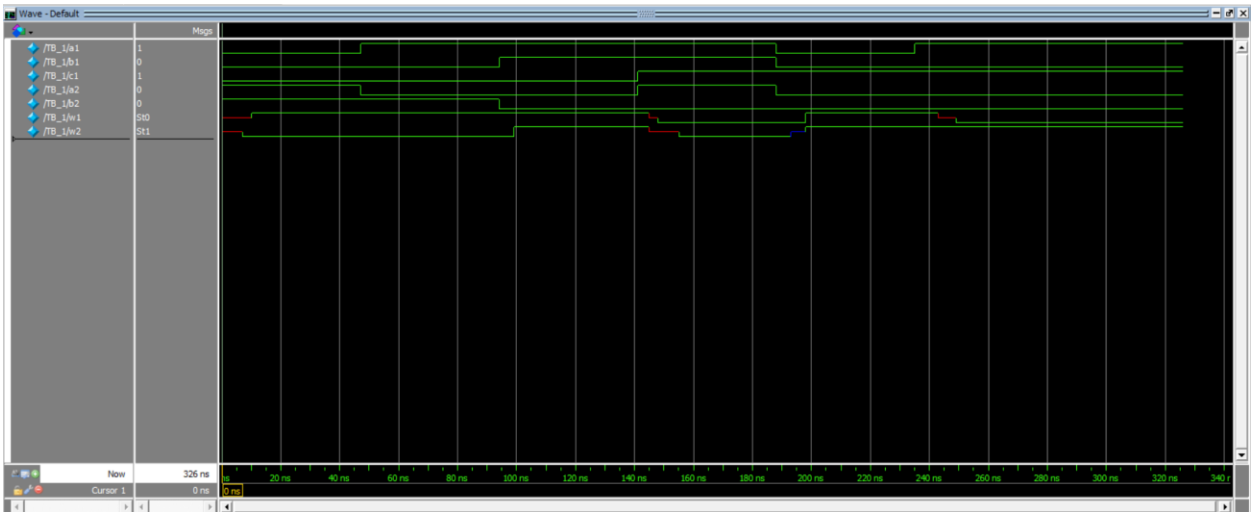
Part 1

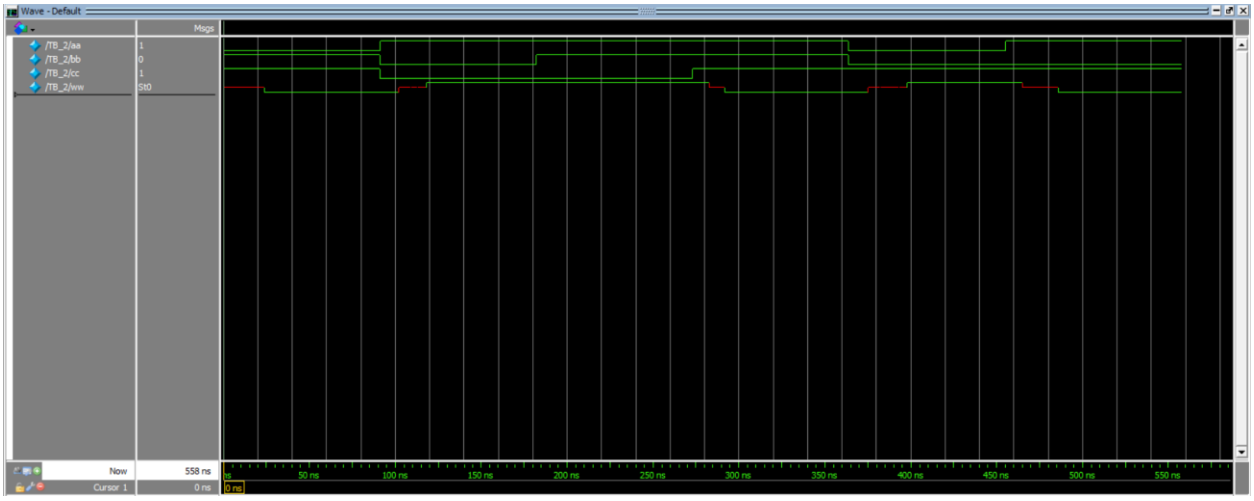


```
`timescale 1ns/1ns
module myNor_switch(input a, b, output w);
supply1 vdd;
supply0 gnd;
wire j;
pmos #(5, 6, 7) T1(j, vdd, a), T2(w, j, b);
nmos #(3, 4, 5) T3(w, gnd, a), T4(w, gnd, b);
endmodule
////////////////////////////////////////////////////////////////////////////////
`timescale 1ns/1ns
module myOAI_switch(input a, b, c, output w);
supply1 vdd; supply0 gnd;
wire i,j;
pmos #(5, 6, 7) T1(i, vdd, a), T2(w, i, b), T3(w, vdd, c);
nmos #(3, 4, 5) T4(j, gnd, a), T5(j, gnd, b), T6(w, j, c);
endmodule
////////////////////////////////////////////////////////////////////////////////
`timescale 1ns/1ns
module TB_1 ();
  reg a1=0,b1=0,c1=0,a2=1,b2=1;
  wire w1, w2;
  myOAI_switch cut1(a1,b1,c1,w1);
  myNor_switch cut2(a2,b2,w2);
  initial begin
    #47
    a1=1; b1=0; c1=0;  a2=0; b2=1;
    #47
    a1=1; b1=1; c1=0;  b2=0; a2=0;
    #47
    a1=1; b1=1; c1=1;  a2=1; b2=0;
    #47
    a1=0; b1=0; c1=1;  b2=0; a2=0;
    #47
    a1=1; b1=0; c1=1;
    #91
    $stop;
  end
endmodule
```



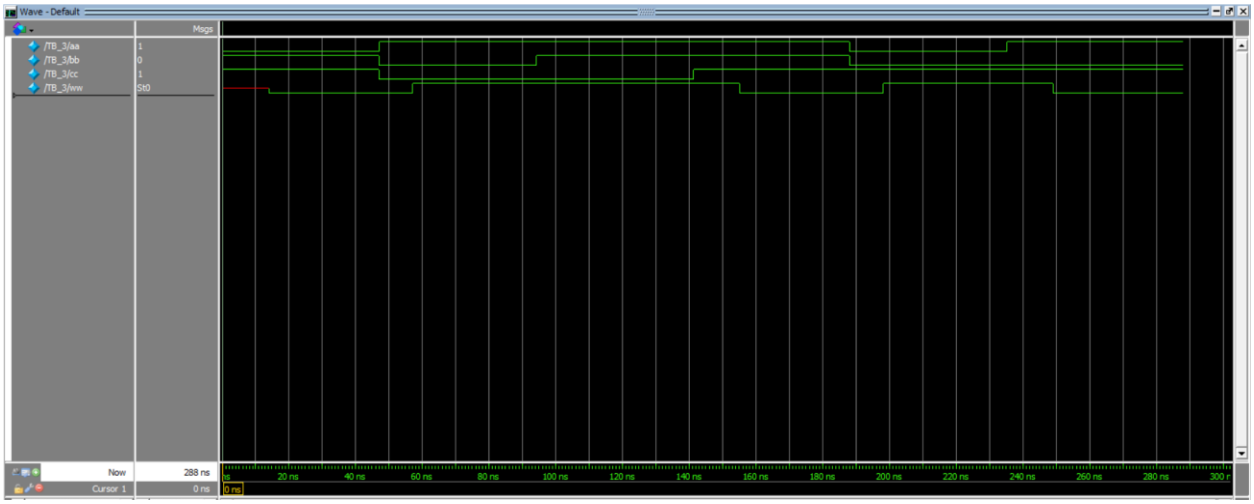
Part 2

```
`timescale 1ns/1ns
module myOAI_norGate(input a, b, c, output w);
wire i, j, k;
myNor_switch n1(a, b, i), n2(c, c, j), n3(i,j,k), n4(k, k, w);
endmodule
////////////////////////////////////////////////////////////////
`timescale 1ns/1ns
module TB_2();
reg aa = 0, bb = 1, cc = 1;
wire ww;
myOAI_norGate cut(aa, bb, cc, ww);
initial begin
    #47 aa = 1; bb = 0; cc = 0;
    #47 aa = 1; bb = 1; cc = 0;
    #47 aa = 1; bb = 1; cc = 1;
    #47 aa = 0; bb = 0; cc = 1;
    #47 aa = 1; bb = 0; cc = 1;
    #103 $stop;
end
endmodule
```



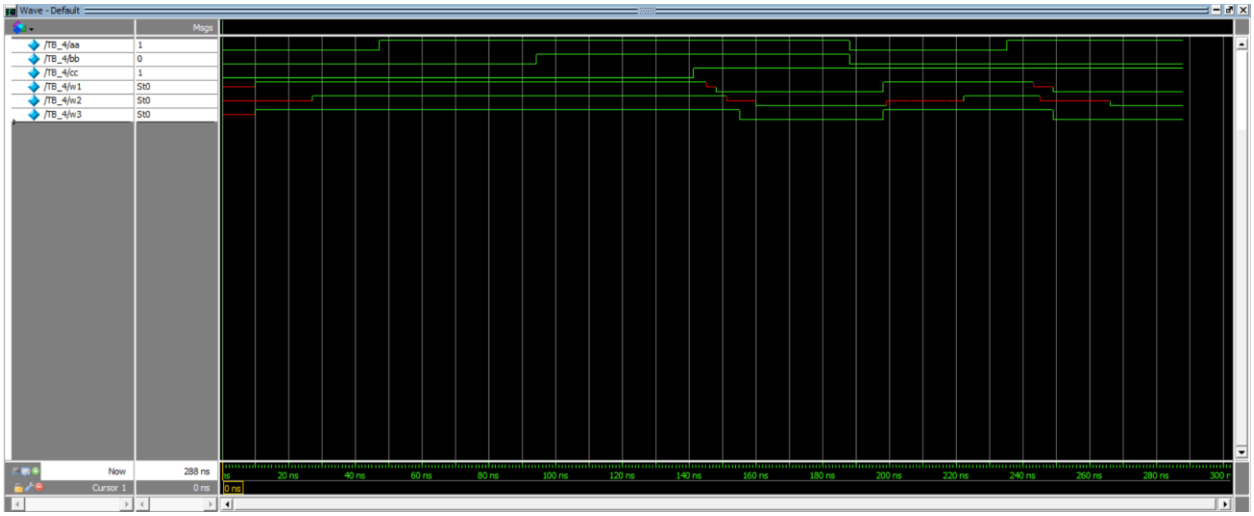
Part 3

```
`timescale 1ns/1ns
module myOAI_boolalg (input a,b,c, output w);
  assign #(10, 14)  w = ~((a|b)&c);
endmodule
////////////////////////////////////////////////////////////////
`timescale 1ns/1ns
module TB_3();
reg aa = 0, bb = 1, cc = 1;
wire ww;
myOAI_boolalg cut(aa, bb, cc, ww);
initial begin
    #47 aa = 1; bb = 0; cc = 0;
    #47 aa = 1; bb = 1; cc = 0;
    #47 aa = 1; bb = 1; cc = 1;
    #47 aa = 0; bb = 0; cc = 1;
    #47 aa = 1; bb = 0; cc = 1;
    #53 $stop;
end
endmodule
```



Part 4

```
`timescale 1ns/1ns
module TB_4();
reg aa = 0, bb = 0, cc = 0;
wire w1, w2, w3;
myOAI_switch cut1(aa, bb, cc, w1);
myOAI_norGate cut2(aa, bb, cc, w2);
myOAI_boolalg cut3(aa, bb, cc, w3);
initial begin
    #47 aa = 1; bb = 0; cc = 0;
    #47 aa = 1; bb = 1; cc = 0;
    #47 aa = 1; bb = 1; cc = 1;
    #47 aa = 0; bb = 0; cc = 1;
    #47 aa = 1; bb = 0; cc = 1;
    repeat(7) #53 $stop;
end
endmodule
```

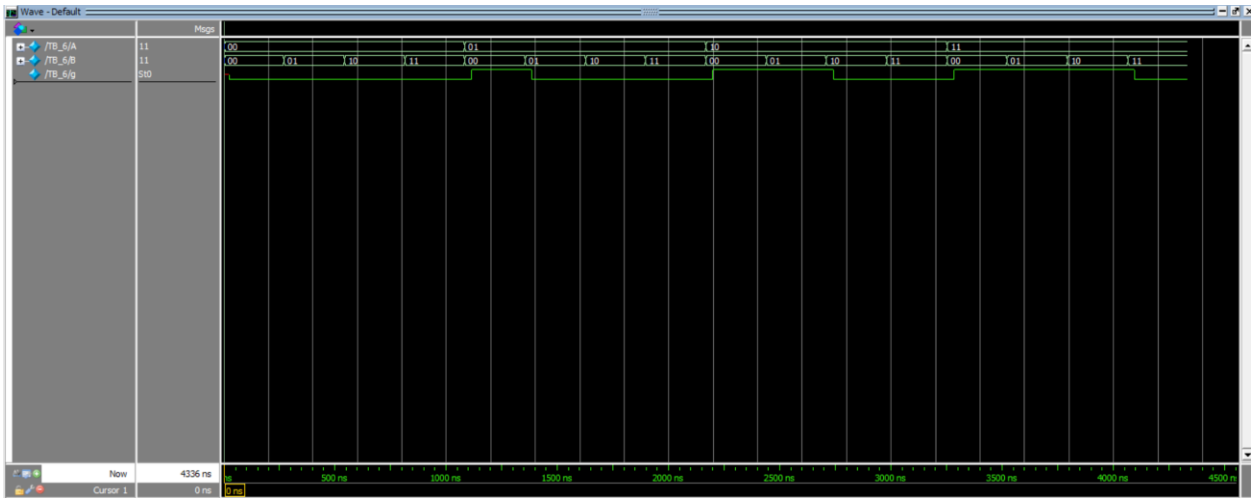


Part 5

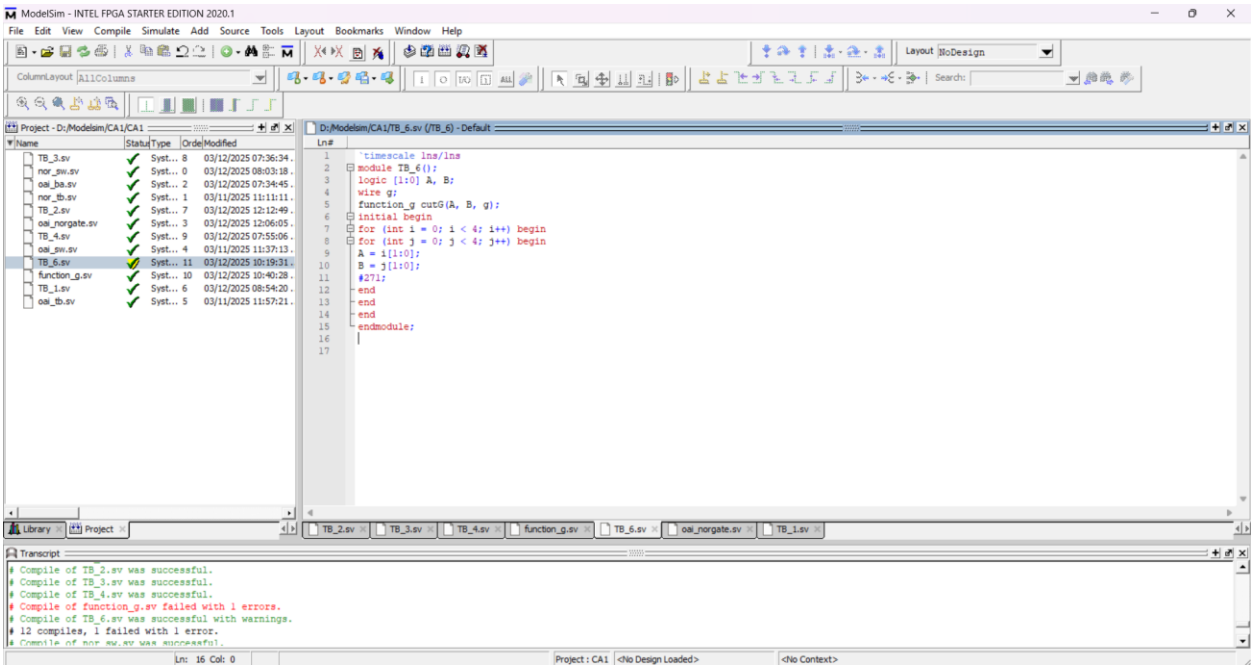
```
`timescale 1ns/1ns
module myNOT(input a, output b);
supply1 vdd;
supply0 gnd;
pmos #(5, 6, 7) T1(b, vdd, a);
nmos #(3, 4, 5) T2(b, gnd, a);
endmodule

module function_g(input[1:0] A, input[1:0] B, output g);
wire i, j, a0, a1, b0, b1;
myNOT N1(.a(A[0]), .b(a0));
myNOT N2(.a(B[0]), .b(b0));
myNOT N3(.a(B[1]), .b(b1));
myOAI_boolalg OAI1(.a(A[1]), .b(b1), .c(b0), .w(i));
myOAI_boolalg OA2(.a(A[1]), .b(A[1]), .c(b1), .w(j));
myOAI_boolalg OA3(.a(a0), .b(i), .c(j), .w(g));
endmodule
```

Part 6

```
`timescale 1ns/1ns
module TB_6();
logic [1:0] A, B;
wire g;
function_g cutG(A, B, g);
initial begin
for (int i = 0; i < 4; i++) begin
for (int j = 0; j < 4; j++) begin
A = i[1:0];
B = j[1:0];
#271;
end
end
end
endmodule;
```



Essential


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Project - D:/Modelsim/CA1/CA1
Name Status Type Order Modified
TB_3.sv Syst... 8 03/12/2025 07:36:34
nor_sw.sv Syst... 0 03/12/2025 08:03:18
oai_ba.sv Syst... 2 03/12/2025 07:34:45
nor_tb.sv Syst... 1 03/11/2025 11:11:11
TB_2.sv Syst... 7 03/12/2025 12:12:49
oai_norgate.sv Syst... 3 03/12/2025 12:06:05
TB_4.sv Syst... 9 03/12/2025 07:55:06
oai_sw.sv Syst... 4 03/11/2025 11:37:13
TB_6.sv Syst... 11 03/12/2025 10:19:31
function_g.sv Syst... 10 03/12/2025 10:40:28
TB_1.sv Syst... 6 03/12/2025 08:54:20
oai_tb.sv Syst... 5 03/11/2025 11:57:21
D:/Modelsim/CA1/TB_6.sv (/TB_6) - Default
`timescale 1ns/1ns
module TB_6();
logic [1:0] A, B;
wire g;
function_g cutG(A, B, g);
initial begin
for (int i = 0; i < 4; i++) begin
for (int j = 0; j < 4; j++) begin
A = i[1:0];
B = j[1:0];
#271;
end
end
end
endmodule;
TB_2.sv TB_3.sv TB_4.sv function_g.sv TB_6.sv oai_norgate.sv TB_1.sv
Transcript
Compile of TB_2.sv was successful.
Compile of TB_3.sv was successful.
Compile of TB_4.sv was successful.
Compile of function_g.sv failed with 1 errors.
Compile of TB_6.sv was successful with warnings.
12 compiles, 1 failed with 1 error.
Ln: 16 Col: 0
Project : CA1
<No Design Loaded>
<No Context>