SystemC Exam WS 18/19

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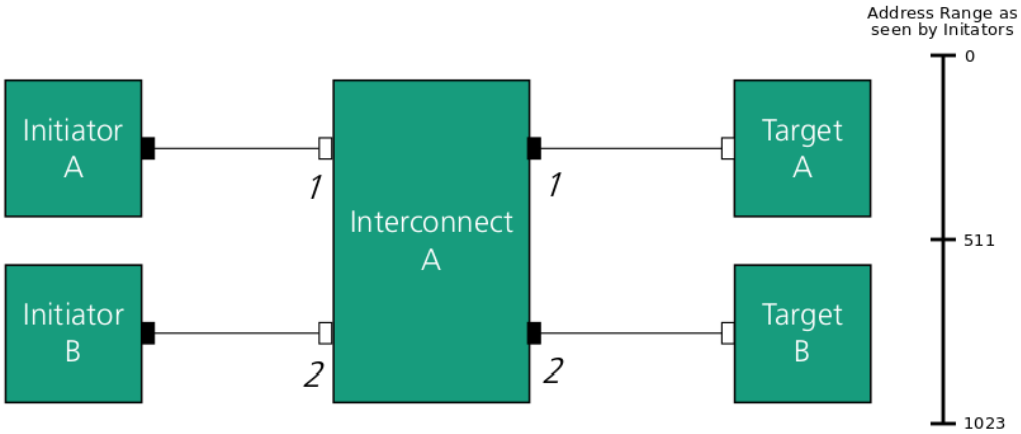
Grade: Both 1.0

1. Introduction/Virtual Prototypes
   - Advantages of Virtual Prototypes
   - Explain Shift Left
   - Accuracy vs. Speed Tradeoff
2. System Models
   - What are system models?
   - Describe advantages/disadvantages of system models.
   - What are disadvantages of FSMs?
   - Which other system models where covered in the lecture? (Petri Nets, KPN, DEM)
   - KPN
     - Draw a simple KPN
     - Explain nodes (= processes) and arcs (= infinite FIFOs)
     - How do we write into (non-blocking) and read from FIFO (blocking)?
     - What is the advantage of KPN? (determinism)
   - Petri Nets
     - Explain Petri Net by drawing a simple example
     - How often can it fire?
     - How do Inhibitor Arcs work?
3. SystemC Basics
   - SystemC Kernel
     - Given: Drawing of RS Latch
     - Write down equations
     - How to model this in simulator? (in a process)
     - Explain behaviour according to inputs w.r.t. SystemC Kernel
     - Explain Feedback Loops
   - Difference between wallclock time and simulation time
4. SystemC Advanced
   - Primitive Channels
     - Name request_update(), update() and default_event()
     - Which functions have to be implemented and which only called?
     - Where is request_update() called e.g. for sc_fifo or sc_signal? (Custom signal example in slides)
5. TLM LT
   - What is the basic idea of TLM?
   - Does LT implement blocking or non-blocking transport?
   - What do we use as transaction object? (Generic Payload)
   - Is it used with call-by-value or call-by-reference?
   - How can we further speedup simulation? (Temporal Decoupling)
   - Explain Temporal Decoupling in one sentence?
   - Do context switches consume wallclock or simulation time?
   - Is the quantum (e.g. 1 us) wallclock or simulation time?
6. TLM AT
   - Draw the 4 Phase Handshake and explain the phases

- How can we model backpressure? What is the basis in the protocol for this? (Exclusion Rule)
- What is the GP Pool and why do we implement it?
- Explain acquire/release mechanism

7. TLM Advanced
   - Given:



   - How can a transaction get to the desired target when initiator sees the drawn address range? (Modification od address/Routing by Interconnect)
   - How does the Interconnect do this? (Substract 512 from address when it is larger than 511 and choose socket 2)
   - In which protocol phase is the modification done? (BEGIN_REQ)
   - How can the response for a specific transaction be routed to the correct initiator? (Interconnect could maintain routing table)
   - How can the routing table be implemented? (As a map)
   - Another possibility to route the response? (Use private payload extension for interconnect)
8. gem5
   - Draw and explain 2 Phase protocol
   - Explain Backpressure
   - Sampling (Paper recommendation: "*Full Speed Ahead: Detailed Architectural Simulation at Near Native Speed*")
     - What is sampling?
     - How do we get to the points of interest/sample points? (Fast Forwarding)
     - How do we warm caches before sampling? (Functional Mode)
   - Elastic Traces (Paper recommendation: "*Exploring System Performance using Elastic Traces: Fast, Accurate and Portable*")
     - Advantage of traces in general
     - How much faster is it compared to simulation? (6-8 times)
     - What is the disadvantage of fixed traces? (No adaption to other memory systems possible → low accuracy)
     - Explain Elastic Traces
     - What is a "Trace" actually now? (Dependency Graph)