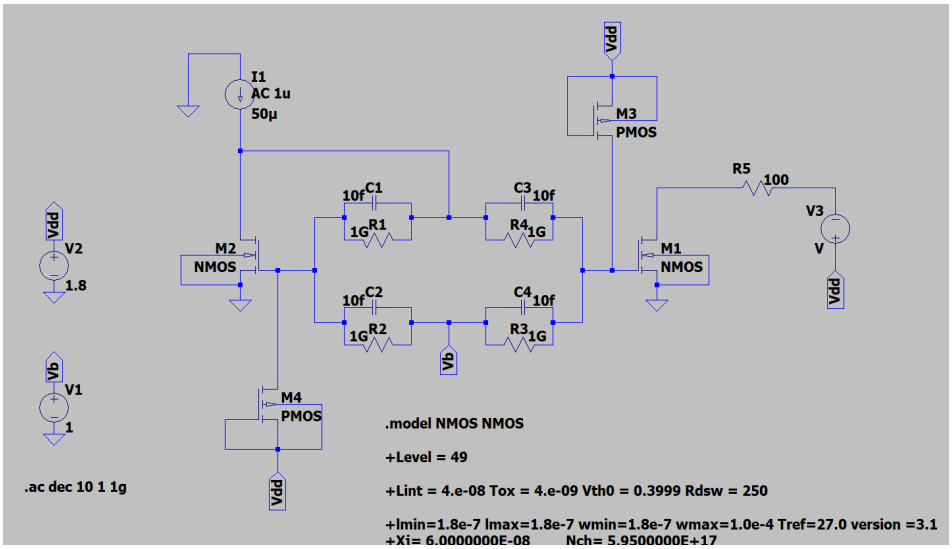
Schematic:



Script:

.include 180.txt

.model NMOS NMOS
.model PMOS PMOS

M1 2 5 0 0 NMOS l=1u w=2u
M2 1 4 0 0 NMOS l=1u w=2u
M3 Vdd Vdd 5 Vdd PMOS l=1u w=24u
M4 4 Vdd Vdd Vdd PMOS l=1u w=24u

C1 4 1 10f
C2 4 Vb 10f
R1 4 1 1G
R2 4 Vb 1G
C3 5 1 10f
C4 5 Vb 10f
R4 5 1 1G
R3 5 Vb 1G

R5 3 2 100

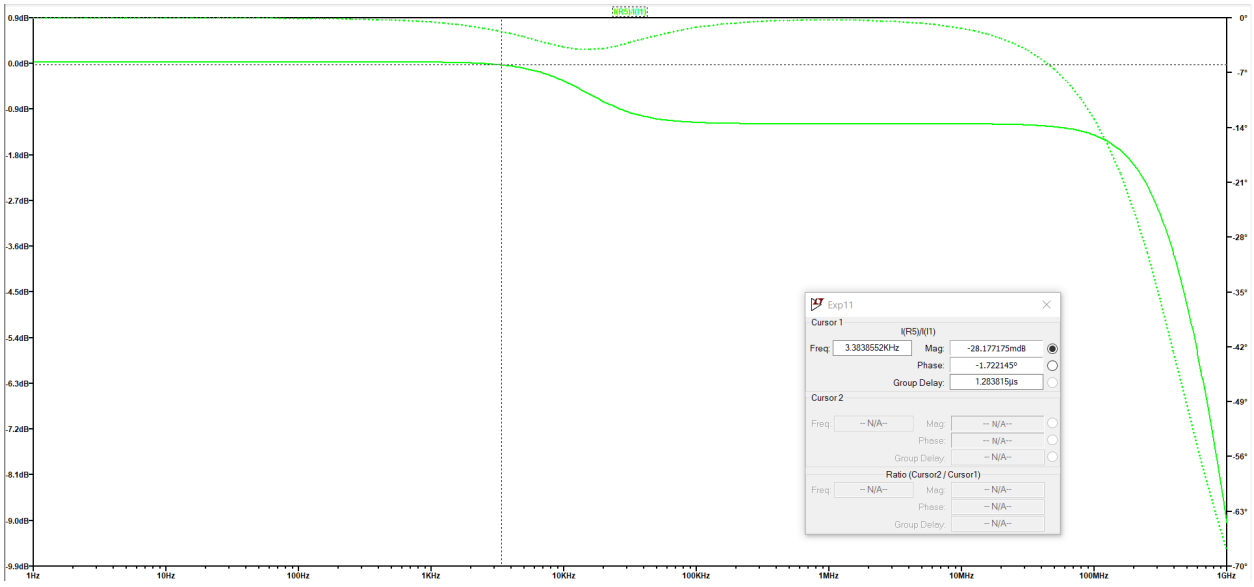
V1 Vb 0 1
V2 Vdd 0 1.8
V3 Vdd 3 V
*V3 Vdd 3 1.8 AC 1u

I1 0 1 50µ AC 1u

.ac dec 10 1 1g
.probe
.end

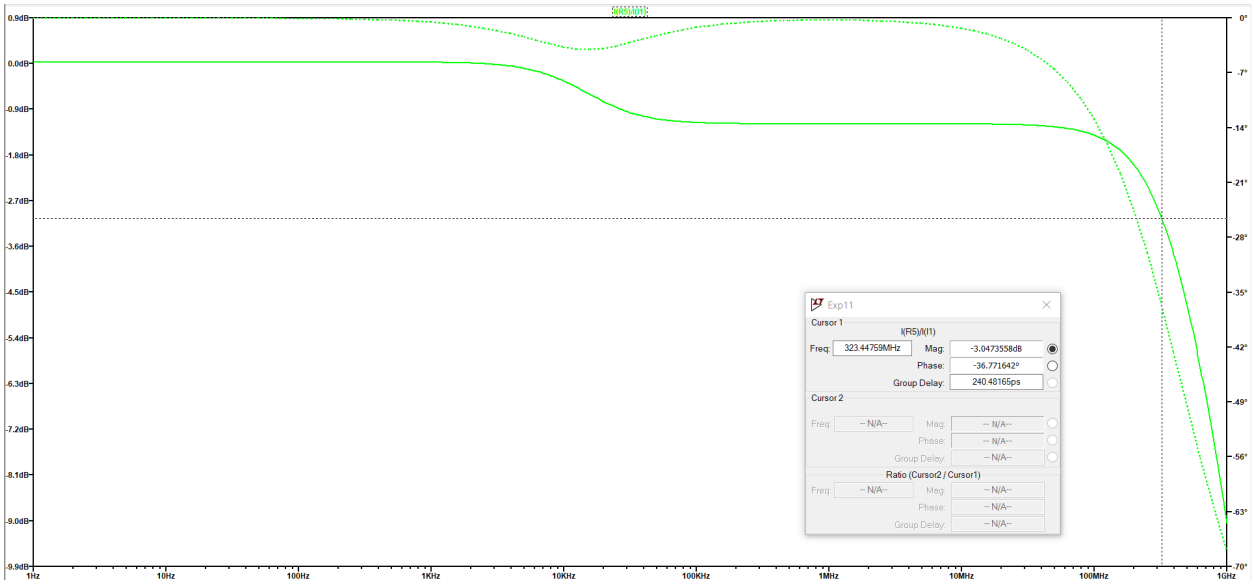
Outputs:

a) Gain (db)



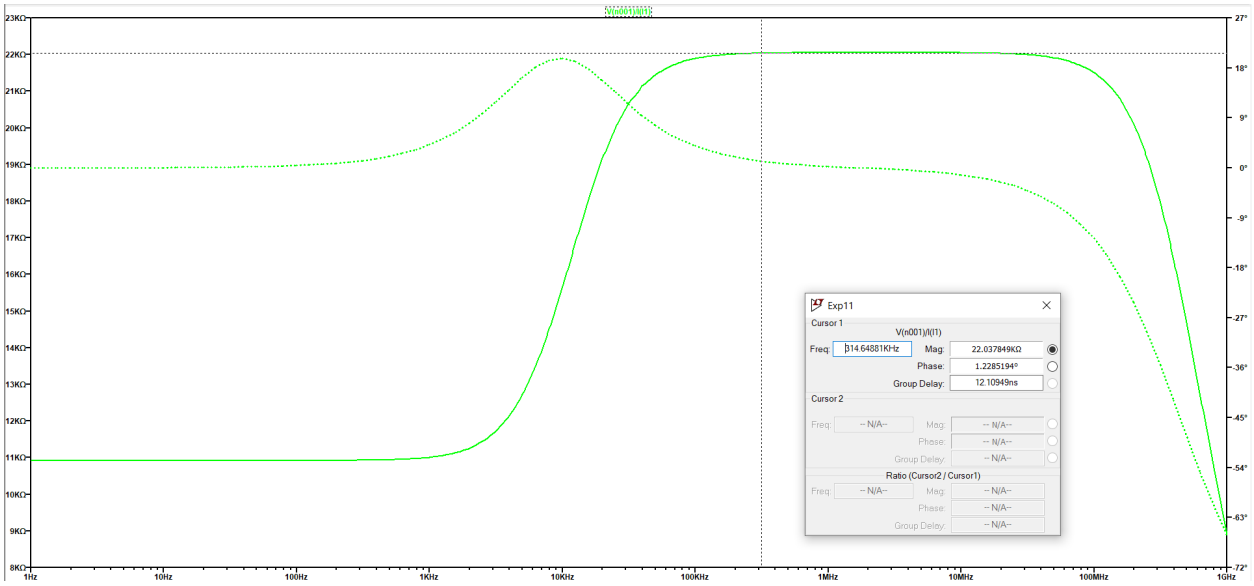
$\approx 0db$

b) Bandwidth



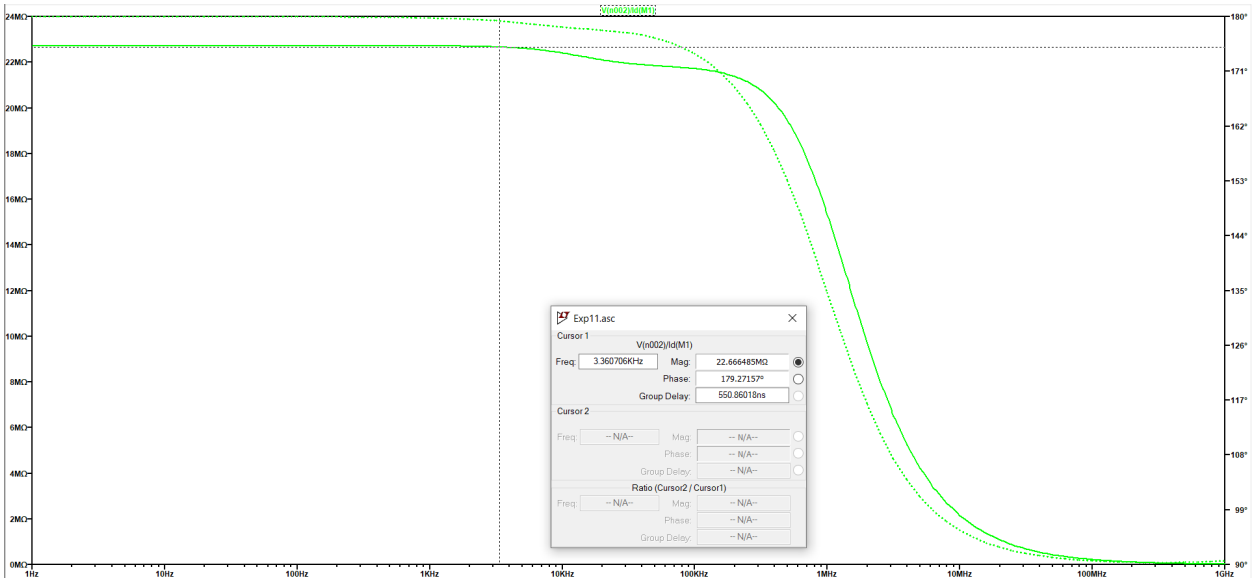
$\approx 323MHz$

c) Input impedance



$\approx 22k\Omega$

d) Output impedance



$\approx 23M\Omega$