DEEKSHA CHANDRAHASA NAIK

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Professional Summary

A motivated and detail-oriented engineering graduate with a strong foundation in VLSI and CMOS design. Skilled in RTL coding and digital logic implementation, with hands-on experience in tools such as NGSpice and Vivado. Committed to continuous learning and delivering efficient, reliable hardware solutions through thoughtful design and verification practices.

Skills

HDLs : Verilog
HVL : System Verilog (Basics)
EDA Tool : Xilinx Vivado, Cadence
Circuit Simulation: NGSPICE, PSpice
IDEs : Arduino IDE,Wokwi

Education

Education	College	Year of Passing	Percentage
Bachelors of Engineering in ECE	Govt. SKSJTI	2025	8.88 CGPA
PUC	Govt. PU College, Allanki	2021	88.3%
X	Sri Sharadamba High School, Magod	2019	88.3%

Internship Experience

1. Internship Title: VLSI
   Duration : January 2025 - Present
   Company: M/S Eduguidance Consultancy Private Limited
2. Internship Title: Digital Electronics
   Duration : October 2023 – December 2023
   Company: Yuvasaarathi

Project Details

VLSI Projects:

Project 1: Skitter based uncertainty detection
EDA Tools: Xilinx Vivado
SPICE Tool: NGSPICE
Description: Constructed a Skitter circuit using NGSpice and Vivado to monitor clock period variations under voltage fluctuations (0.8V–1.3V), by simulating buffer delays, inserting delay-compensated flip-flops, using XOR gates for transition detection and generating histogram-based analysis for jitter characterization and dynamic power optimization.

Project 2: Efficient MSFF Circuit Design
SPICE Tool: NGSPICE
Description: Implemented and simulated a transmission gate MSFF with keeper logic in NGSpice, measured rise/fall delays under width variations, and used Energy Delay Product (EDP) analysis to select the worst-case flip-flop; additionally calculated power for varying activity factors to assess dynamic performance and efficiency.

Project 3: Sense Amplifier Flip-Flop
SPICE Tool: NGSPICE
Description: Designed and compared Sense Amplifier Flip-Flop (SAFF) and Master-Slave Flip-Flop (MSFF) using NGSpice by analyzing power, delay and area, evaluated energy vs delay trade-offs and performed activity factor–based analysis to determine efficiency across power switching conditions.

Project 4: Hybrid Latch Flip-Flop
SPICE Tool: NGSPICE
Description: Developed a Hybrid Latch Flip-Flop (HLFF) using NGSpice and compared with MSFF interms of energy, delay and power efficiency across varying activity factors to determine suitability for low-power and high-performance digital designs.

Project 5: Frequency-Driven Cache Management with Dynamic Migration for Data Prioritization and Power-Conscious Architecture
SPICE Tool: NGSPICE
Description: Built an 8-block hybrid cache system with LRU-LFU policies, data migration, and integrated low-power techniques like clock gating and inactivity-based power management for enhanced performance and energy efficiency.

Work Experience

Fresher | Open to full-time opportunities in the VLSI domain.

Hobbies

- Sports
- Listening to music
- Cooking

Languages Known

- English
- Kannada
- Konkani

Accomplishments

- Secured 2nd Runner-Up position in a hackathon conducted by Siemens for the project titled “Efficient Waste Management System”.
- First Runner-up in *Aikiya*, an inter-college technical fest