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		PAGE: 11 pages

DEVICE SPECIFICATION FOR

TFT-EPD Open-Cell

MODEL No.

LP285A6NW01

These parts are complied with the RoHS directive.

*If you have any problems to this specification, please let us know before placing an order.

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RECORDS OF REVISION

Model No.: LP285A6NW01

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	MARKS
LD-2025202A	21-Feb-25	-	-	-	

1. Application

This specification applies to the following TFT-EPD Open-Cell. Each driving characteristic is defined in combination with the following C-PWB (Control-PWB) which is sold separately by SDTC or equivalent.

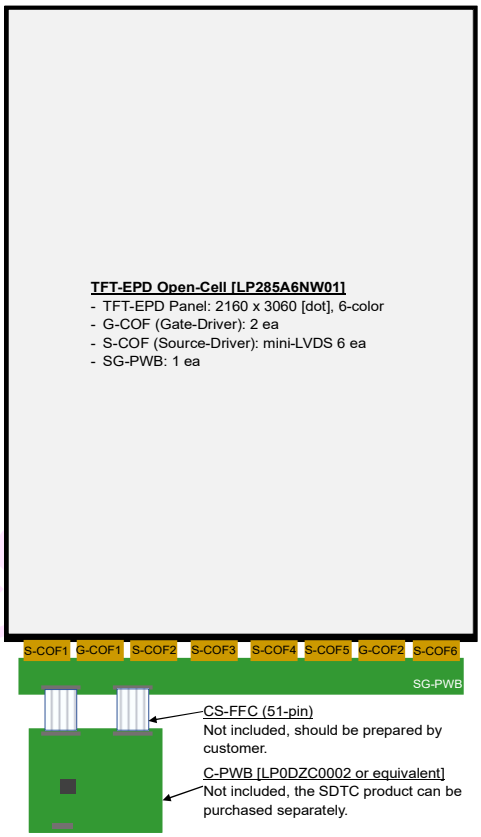
Model No.	SDTC Product No.	Mating C-PWB		Remarks
		Model No.	SDTC Product No.	
LP285A6NW01	A1LP285A6NW01	LP0DZC0002	A1LP0DZC0002	

In case of using the device for applications such as control and safety equipment for transportation, aircraft, trains, automobiles, etc., rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment, and medical or other equipment for life support.

SC and SDTC assumes no responsibility for any damage resulting from the use of the device that does not comply with the instructions and the precautions specified in this specification.

Contact and consult with a SDTC sales representative for any questions about this product.



2. Overview

This TFT-EPD Open-Cell has the following features.

- A2 Size and High Resolution (2160 x 3060) reflective EPD (Electrophoretic Display)
- 6 colors (White/Red/Green/Blue/Yellow/Black) displayable E Ink Spectra 6® FPL (Front Panel Laminate)
- Driving Circuit (SG-PWB/Gate-Drivers/mini-LVDS Source-Drivers) compatible with Tcon-IC(T2000) designated by E Ink.

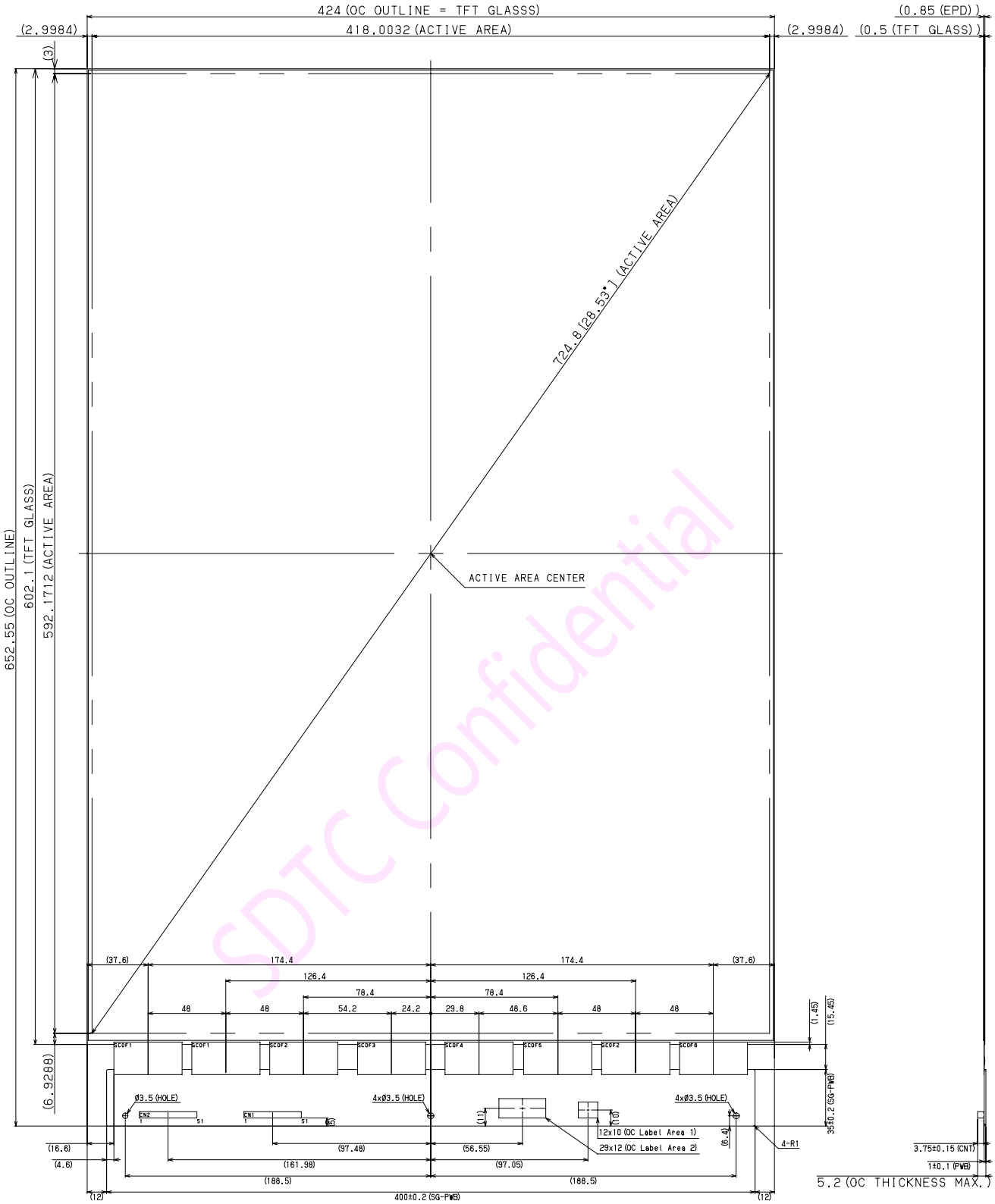
3. Mechanical Specifications

3.1. Main Specifications

Items	Specifications	Units
Display size	418.0032 (H) x 592.1712 (V) (Aspect Ratio = 1:1.42)	mm
(Active Area)	72 [28.5”] (Diagonal)	cm
Pixel format	2160 (H) x 3060 (V)	pixel
Pixel pitch	0.1935 (H) x 0.1935 (V)	mm
Pixel configuration	Rectangle	-
Display mode	Reflective Mode	-
Outline dimensions [1)]	424.00 (H) x 652.55 (V) x 5.2 (D Max.)	mm
Weight	0.5	kg
Surface treatment [2)]	Anti-Glare	-

1) Outline dimensions are shown the drawing in section 3.2. The thickest point is 51-pin-CNT of SG-PWB.
2) With the protection film of FPL removed.

3.2. Outline Dimensions



[Unit: mm]

4. Driving Specifications

4.1. Interface Specifications

CN1 of SG-PWB

- Using connector: 187059-51221 [P-TWO] or compatible
- Mating connector: 187104-51001-3 [P-TWO] or compatible

Pin No.	Pin Names	Functions	Remarks
1	MODE	Gate driver output control	2)
2	XON	No Connection	
3	STBYB	mini-LVDS enable	1)
4	NC	No Connection	
5	NC	No Connection	
6	NC	No Connection	
7	NC	No Connection	
8	VGL	Gate Driver Negative Power	
9	VGL	Gate Driver Negative Power	
10	NC	No Connection	
11	VN3	Source Driver Negative Power	
12	VN3	Source Driver Negative Power	
13	VN3	Source Driver Negative Power	
14	NC	No Connection	
15	VN2	Source Driver Negative Power	
16	VN2	Source Driver Negative Power	
17	VN2	Source Driver Negative Power	
18	NC	No Connection	
19	VN1	Source Driver Negative Power	
20	VN1	Source Driver Negative Power	
21	VN1	Source Driver Negative Power	
22	NC	No Connection	
23	GND	Ground	
24	GND	Ground	
25	NC	No Connection	
26	VDD	Logic Power	
27	VDD	Logic Power	
28	NC	No Connection	
29	VP1	Source Driver Positive Power	
30	VP1	Source Driver Positive Power	
31	VP1	Source Driver Positive Power	
32	NC	No Connection	
33	VP2	Source Driver Positive Power	
34	VP2	Source Driver Positive Power	
35	VP2	Source Driver Positive Power	
36	NC	No Connection	
37	VP3	Source Driver Positive Power	
38	VP3	Source Driver Positive Power	
39	VP3	Source Driver Positive Power	
40	NC	No Connection	
41	VGH	Gate Driver Positive Power	
42	VGH	Gate Driver Positive Power	
43	NC	No Connection	
44	NC	No Connection	
45	NC	No Connection	
46	VCOM	Common Voltage	6)
47	VCOM	Common Voltage	6)
48	NC	No Connection	
49	VCOM	Common Voltage	6)
50	VCOM	Common Voltage	6)
51	VCOM	Common Voltage	6)

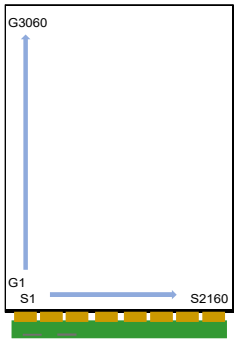
CN2 of SG-PWB

- Using connector: 187059-51221 [P-TWO] or compatible
- Mating connector: 187104-51001-3 [P-TWO] or compatible

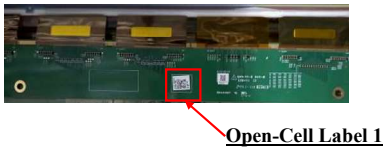
Pin No.	Pin Names	Functions	Remarks
1	DSEL	Source driver data input select	3)
2	LEH	Source driver latch enable	
3	OEH	Source driver output enable	4)
4	UD	Gate driver scan direction control	5)
5	SHR	Source driver scan direction control	5)
6	SPV2	Gate driver start pulse	5)
7	SPV1	Gate driver start pulse	5)
8	SPH2	Source driver start pulse	5)
9	SPH1	Source driver start pulse	5)
10	GND	Ground	
11	CKV	Gate clock	
12	GND	Ground	
13	LV11N	mini-LVDS data signal	6)
14	LV11P	mini-LVDS data signal	6)
15	GND	Ground	
16	LV10N	mini-LVDS data signal	6)
17	LV10P	mini-LVDS data signal	6)
18	GND	Ground	
19	LV9N	mini-LVDS data signal	6)
20	LV9P	mini-LVDS data signal	6)
21	GND	Ground	
22	LV8N	mini-LVDS data signal	6)
23	LV8P	mini-LVDS data signal	6)
24	GND	Ground	
25	LV7N	mini-LVDS data signal	6)
26	LV7P	mini-LVDS data signal	6)
27	GND	Ground	
28	LV6N	mini-LVDS data signal	6)
29	LV6P	mini-LVDS data signal	6)
30	GND	Ground	
31	CLKN	mini-LVDS data clock	6)
32	CLKP	mini-LVDS data clock	6)
33	GND	Ground	
34	LV5N	mini-LVDS data signal	6)
35	LV5P	mini-LVDS data signal	6)
36	GND	Ground	
37	LV4N	mini-LVDS data signal	6)
38	LV4P	mini-LVDS data signal	6)
39	GND	Ground	
40	LV3N	mini-LVDS data signal	6)
41	LV3P	mini-LVDS data signal	6)
42	GND	Ground	
43	LV2N	mini-LVDS data signal	6)
44	LV2P	mini-LVDS data signal	6)
45	GND	Ground	
46	LV1N	mini-LVDS data signal	6)
47	LV1P	mini-LVDS data signal	6)
48	GND	Ground	
49	LV0N	mini-LVDS data signal	6)
50	LV0P	mini-LVDS data signal	6)
51	GND	Ground	

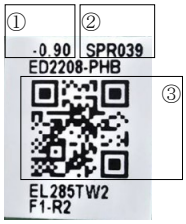
1) STBYB = L: mini-LVDS standby.
2) MODE = H: Normal Single Pulse / MODE = L: No Output Pulse
3) DSEL = H: 12-pair mini-LVDS (with TTL_SEL = L)
4) OEH = H: Source outputs are enabled / OEH = L: Source outputs forced to GND when output polarity change. (Default)
5) Set the scan direction as follows.

Scan Direction	UD	SPV1	SPV2	SHR	SPH1	SPH2	Remarks
S1 to S2160 G1 to G3060	H	Input	Output	L	Input	Output	Setting of LQ0DZC0002



6) The Common Voltage (VCOM) and Wave Form (WF) for optimal image control for each individual TFT-EPD Open-Cell must be written into the ROM of the C-PWB by the customer. Each information is shown on the Open-Cell Label 1 as follows.





① Vcom Value: e.g., -0.9 V
② FPL Lot No.: e.g., SPR039
③ QR Code: e.g., HC3R2**SPR039**GZ9V00005AT-**0.9**
① ②

Parameters	Contents	References
VCOM	Write the value listed on the Open-Cell Label 1. e.g., -0.9 V	① of Open-Cell Label 1
WF	Select and write a file in which the FPL Lot No. on the Open-Cell Label 1 matches the digits that indicates it in the file name of the WF file (.wbf) provided separately. e.g., E6 _ **SPR039** _ L10228_EL285TW2F1-R2_ED2208PHB_TC .wbf 1 **2** 1 3 1: Manufacturer Management Digit **2: FPL Lot No.** 3: File extension	② of Open-Cell Label 1

4.2. Absolute Maximum Ratings

(GND = 0 V)

Items	Symbols	Conditions	Ratings	Units	Remarks
Logic power	VDD	Ta = 25ºC	-0.3 to 5	V	
Source driver positive power	VP3	Ta = 25ºC	-0.3 to VN3+50	V	
	VP2		-0.3 to VP3	V	
	VP1		-0.3 to VP3	V	
Source driver negative power	VN1	Ta = 25ºC	VN3 to 0.3	V	
	VN2		VN3 to 0.3	V	
	VN3		-25 to 0.3	V	
Gate driver positive power	VGH	Ta = 25ºC	-0.3 to 55	V	
Gate driver negative power	VGL	Ta = 25ºC	-32 to 0.3	V	
Gate driver peak to peak	VG_{pp}	Ta = 25ºC	-0.3 to 3.0	V	VGH-VGL
Storage temperature	Tstg	-	-25 to +60	ºC	
Operation temperature	Topa	-	0 to +50	ºC	

- Humidity: 95% RH Max. (Ta ≦ 40ºC)
- Maximum wet-bulb temperature at 39ºC or less. (Ta > 40ºC), No condensation.
- The surface temperature of the display should be kept below 50ºC and uniform. Otherwise, display performance may be affected.

4.3. Electrical Characteristics of Input Signals

GND = 0 V

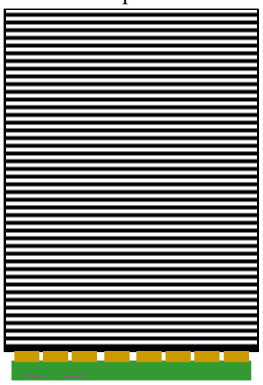
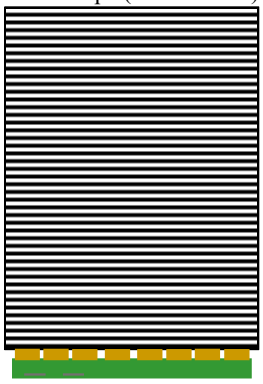
Items		Symbols	Min.	Typ.	Max. [4]		Units	Remarks
					1	2		
Supply voltages	Logic	VDD	2.7	3.3	3.6		V	
	Gate	VGH	26	27	28		V	
		VGL	-21	-20	-5		V	
	Source	VN1	-14	Adjusted	-5		V	
		VN2	-14	Adjusted	-5		V	
		VN3	-16	-15	-14		V	
		VP1	5	Adjusted	14		V	
		VP2	5	Adjusted	14		V	
		VP3	14	15	16		V	
	Common [1]	VCOM	-3.5	Adjusted	-0.3		V	
Current consumption [2]	Logic	IDD	-	22	23		mA	VDD = 3.3 V
	Gate	IGH	-	3	5		mA	VGH = 27 V
		IGL	-	8	19		mA	VGL = -20 V
	Source	IN1	-	7	30		mA	VN1 = -8 V
		IN2	-	7	27		mA	VN2 = -8.6 V
		IN3	-	5	167	407	mA	VN3 = -15 V
		IP1	-	7	9		mA	VP1 = 7.4 V
		IP2	-	3	36	98	mA	VP2 = 6.4 V
		IP3	-	10	196	316	mA	VP3 = 15 V
	Common	ICOM		71	74		V	
Power Consumption [3]	Active	P	-	1229	5344	9079	mW	
	Standby	Pstby	-	-	66		mW	

- These values are only guaranteed under the Tcon-IC and WF (Wave Form) provided by E Ink.

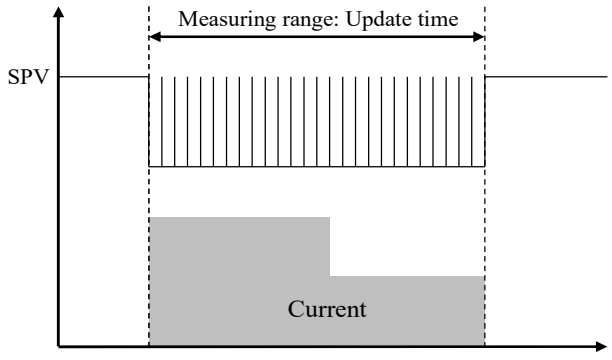
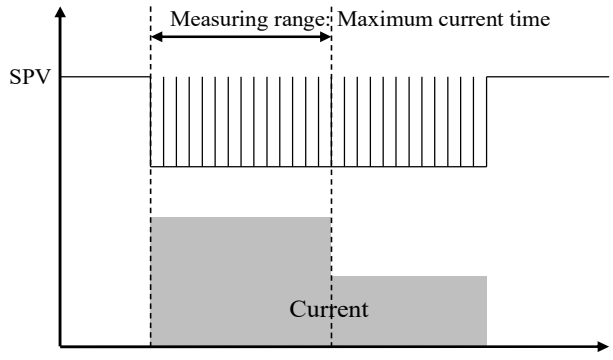
1) VCOM is recommended to be set within ±0.1 V of the optimum value for the FPL characteristics.

2) The maximum current consumption is for reference only.

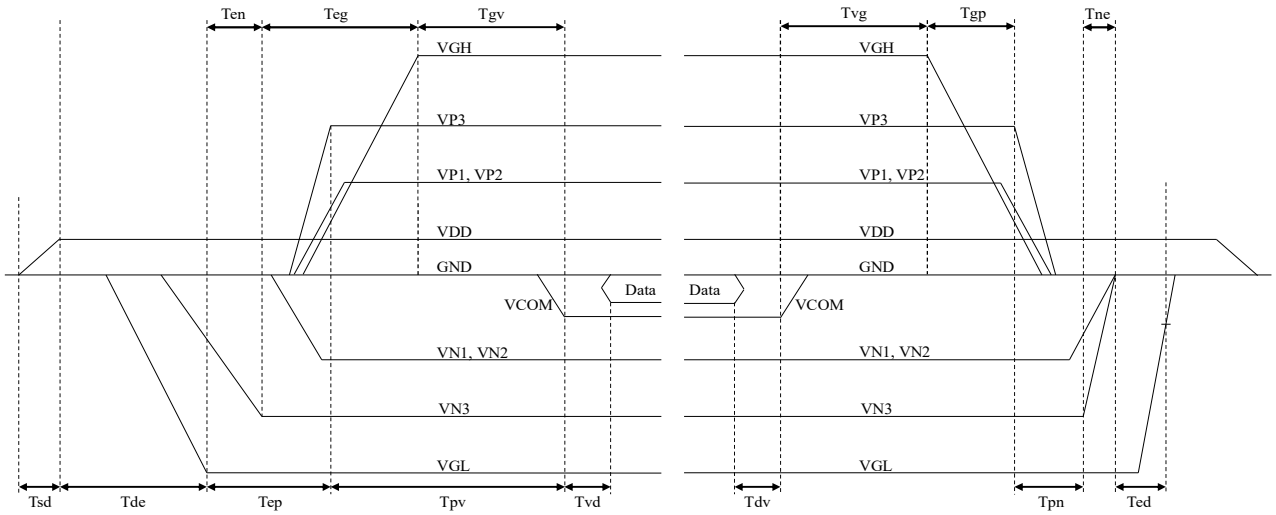
3) The typical average current for power consumption is defined in the following screen patten transitions at 50 Hz waveform.

Typ.		Max.	
6-color Horizontal Stripe	6-clocor Vertical Stripe	2H Line Stripe	2H Line Stripe (2H line shift)
			

4) The measurement range of current consumption defined by the following diagrams.

Max. 1: for Device Battery-Life Estimation Only	Max. 2
	

4.4. Power Sequences



ON	Min.	Max.	Units	Remarks
Tsd	30	-	µs	
Tde	100	-	µs	
Tep	1000	-	µs	
Tpv	10	-	µs	
Tvd	10	-	µs	
Ten	0	-	µs	
Tng	1000	-	µs	

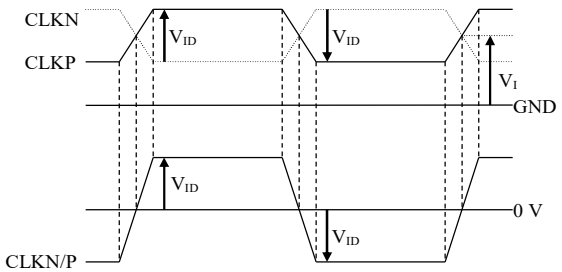
OFF	Min.	Max.	Units	Remarks
Tdv	100	-	µs	
Tvg	0	-	µs	
Tgp	0	-	µs	
Tpn	0	-	µs	
Tne	0	-	µs	
Ted	0.5	-	s	1)

1) Discharged point: -7.4 V

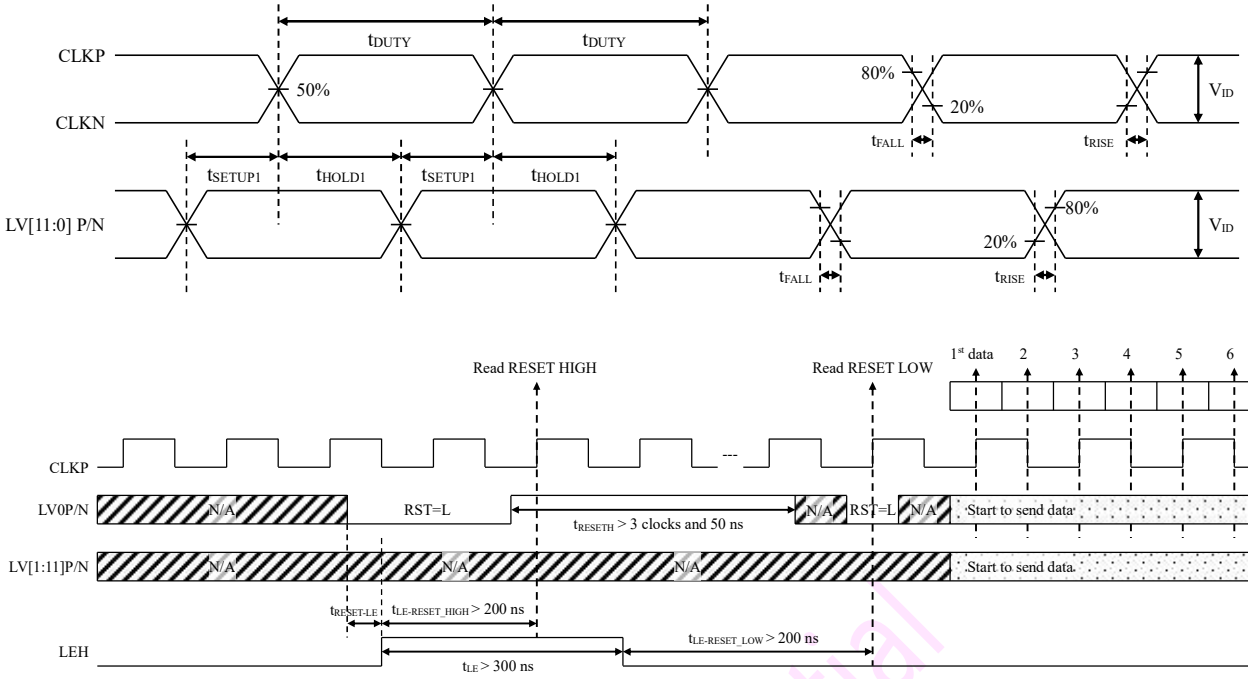
4.5. Timing Characteristics of Input Signals

Items		Symbols	Min.	Typ.	Max.	Units	Remarks
Refresh Rate		-	0	-	50	Hz	
Source	mini-LVDS differential voltage	V_{ID}	300	-	-	mV	1)
	mini-LVDS common mode input voltage range	V_I	0.4	1.0	VDD-1.4	V	1)
	Clock frequency	F_{CLK}	-	-	150	MHz	2)
	Clock duty	t_{DUTY}	45	-	55	%	2)
	Clock setup time	t_{SETUP1}	1.1	-	-	ns	2)
	Clock hold time	t_{HOLD1}	1.1	-	-	ns	2)
	Rise time	t_{RISE}	-	-	0.15	UI	2)
	Fall time	t_{FALL}	-	-	0.15	UI	2)
	LE rising to reset input time	$t_{LE\text{-}RESET\_HIGH}$	200	-	-	ns	2)
	LE falling to reset input time	$t_{LE\text{-}RESET\_LOW}$	200	-	-	ns	2)
	Reset high period	t_{RESETH}	3	-	-	CLK	2)
	Receiver off to LE timing	$t_{REC\text{-}OFF}$	40	-	-	CLK	3)
	LE width	t_{LE}	300	-	-	ns	2)
Gate	Clock rise time	T_{rck}	-	-	100	ns	
	Clock fall time	T_{fck}	-	-	100	ns	
	Clock pulse width (low)	T_{clkl}	500	-	-	ns	
	Clock pulse width (high)	T_{clkh}	500	-	-	ns	
	Start pulse rise time	T_{rspv}	-	-	100	ns	
	Start pulse fall time	T_{fspv}	-	-	100	ns	
	Start pulse setup to Clock	T_{su}	100	-	Tclkh-100	ns	
	Start pulse hold from Clock	T_h	100	-	Tclkh-100	ns	

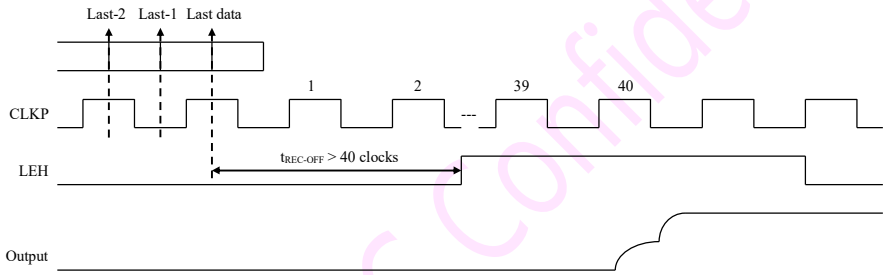
1) mini-LVDS clock



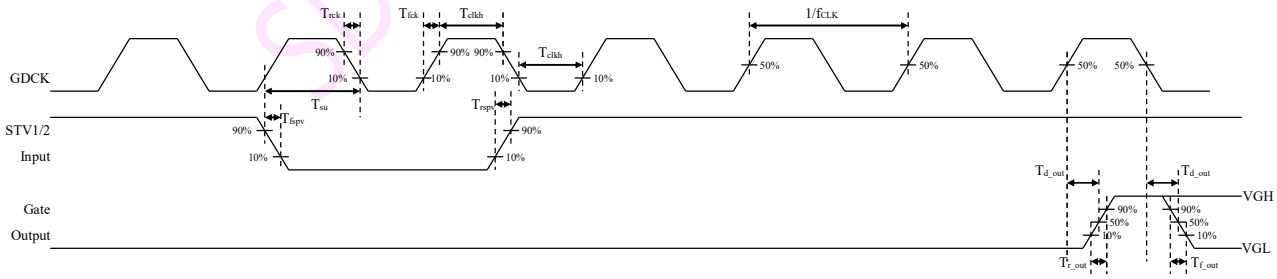
2) mini-LVDS timing for receiving data.



3) mini-LVDS last data sampling to LE timing



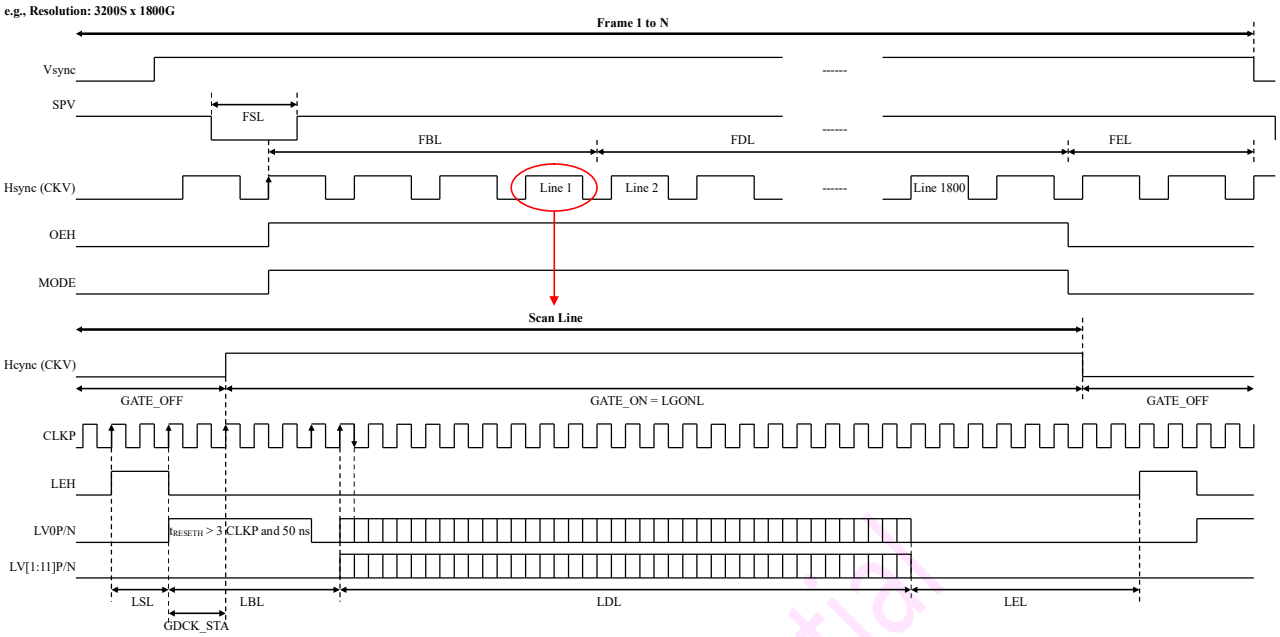
4) Gate Timing Waveform



- First gate line on timing: After 5-CLK, Gate OUT1 is on.

4.6. Controllers Timing

The timing mode is depicted on the following figure, and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.



- For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL.
- SDCK = XCL, LV[0:11]P/N = LV0P to LV11N, SDCE_L = XSTL, GDCL = CKV, GDSP = SPV, GDOE = Mode 1, SDOE = XOE
- Timing Parameters Table (Mode = 3, SDCK = 48 MHz, Pixel Per SDCK = 8, Image Resolution = 4320 x 1530)

Parameters	LSL	LBL	LDL	LEL	GDCK_STA	LGONL	Units
SDCK	19	20	540	40	3	475	clock
Period	0.4	0.42	11.25	0.83	0.06	9.9	µs

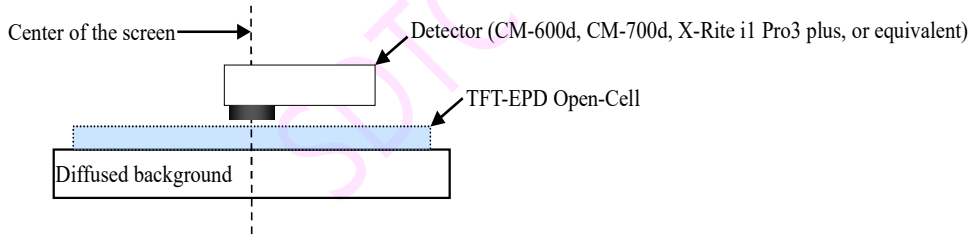
Parameters	FSL	FBL	FDL	FEL	FR	Units
Lines	1	4	1530	5	-	lines
Period	12.9	51.6	19737	64.5	19866 (50 Hz)	µs

5. Optical Characteristics

Ta = 25ºC

Parameters			Symbols	Conditions	Min.	Typ.	Max.	Units	Remarks
Reflectance			R	White	30	34	-	%	
Contrast ratio [1)]			CR	-	15	22	-	-	
Update time			T_{UPTADE}	Image 1 to Image 2	-	15	-	s	
Color space	White	L*	W	-	-	66.5	-	-	
		a*			-	-4	-	-	
		b*			-	0	-	-	
		⊿E2000			-	-	6	-	
	Red	L*	R		-	26.5	-	-	
		a*			-	41	-	-	
		b*			-	30	-	-	
		⊿E2000			-	-	6	-	
	Green	L*	G		-	32	-	-	
		a*			-	-22	-	-	
		b*			-	5	-	-	
		⊿E2000			-	-	8	-	
	Blue	L*	B		-	27	-	-	
		a*			-	6	-	-	
		b*			-	-35	-	-	
		⊿E2000			-	-	6	-	
	Yellow	L*	Y		-	62	-	-	
		a*			-	-11	-	-	
		b*			-	65	-	-	
		⊿E2000			-	-	6	-	
	Black	L*	K		-	12	-	-	
		a*			-	7	-	-	
		b*			-	-11	-	-	
		⊿E2000			-	-	6	-	

- These values are defined only when driven using the SDTC C-PWB[LQ0DZC0002] or equivalent.
- The measurement method and equipment are as follows.



1) The contrast ratio is defined as the following,

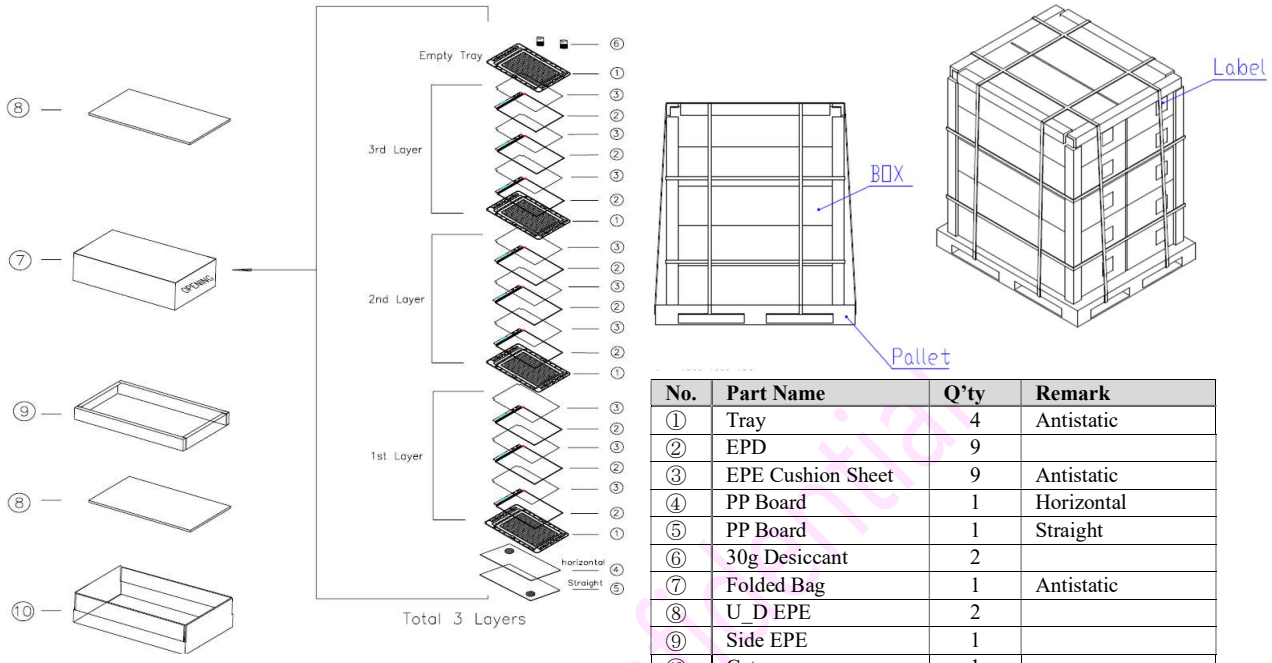
$$CR = \frac{\text{Reflectance when white is displayed on the entire screen}}{\text{Reflectance when black is displayed on the entire screen}}$$

6. Delivery Specifications

6.1. Packing Form

	1-pallet (Max. 10-box)	(1-box)
Size	1200 x 1000 x 1270 [mm]	(980 x 890 x 230 [mm])
Q'ty	90 Open-Cells Max.	(9 Open-Cells = 3 Open-Cells x 3 trays)
Mass	About 140 kg	(About 13 kg)

- Do not guarantee the transportation by a box.



No.	Part Name	Q'ty	Remark
①	Tray	4	Antistatic
②	EPD	9	
③	EPE Cushion Sheet	9	Antistatic
④	PP Board	1	Horizontal
⑤	PP Board	1	Straight
⑥	30g Desiccant	2	
⑦	Folded Bag	1	Antistatic
⑧	U_D EPE	2	
⑨	Side EPE	1	
⑩	Catron	1	

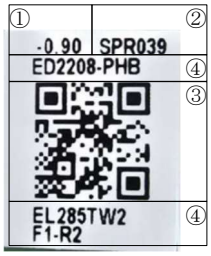
6.2. Labels

Open-Cell Label

The following labels are attached on the SG-PWB.

Open-Cell Label 1

e.g.,



① VCOM Value
② FPL Lot No.
③ QR Code
e.g., HC3R2 SPR039 G Z 9 V00005AT^ -0.9
1 2 1 3 4 1 5
1: E Ink Management Digit
2: FPL Lot No.
3: Production Year (2025=A, 2026=B, …)
4: Production Month (1 to 9, A, B, C)
5: VCOM Value
("^": Space)
④ E Ink Management Area

Open-Cell Label 2

e.g.,

Model No. : LP285A6NW01 ①
S/N : HC3R2GZ9V00005AT ②
③

① Model No. [1] or Blank
② Serial No.: Except 2 and 5 from QR Code of Label 1 or Blank
③ Suffix [1]

Packing Label

The following label is attached on each box.

e.g.,

Model No.: **LP285A6NW01** ①
Production No.: **(4S)LP285A6NW01** ②
Lot No.: **(1T)2025.02.28 A00001** ③
Quantity: **(Q) 9 pcs** ④
⑤

SHARP Logistics Label MADE IN CHINA

① Model No. [1]
② Model No. + Suffix [1]
③ Packing Lot No.
④ Open-Cell Quantity (cell/box)
⑤ SDTC Management Area

③ Packing Lot No.
e.g.,
2025.02.28 _ A 00001
1 2 3 4
1: Printing Date
2: Space
3: SDTC Management Digit
4: Sequence No.

1) Model List

Model No.	Suffix	Finished Plant	Remarks
LP285A6NW01	(Non)	TOC	

7. Reliability

No.	Test Items	Conditions
1	High temperature storage test [1), 2)]	Ta = 60ºC, 35% RH, 240 hours
2	Low temperature storage test [1), 2)]	Ta = -25ºC, 240 hours
3	High temperature and high humidity storage test [1), 2)]	Ta = 60ºC, 80% RH, 240 hours (No condensation)
4	High temperature and high humidity operation test [2), 3)]	Ta = 40ºC, 90% RH, 240 hours (No condensation)
5	High temperature operation test [2), 3)]	Ta = 50ºC, 30% RH, 240 hours
6	Low temperature operation test [2), 3)]	Ta = 0ºC, 240 hours
7	Temperature cycle storage test [1), 2)]	Ta = -25ºC (30 min) ←→ 60ºC (30 min), 50 cycle
8	ESD test	Input: ±250 V, 0-ohm, 200 pF (Machine Model, Non-operation)

- There is no display defect, line defect, no image, etc., in the standard conditions.
- All the cosmetic specification is judged before the reliability stress.

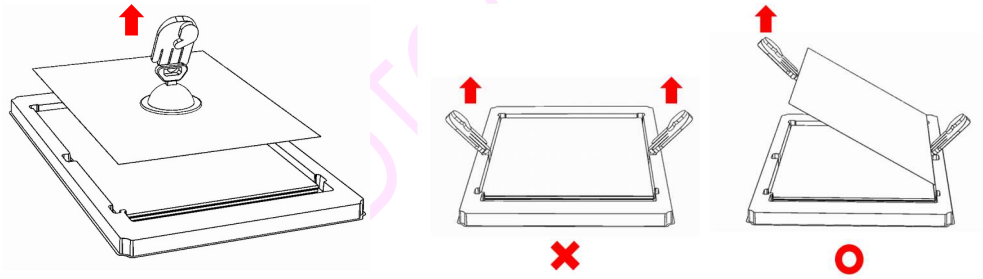
1) Display the White Pattern
2) With the protection film of FPL removed
3) Use the SDTC C-PWB [LP0DZC0002] for operation.

8. Precautions

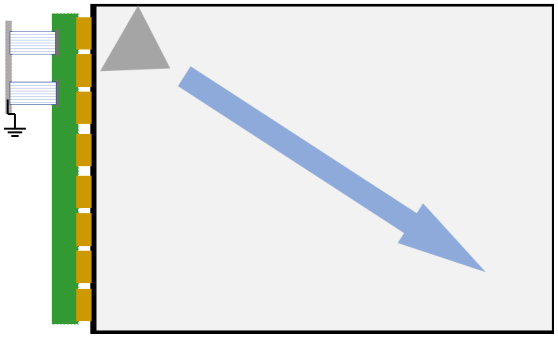
1) Handle the Open-Cell with the extreme care using the grounded anti-static wrist band to protect TFTs and electronic circuits with CMOS-ICs from electrostatic breakdown.
   - Reference: Process control standard of sharp

No.	Items	Management standard value and performance standards
1	Anti-static mat (floor)	1 to 50 [Mohm]
2	Anti-static mat (shelf, desk)	1 to 100 [Mohm]
3	Ionizer	Attenuate from ±1000 V to ±100 V within 2 sec
4	Anti-static wrist band	0.8 to 10 [Mohm]
5	Anti-static wrist band entry and ground resistance	Less than 1000 ohm
6	Temperature	22 to 26 [ºC]
7	Humidity	60 to 70 [%]

2) Use the suction cup tool to remove the Open-Cell from the tray. If the suction cup tool is not used, be sure to lift the panel from one side.



3) After removal the Open-Cell from the tray, store it in a 25ºC environment to prevent warping.
4) This Open-Cell is with the Protection Film on FPL. Take care following notices within the removal of it.



- Be sure to peel off slowly (recommended more than 60 sec) and constant speed.
- Peeling direction shows the left Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground all terminals of the SG-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch the COF and the PWB.
- After the protection film is removed, only cleaning with water or neutral detergent diluted 100 times is possible.

5) Pay attention not to scratch the FPL and the Glass surface.
6) Do not touch with chemical-treated clothes or greasy fingers, etc., as some components may degrade the surface.
7) Dust on the surface of each component should be blown away with an N2 blower such as an ionizing air gun with anti-static measures.
8) Wipe off water drop immediately to prevent discoloration or spots.
9) Wipe the FPL surface with the absorbent cotton or other soft cloth.
10) Do not paste any labels on the FPL surface to prevent from remaining the adhesive material.

11) Handle the Open-Cell with great care so that it is not dropped or bumped on a hard surface to prevent the glass, the main constituent material, from breaking or cracking.
12) Do not press beyond 10 N locally on the display area to prevent permanent Display Mura.
13) Shade the glass surface, including edges, to avoid long-term exposure to external lights to prevent a TFT threshold voltage from shifting due to photoexcitation.
14) Take care to keep the COF and PWB from any stress or pressure when handling or installing the Open-Cell.
15) Design the module not to fix the PWB with screw or tape to prevent the disconnection of an COF by the thermal shock or physical damage.
16) Do not store the Open-Cell in the environment of oxidization or deoxidization gas for a long time and not use such materials as reagent, solvent, adhesive, resin, etc., which generate these gasses when assembling them into cabinets to prevent corrosion and discoloration.
17) Applying too much force and stress to the PWB and the COF may cause a malfunction electrically and mechanically.
18) In case that the COF is needed to bend, note that the radius of bending must be over 0.65 mm in 2 mm outside from the Driver-IC edges.
19) Design the module so that the COF contacts a high thermal conductivity material to radiate heat of the IC, the recommended operating maximum temperature is 75°C at a chip surface.
20) Handle with care based on the general connector's specification when inserting and removing it.
21) Turn off the power supply when inserting or disconnecting the cable.
22) It is recommended that the display surface be protected by a transparent protective plate with sufficient strength against external forces.
23) Consider the design of power protection circuit in case of failure of this Open-Cell according to the customer's operating conditions.
24) EMC should be fully verified with the customer's final product.
25) Periodic screen rewrites are recommended to prevent an image sticking caused by fixed pattern displays over long periods of time.
26) Entire screen should be white for long-term storage. (It is also white when shipped.)
27) The chemical compound, which causes the destruction of ozone layer, is not being used.
28) This Open-Cell is corresponded to RoHS.
29) The ozone-depleting substances is not used.
30) Follow the regulations when the Open-Cell is scrapped.
31) Wash with water and soap in case of contact with electrophoretic material.
32) When parts specifications or materials and production process will be changed, SDTC will submit to written proposal to the customer and change these after customer's acceptance.
33) Refer to the latest Design Notice for other precautions as well.
34) When any question or issue occurs, it shall be solved by mutual discussion.

9. Storage Conditions of the Open Cell in the Box

-	Temperature	0°C to 40°C (Recommend)
-	Humidity	80% RH or less (Recommend)
-	Reference condition	20°C to 35°C, 85% RH or less (Summer) 5°C to 15°C, 85% RH or less (Winter) Total storage time (40°C, 80% RH): 240 hours or less
-	Shade	Be sure to shelter from the direct light.
-	Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
-	Anticondensation	Be sure to put cartons on the airy pallet or base, do not put it on floor, and store them with removing from wall. Take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
-	Vibration	Refrain from keeping the product in the place which always has vibration.
-	Storage life	6 months