Embedded Systems Project Report (A2)

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Topic :

Deriving complete Data flow graphs (DFG) of processor/system modules.

Understanding of the problem :

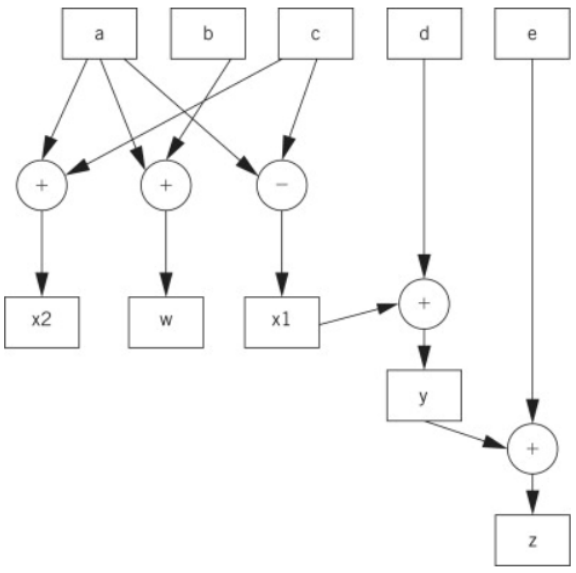
The task is to draw DFG of a Verilog file in a simplified text format. We have used C++ language to do so.

Input format –

Input is in the format of a txt file. Save a Verilog code file in the form of txt file named as input.txt.

Output format –

Due to the restriction of language, we have to represent the graph in form of text. In the output, there will be four columns with certain number of rows. The first two columns in each row represent the two variables on which operation is being done. The third column will represent what operation is being carried on the variables. The fourth column will represent the resulting variable of the operation.



Therefore, the DFG of the above graph in our output representation must be –

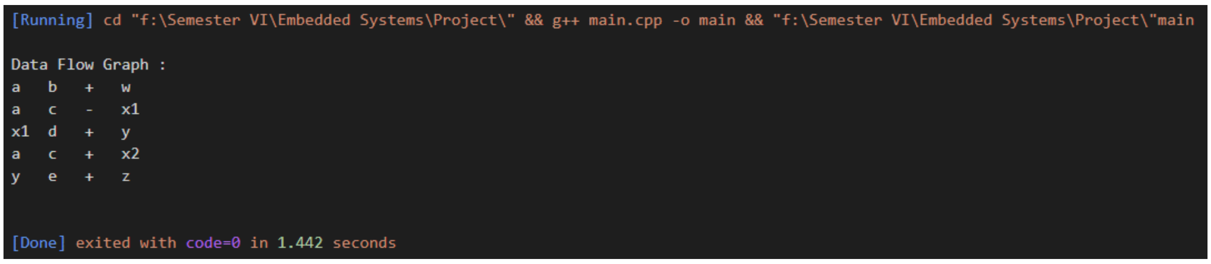
a	b	+	w
a	c	-	x1
x1	d	+	y
a	c	+	x2
y	e	+	z

Preliminary Code Implementation :

For preliminary testing of the code, we took the input as given in https://www.sciencedirect.com/topics/engineering/data-flow-graph Fig. 5.4 which is attached below.

$$w = a + b;$$
$$x = a - c;$$
$$y = x + d;$$
$$x = a + c;$$
$$z = y + e;$$

The DFG of this input is expected to be as shown in our output format. The output of our code for this input is shown below.



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[Running] cd "f:\Semester VI\Embedded Systems\Project\" && g++ main.cpp -o main && "f:\Semester VI\Embedded Systems\Project\"main

Data Flow Graph :
a   b   +   w
a   c   -   x1
x1  d   +   y
a   c   +   x2
y   e   +   z


[Done] exited with code=0 in 1.442 seconds
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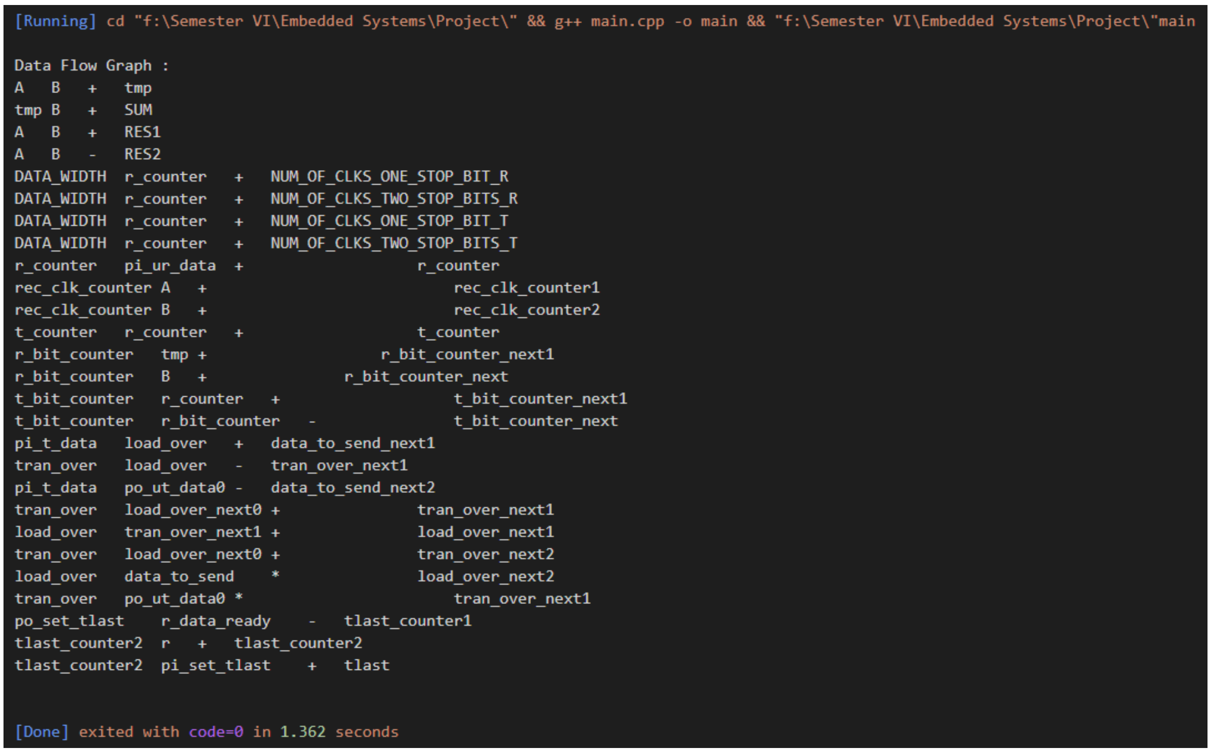
As it can be seen clearly, our code is re-written in single-assignment form in which a variable appears only once on the left side of equation (fourth column in our DFG) and then the DFG is drawn. Here, the two x's in the input equations are renamed as x1 and x2. The DFG in output matches our expected result. Therefore, our code has passed the preliminary test.

Detailed Evaluation :

Now, we evaluated the performance of our code on larger files. First, we tried to draw a DFG of a Verilog file of 550 lines. The input file is attached in the zip as “input1.txt”. We got the following output :



```
[Running] cd "f:\Semester VI\Embedded Systems\Project\" && g++ main.cpp -o main && "f:\Semester VI\Embedded Systems\Project\"main

Data Flow Graph :
A   B   +   tmp
tmp B   +   SUM
A   B   +   RES1
A   B   -   RES2
DATA_WIDTH  r_counter   +   NUM_OF_CLKS_ONE_STOP_BIT_R
DATA_WIDTH  r_counter   +   NUM_OF_CLKS_TWO_STOP_BITS_R
DATA_WIDTH  r_counter   +   NUM_OF_CLKS_ONE_STOP_BIT_T
DATA_WIDTH  r_counter   +   NUM_OF_CLKS_TWO_STOP_BITS_T
r_counter   pi_ur_data  +                   r_counter
rec_clk_counter A   +                           rec_clk_counter1
rec_clk_counter B   +                           rec_clk_counter2
t_counter   r_counter   +                   t_counter
r_bit_counter   tmp +                   r_bit_counter_next1
r_bit_counter   B   +               r_bit_counter_next
t_bit_counter   r_counter   +                   t_bit_counter_next1
t_bit_counter   r_bit_counter   -               t_bit_counter_next
pi_t_data   load_over   +   data_to_send_next1
tran_over   load_over   -   tran_over_next1
pi_t_data   po_ut_data0 -   data_to_send_next2
tran_over   load_over_next0 +               tran_over_next1
load_over   tran_over_next1 +               load_over_next1
tran_over   load_over_next0 +               tran_over_next2
load_over   data_to_send    *               load_over_next2
tran_over   po_ut_data0 *                       tran_over_next1
po_set_tlast    r_data_ready    -   tlast_counter1
tlast_counter2  r   +   tlast_counter2
tlast_counter2  pi_set_tlast    +   tlast


[Done] exited with code=0 in 1.362 seconds
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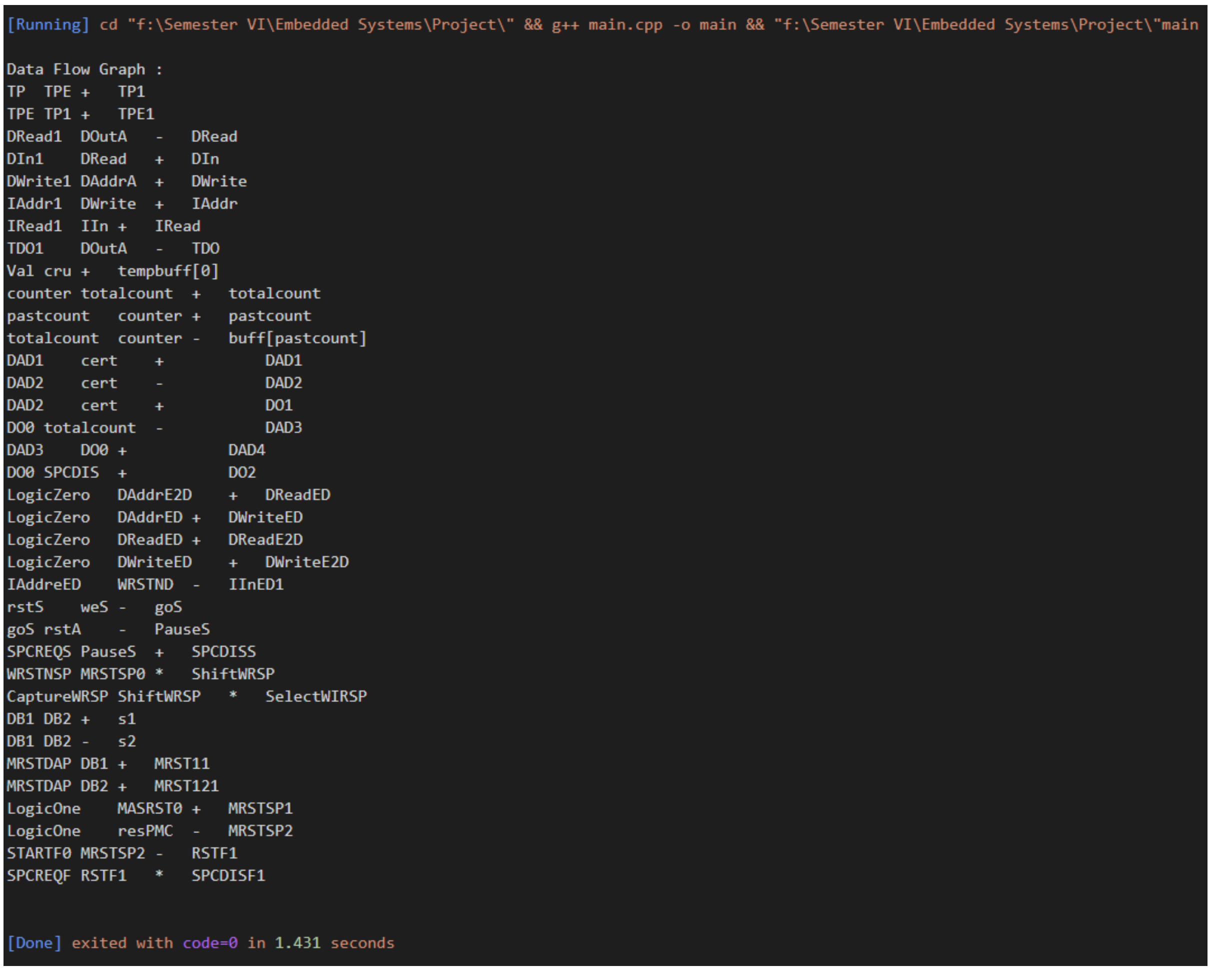
On matching this output manually with the code, we got our results matched. The conversion to single-assignment form and the resulting DFG are both accurate. Therefore, our code performs good for Verilog files of over 500 lines.

Now, we will test our code on even bigger files of over 1000 lines. We tried to draw a DFG of a Verilog code file of 1200 lines. The input file is attached in the zip as “input2.txt”. We got the output as shown in below figure.



```
[Running] cd "f:\Semester VI\Embedded Systems\Project\" && g++ main.cpp -o main && "f:\Semester VI\Embedded Systems\Project\"main

Data Flow Graph :
TP  TPE +   TP1
TPE TP1 +   TPE1
DRead1  DOutA   -   DRead
DIn1    DRead   +   DIn
DWrite1 DAddrA  +   DWrite
IAddr1  DWrite  +   IAddr
IRead1  IIn +   IRead
TDO1    DOutA   -   TDO
Val cru +   tempbuff[0]
counter totalcount  +   totalcount
pastcount   counter +   pastcount
totalcount  counter -   buff[pastcount]
DAD1    cert    +           DAD1
DAD2    cert    -           DAD2
DAD2    cert    +           DO1
DO0 totalcount  -           DAD3
DAD3    DO0 +           DAD4
DO0 SPCDIS  +           DO2
LogicZero   DAddrE2D    +   DReadED
LogicZero   DAddrED +   DWriteED
LogicZero   DReadED +   DReadE2D
LogicZero   DWriteED    +   DWriteE2D
IAddreED    WRSTND  -   IInED1
rstS    weS -   goS
goS rstA    -   PauseS
SPCREQS PauseS  +   SPCDISS
WRSTNSP MRSTSP0 *   ShiftWRSP
CaptureWRSP ShiftWRSP   *   SelectWIRSP
DB1 DB2 +   s1
DB1 DB2 -   s2
MRSTDAP DB1 +   MRST11
MRSTDAP DB2 +   MRST121
LogicOne    MASRST0 +   MRSTSP1
LogicOne    resPMC  -   MRSTSP2
STARTF0 MRSTSP2 -   RSTF1
SPCREQF RSTF1   *   SPCDISF1


[Done] exited with code=0 in 1.431 seconds
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On matching this output manually with the code, we got our results matched. The conversion to single-assignment form and the resulting DFG are both accurate. Therefore, our code performs good for Verilog files of over 1000 lines.

Hence, our code has performed accurately on multiple test cases. Scalability of the code has been proven by taking bigger files as well. Therefore, our implementation of DFG in C++ is successful.

<u>THE END</u>