Model Usage Notes:

A. Features have been modeled

1. Output Voltage Setting

2. Programmable Soft-Start

3. Frequency and Operation Mode Selection

4. Low-side FET Zero-Crossing

5. Current Sense and Positive Overcurrent Protection(OCP)

6. Low-side FET Negative Current Limit

7. Power Good

8. Over Voltage Protection(OVP)

9. Under Voltage Protection(UVP)

10. Output Voltage Discharge

11. EN/VIN UVLO Protection

12. BOOT functionality

B. Features have not been modeled

1. Operating Quiescent Current

2. Shutdown Current

3. Temperature dependent characteristics

4. Ground Pins have been tied to 0V internally and hence model does not support Inverting topologies.

Application Notes:

1. The TPS543B22 model is encrypted and will only run in PSPICE Versions 17.4 and up.

2. The design is similar to the EVM schematic and has been designed for the same input voltage, output load and output voltage conditions.

3. The testbench has been configured Vin = 12V, Vout = 1V and Iout = 20A.

4. This model has been corner tested for an input voltage range of 4V to 18V and a load current range of 100mA to 20A.

5. The RMODE resistor(R6) is reduced to 4.02k to set Soft-Start time as 1ms to reduce simulation time.

6. The operating quiescent current have not been modeled.

7. Thermal shutdown characteristics of the part have not been modeled.

8. Ground pins have been tied to 0V internally. Therefore, this model cannot be used for inverting topologies

9. The simulation runs for 1.2ms and takes approximately 2hours to run on a 4 core 2.8GHz machine