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Title: TOP

ID: ABX00043

Revision: V3.7

Date: 10/02/2022

Time: 10:54:19

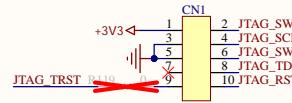
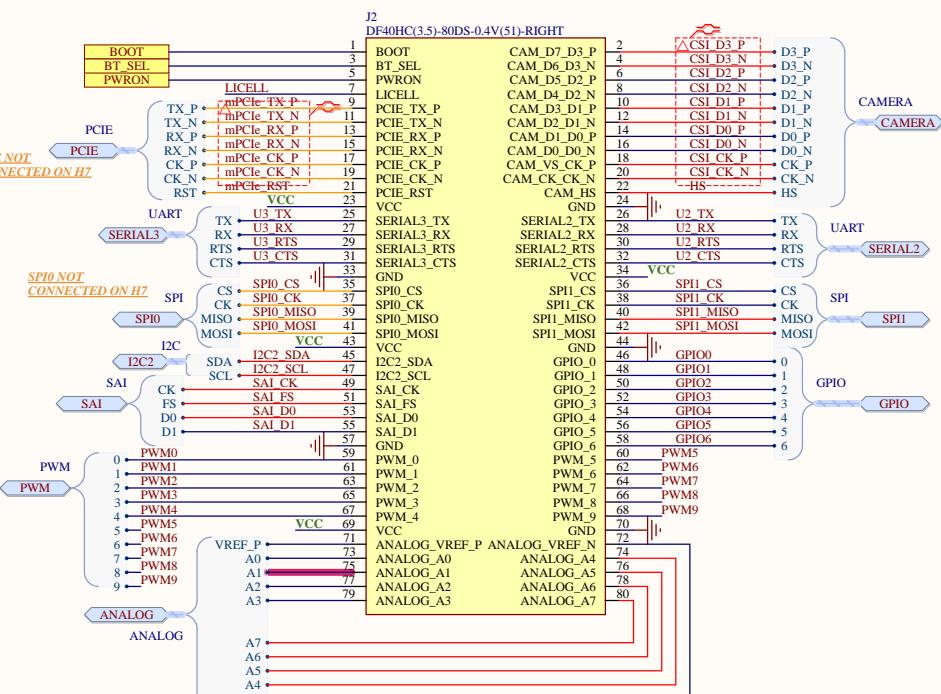
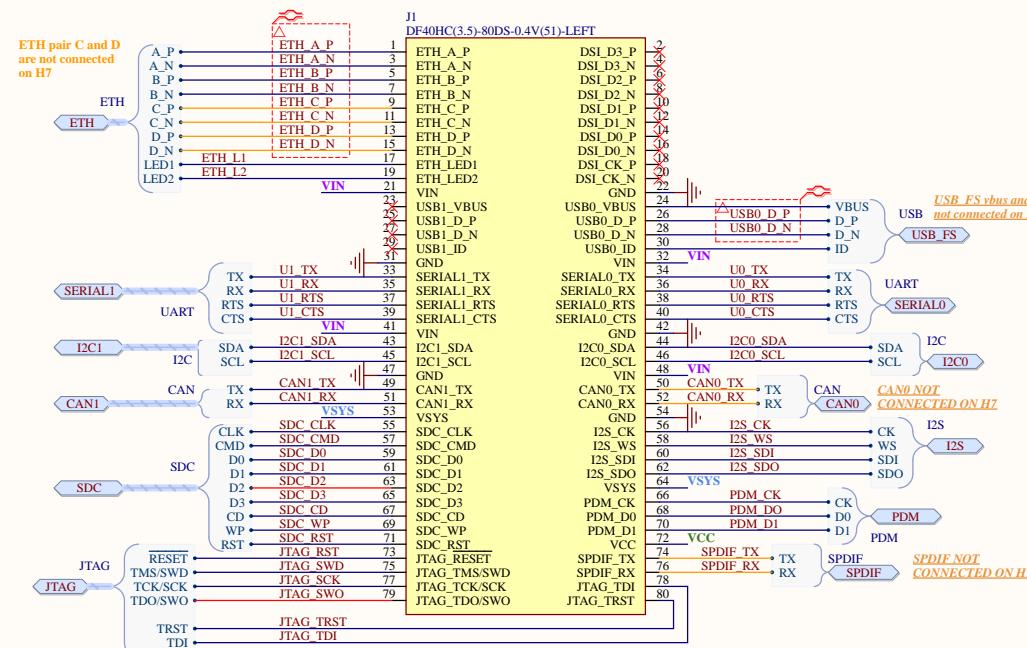
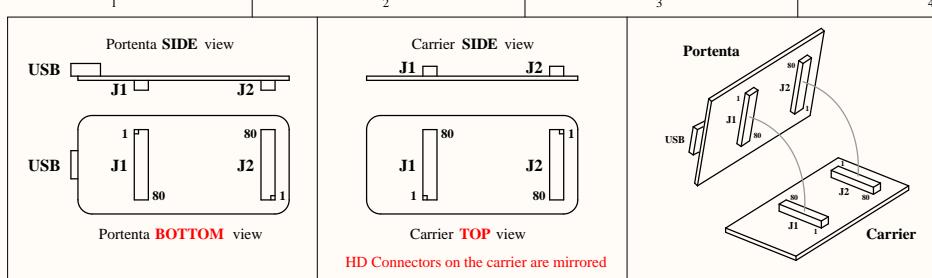
Sheet 1 of 14

File: TOP.SchDoc

Author: Arturo Guadalupi



RevAuthor: S. Navaretti



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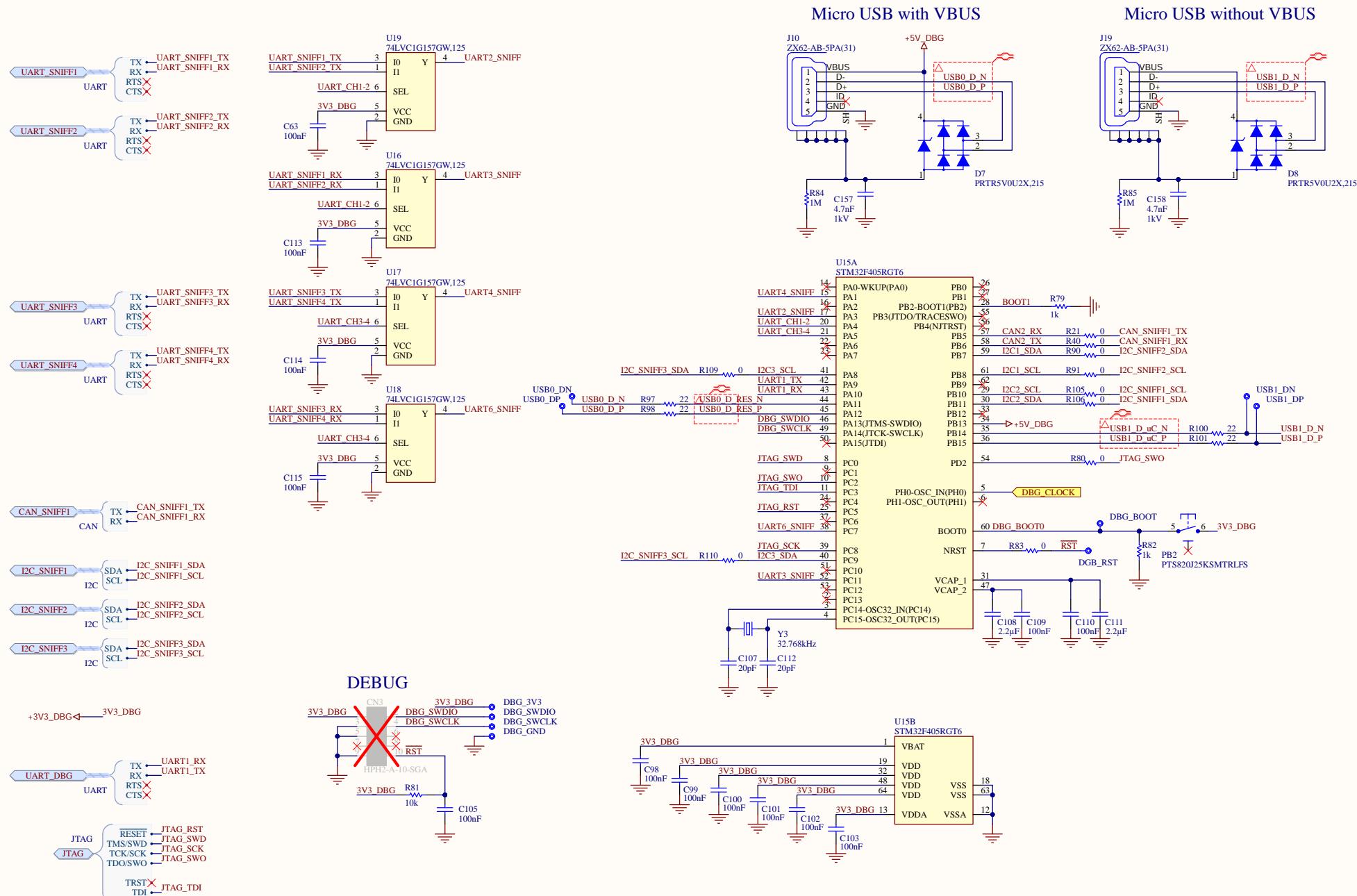
POWER NETS TABLE			
NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U10) programmable output.
VCC	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U10) programmable output.
VSYS	PORTENTA RESERVED OUTPUT	RESERVED, DO NOT USE 3.5V to 4.2V, max 600mA.	Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the buck inside the PMIC itself.
LICELL	PORTENTA INPUT	Coinc cell max 3.6V, max 46uA.	Max 4uA with PMIC (U10) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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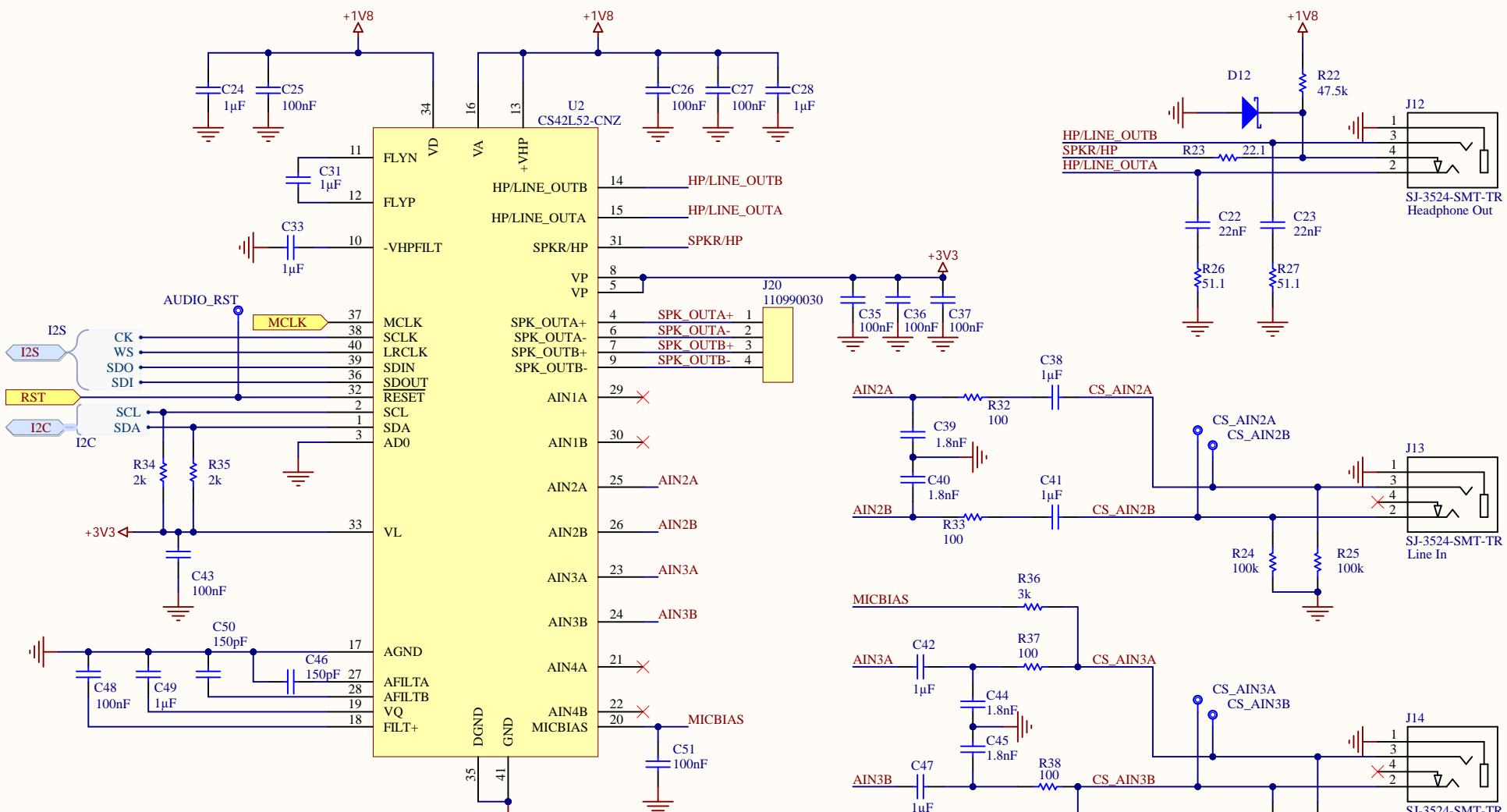
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Title: DEBUGGER

ID: ABX00043	Revision: V3.7
Date: 10/02/2022	Time: 10:54:25
Sheet 3 of 14	
File: DEBUGGER.SchDoc	Author: Arturo Guadalupi



1 2 3 4



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Title: **AUDIO**

ID: **ABX00043**

Revision: **V3.7**

Date: **10/02/2022**

Time: **10:54:29**

Sheet **4** of **14**

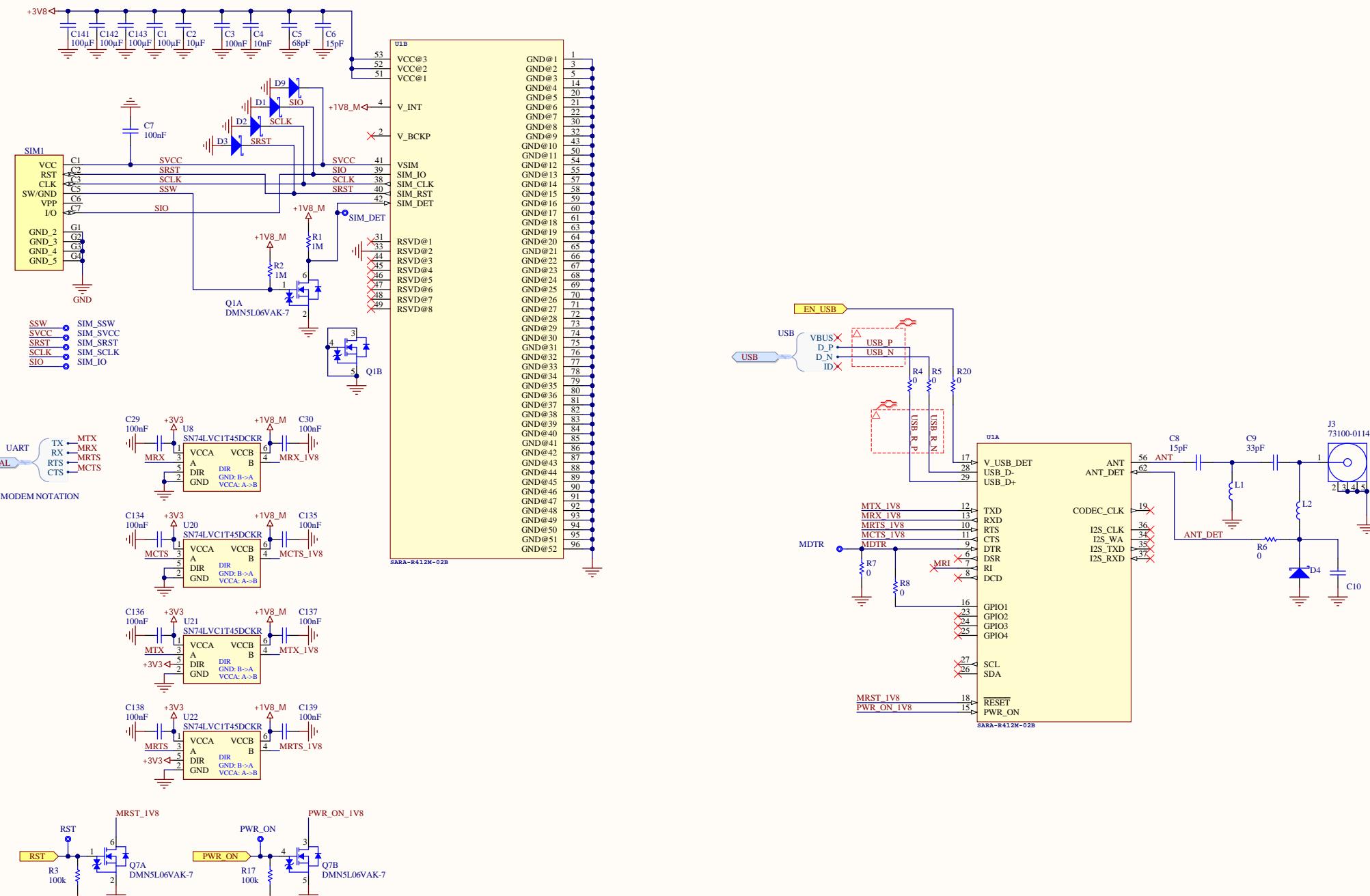
File: **AUDIO.SchDoc**

Author: **Arturo Guadalupi**

RevAuthor: **S. Navaretti**



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Title: CELL MODEM

ID: ABX00043

Revision: V3.7

Date: 10/02/2022

Time: 10:54:33

Sheet 5 of 14

File: CELL_MODEM.SchDoc

Author: Arturo Guadalupi

RevAuthor: S. Navaretti



A

A

B

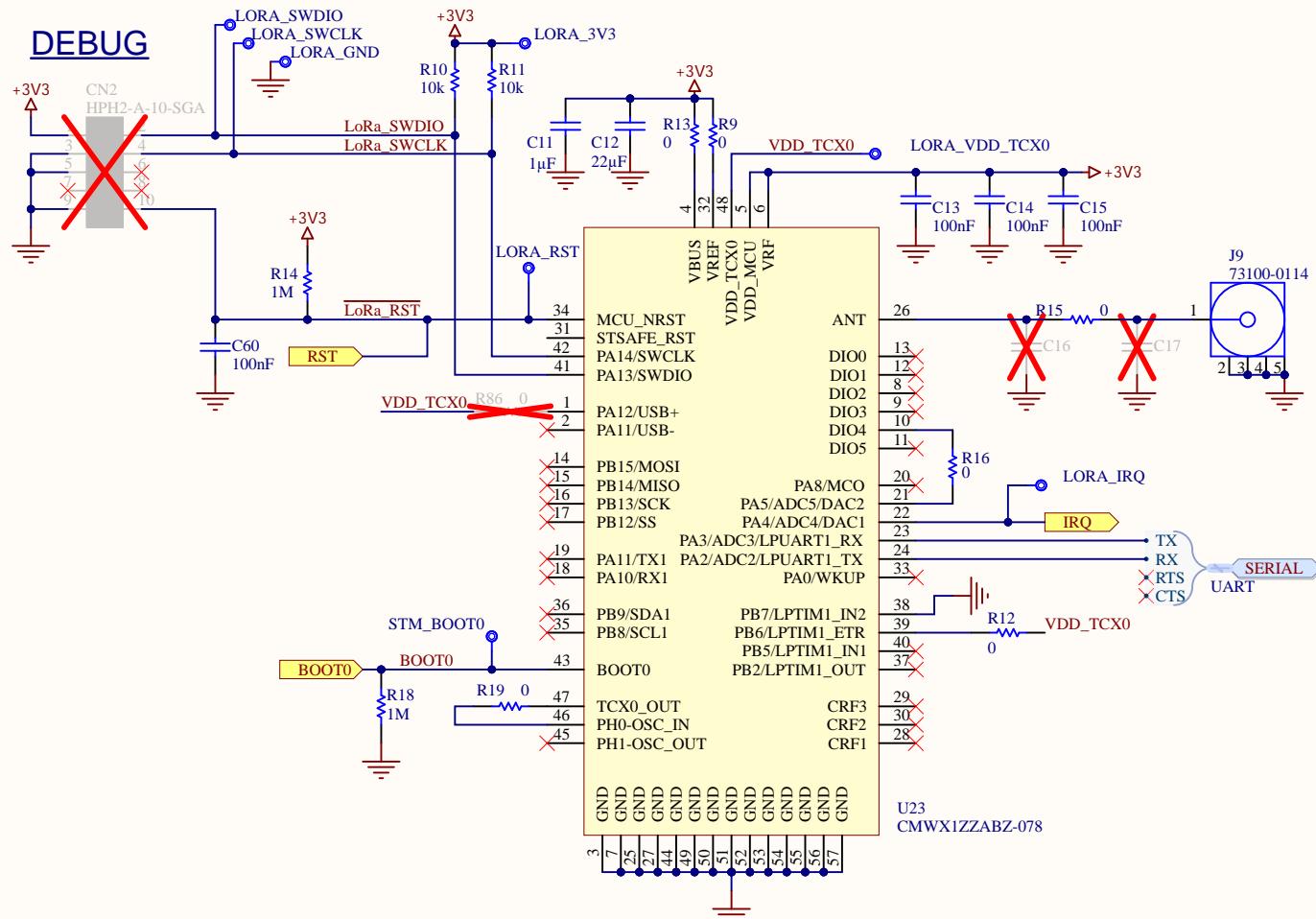
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Title: **LORA**

ID: **ABX00043**

Revision: **V3.7**

Date: **10/02/2022** Time: **10:54:37**

Sheet **6** of **14**

File: **LORA.SchDoc**

Author: **Arturo Guadalupi**



Top side		Bottom side	
1		2	3.3V
3	Reserved****	4	GND
5	Reserved****	6	1.5V
7	CLKREQ#	8	VCC**
9	GND	10	I/O**
11	REFCLK-	12	CLK**
13	REFCLK+	14	RST**
15	N/C or GND	16	VPP**
Mechanical key			
17	Reserved	18	GND
19	Reserved	20	Reserved***
21	GND	22	PERST#
23	PERn0	24	+3.3vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	Reserved*	38	USB_D+
39	Reserved*	40	GND
41	Reserved*	42	LED_WWAN#
43	Reserved*	44	LED_WLAN#
45	Reserved*	46	LED_WPAN#
47	Reserved*	48	+1.5V
49	Reserved*	50	GND
51	Reserved*	52	+3.3V

*Reserved for future second PCI Express Lane (if needed). Pin 51 has changed to be W_DISABLE2#

**Reserved for future Subscriber Identity Module (SIM) interface (if needed)

***Reserved for future wireless disable signal (if needed)

****Reserved for future wireless coexistence control interface (if needed)

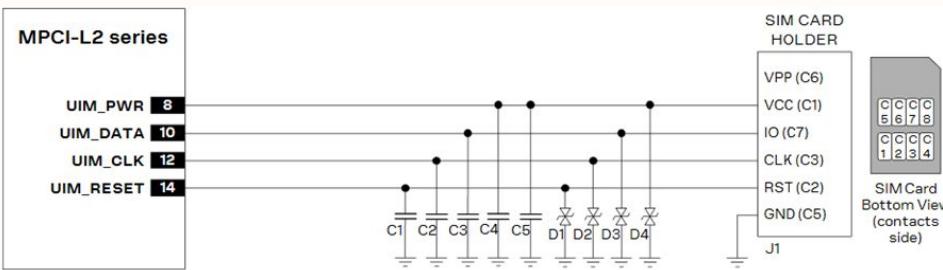
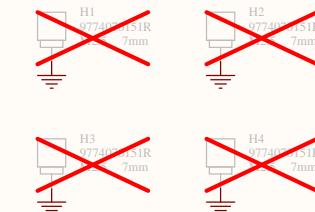
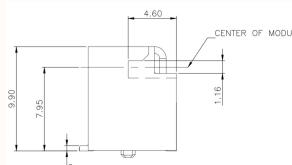
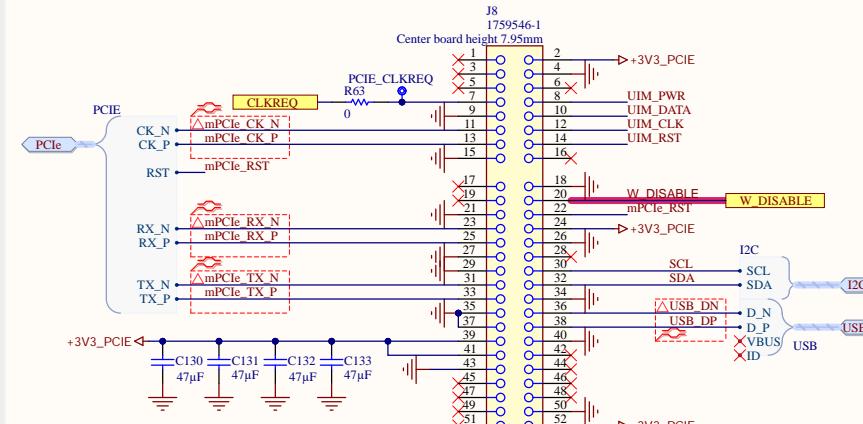
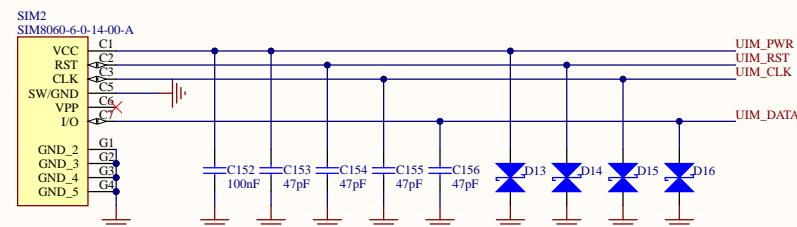


Figure 50: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented



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Title: MINI PCIe

ID: ABX00043

Revision: V3.7

Date: 10/02/2022

Time: 10:54:41

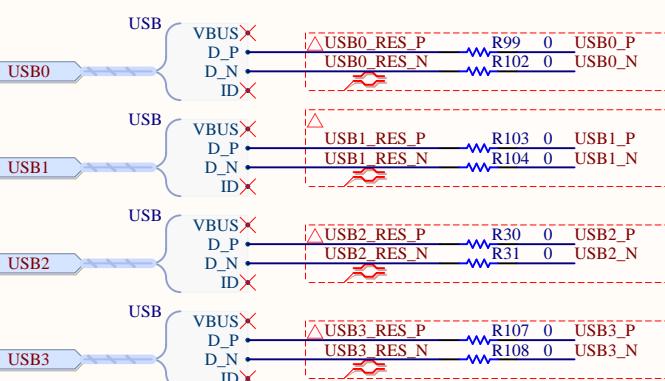
Sheet 7 of 14

File: MINI_PCIE.SchDoc

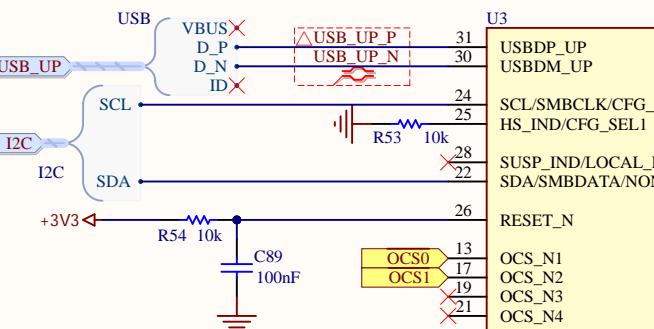
Author: Arturo Guadalupi



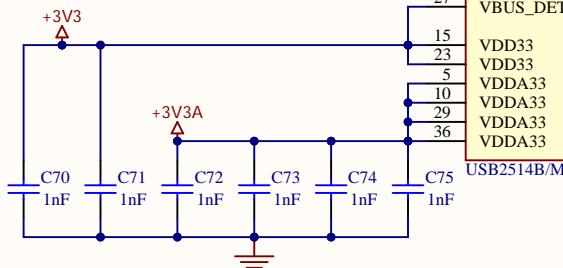
1 2 3 4



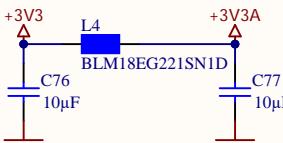
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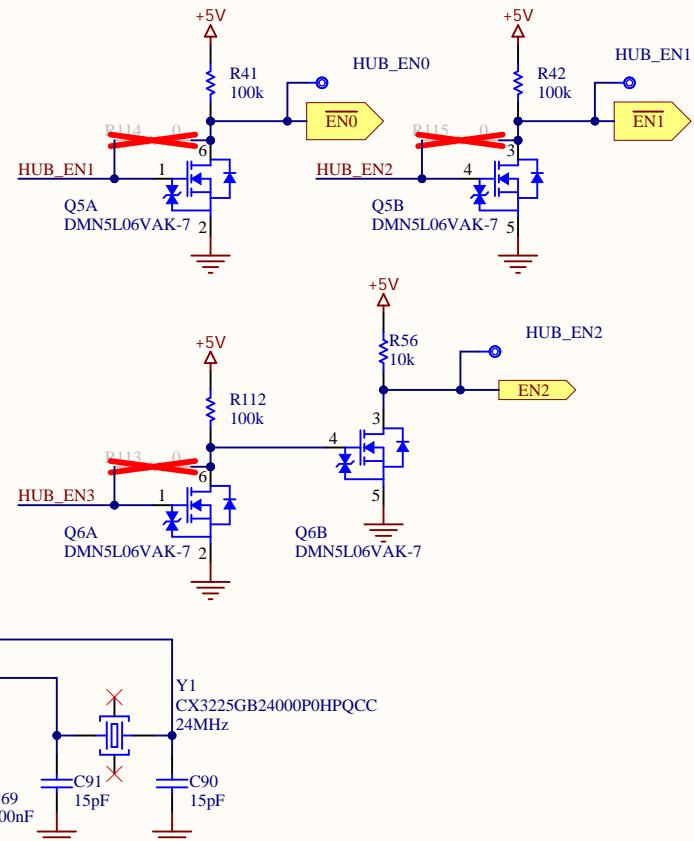


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USBDP_UP	USB0_P
USBDM_UP	USB1_P
SCL/SMBCLK/CFG_SEL0	USB2_P
HS_IND/CFG_SEL1	USB3_P
SUSP_IND/LOCAL_PWR/NON_REM0	USB0_N
SDA/SMBDATA/NON_REM1	USB1_N
RESET_N	USB2_N
OCS_N1	USB3_N
OCS_N2	HUB_EN1
OCS_N3	HUB_EN2
OCS_N4	HUB_EN3
TEST	HUB_EN4
VBUS_DET	RBIAS
VDD33	XTALIN/CLKIN
VDD33	XTALOUT
VDDA33	CRFILT
VDDA33	PLLfilt
VDDA33	EP



1 2 3 4

Title: **USB HUB**

ID: **ABX00043**

Revision: **V3.7**

Date: **10/02/2022**

Time: **10:54:44**

Sheet **8** of **14**

File: **USB_HUB.SchDoc**

Author: **Arturo Guadalupi**

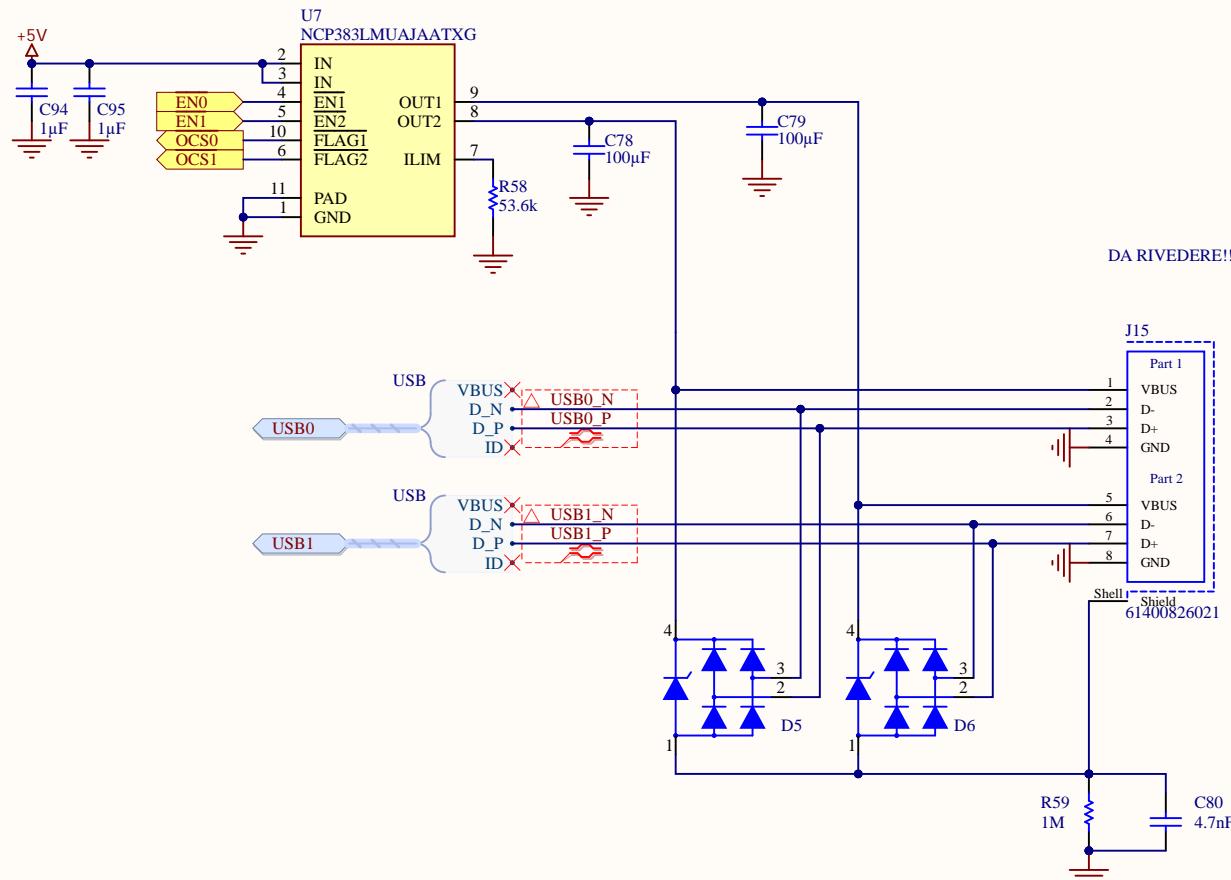


RevAuthor: **S. Navaretti**

1 2 3 4

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DA RIVEDERE!!!

B

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Title: USB CONNECTORS

ID: ABX00043

Revision: V3.7

Date: 10/02/2022 Time: 10:54:47

Sheet 9 of 14

File: USBA_CONNECTORS.SchDoc

Author: Arturo Guadalupi



A

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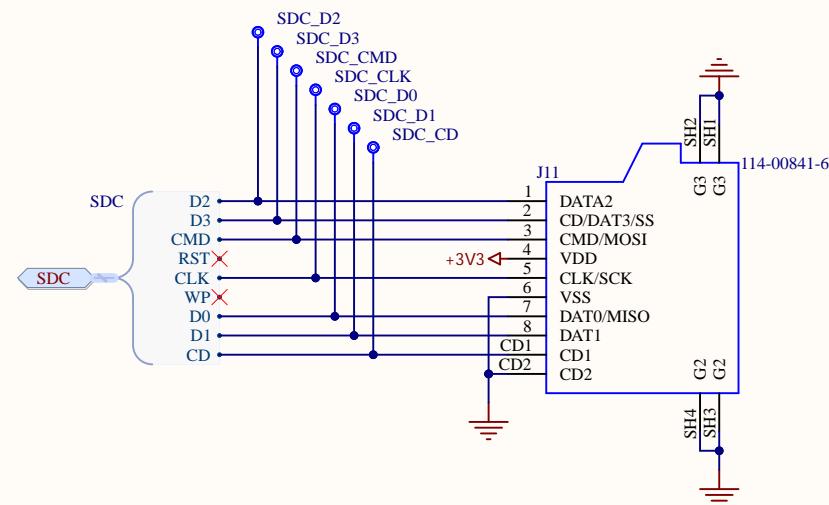
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Title: SD CARD

ID: ABX00043

Revision: V3.7

Date: 10/02/2022 Time: 10:54:57

Sheet 10 of 14

File: SD_CONNECTOR.SchDoc

Author: Arturo Guadalupi



A

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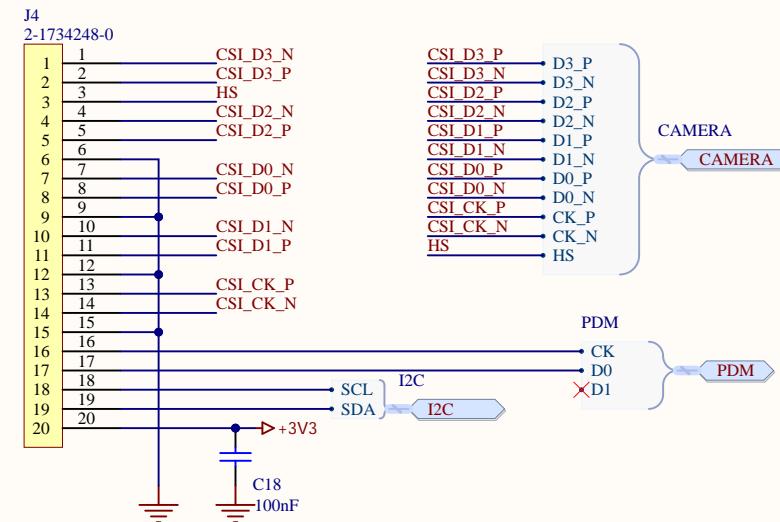
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Title: CAMERA CONNECTOR

ID: ABX00043

Revision: V3.7

Date: 10/02/2022 Time: 10:55:02

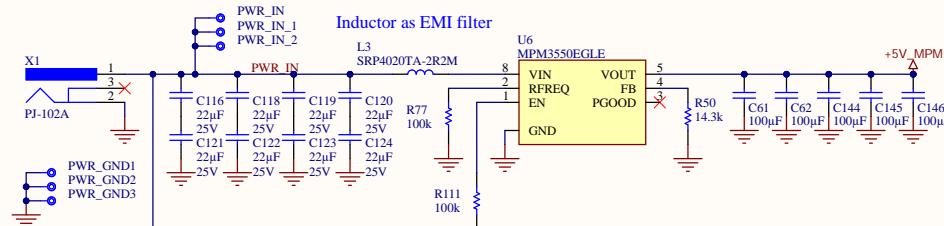
Sheet 11 of 14

File: CAMERA_CONNECTOR.SchDoc

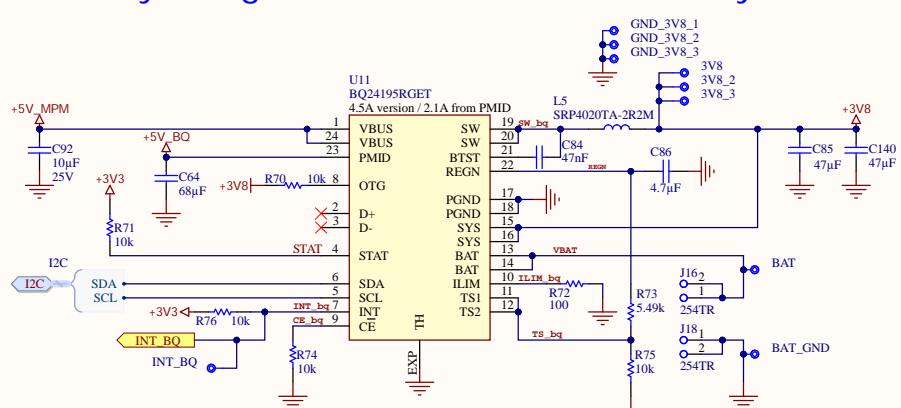
Author: Arturo Guadalupi



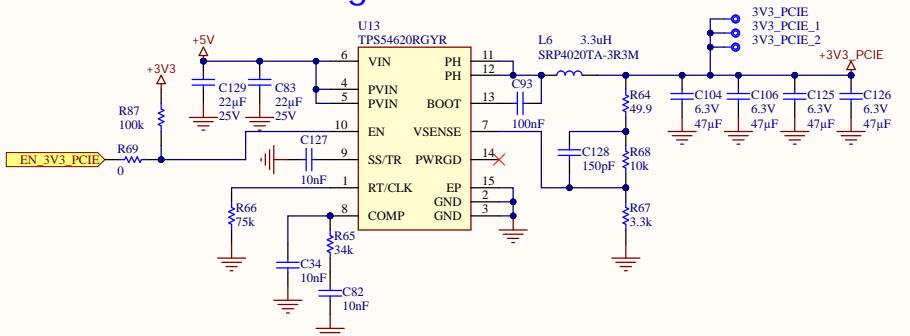
Power in from jack, +5V step down



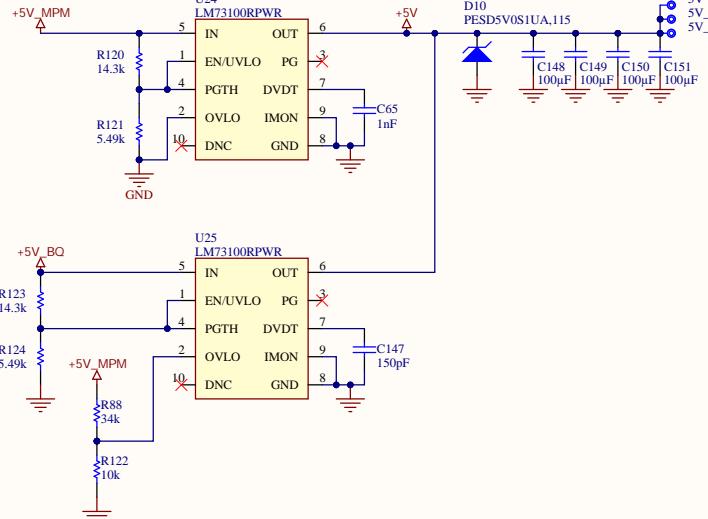
Battery charger and +5V boost from battery



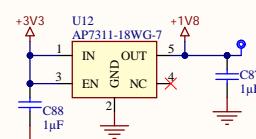
PCIE dedicated high current 3V3



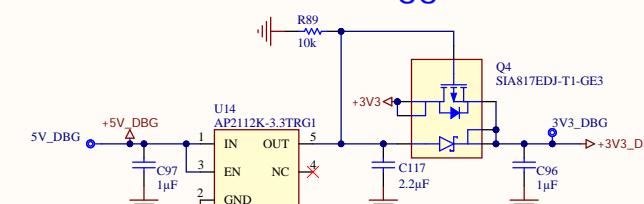
Power OR between +5V from jack or battery boost



Audio 1V8 linear regulator



Dedicated Debugger PWR



PIN DESCRIPTIONS

Pin	Name	RS-232	RS-485 Full Duplex	RS-485 Half Duplex
1		Ground		
2	GND			
3	T1OUT, B/Z	Transmitter 1 Output	Z Driver Neg Output	B/Z Neg Input/Output
4	T2OUT, A/Y	Transmitter 2 Output	Y Driver Pos Output	A/Y Pos Input/Output
5				
6	R1OUT	Receiver 1 Output	X	X
7	R2OUT, RO	Receiver 2 Output	Receiver TTL Output	Receiver TTL Output
8				
9				
10	SHDN		Low power shutdown mode when low	
11	SLEW		Data rate limited to 250kbytes when low	
12	FD_TX_TERM	X	120Ω A-B termination enabled when both TERM and FD_TX_TERM are high	X
13	TERM	X	120Ω A-B termination enabled when high	
14	RS-485/RS-232	0	1	1
15	HALF/FULL	X	0	1
16				
17	GND		Ground	
18	R2IN, A	Receiver 2 Input	A Pos Receiver Input	X
19	R1IN, B	Receiver 1 Input	B Neg Receiver Input	X
20	RE	X	Receiver enabled when low	
21	T2IN, DE	Transmitter 2 Input	Driver enabled when high	
22	T1IN, DI	Transmitter 1 Input	Driver TTL Input	
23				
24	V-		Charge pump negative supply, 0.1μF from ground	
25	C2-		Charge pump cap 2 negative lead	
26	C2+		Charge pump cap 2 positive lead, 0.1μF	
27	V+		Charge pump positive supply, 0.1μF to ground	
28	C1+		Charge pump cap 1 positive lead, 0.1μF	
29	VL		Logic Supply for TTL Inputs and Outputs, $V_L = +1.65V$ to $+5.5V$ or tie to V_{CC}	
30	VCC		Main Supply, $V_{CC} = +3.0V$ to $+5.5V$, bypass to ground with 1.0μF	
31				
32	C1-		Charge pump cap 1 negative lead	

TABLE 3: RS-485/422 TX TRUTH TABLE

SHDN	RS-485/RS-232	DE/T2IN	D1T1IN	Z(B)/T1OUT	Y(A)/T2OUT
0	X	X	X	1/8th unit load	1/8th unit load
1	1	0	X	1/8th unit load	1/8th unit load
1	1	1	0	1	0
1	1	1	1	0	1
X	0	X	X	X	RS-232 Mode

TABLE 4: RS-485/422 RX TRUTH TABLE

RS-485/RS-232	SHDN	HALF/FULL	RE	(A-B)	(Y-Z)	RO/R2OUT
1	0	X	X	X	X	High-Z
1	1	0	0	0	$\geq -50mV$	1
1	1	0	0	0	$\leq -200mV$	0
1	1	0	0	0	Floating	X
1	1	1	0	0	$\geq -50mV$	1
1	1	1	0	0	$\leq -200mV$	0
1	1	1	0	0	Floating	1
1	1	1	X	1	X	High-Z
0	X	X	X	X	X	RS-232 Mode

TABLE 5: RS-485/422 TERMINATION TRUTH TABLE

FD_TX_TERM	TERM	RS-485/RS-232	HALF/FULL	TX TERM	RX TERM
Pins 12	Pins 13	Pins 14	Pins 15	Pins 3-4	Pins 18-19
X	0	1	0	-	-
0	1	1	0	-	ON
X	0	1	1	-	ON
X	1	1	1	ON	-
X	X	0	0	X	-

The DE and RE pins have no effect on the termination setting in any mode.



RJ45 connector

RJ10, RJ45 CAN Bus PinOut

RJ45 Pin #	RJ10 Pin #	Signal name	Signal Description
1	2	CAN_H	Dominant High
2	3	CAN_L	Dominant Low
3	4	CAN_GND	Ground
4	-	Reserved	Upgrade Path
5	-	Reserved	Upgrade Path
6	-	CAN_SHLD	CAN Shield, Optional
7	-	CAN_GND	Ground
8	1	CAN_V+	Power, Optional

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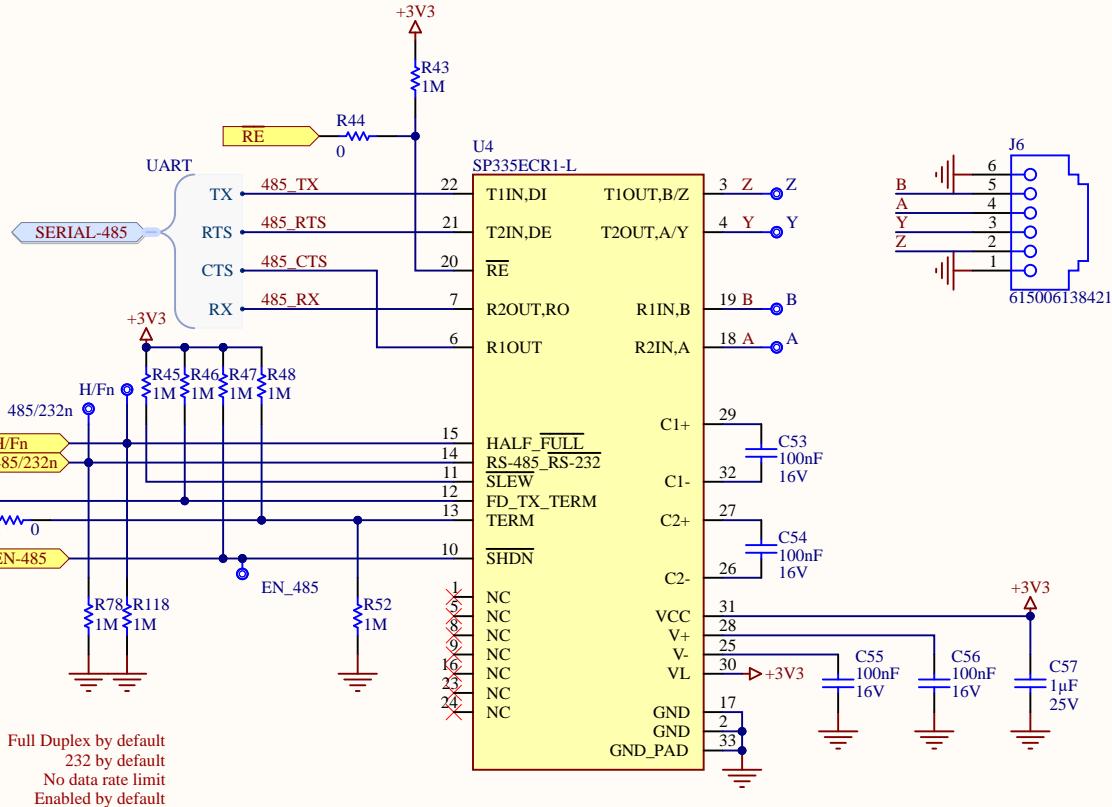
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TABLE 1: RS-232 TX TRUTH TABLE

SHDN	RS-485/RS-232	D1T1IN, DE/T2IN	Z(B)/T1OUT, Y(A)/T2OUT
0	X	X	1/8th unit load
1	0	0	0
1	0	1	1
1	1	1	X

TABLE 2: RS-232 RX TRUTH TABLE

SHDN	RS-485/RS-232	B1T1IN, A/R2IN	R1OUT, R2OUT
X	0	0	1
X	0	1	0
X	0	Inputs open	1
X	1	X	R1OUT High-Z, R2OUT in RS-485 Mode

**Title: FIELDBUS**

ID: ABX00043

Revision: V3.7

Date: 10/02/2022 Time: 10:55:08

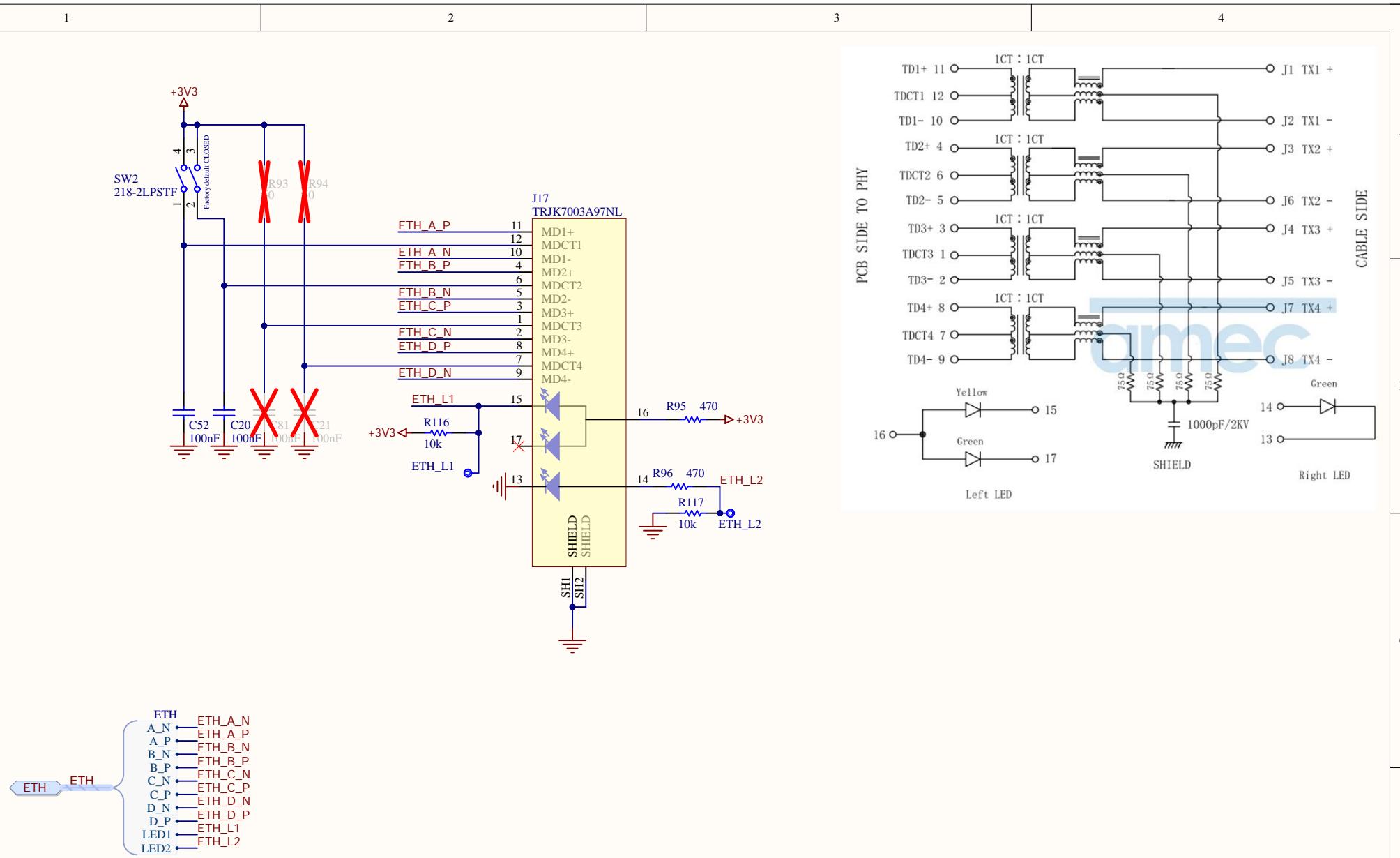
Sheet 13 of 14

File: FIELDBUS.SchDoc

Author: Arturo Guadalupi



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