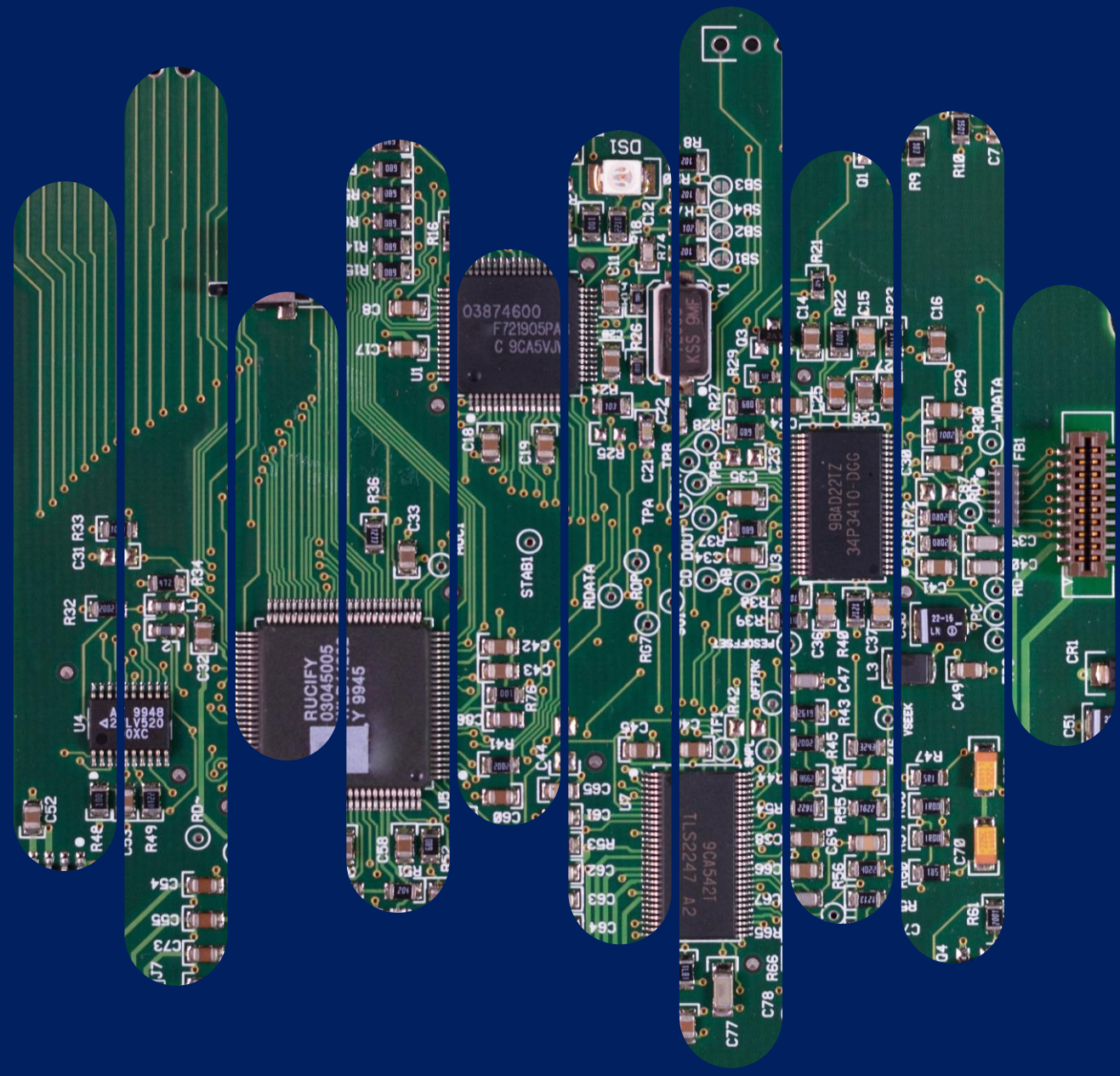
Electronic Devices

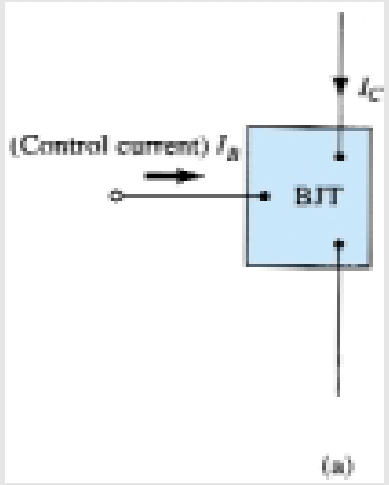


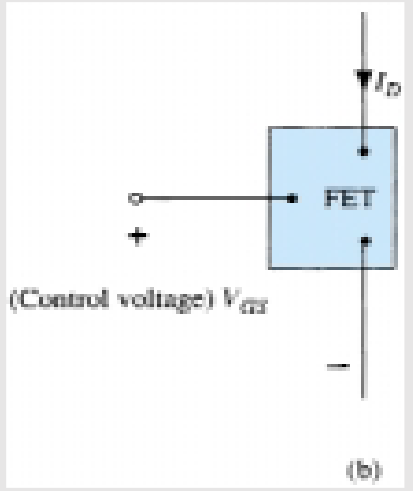
CHAPTER 4

The Field Effect Transistor

4.2 JFET Construction

FET is a three terminal device used for applications similar to BJTs.
However , there are important differences between the two





BJT transistor is a current-controlled device as depicted , while the JFET transistor is a voltage-controlled device as shown

4.2 JFET Construction

Similarities in Applications:

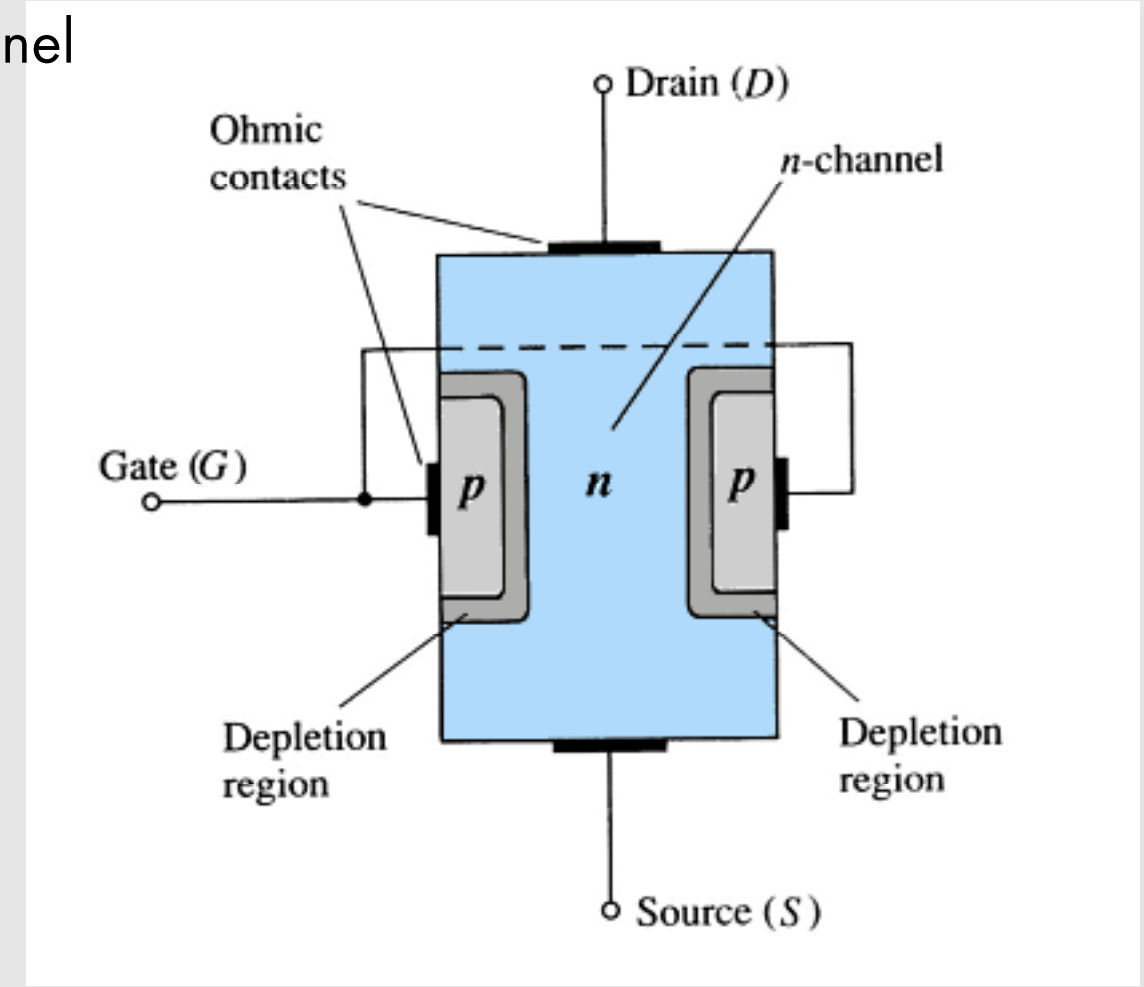
-Amplifiers
-Oscillators
-Switching devices
-Impedance matching circuits

Differences:

-FETs are unipolar devices where as BJTs are bipolar
-FETs are voltage controlled devices. BJTs are current controlled devices.
-FETs have a higher input impedance. BJTs have higher gains.
-FETs are less sensitive to temperature variations and are more easily integrated on ICs.
-FETs are less noisy than bipolar devices as they have only one type of charge carriers

4.2 JFET Construction

There are three terminals
Drain (D) and Source (S) are connected to n-channel
Gate(G) is connected to the p-type material



There are three basic operating conditions for a JFET:

- $V_{GS} = 0$, V_{DS} increasing to some positive value
- $V_{GS} < 0$, V_{DS} at some positive value
- Voltage-controlled resistor

4.2 JFET Construction

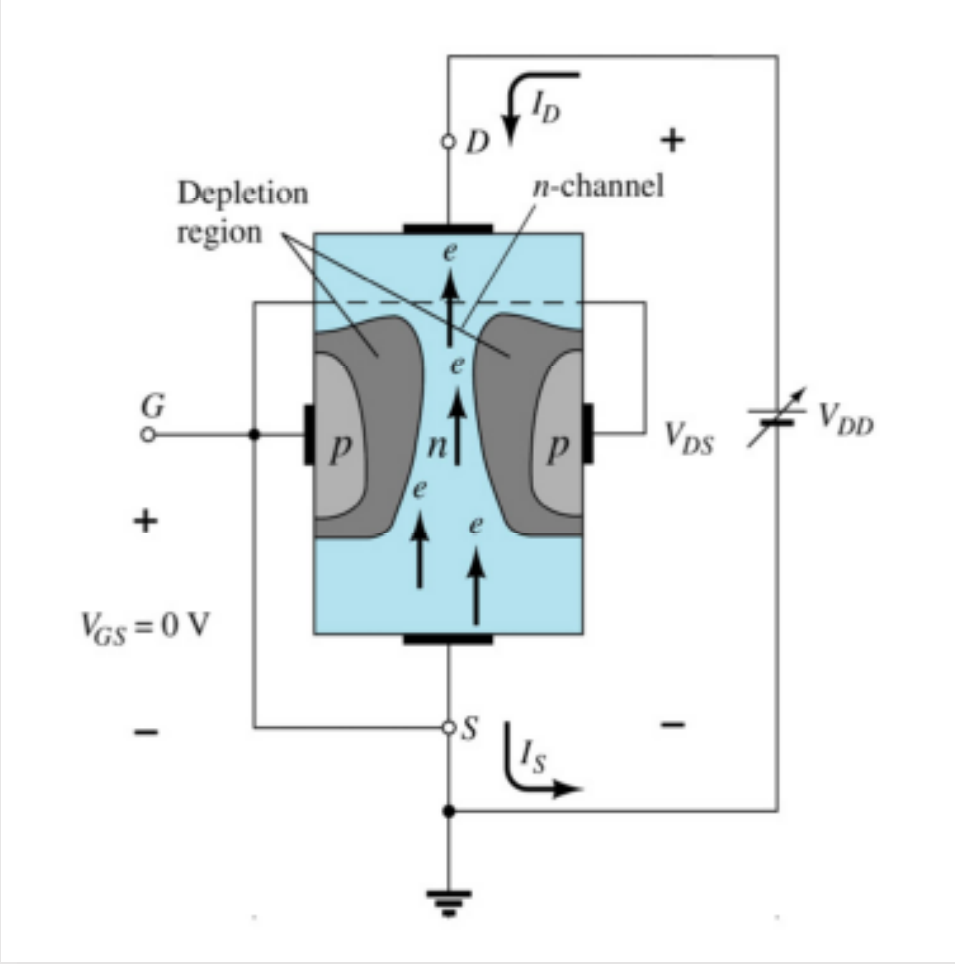
JFET Operating Characteristics: $V_{GS} = 0$ V

Three things happen when $V_{GS} = 0$ and V_{DS} is increased from 0 to a more positive voltage

- The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.

- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.

- Even though the n-channel resistance is increasing, the current (I_D) from source to drain through the n-channel is increasing. This is because V_{DS} is increasing.

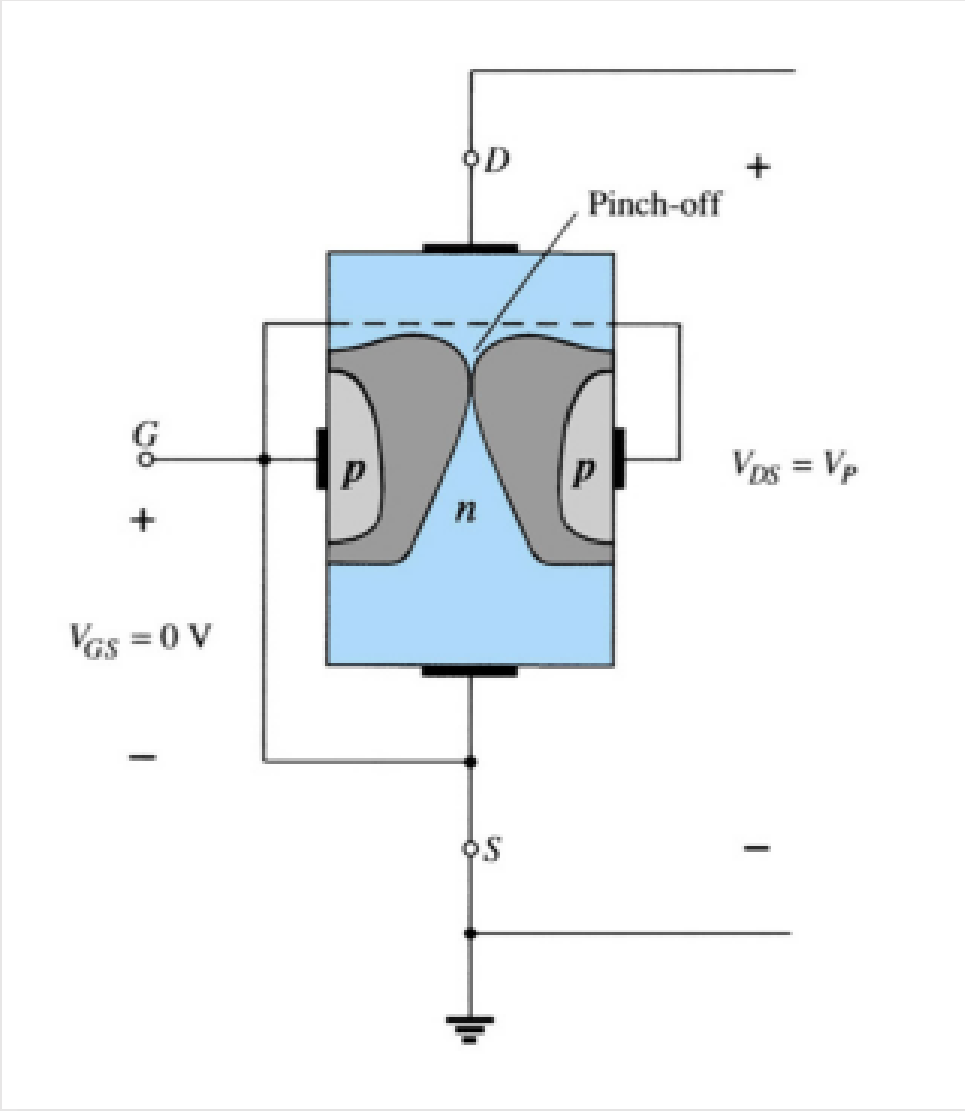


4.2 JFET Construction

JFET Operating Characteristics: Pinch off

If V_{GS} = 0 and V_{DS} is further increased to a more positive voltage, then the depletion zone gets so large that it pinches off the n-channel.

This suggests that the current in the n-channel (I_D) would drop to 0A, but it does just the opposite–as V_{DS} increases, so does I_D.

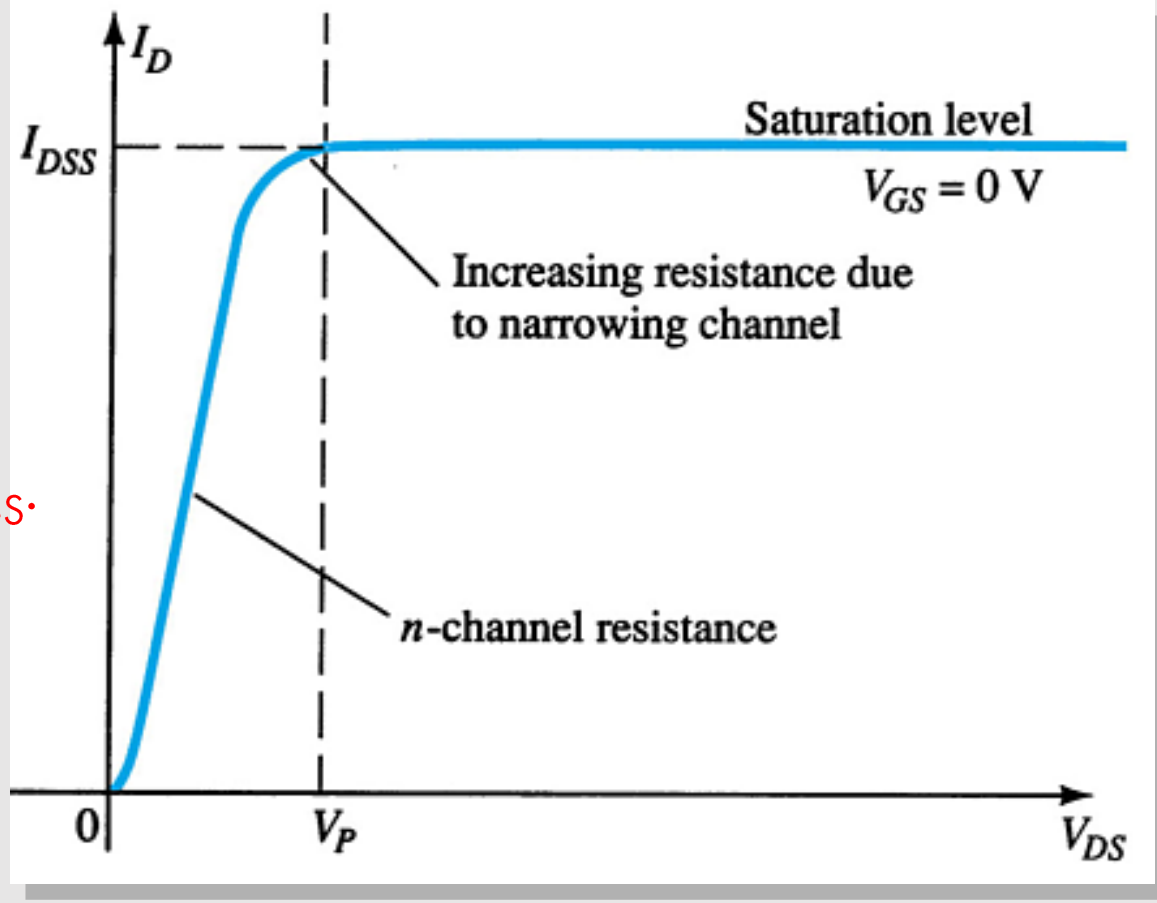


4.2 JFET Construction

JFET Operating Characteristics: Saturation

At the pinch-off point:

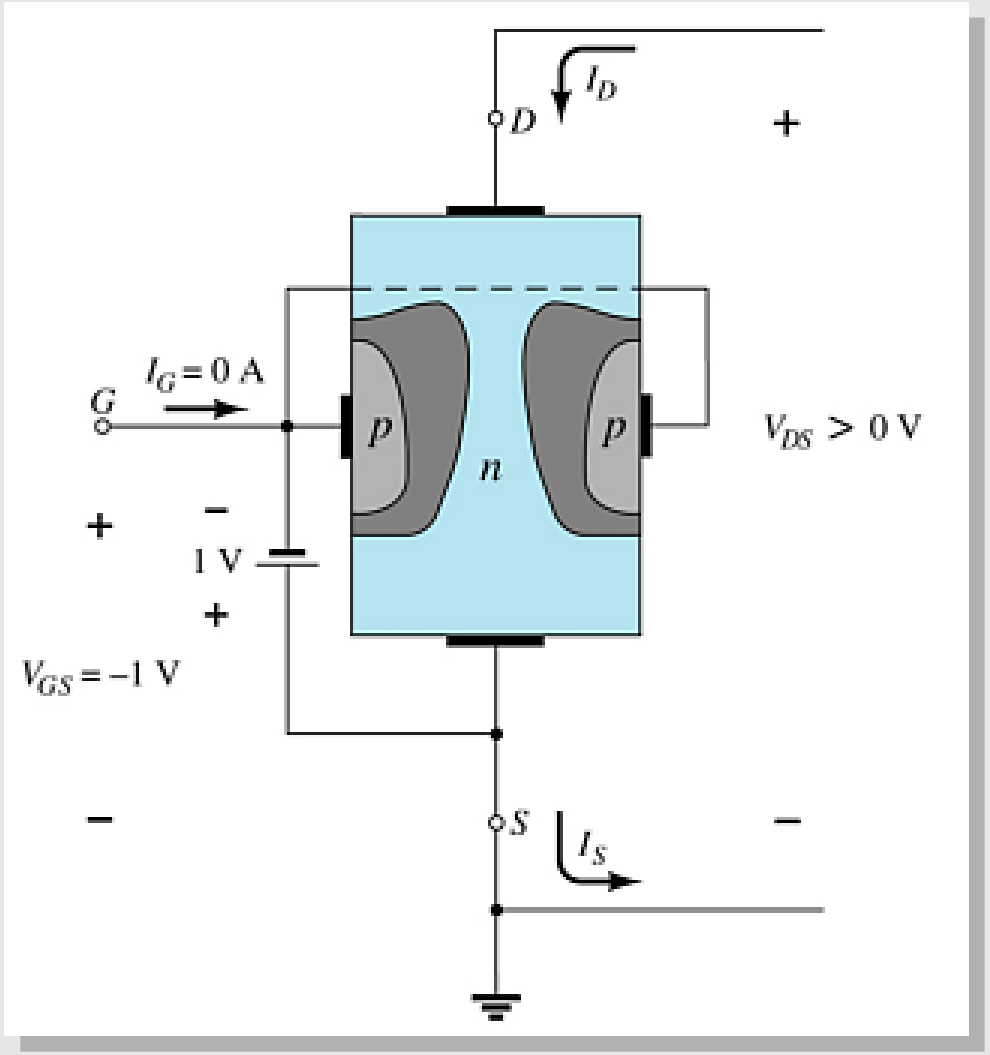
- Any further increase in V_{DS} does not produce any increase in I_D. V_{DS} at pinch-off is denoted as V_p.
- I_D is at saturation or maximum. It is referred to as I_{DSS}.
- The ohmic value of the channel is maximum.



4.2 JFET Construction

JFET Operating Characteristics

As V_{GS} becomes more negative, the depletion region increases.

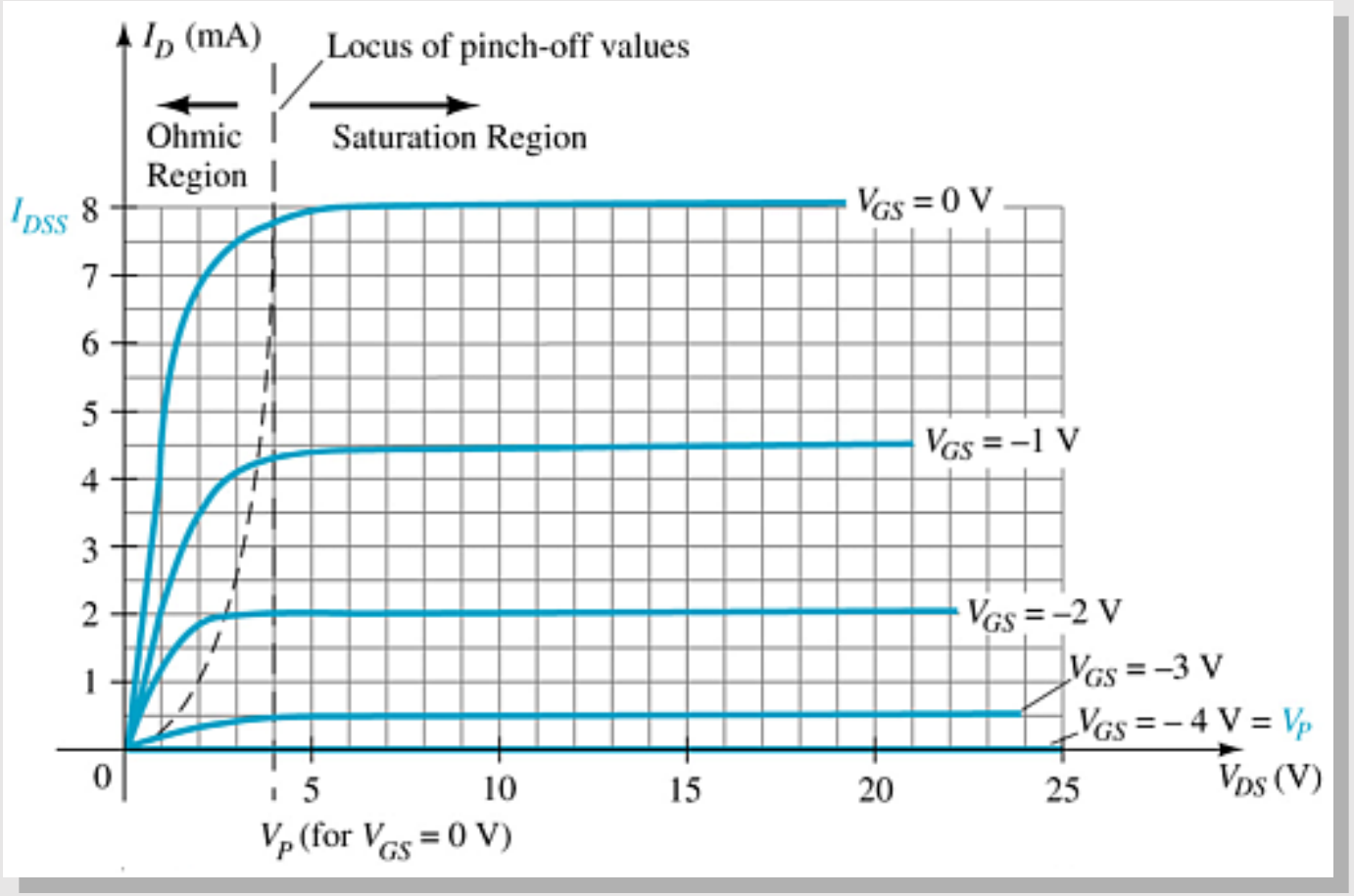


4.2 JFET Construction

JFET Operating Characteristics

As V_{GS} becomes more negative:

- The JFET experiences pinch-off at a lower voltage (V_P).
- I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- Eventually I_D reaches 0 A. V_{GS} at this point is called V_p or $V_{GS(off)}$..



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

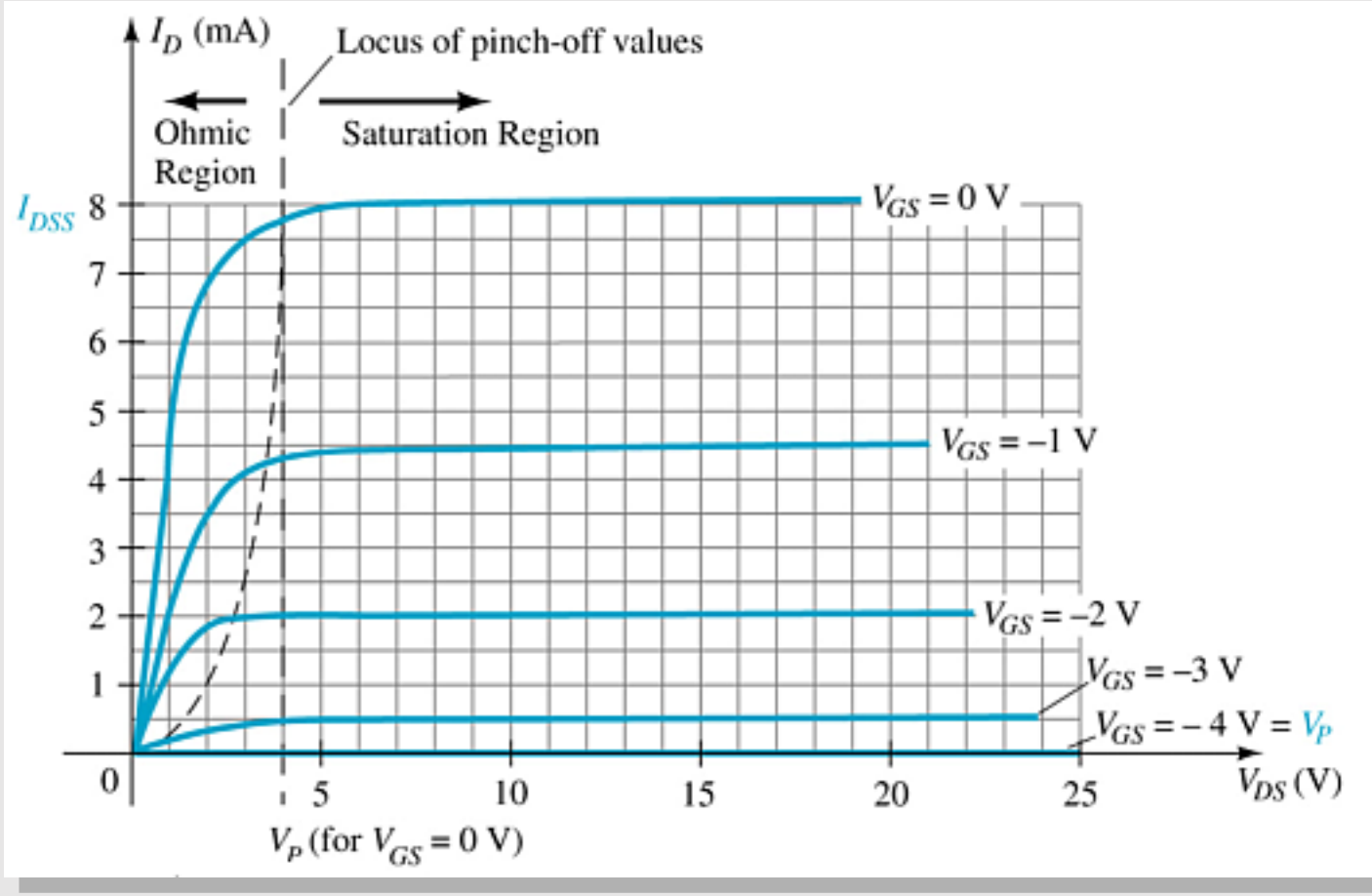
4.2 JFET Construction

JFET Operating Characteristics

The region to the left of the pinch-off point is called the ohmic region.

The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

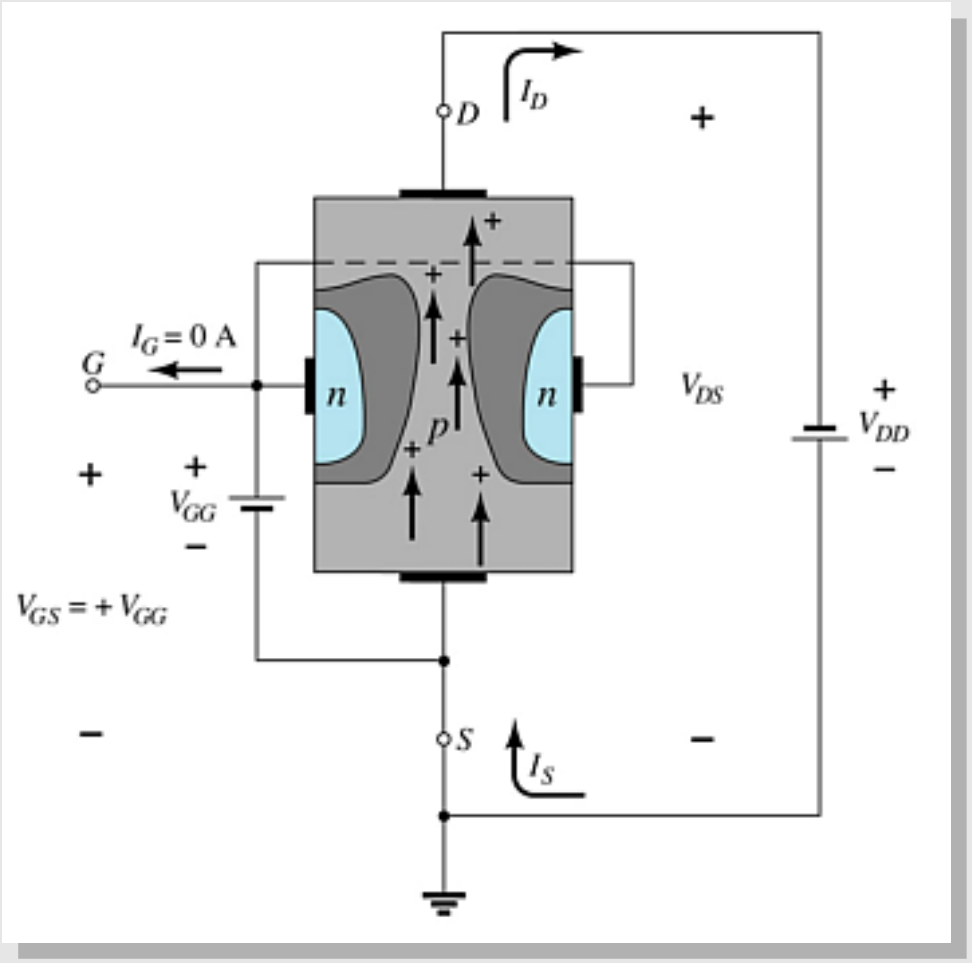
$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$



4.2 JFET Construction

p-Channel JFETS

The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.

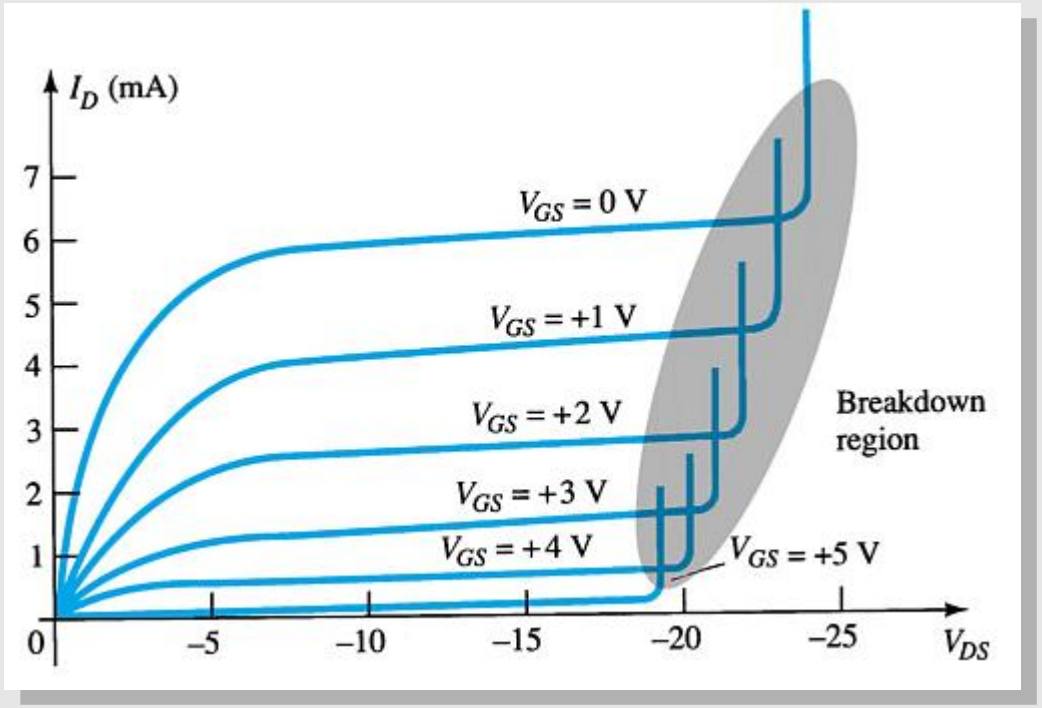


4.2 JFET Construction

p-Channel JFET Characteristics

As V_{GS} increases more positively

- The depletion zone increases
- I_D decreases ($I_D < I_{DSS}$)
- Eventually $I_D = 0$ A



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

4.2 JFET Construction

JFET Transfer Characteristics

The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.

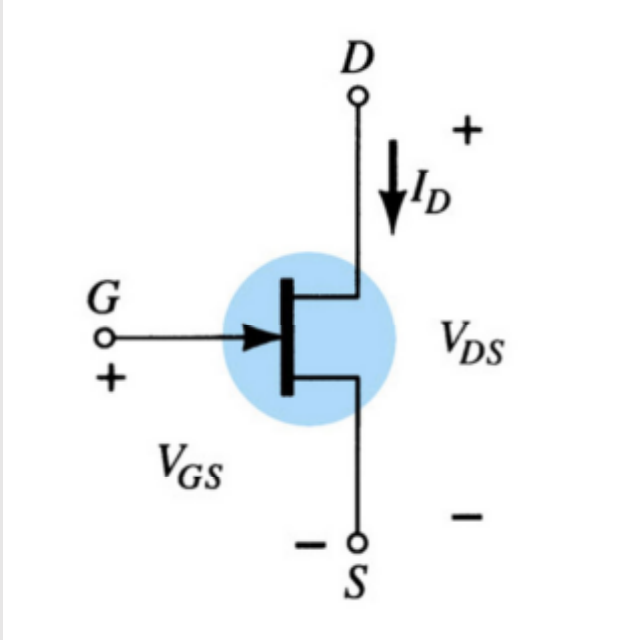
In a BJT, β indicates the relationship between I_B (input) and I_C (output).

In a JFET, the relationship of V_{GS} (input) and I_D (output) is a little more complicated:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

4.2 JFET Construction

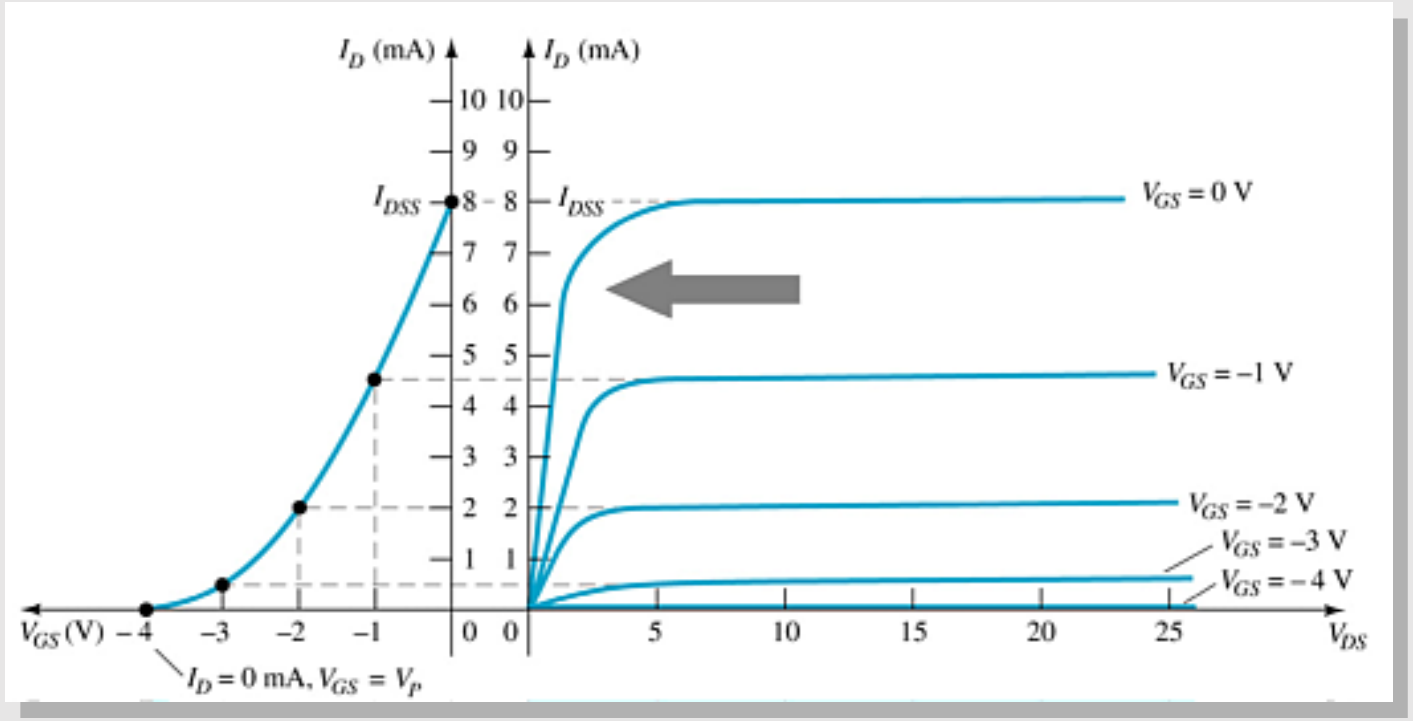
N-channel JFET symbol



4.2 JFET Construction

JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.



4.2 JFET Construction

Plotting the JFET Transfer Curve

Using I_{DSS} and Vp ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

Step 1

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Solving for V_{GS} = 0V $\quad I_D = I_{DSS}$

Step 2

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Solving for $V_{GS} = V_p$ ($V_{GS(off)}$) $\quad I_D$ = 0A

Step 3

Solving for V_{GS} = 0V to V_p $\quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

4.3 JFET Biasing

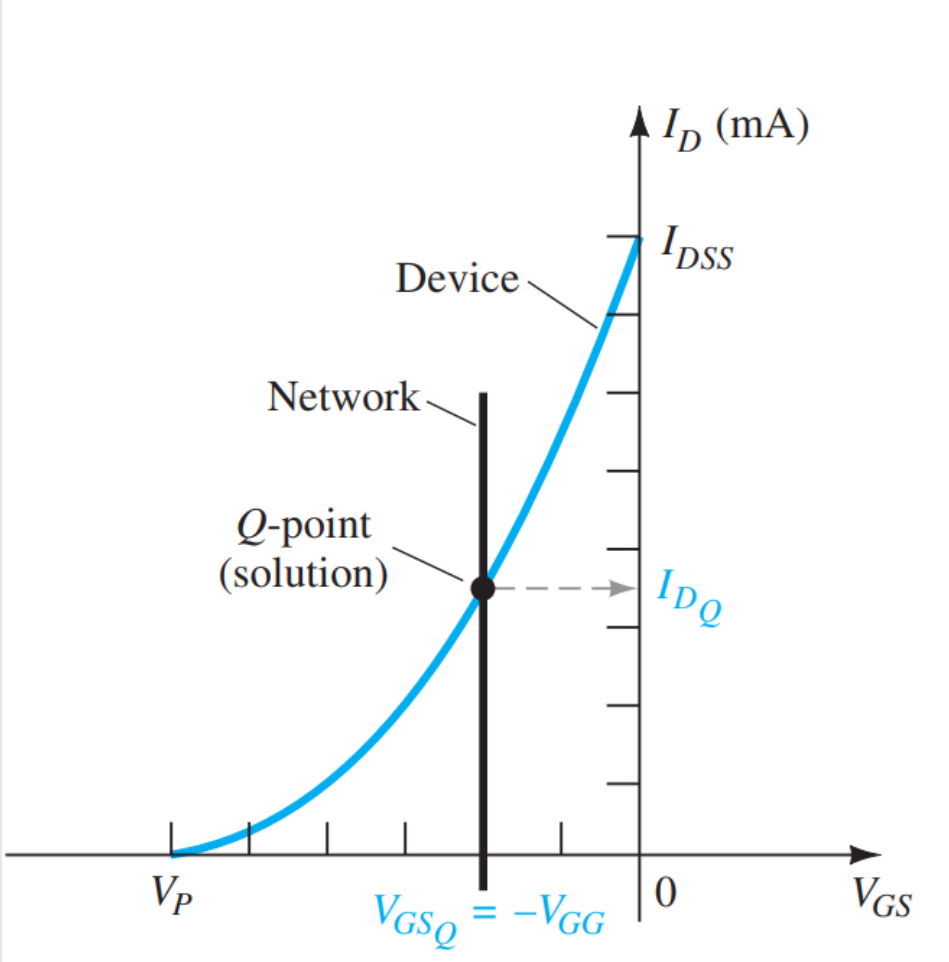
For all FETs

$$I_G \cong 0A$$
$$I_D = I_S$$

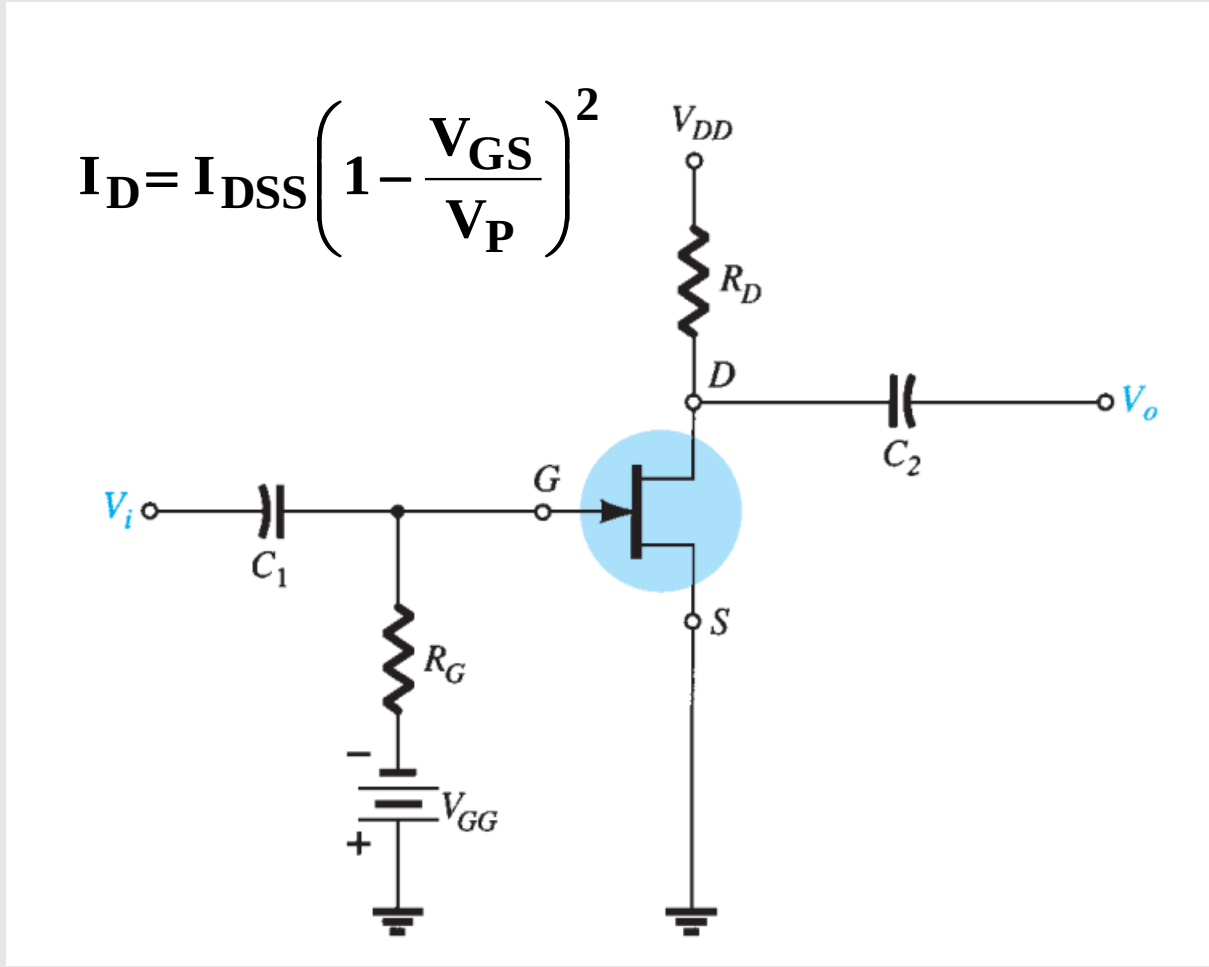
$$\mathbf{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

4.3 JFET Biasing

Fixed-bias Configuration



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

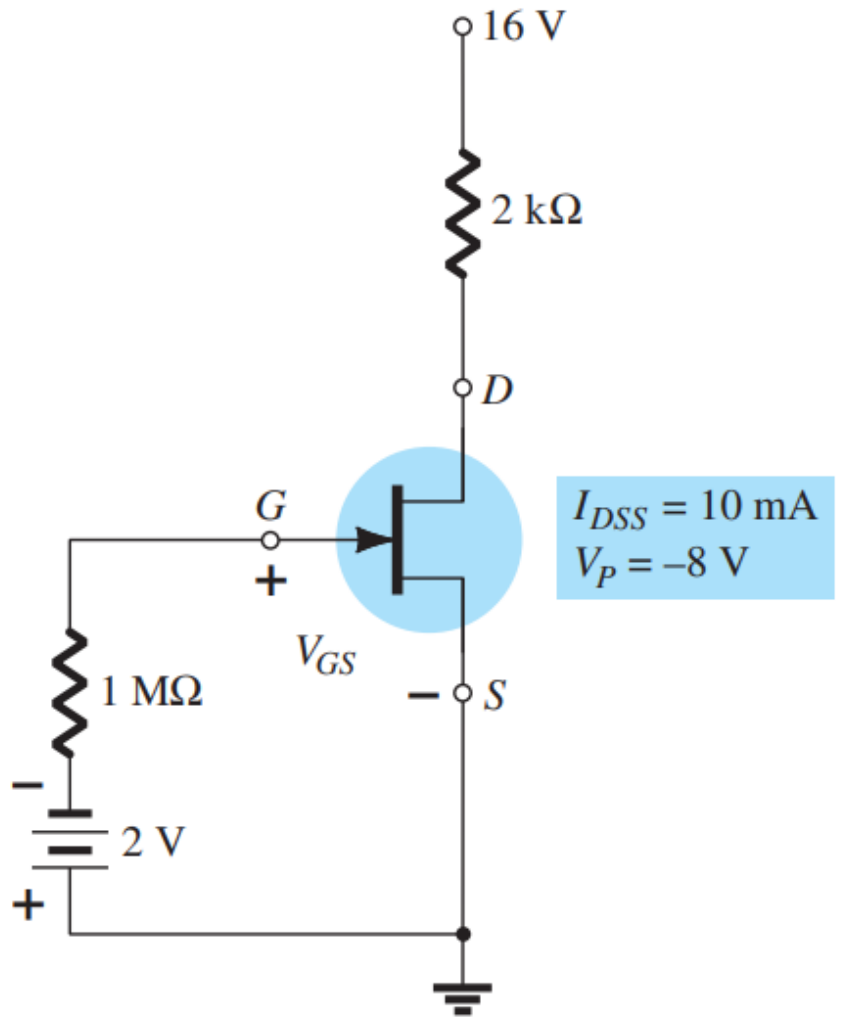


4.3 JFET Biasing

Fixed-bias Configuration

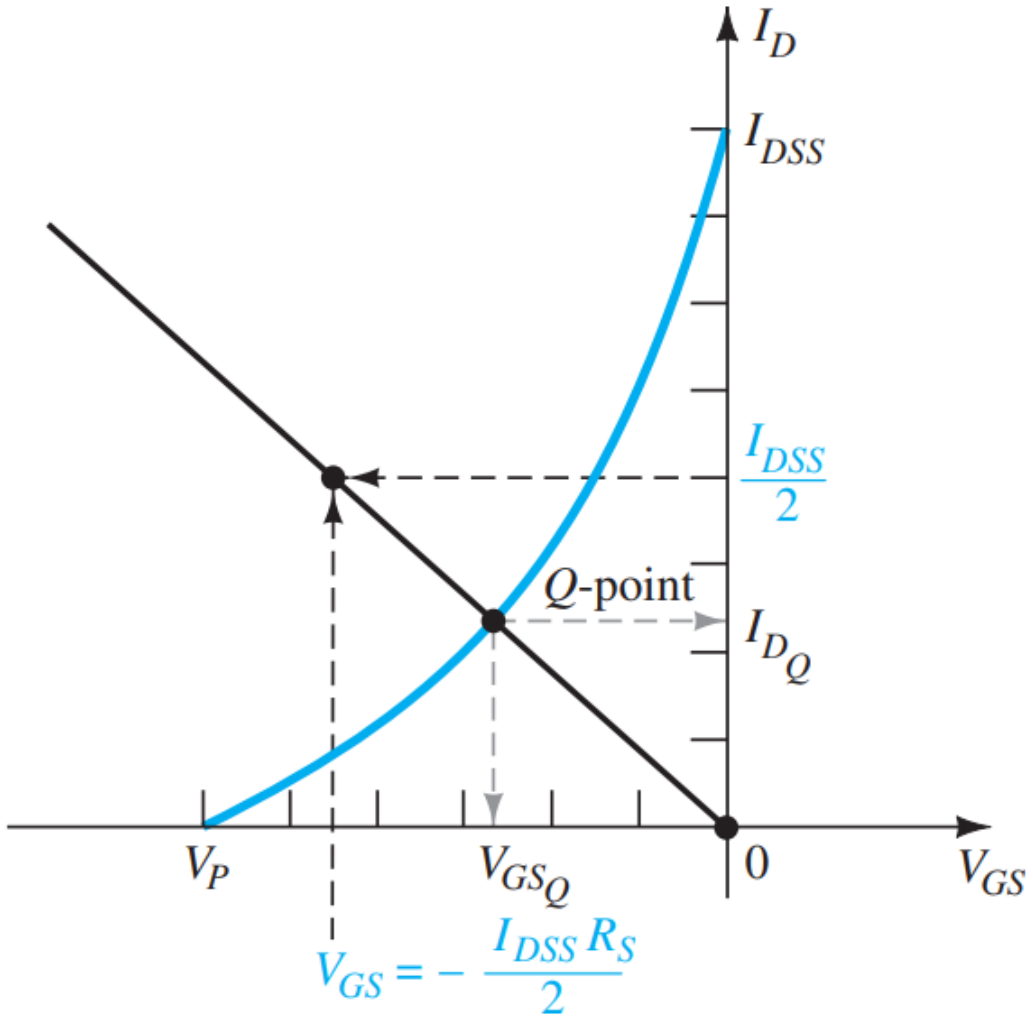
EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

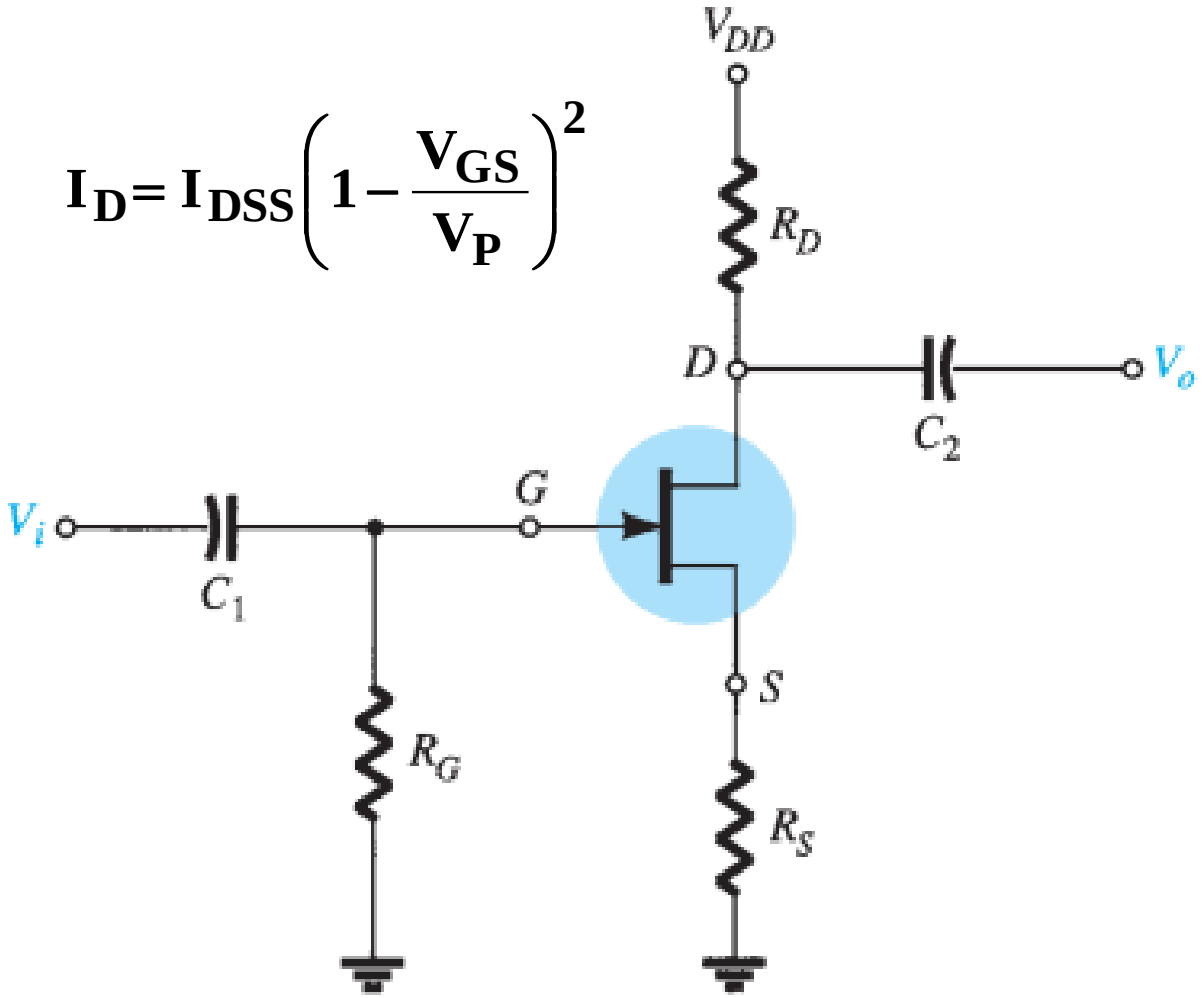


4.3 JFET Biasing

Self bias Configuration



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

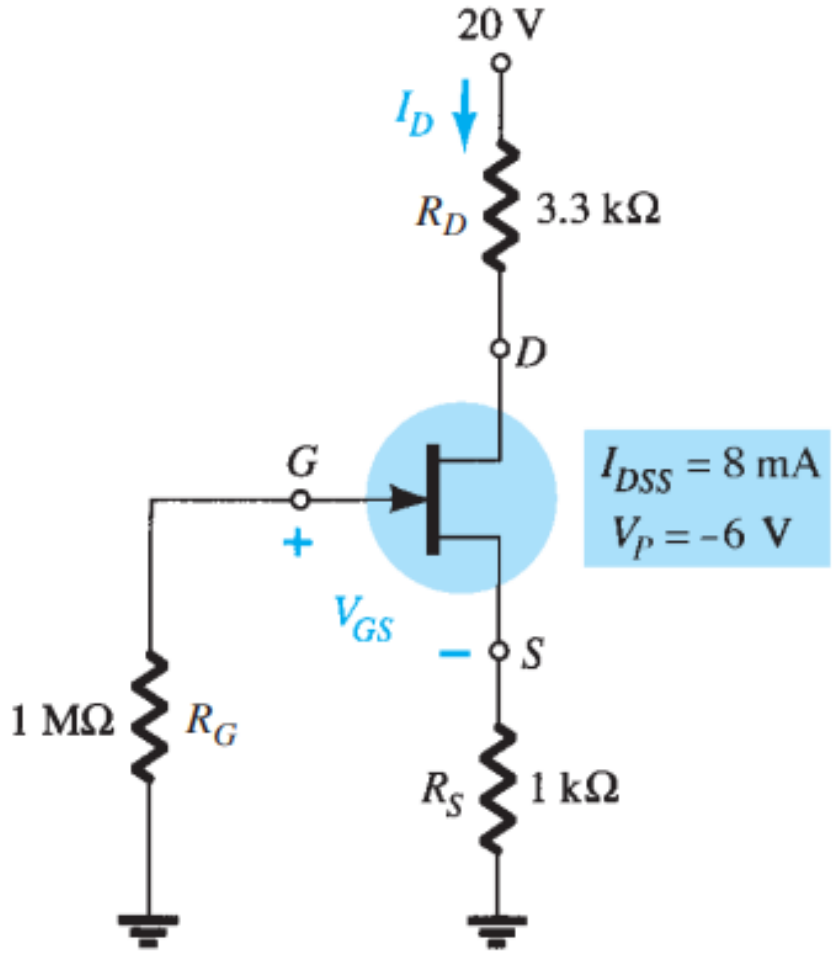


4.3 JFET Biasing

Self bias Configuration

EXAMPLE 7.2 Determine the following for the network of Fig. 7.12:

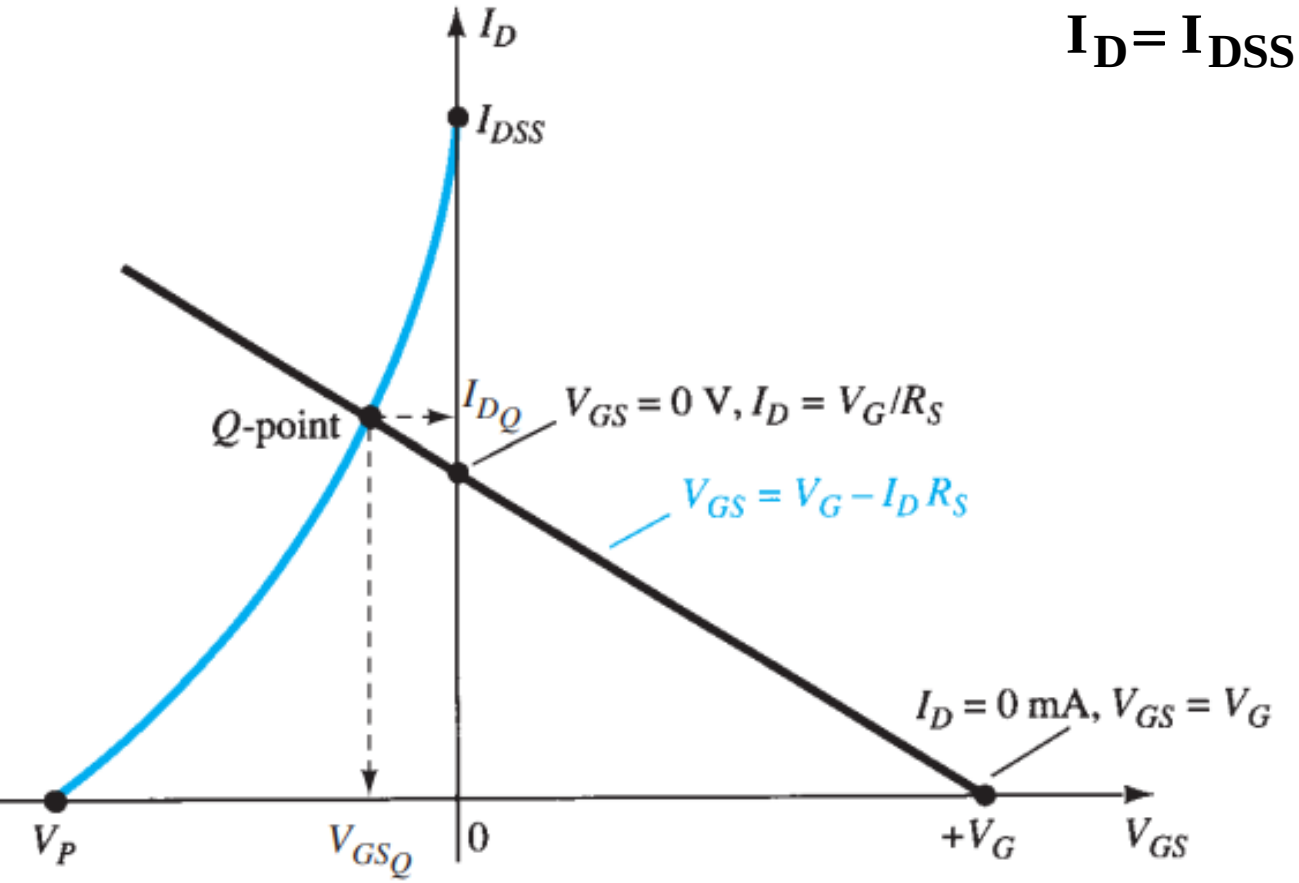
a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

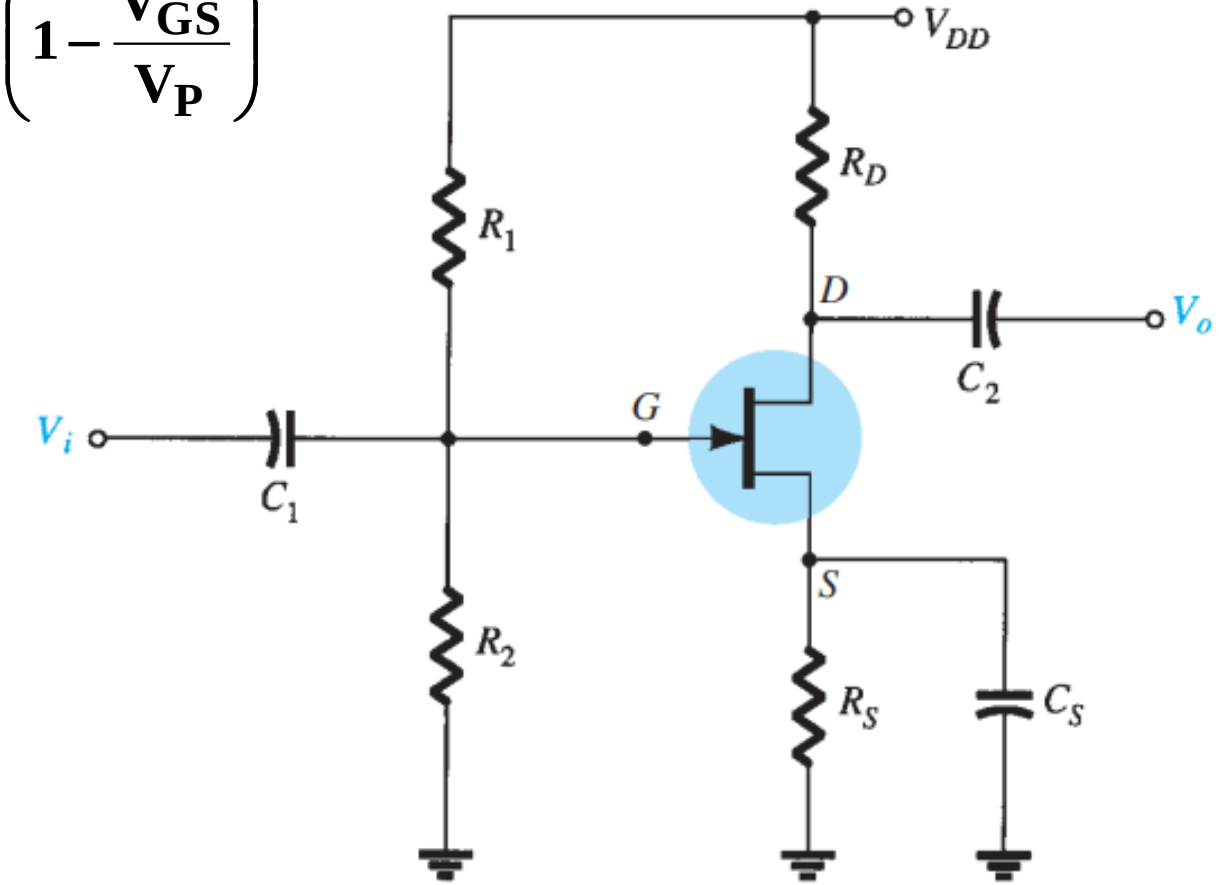


4.3 JFET Biasing

Voltage divider Configuration

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$





4.2 JFET Construction

MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.

There are two types of MOSFETs:

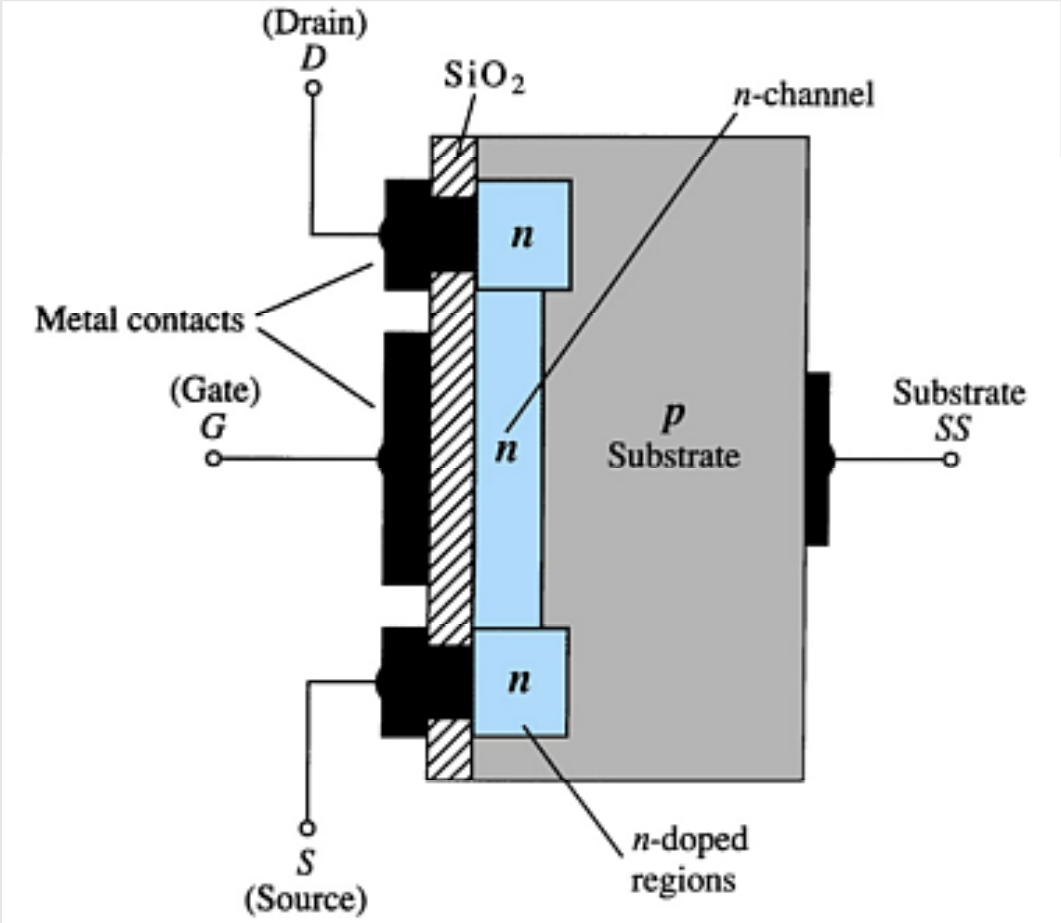
- Depletion-Type
- Enhancement-Type

4.2 JFET Construction

Depletion-Type MOSFET Construction

The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of SiO_2.

The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called Substrate (SS).

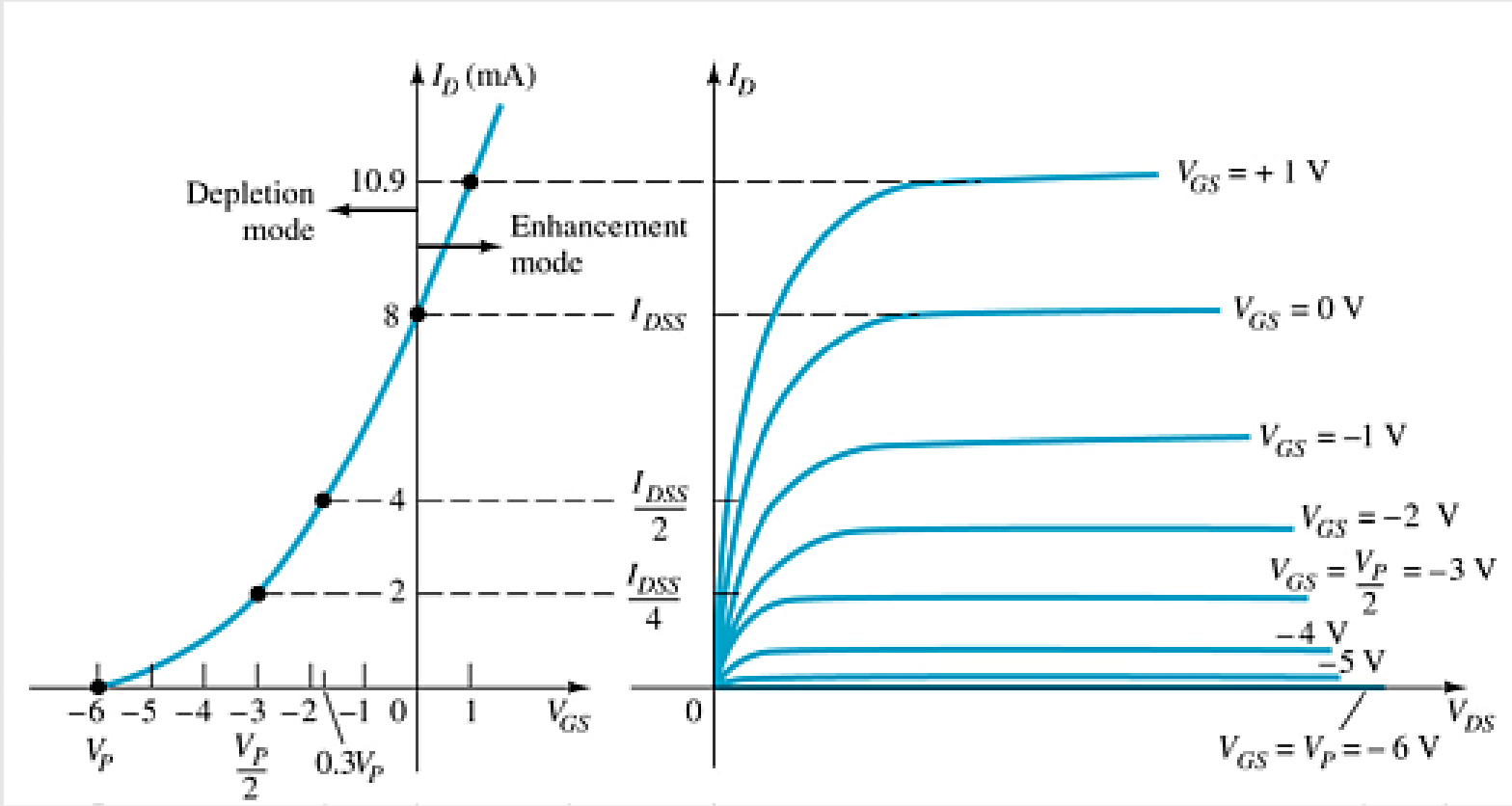


4.2 JFET Construction

Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

- Depletion mode
- Enhancement mode



4.2 JFET Construction

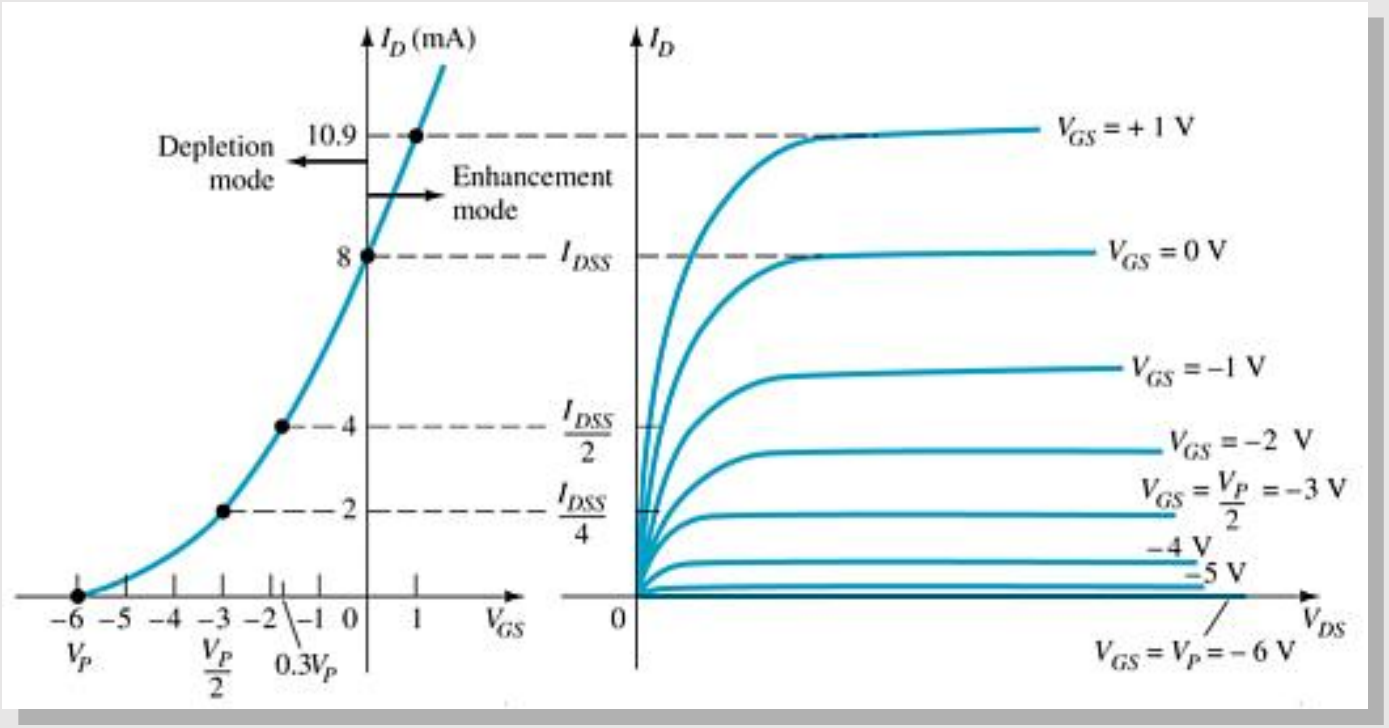
D-Type MOSFET in Depletion Mode

Depletion Mode

The characteristics are similar to a JFET.

- When $V_{GS} = 0$ V, $I_D = I_{DSS}$
- When $V_{GS} < 0$ V, $I_D < I_{DSS}$
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



4.2 JFET Construction

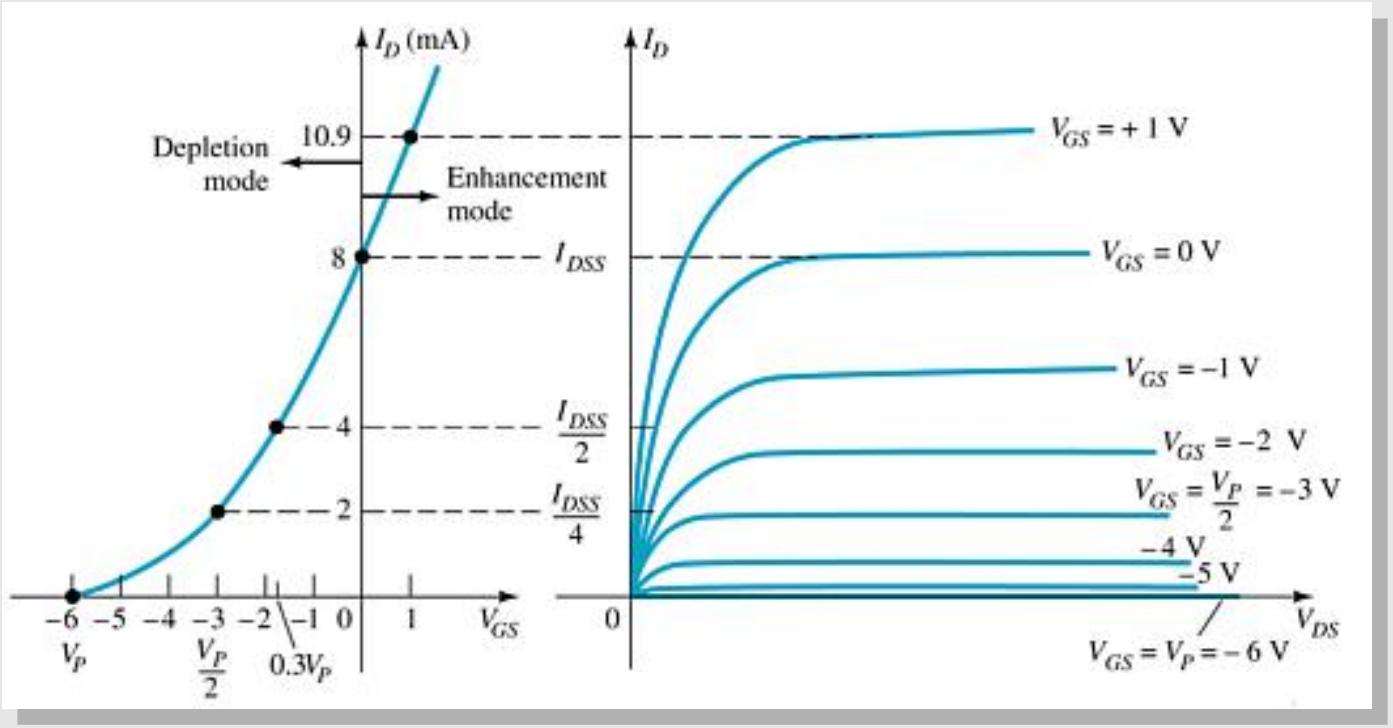
D-Type MOSFET in Enhancement Mode

Enhancement Mode

- $V_{GS} > 0$ V
- I_D increases above I_{DSS}
- The formula used to plot the transfer curve still applies:

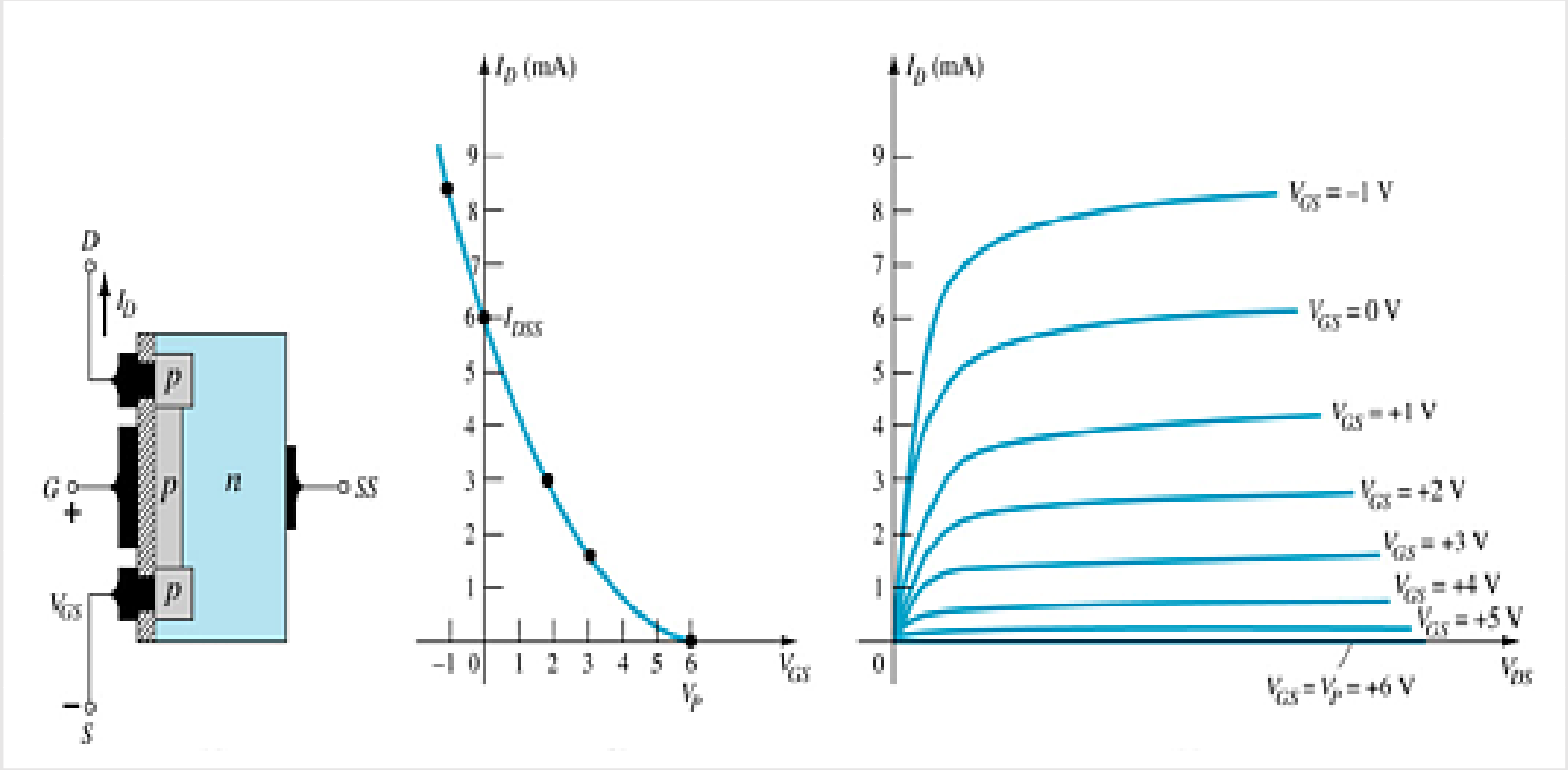
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Note that V_{GS} is now a positive polarity



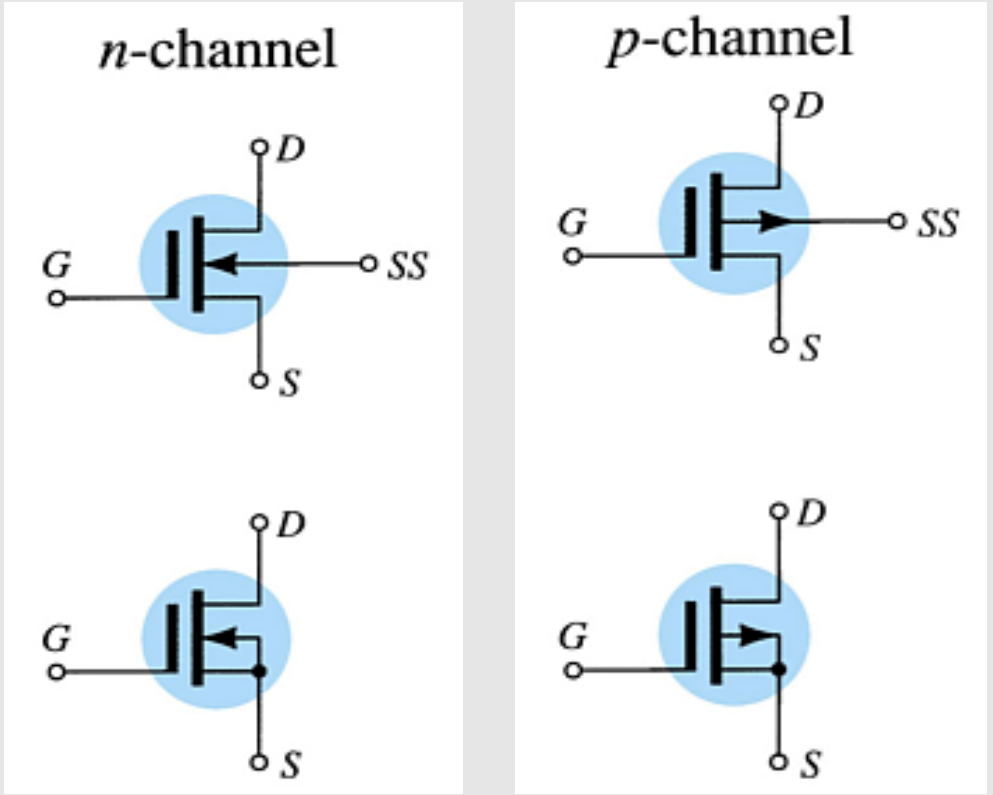
4.2 JFET Construction

p-Channel D-Type MOSFET



4.2 JFET Construction

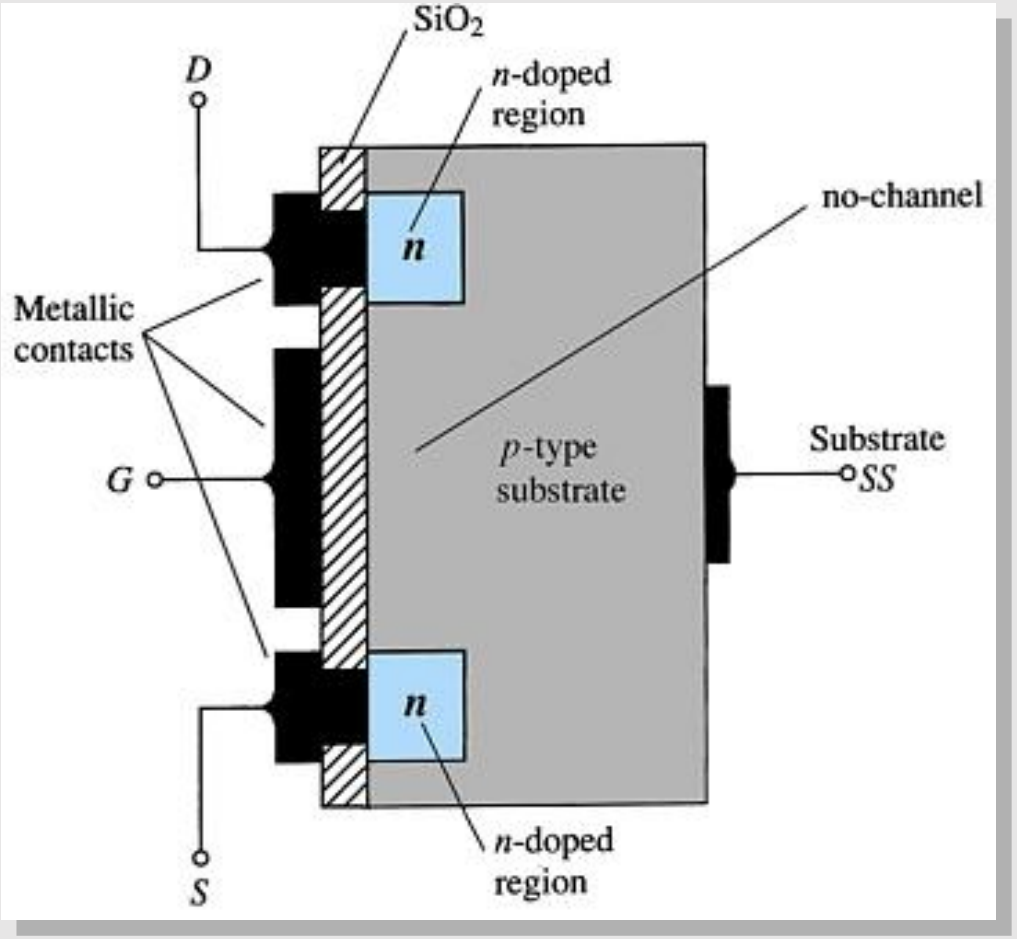
D-Type MOSFET Symbols



4.2 JFET Construction

E-Type MOSFET Construction

- The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel
- The Gate (G) connects to the *p*-doped substrate via a thin insulating layer of SiO_2
- There is no channel
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the Substrate (SS)

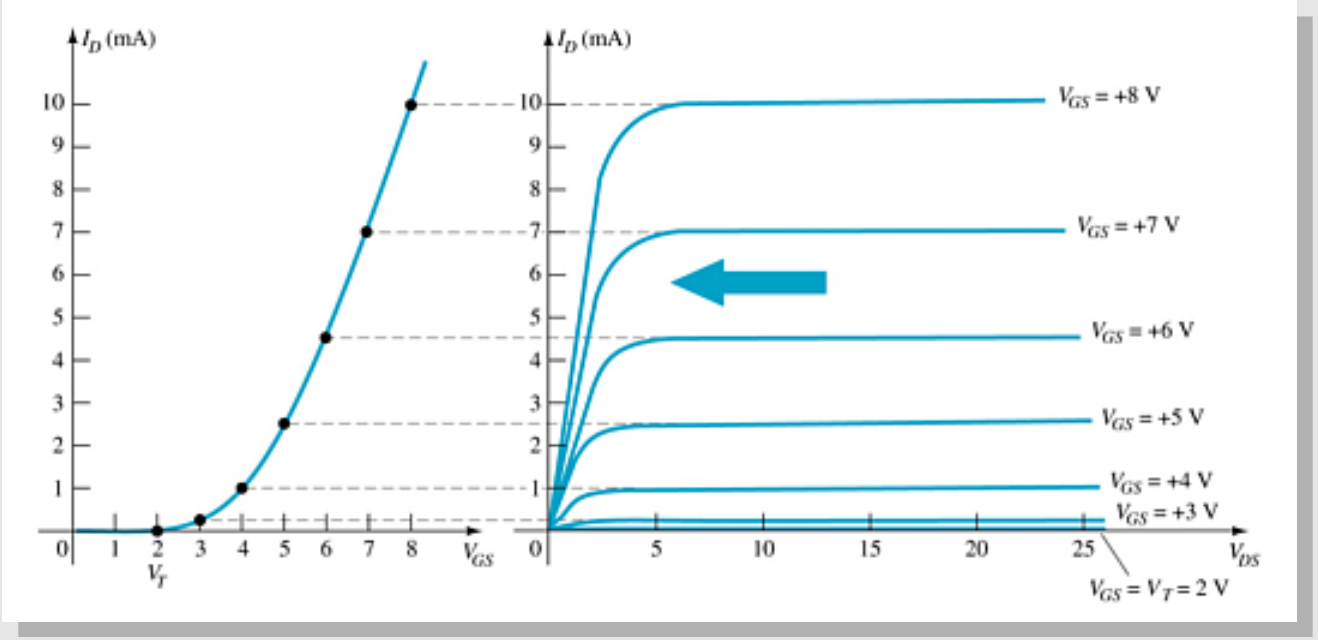


4.2 JFET Construction

Basic Operation of the E-Type MOSFET

The enhancement-type MOSFET operates only in the enhancement mode.

- V_{GS} is always positive
- As V_{GS} increases, I_D increases
- As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level, V_{DSsat} is reached



4.2 JFET Construction

E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

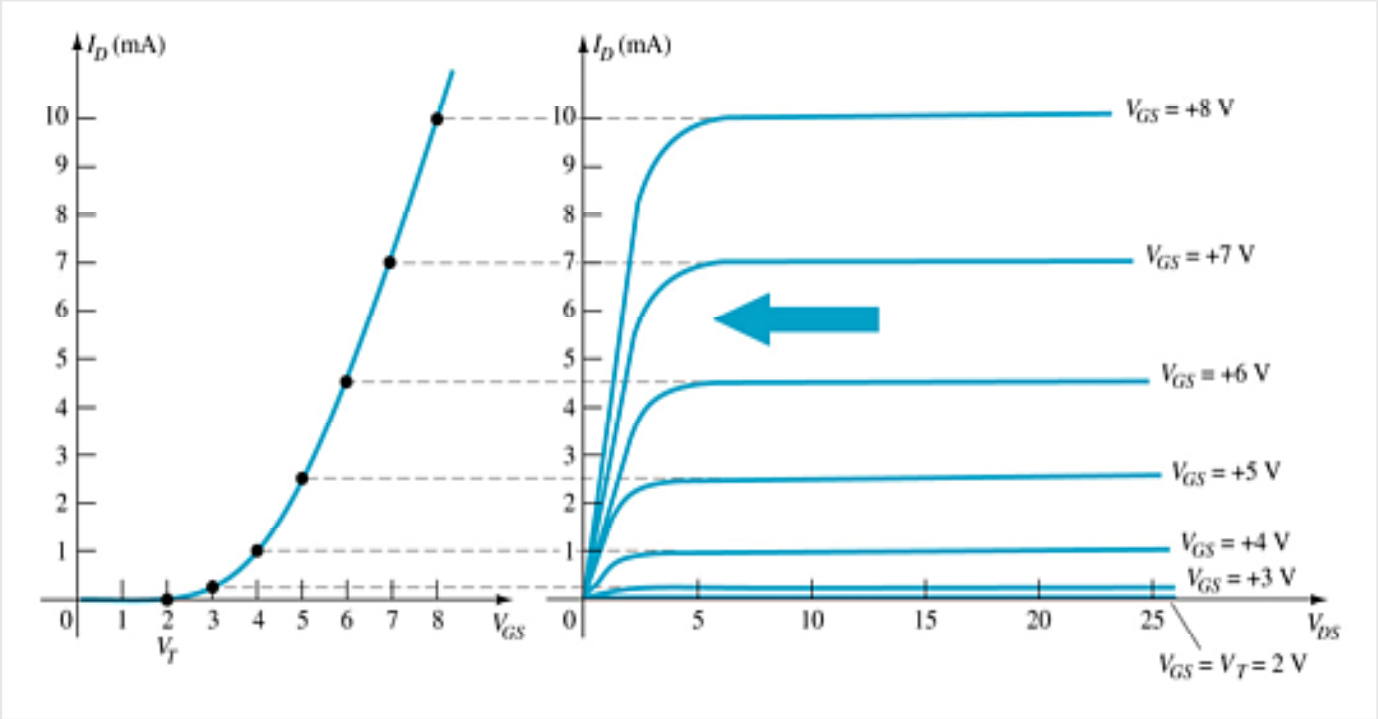
$$\mathbf{I_D = k(V_{GS} - V_T)^2}$$

Where:

V_T = threshold voltage or voltage at which the MOSFET turns on

k, a constant, can be determined by using values at a specific point and the formula:

$$\mathbf{k = \frac{I_{D(ON)}}{(V_{GS(ON)} - VT)^2}}$$

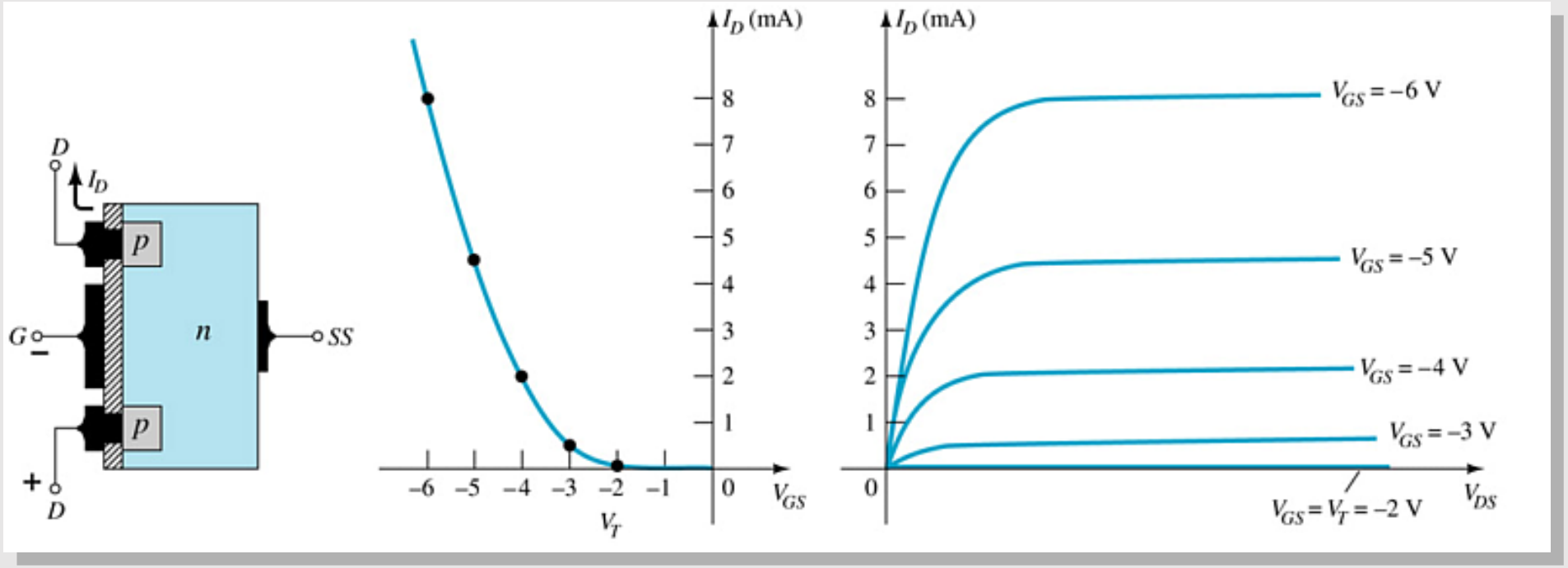


V_{DSsat} can be calculated by:

$$\mathbf{V_{Dsat} = V_{GS} - V_T}$$

4.2 JFET Construction

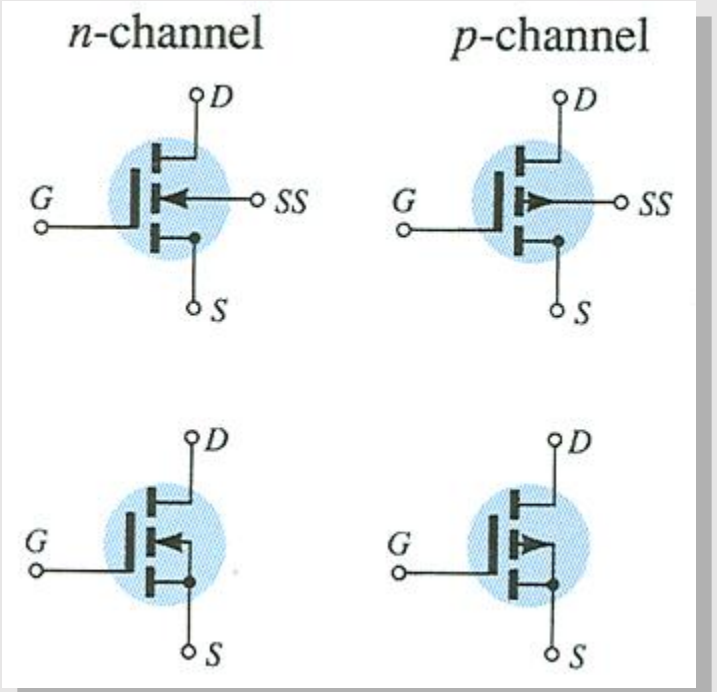
p-Channel E-Type MOSFETs



The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

4.2 JFET Construction

MOSFET Symbols



4.2 JFET Construction

Summary Table