VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of the UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE ENGIEERING AND INFORMATION SYSTEMS

BITE301L - COMPUTER ARCHITECTURE AND ORGANIZATION

PRACTICE SHEET – 1

1. Write the assembly language code for evaluating the following using assembly notations. Assume memory locations for storing the instructions and the data values.
    a. F = A+B/C
    b. F=XYZ * X/Z
    c. F = E+F/G*A-B
    d. A=A+B*C+D/E
2. Identify the addressing modes and the effective address for the following if PC is 300, Index register is 500, Base register is 400, R1 is 250 and the instruction is stored is 300 and the operands are stored in 301 and 302.
    a. MOV R1, (R2)
    b. MOV R1, 30(R2)
    c. MOV R1, R2
    d. MOV (BR), R2
    e. MOV (BR+IR), R2
    f. MOV R2, #500
    g. MOV R1, (1000)
    h. JMP 2000
3. Compute Memory Traffic, total memory for encoding and storing code for 3,2,1,0 address machines that implements the following expression evaluations. Assume that the opcode occupies one byte, addresses occupy three bytes, data values also occupy two bytes and 1 byte word length.
    a. F=X*Y*Z/W
    b. F=A/B/C*D
    c. P = A*B*C*20
    d. X=W-Y-Z+13
4. Show step by step multiplication process using Booth Algorithm.
    a. +31 * +30
    b. (-31) * (-30)
    c. (+31) * (-30)
    d. (-31) * (+30)

5. A computer employs RAM chips of 128 * 4 and ROM chips of 128 * 8. Design the memory system with memory mapped I/O which needs 512 * 16 of RAM, 512 * 16 of ROM.
6. A computer employs RAM chips of 128 * 16 and ROM chips of 128 * 8. Design the memory system with memory mapped I/O which needs 512 * 16 of RAM, 1024 * 16 of ROM.
7. Design the following set of instructions using a 5 stage instruction pipeline. If any hazards occur, identify those hazards and redesign the pipeline for rectifying each hazard. Assume that for 1 instruction, it takes 20 ns and there is no latency delay.
    a. MOV R2, R4
       MUL R4, R5, R6
       SUB R7, R8, R9
       STORE R9, (A)

    b. ADC R1,R3
       MUL R4,R5,R6
       SUB R6,R7,R8
       MOV R8, (B)

8. Design the following set of instructions using a 4 stage instruction pipeline. If any hazards occur, identify those hazards and redesign the pipeline for rectifying each hazard. Assume that for 1 instruction, it takes 10 ns and there is a latency delay of 1 ns. Also consider that for fetching it takes 3ns, decoding as 2 ns, execution as 3 ns and write back to be 2 ns.

    a. MOV R2, R4
       MUL R4, R5, R6
       SUB R7, R8, R9
       STORE R9, (A)

    b. ADC R1,R3
       MUL R4,R5,R6
       SUB R6,R7,R8
       MOV R8, (B)