VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SLOT: C2+TC2

School of Computer Science Engineering and Information Systems
Winter Semester 2023-2024
Continuous Assessment Test – II

Programme Name & Branch : B.Tech. (IT)
Course Name & code : BITE301L & Computer Architecture and Organization
Class Number (s) : VL2023240503717, VL2023240503759, VL2023240503768
Faculty Name (s) : Dr.Meenatchi S, Dr.Praveen kumar Reddy, Dr.Balasubramani M
Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Q.No.	Question	Max Marks	CO	BL
1.	A computer employs RAM chips of 512 x 8 and ROM chips of 1024 x 8. The computer system needs 1024x16 of RAM, 1024 x 16 of ROM and two interface units with 256 registers each. a) Calculate the design parameters. [3 marks] b) Design a memory-address map for the above system. Give the address range in hexa-decimal. [3 marks] c) Show the chip layout for the above design. [4 marks]	10	CO4	BL3
2.	You have been asked to design a cache with the following properties: • Size of Data words is 32 bits • A cache block will contain 2048 bits of data • The cache is direct mapped • The address supplied from the CPU is 32 bits long • There are 2048 blocks in the cache. a) Show the physical address format. [3 marks] b) Represent the number of bits in offset, index and tag, if we make our cache 2-way set-associative instead of direct mapped. [3 marks] c) Represent the number of bits in offset, index and tag, if we make our cache 4-way set-associative instead of direct mapped. [4 marks]	10	CO4	BL4
3.	(i) Consider a system with 8-bit addresses and 16-byte pages. A process in this system has 4 logical pages, which are mapped to 3 physical frames in the following manner: logical page 0 maps to physical frame 2, page 1 maps to frame 0, page 2 maps to frame 1, and page 3 is not mapped to any physical frame. The process may not use more than 3 physical frames. On a page fault, the demand paging system uses the LRU policy to evict a page. The MMU has a TLB cache that can store 2 entries. The TLB cache also uses the Optimal policy to store the most recently used mappings in cache. Now, the process accesses the following logical addresses in	5	CO4	BL4

	order: 7, 17, 37, 20, 40, 60. a) Indicate whether the above accesses would result in a page fault. Assume that the TLB cache is empty before the access begin. [3 marks] b) Give the page number associated with the memory access that leads to page fault. [1 mark] c) Which page under LRU would be replaced with the page which caused the page fault? [1 mark] (ii) Represent -13.275_{10} and 12.48_{10} in double precision IEEE-754 format.	5		
4.	A computer program involves multiplying two signed numbers (stored as 8 bit) -21 and +17. Illustrate how this operation would be handled by Booth's algorithm.	10	CO3	BL3
5.	Perform division operation on the operands: dividend = -27 and divisor = + 22 using restoring division algorithm. Show the contents of the quotient and remainder registers during the operations.	10	CO3	BL3

NOTE*: Please refer below to the BL – Bloom's Taxonomy Levels and mention the respective level in the questions.

Bloom's Taxonomy Levels	**Category**
BL1	Remembering
BL2	Understanding
BL3	Applying
BL4	Analyzing
BL5	Evaluating
BL6	Creating