VIT
Vellore Institute of Technology

Slot: C1+TC1

School of Computer Science Engineering and Information Systems

Winter Semester 2023-2024

Continuous Assessment Test – I

Programme Name & Branch: B. Tech. IT
Course Name & code : Computer Architecture and Organization BITE301L
Class Number (s) : VL2023240506486, VL2023240503712, VL2023240503765
Faculty Name (s) : Dr. SwarnaPriya R M, Dr. Meenatchi S, Dr. Balasubramani M
Exam Duration : 90 Min. Maximum Marks: 50

Answer all the Questions: (5 * 10 = 50 Marks)

1. (a) The number $(934)_{10}$ has to be stored in a computer's memory which has a word length of 32 bits starting from byte address 0x300. Assume that the system is byte-addressable. Show how the given integer would be stored in memory. **(5 Marks)**

Address	Big-Endian		Little-Endian	
	Binary	Hex Pattern	Binary	Hex Pattern
0x300				
0x301				
. . .				

(b) Suppose the memory of a computer is as follows (address 100 contains the hex value CA, etc.). Assume also that these four byte memory locations hold one 32 bit integer. What integer value is this on a little-endian machine? Show the steps and interpretations. **(5 Marks)**

Address 100	Address 101	Address 102	Address 103
CA	FE	BA	BE

2. Consider the following data given. Analyze the instructions and specify the addressing mode, calculate the effective address of the memory operand and the value in accumulator in each of the following instructions.

Memory Address	Value
100:	LOAD
101:	Operand
150:	323
200:	340
260:	333

299:	490
300:	550
350:	700
360:	776
560:	800

R1 : 200
R2: 300

(i) LOAD #1000
(ii) LOAD 150(R1)
(iii) LOAD (R2)
(iv) LOAD –(R2)
(v) LOAD 60(R2,R1)

3. Write an Assembly language program for the following expressions using assembly notations.

A=(B-C)*D

Consider that the data values are stored in memory location starting from 600 onwards and the program is stored from memory location 200 onwards. Assume that B is 5, C is 2 and D is 5. Store one instruction in one memory location. Assume that one location store one instruction.

Represent the memory as follows:

MEMORY:
200.
201.
202.
.
.
.
600.
601.
602.

Interpret the flow of execution in a typical Computer for the above code using the following representation step by step.

PC	
MAR	
MDR	
IR	
Any register in processor	

4. Compute the memory traffic, total memory for encoding and storing code that implements the expression evaluation A= (B-C)*(G/D). Assume that opcode occupy two byte, address occupies four bytes, and 2 byte word length for 0,1,2,3 address machines. Give proper justifications wherever required. (Use the template for writing the code)

3-addr	2-addr	1-addr	0-addr

Template: (Follow for all types)

3-addr Instruction

Instruction	Memory to Store	Memory to Encode	M/A's to Fetch	M/A's to Execute	Total Memory Traffic
ADD ...					
				Total	

After computation for each case, give the comparison in the following template.

Instruction Type	Memory To Store in Bytes	Memory to Encode in Bytes	MAT to fetch an Instruction	MAT to Execute an Instruction	Memory Traffic
3-addr					
2-addr....					

5. (a) Consider that you have designed a system which has totally 10 locations in main memory and 5 locations in cache. Calculate the hit and miss rate for the given scenario. **(5 Marks)**

Cache Memory

{1} 23
{9} 56
{6} 78
{5} 34
{4} 87

Main Memory

Memory Address	Value
1	23
2	45
3	67
4	87
5	34
6	78
7	89
8	34
9	56
10	58

The contents of main memory are as given above. The contents in the cache when the execution starts are also given above where {1} specifies the memory location from where the data is moved inside the cache. Assume that if a data is not found in the cache, it must first be fetched from the main memory to the cache and then fetched from the cache to be executed. The 10 read access request for data are as follows. Assume that when the cache is full, the data which was inserted very first is replaced that is FIFO. The first data inserted is in the top, and the next immediate location is the second, etc.....

1. Data from memory address 1
2. Data from memory address 9

3. Data from memory address 6
4. Data from memory address 5
5. Data from memory address 4
6. Data from memory address 1
7. Data from memory address 7
8. Data from memory address 8
9. Data from memory address 9
10. Data from memory address 3

(b) Consider the bit patterns shown below. Interpret them based on Sign-magnitude representation, 1's complement representation and 2's complement representation. Provide their value as decimal numbers. **(3 Marks)**

(i) 1111 1111 0000 1010
(ii) 0111 1111 1101 1111

Consider that the system is following a 2's complement representation and a 5 bit representation. Perform 2's complement addition on the following decimal pair using this system. Also interpret the result. (-10) and (-13) **(2 Marks)**