Vellore Institute of Technology
(Deemed to be University under section 3 of the UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE ENGIEERING AND INFORMATION SYSTEMS

BITE301L - COMPUTER ARCHITECTURE AND ORGANIZATION

PRACTICE SHEET – 2

1. Show step by step division process using Restoring Division Algorithm
    a. (+15)/(+3)
    b. (+12)/(+3)
    c. (-22)/(+5)
    d. (-42)/(+3)
    e. (-50)/(+5)
2. Show step by step division process using Non-Restoring Division Algorithm
    a. (+12)/(+10)
    b. (+52)/(+3)
    c. (+50)/(+11)
    d. (+63)/(+4)
3. Perform 2's complement Addition or Subtraction
    a. (+12) + (+21)
    b. (-12) + (-21)
    c. (-12) + (+21)
    d. (+12) + (-21)
    e. (+12) – (+21)
    f. (-12) - (-21)
    g. (-12) - (+21)
    h. (+12) - (-21)
4. Represent the following in sign magnitude, 1's complement and 2's complement representation
    a. -16
    b. -35
    c. +34
    d. +87
5. Represent the following in Big-Endian and Little-Indian format using Hex pattern . Consider that the machine is a 32-bit and the values are stored in memory address starting from 1000.
    a. "COLLEGE"
    b. "Hello"
    c. $(124)_{10}$

d. $(12AB)_{16}$

6. A block-set associative cache memory consists of 128 blocks divided into two block sets . The main memory consists of 16,384 blocks and each block contains 256 eight bit words.
   a. How many bits are required for addressing the main memory?
   b. How many bits are needed to represent the TAG, SET and WORD fields?
7. A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____.