ITEX 111 Digital Logic

Course Title**: Digital Logic** **Course Code:** ITEX 111

Semester: II

Credit Hours: 3 (2+1)

Nature of the course: T/P

2. Course Description and Goals

The course covers the basics of digital logic, its implementation and applications. The course includes the fundamental concepts of Boolean algebra, its implementation through Logic Gates, its application for circuit analysis, flip-lops, counters logic devices and synchronous and asynchronous sequential logic circuit and more. The main objective of this course is to introduce the learners with the basic ideas about digital design, its components and implementation.

2. Learning Outcomes

On completion of this course, the students will be able to:

e) understand the basics and principles of digital circuitry
f) identify and understand various digital components and hardware in circuit design
g) explain the implementation and functions of various components like registers, flip flops, counters
h) explore the design and development of other complex circuits by self-study

3. Content with specific objectives

Specific objectives	Contents
6. Explain the basic difference between digital and analog quantities 7. Show how voltage levels are used to represent digital quantities 8. Understand various parameters of a pulse waveform like rise time, fall time, pulse width, frequency, period, duty cycle 9. Understand number system concepts, use and conversion	**Unit One: Introduction (6 hrs.)** 1. Digital Signals, Digital Waveforms 2. Digital Logic, Digital Operations 3. Digital IC, Computers 4. Clock Waveforms 5. Number Systems and conversions 6. Binary arithmetic **7.** Different types of Coding (ASCII, BCD, Gray code, Excess 3 Code)

10. determine 1's and 2's complement of a binary number 11. apply arithmetic operations to binary numbers 12. Understand various coding ideas	
1. Explain the basic logic functions of NOT, OR and AND 2. Describe several types of logic operations and algebra 3. Understand Universal gates and special gates 4. Realize the universal gates as the basic gates 5. state and prove de-Morgan's theorem 6. define canonical and standard form of Boolean expression 7. Understand and convert SOP to POS and vice-versa 8. Simplify the Boolean expressions using K-map method for both SOP and SOP form and including Don’t Care conditions 9.	**Unit Two: Logic Gates (5 hrs.)** 12. Basic Gates: NOT, OR, AND 13. Universal Gates: NOR, NAND 14. Special Gates: XOR, XNOR 15. Realization of other Gates from Universal Gates 16. Boolean Algebra 17. K Map, SOP, POS, Don’t Care Conditions
1. Explain combinational circuits with their features 2. implement digital logic for half adder, full adder, half subtractor, full subtractor with their functional expressions,	**Unit Three: Combinational Logic Design (10 hrs.)** 1. Multiplexer, Demultiplexer 2. Encoder, Decoder 3. Half Adder, Full Adder 4. Parity Generator, Checker **5.** Concept of ROM, PROM, EPROM, PLA, PAL

logic diagram and truth tables and timing diagram 3. explain the concept of encoder and decoders 4. design a logic circuit to decode any combination of bits 5. Use BCT to 7 segment decoder in display systems 6. Describe decimal to binary priority encoder, 7. implement 4-bit parallel adder 8. explain functioning of 9-bit parity generator and checker 9. Explain the concept of programming logic with reference to PROM, EPROM, PAL and PLA with circuit and tables	
1. Differentiate between latch and flip-flop 2. Differentiate between level triggering and edge triggering with their features 3. Explain RS, JK, JK master-slave, D&T flip-flops with their logic diagram, graphical symbol, characteristics table, excitation table 4. How SISO, SIPO, PISO and PIPO shift registers operate 5. Explain ripple counter with circuit, state, and timing diagram	**Unit Four: Counter and Registers (13 hrs)** 1. Flip flops: RS, JK, JK master-slave, D & T flip flops (level trigger, edge trigger, excitation table) 2. Synchronous and Asynchronous Counters 3. Ripple Counter 4. Ring Counter 5. Modulus Counter 6. Decade Counter 7. A digital Clock 8. Types of Registers 9. Serial in Parallel Out 10. Serial in Serial Out 11. Parallel in Parallel Out 12. Parallel in Series Out 13. Shift Registers

6. explain ring counter with circuit, state, and timing diagram 7. Explain modulus counter with circuit and state diagram	
1. define finite state machine with examples 2. explain Mealy and Moore models of finite state machines 3. describe state, state diagram and state table of sequential circuit 4. understand and describe the design procedure of sequential machines 5. use the flip flops to realize the synchronous machines 6. understand the basics of asynchronous sequential circuits	**Unit Five: Sequential Circuits and design (7 hrs.)** 1. Concept of state, state diagram 2. Transition Tables, redundant states 3. Using flip flops to realize the synchronous models **4.** Asynchronous Sequential Circuits concepts and design
1. to understand the basic working of a processor 2. describe the functions and working of ALU 3. to describe bus architecture 4. to design a basic ALU using logic gates and simple components.	**Unit Six: Introduction to ALU Design (4 hrs.)** 1. CPU overview 2. ALU 3. Bus architecture **4.** Designing a basic ALU

18. Major Teaching and Learning Strategy

The facilitator and the learners will both develop their level of understanding and information about the subject matter. The digital design components should be explored as practically as possible. Learners need to be more enthusiastic to learn the theories and participate in its implementation to design digital circuits to their best knowledge. Group discussions and participation in group is recommended mostly for depth understanding of the subject matter. Facilitator is responsible for developing classroom materials required for teaching-learning process, use of multimedia is recommended as visuals/images would prove more fruitful for student involvements.

19. Assessment Plan

a. In-semester

b. End-semester

20. References

a. Brain Holdsworth, “Digital Logic Design”, Elsevier Science, Latest Edition

b. M. Morris Mano, “Digital Logic & Computer Design”

c. Donald P. Leach, Albert Paul Malvino and Goutam Saha, “Digital Principles and Applications” Tata McGraw-Hill