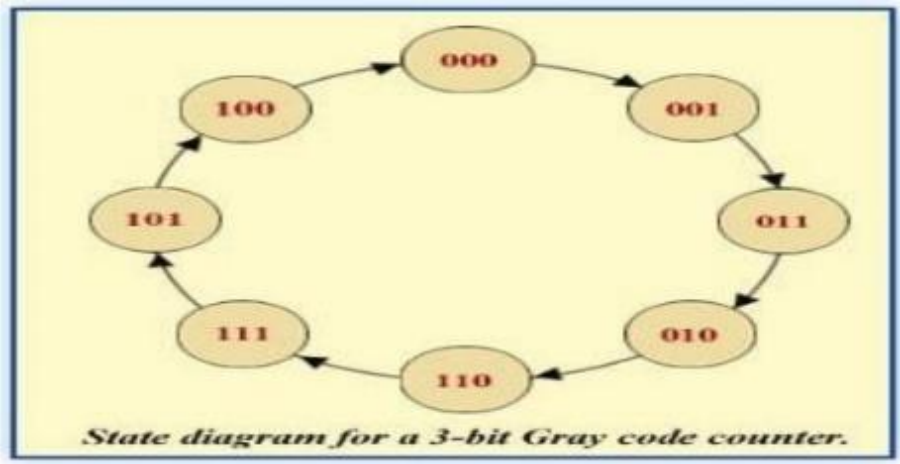
CS 220 ASSIGNMENT 4

1. **State Assignment Table:**

Sr. No.	*State Name*	*State*
1.	S_0	1'b000
2.	S_1	1'b001
3.	S_2	1'b011
4.	S_3	1'b010
5.	S_4	1'b110
6.	S_5	1'b111
7.	S_6	1'b101
8.	S_7	1'b100

2. **State Diagram:**



State diagram for a 3-bit Gray code counter.

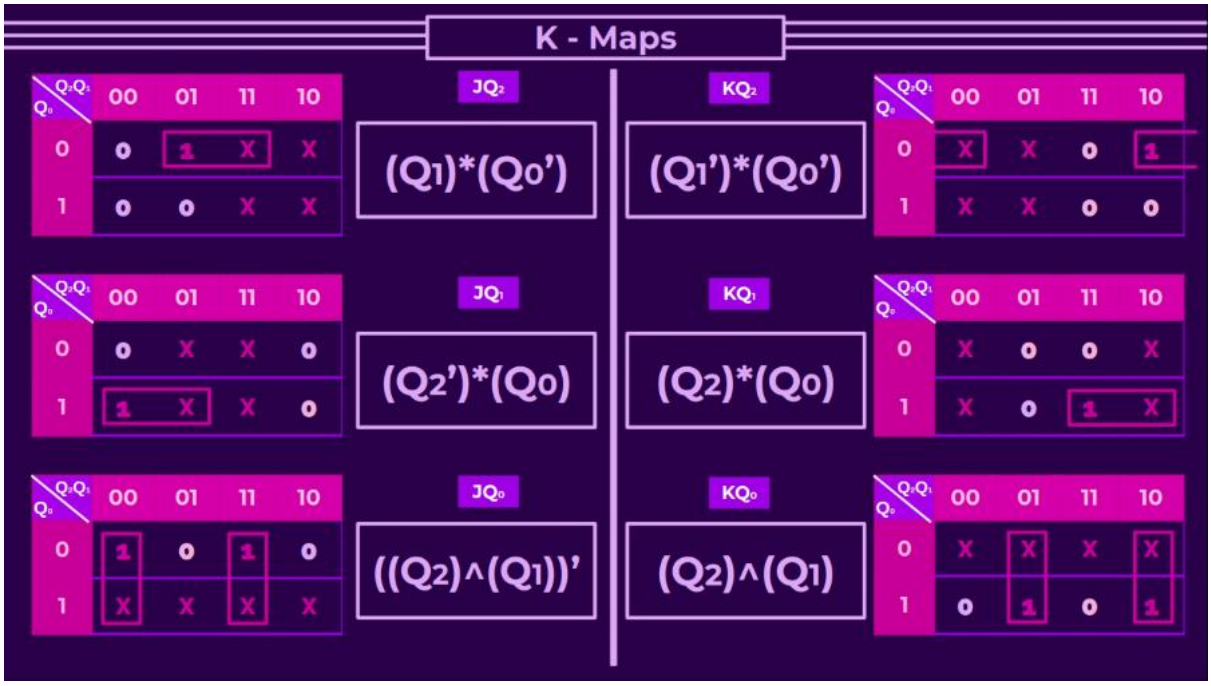
Output is high only when state transits from S_7 to S_0.

Elsewhere output is low.

3. **Karnaugh Maps and logic Equations:**

K-Maps for the Gray code Counter is given below. The circuit consists of 3 J-K Flip-flop and thus the K-Maps corresponds to the 6 J and K values of the three Flip-flops.

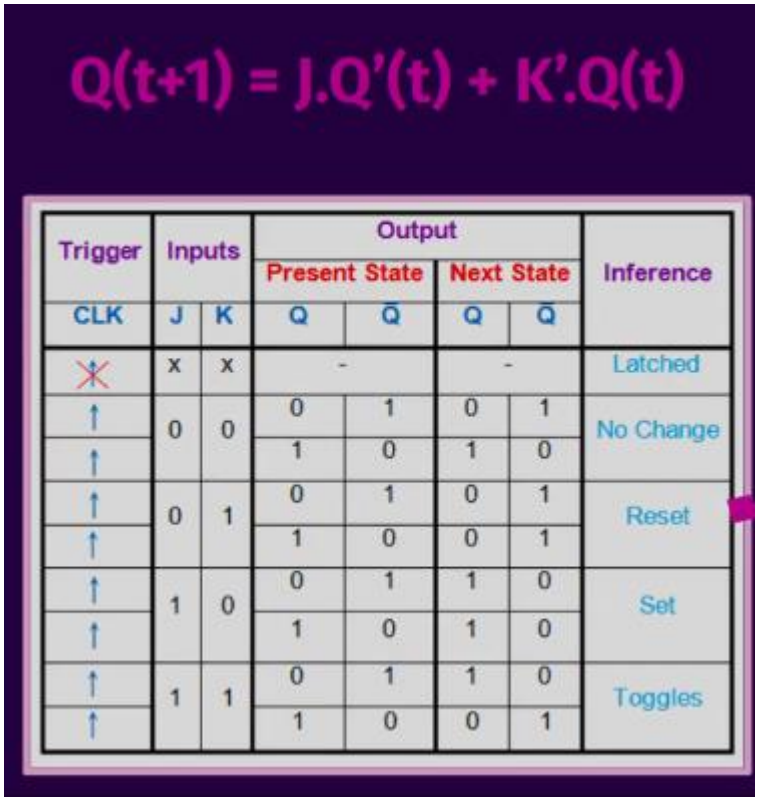
The Logic Equation corresponding to each output is also given below.



Note: Here JQ_2, JQ_1, etc. means J or K outputs of the corresponding Flip-flop 0, 1 or 2.

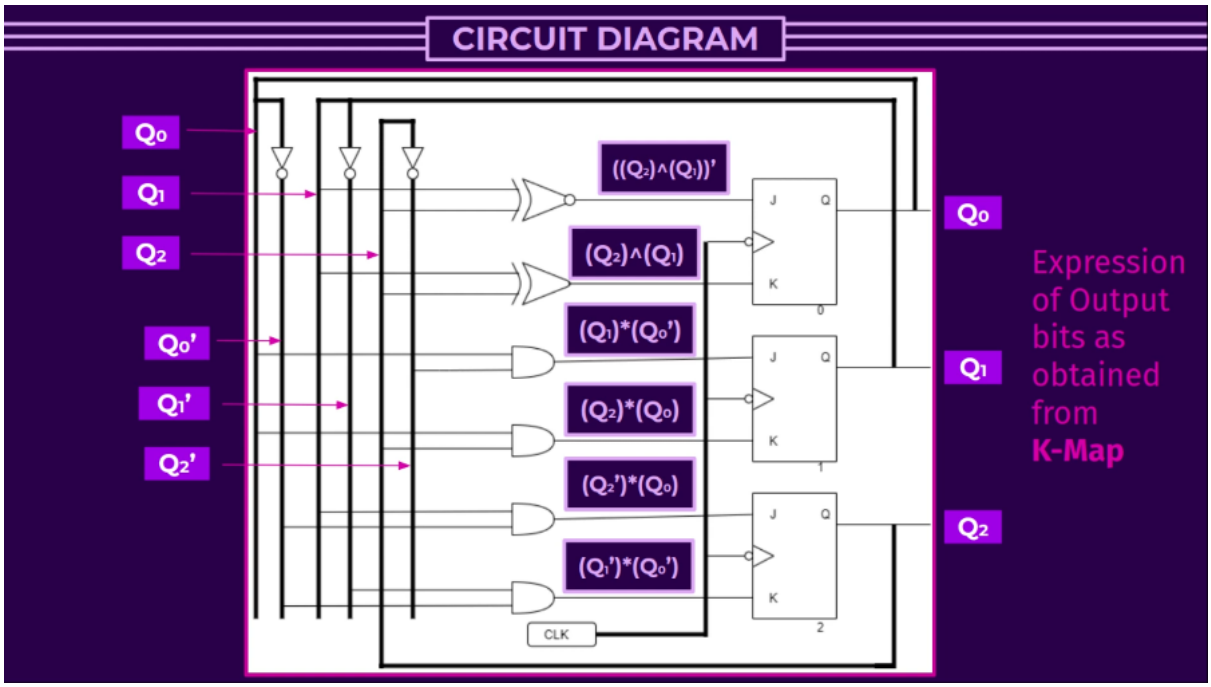
Cross means don't care condition.

4. **J-K Transition Table:**



Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	$\bar{Q}$	Q	$\bar{Q}$	
✕	x	x	-		-		Latched
↑	0	0	0	1	0	1	No Change
↑			1	0	1	0	
↑	0	1	0	1	0	1	Reset
↑			1	0	0	1	
↑	1	0	0	1	1	0	Set
↑			1	0	1	0	
↑	1	1	0	1	1	0	Toggles
↑			1	0	0	1	

5. Circuit Diagram:



6. Output Table:

Sr. No.	Clock	State	Output (z)
1.	High	S_0	0
2.	Low		0
3.	High	S_1	0
4.	Low		0
5.	High	S_2	0
6.	Low		0
7.	High	S_3	0
8.	Low		0
9.	High	S_4	0
10.	Low		0
11.	High	S_5	0
12.	Low		0
13.	High	S_6	0
14.	Low		0
15.	High	S_7	1
16.	Low		0

7. State and Excitation Table:

Current State	Next State	Output
S_0	S_1	0
S_1	S_2	0
S_2	S_3	0
S_3	S_4	0
S_4	S_5	0
S_5	S_6	0
S_6	S_7	0
S_7	S_0	1