COEP TECHNOLOGICAL UNIVERSITY (COEP Tech)

A Unitary Technological University of Government of Maharashtra

(Formerly College of Engineering Pune (COEP))

MID Semester Examination

Programme: B. Tech. **Semester: V**

Course Code: CT-21007 **Course Name: Computer Organization**

Branch: Computer Science & Engineering **Academic Year: 2024-25**

Duration: 1.5 Hrs. **Max Marks: 30**

Date: 25/09/2024 **MIS No.** | | | | | | | | | |

Instructions:

1. Figures to the right indicate the full marks.
2. Mobile phones and programmable calculators are strictly prohibited.
3. Writing anything on question paper is not allowed.
4. Exchange/Sharing of stationery, calculator etc. not allowed.
5. Write your MIS Number on Question Paper. Assume suitable data wherever required.

			Marks	CO	PO
Q 1	A	Our favorite program runs in 10 seconds on computer A, which has a 3 GHz clock. We are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target? $\text{Clock Rate}_B = \frac{\text{Clock Cycles}_B}{\text{CPU Time}_B} = \frac{1.2 \times \text{Clock Cycles}_A}{6s}$ $\text{Clock Cycles}_A = \text{CPU Time}_A \times \text{Clock Rate}_A$ $= 10s \times 2GHz = 20 \times 10^9$ $\text{Clock Rate}_B = \frac{1.2 \times 20 \times 10^9}{6s} = \frac{24 \times 10^9}{6s} = 4GHz$	3	1, 2	1, 2, 3, 4, 9, 12
	B	Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (classes A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2?	3		

Class	P1 @ **2.5 GHz**	P2 @ **3.0 GHz**	**%** of instruction
A	1	2	10
B	2	2	20
C	3	2	50
D	3	2	20

Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time = No. instr. × CPI/clock rate

Total time P1 = $(10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5 \times 10^9) = 10.4 \times 10^{-4}$ s

Total time P2 = $(10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(3 \times 10^9) = 6.66 \times 10^{-4}$ s

CPI(P1) = $10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$

CPI(P2) = $6.66 \times 10^{-4} \times 3 \times 10^9/10^6 = 2.0$

Q 2 A Differentiate between hardwired and micro-programmed ways of control unit design.

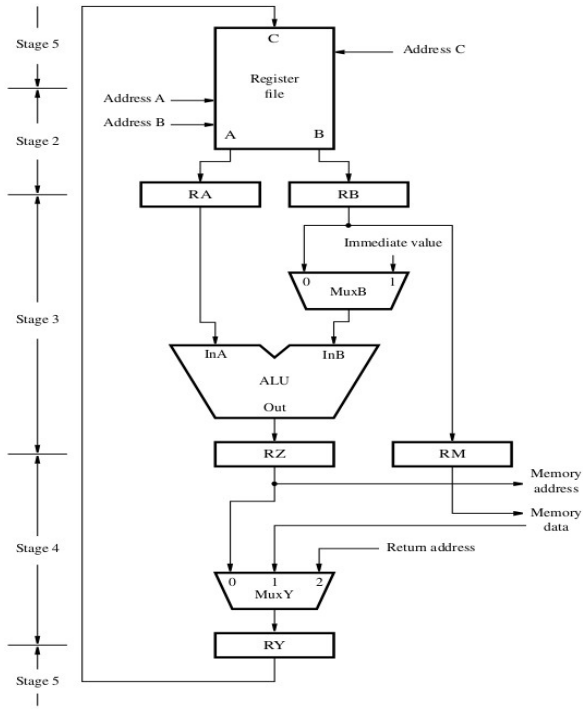
Hardwired Control Unit	Microprogrammed Control Unit
Hardwired control unit generates the control signals needed for the processor using logic circuits	Microprogrammed control unit generates the control signals with the help of micro instructions stored in control memory
Hardwired control unit is faster when compared to microprogrammed control unit as the required control signals are generated with the help of hardwares	This is slower than the other as micro instructions are used for generating signals here
Difficult to modify as the control signals that need to be generated are hard wired	Easy to modify as the modification need to be done only at the instruction level
More costlier as everything has to be realized in terms of logic gates	Less costlier than hardwired control as only micro instructions are used for generating control signals
It cannot handle complex instructions as the circuit design for it becomes complex	It can handle complex instructions
Only limited number of instructions are used due to the hardware implementation	Control signals for many instructions can be generated
Used in computer that makes use of Reduced Instruction Set Computers(RISC)	Used in computer that makes use of Complex Instruction Set Computers(CISC)

3 | 1, 2 | 1, 2, 3, 4, 9, 12

B Discuss the different components required for datapath design.

program counter (PC), instruction and data memories, the register file, the ALU, and adders.

3



Q 3 A Explain the step of actions that are required/ taken to fetch and execute Load, Store and Branch types of instructions.

3 | 1, 2 | 1, 2, 3, 4, 9, 12

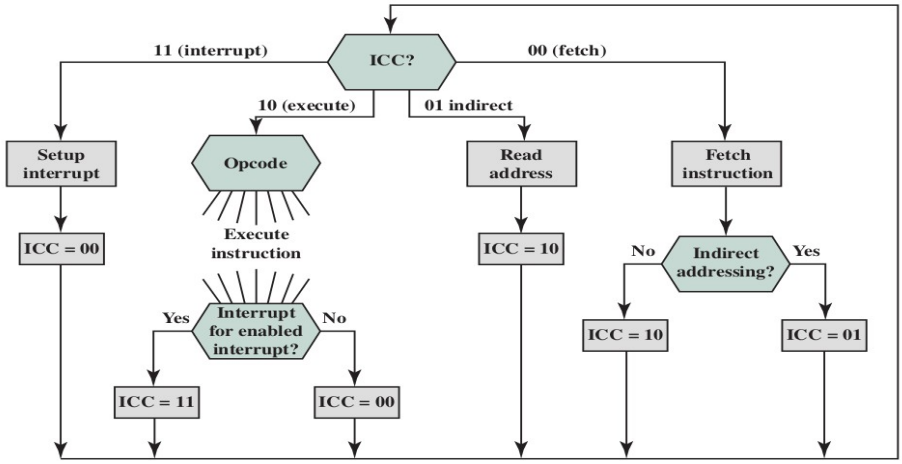
Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R7]
3	RZ ← [RA] + Immediate value X
4	Memory address ← [RZ], Read memory, RY ← Memory data
5	R5 ← [RY]

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R8], RB ← [R6]
3	RZ ← [RA] + Immediate value X, RM ← [RB]
4	Memory address ← [RZ], Memory data ← [RM], Write memory
5	No action

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction
3	PC ← [PC] + Branch offset
4	No action
5	No action

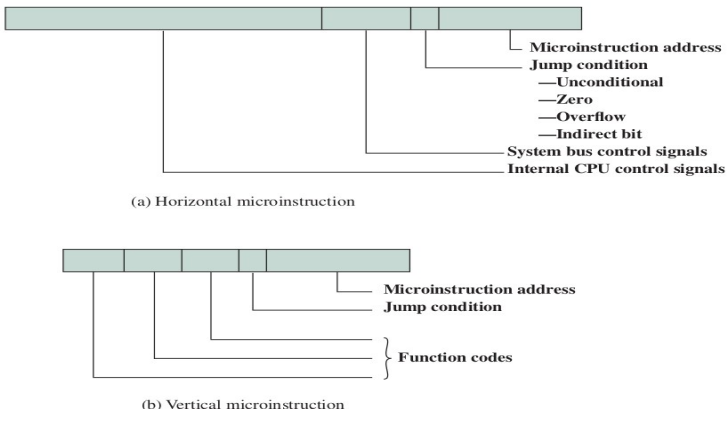
Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R5], RB ← [R6]
3	Compare [RA] to [RB], If [RA] = [RB], then PC ← [PC] + Branch offset
4	No action
5	No action

B Draw and discuss the flowchart of instruction cycle.



Q 4

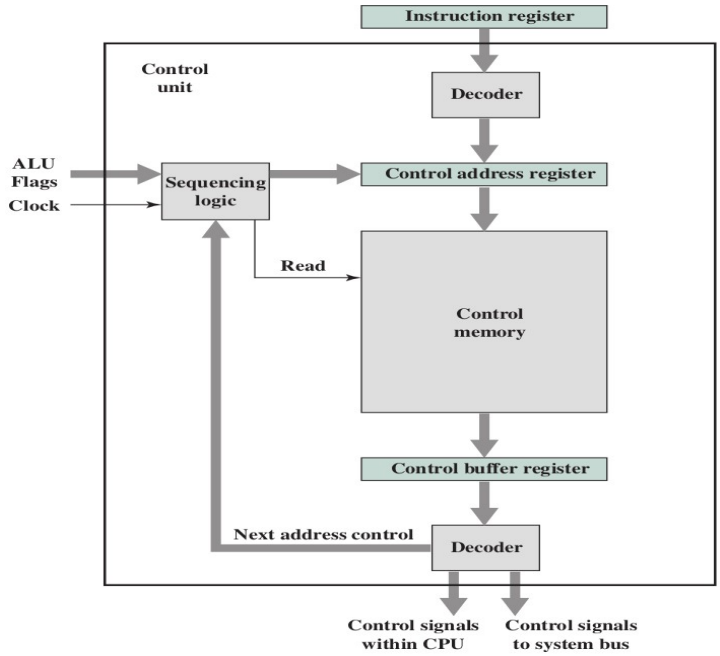
A What is the role of control signal? How a microinstruction is represented with different ways? 3



3 purposes where control signals act. 3

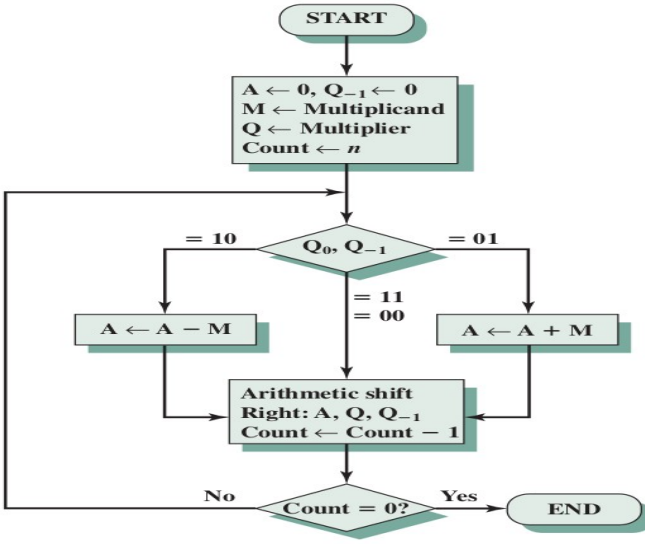
B How does the microprogrammed control unit function?

1, 2, 3, 4, 9, 12



Q 5

Draw the flowchart for Booth's Algorithm using Twos Complement Multiplication.



Multiply each of the following pairs of signed 2's-complement numbers using the Booth's algorithm. Assume that A is the multiplicand and B is the multiplier.

A = 010111 and B = 110110

6 | 1, 2 | 1, 2, 3, 4, 9, 12

Multiplicand A in Register 'M' =010111**(Multiplicand)**
Two's Complement of 'M' = 101001
Multiplier B in Register 'Q' =110110 **(Multiplier)**

Cycle	A	Q	Q_{-1}	Action
Initialize	0 0 0 0 0 0	1 1 0 1 1 0	0	
	Check Q_0 Q_{-1} = 00			
Cycle1	0 0 0 0 0 0	0 1 1 0 1 1	0	Arithmetic Shift
	Check Q_0 Q_{-1} = 10			
Cycle2	1 0 1 0 0 1	0 1 1 0 1 1	0	A = A – M = A + 2's (I
	1 1 0 1 0 0	1 0 1 1 0 1	1	Arithmetic Shift
	Check Q_0 Q_{-1} = 11			
Cycle3	1 1 1 0 1 0	0 1 1 0 1 0	1	Arithmetic Shift
	Check Q_0 Q_{-1} = 01			
Cycle4	0 1 0 0 0 1	0 1 0 1 1 0	1	A = A + M
	0 0 1 0 0 0	1 0 1 0 1 1	0	Arithmetic Shift
	Check Q_0 Q_{-1} = 10			
Cycle5	1 1 0 0 0 1	1 0 1 0 1 1	0	A = A – M = A + 2's (I
	1 1 1 0 0 0	1 1 0 1 0 1	1	Arithmetic Shift
	Check Q_0 Q_{-1} = 11			
Cycle6	1 1 1 1 0 0	0 1 1 0 1 0	1	Arithmetic Shift
	Result = AQ = 1 1 1 1 0 0 0 1 1 0 1 0 (-230)			