

Laboratory 4

Code conversion circuits

1. Introduction and Purpose of Experiment

Students will learn to design, simulate and implement circuits for various code converters.

2. Aim and Objectives

Aim: To generate code words using various codes and convert them from one code to another

Objectives: At the end of this lab, the student will be able to

- Develop expressions that convert code words from one code to another
- Develop code converter circuits

3. Experimental Procedure

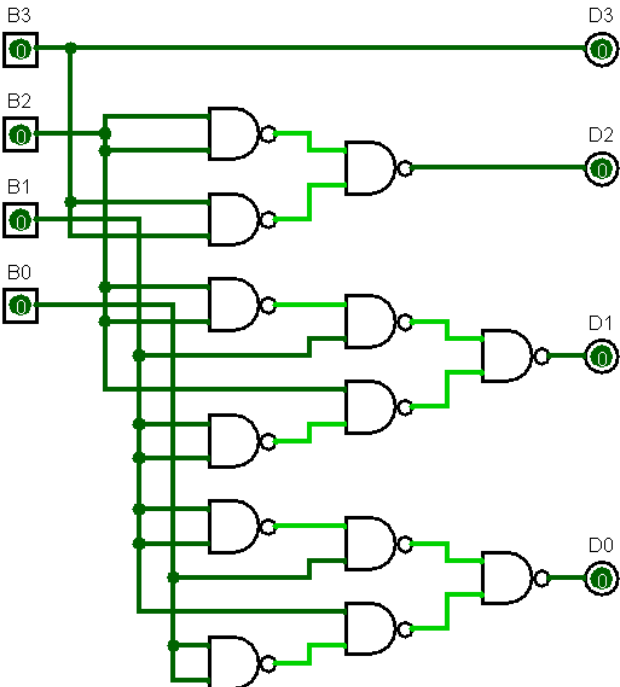
- Write truth tables for the following code converters.
 - BCD to Gray
 - Gray to BCD
 - 4-bit Binary to Excess-3
- Use K-Maps to develop the minimized expressions for the above code converters
- Draw the circuit diagrams using the following gates:
 - BCD to Gray: Using NAND gates
 - Gray to BCD: Using Ex-OR gates
 - 4-bit Binary to Excess-3 using NOR Gates
- Use Logisim to generate truth tables and circuit diagrams for all the code converters.
- Implement the code converters and show the output to the course leader.
- Show in detail how adders and subtractors are useful in developing these code converters.

Your document should include:

- Handwritten truth tables, expressions and circuit diagrams for the code converters
- Logisim screenshots
- Answer to 3(h)

3.a.i

BCD to GRAY using NAND Gates



| B3 | B2 | B1 | B0 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

Output: Format:

| | | B1, B0 | | | |
|--------|----|--------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| B3, B2 | 00 | 0 | 0 | 0 | 0 |
| | 01 | 0 | 0 | 0 | 0 |
| | 11 | 1 | 1 | 1 | 1 |
| | 10 | 1 | 1 | 1 | 1 |

B3

Output: Format:

| | | B1, B0 | | | |
|--------|----|--------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| B3, B2 | 00 | 0 | 0 | 0 | 0 |
| | 01 | 1 | 1 | 1 | 1 |
| | 11 | 1 | 1 | 1 | 1 |
| | 10 | 1 | 1 | 1 | 1 |

B2 + B3

Output: Format:

| | | B1, B0 | | | |
|--------|----|--------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| B3, B2 | 00 | 0 | 0 | 1 | 1 |
| | 01 | 1 | 1 | 0 | 0 |
| | 11 | 1 | 1 | 0 | 0 |
| | 10 | 0 | 0 | 1 | 1 |

$\overline{B2} B1 + B2 \overline{B1}$

Output: Format:

| | | B1, B0 | | | |
|--------|----|--------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| B3, B2 | 00 | 0 | 1 | 0 | 1 |
| | 01 | 0 | 1 | 0 | 1 |
| | 11 | 0 | 1 | 0 | 1 |
| | 10 | 0 | 1 | 0 | 1 |

$\overline{B1} B0 + B1 \overline{B0}$

3.a.ii

GRAY to BCD using XOR Gates

| D3 | D2 | D1 | D0 | B3 | B2 | B1 | B0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

Output:

Format:

| D1, D0 | | | | |
|--------|----|----|----|----|
| D3, D2 | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

D3

Output:

Format:

| D1, D0 | | | | |
|--------|----|----|----|----|
| D3, D2 | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 1 | 1 | 1 | 1 |

$\overline{D3} D2 + D3 \overline{D2}$

Output:

Format:

| D1, D0 | | | | |
|--------|----|----|----|----|
| D3, D2 | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 1 | 1 |
| 01 | 1 | 1 | 0 | 0 |
| 11 | 0 | 0 | 1 | 1 |
| 10 | 1 | 1 | 0 | 0 |

$\overline{D3} \overline{D2} D1 + \overline{D3} D2 \overline{D1} + D3 \overline{D2} \overline{D1} + D3 D2 D1$

Output:

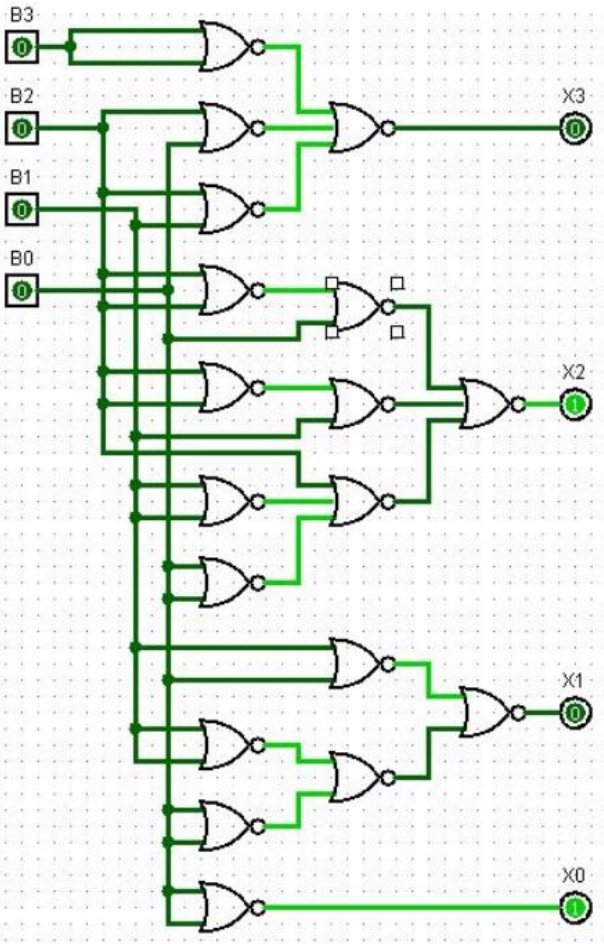
Format:

| D1, D0 | | | | |
|--------|----|----|----|----|
| D3, D2 | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 0 | 1 |
| 01 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |

$\overline{D3} \overline{D2} \overline{D1} D0 + \overline{D3} \overline{D2} D1 \overline{D0} + \overline{D3} D2 \overline{D1} \overline{D0} + \overline{D3} D2 D1 D0 + D3 \overline{D2} \overline{D1} \overline{D0} + D3 \overline{D2} D1 D0 + D3 D2 \overline{D1} \overline{D0} + D3 D2 D1 D0$

3.a.iii

BCD to XS3



| B3 | B2 | B1 | B0 | X3 | X2 | X1 | X0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

Output: X3 Format: Sum of products

B1, B0

| | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 1 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

$B2 \overline{B0} + B2 B1 + B3$

Output: X2 Format: Sum of products

B1, B0

| | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 00 | 0 | 1 | 1 | 1 |
| 01 | 1 | 0 | 0 | 0 |
| 11 | 1 | 0 | 0 | 0 |
| 10 | 0 | 1 | 1 | 1 |

$\overline{B2} \overline{B0} + \overline{B2} B1 + B2 \overline{B1} \overline{B0}$

Output: X1 Format: Sum of products

B1, B0

| | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 00 | 1 | 0 | 1 | 0 |
| 01 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 0 |
| 10 | 1 | 0 | 1 | 0 |

$\overline{B1} \overline{B0} + B1 B0$

Output: X0 Format: Sum of products

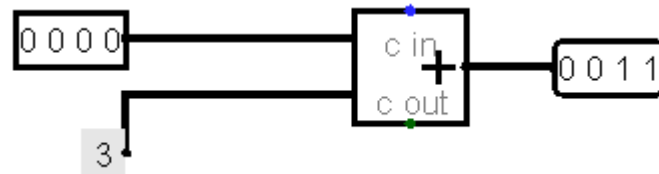
B1, B0

| | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 00 | 1 | 0 | 0 | 1 |
| 01 | 1 | 0 | 0 | 1 |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 0 | 1 |

$\overline{B0}$

3.e

BCD to EXCESS3 can be made using a simple adder circuit. Excess-3 in itself means 3 more than the value, so if we add 3 to the BCD number we get the excess 3 of the BCD number.



A simple 4-bit full adder can be used to do this, where the first number is the BCD number itself and the second number is 3. And we are not interested in the carry-in or carry-out bits and hence are left blank.