RAMAIAH UNIVERSITY OF APPLIED SCIENCES

DEEPAK R Reg. No:18ETCS002041

Laboratory 5

Combinational Circuits-I
Adders and Subtractors

1. Introduction and Purpose of Experiment

   Students will learn to design, simulate and implement adders and subtractors.

2. Aim and Objectives

   Aim: To use adders and subtractors and perform mathematical operations on binary numbers

   Objectives: At the end of this lab, the student will be able to

   - Add and subtract 4-bit binary numbers
   - Use adder circuits to perform subtraction

3. Experimental Procedure

   a. Write truth tables, Boolean expressions and circuit diagrams for the following combinational circuits:
      I. Half and full adder
      II. Half and full subtractor

   b. Using 2 full adders and other additional circuitry, design a circuit capable of adding and subtracting two 2-bit numbers.

   c. Use Logisim to simulate the circuits designed above.

   d. Implement the circuit and show the output to the course leader.

   e. Show in detail how a full adder can be implemented using two half adders.

Your document should include:

- Handwritten truth tables, expressions and circuit diagrams for the combinational circuits in 3(a).
- Design of the circuit
- Logisim screenshots of the designed circuit
- Answer to 3(e)

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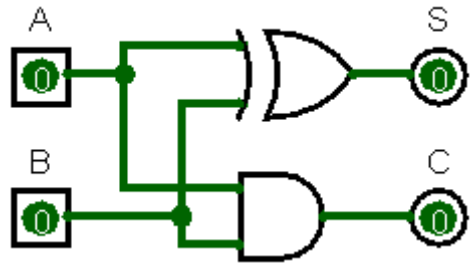
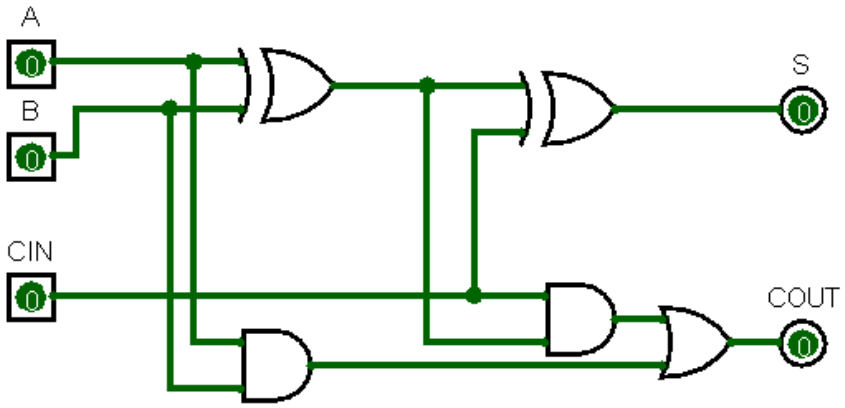
3.a.i

Half and Full Adder



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



A	B	CIN	S	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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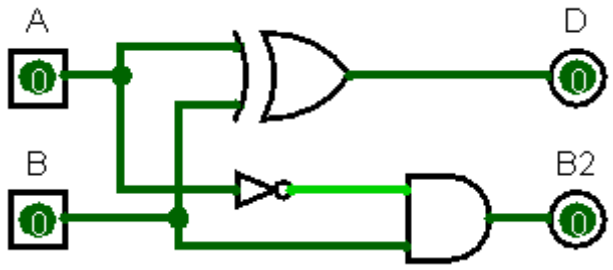
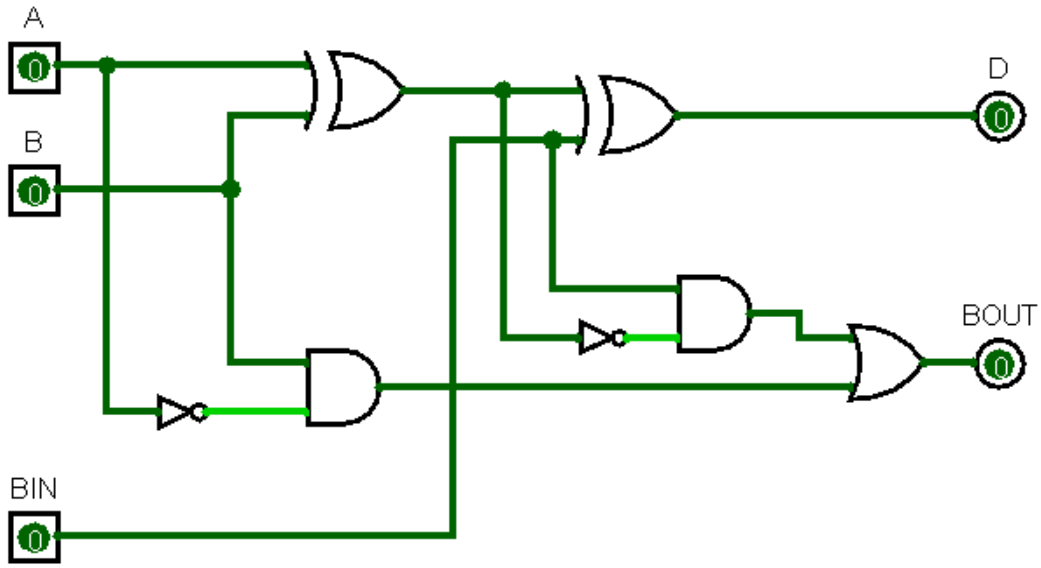
3.a.ii

Half and Full Subtractor



A	B	D	B2
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



A	B	BIN	D	BOUT
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

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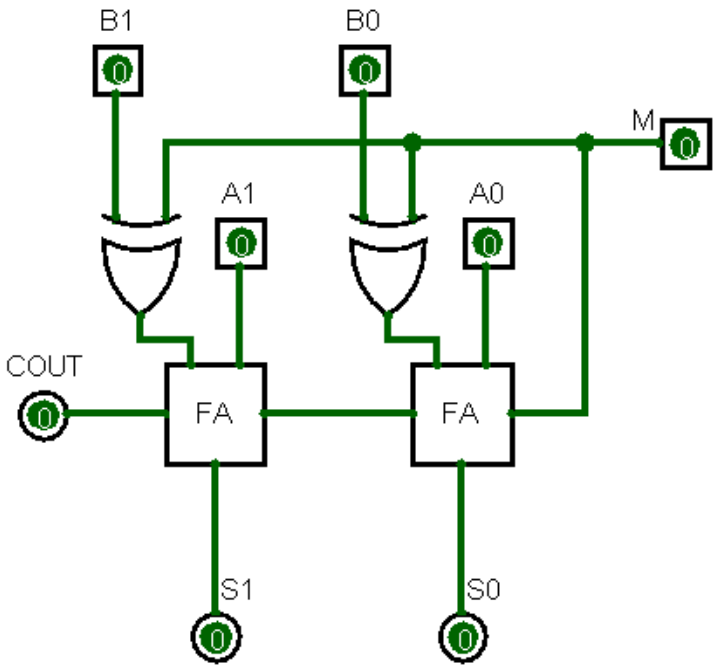
3.b

Adder and Subtractor



Where M is the Addition/Subtraction toggle switch, when M = 0 it is simple addition, and when M = 1 its subtraction, basically when M = 1 it compliments the input B and send carry-in = 1 to the first Full Adder.

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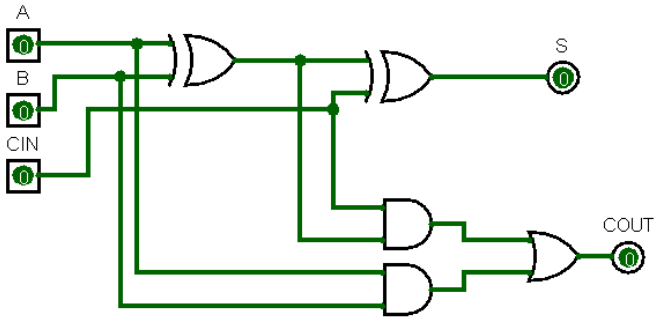
3.e

We can implement a full adder circuit with the help of two half adder circuits. At first, half adder will be used to add A and B to produce a partial Sum and a second half adder logic can be used to add C-IN to the Sum produced by the first half adder to get the final S output.



If any of the half adder logic produces a carry, there will be an output carry. So, COUT will be an OR function of the half-adder Carry outputs. Take a look at the implementation of the full adder circuit shown below.