This video describes the process of chip design, beginning with specifications that are created in a C model , which serve as the golden reference tested with a C testbench. After that, a RTL architect creates a soft copy of the hardware in Verilog RTL , which then constitutes the digital blueprint of the processor, peripherals, macros, and analog IPs. All of these blocks are combined through SoC integration and synthesized, floorplanned, and checked to ensure it will ultimately be converted to GDSII, which is sent out for manufacturing.