Module-1. ADE Model Ouistion paper II. 1a) Explain Construction of LED? 6H b) for the fixed-bias circuit of tog, delemine the operating point (given the transition gain B=100, VBE=0.7V). Also, drew the load line for the circuit. 8M. Re Z AKS AL OLP Signal
Ci C) Explain opamp applición as peck detector 26M. 2a) Explain opamp application as schwitt trigger? 64. 6) Explain voltage to curent converter? 64. C) Enplain R-2R ledder Cileuit ? 8H. 3a) Simplify using 10-map FEaib, (1) = 2m (1,3,5,7,9)+5d(6. (12) 13) ? 6M. b) write sop + pos for F(A,B,C,D) = MM(1,5,6,7,9,12,13 C) Apply EVM method F(W, X, Y, Z) = Em(1,3,5,7,13,14,15,16)? 6M 4a) Explain patricles method with example ? 6 M. b) find a min sop wing Owne Heclustry method: F(a,b,c,d) = &m(1,3,4,5,6,7,10,12,13) +&d(2,9,15) MODULE -3. 50) Reelize F\_(a,b,c) = &m(0,2,3,4,5) + F\_2(a,b,c) = &m(0,2,3 Using Only Q-J/P NAND gate + inveller ? BM. 417) b) enplain the worlding of Simulation for combinetional logic? 60 c) Realize FEW, X1412) = Em(1,2,5,6,8,9,10,11,14,45)

Winy 8:1 MOX. 96M.

- 6a) Restize Fifailic) = Em(0, 8, 5), Fz(a, b, c) = Em(1, 5, 6), f. P3(a,b,c) = Em(2,3) Usig 3:8 decodes ? 6M.
  - b) Realize 7-signest decoder using PLA? BM.
    - c) Whiti a note on programmeble allay logic ? 6 H. MODULE-4
  - Fa) write a VHOL ce de for full-adder + full-subtractor? 871 6) Explain SR flop flop ? 6M.
    - C) Consect Deduce the characteristic equation for D4 Tflip
  - & a) Briefly explain pacicipes + libracies in VHDL? 6M.
    - b) Convert JK flip to SR flip thep 28M.
    - C) Emploin edge-liggued IK flip flop ? 6M.
    - 9a) Explain n-bit Parollel adder with accumulator? 6 M.
      - b) Explain Johnson Countré 96M.
      - C) Explain more model 4 nearly model in brief? 84.
    - 10a) Design 3-bit up-down countre using D ff 984.
      - b) Draw mooke Steli diagram tol seval addie? 64
      - C) Differenciali blu moore + mealy model ? 6 M.

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