Module-1. ADE Model Ours ion Paper III.

La) Disseun LED palameter? 6M.
b) Deure the egns for Emilla-bias when BIT is in CE-mode?

() Explain opamp application as Active filter? 64.

La) Deduce the egns for collection to base bias for CE configuration- ? 619.

6) Explain opamp application as Relamation oscillator ?BM

C) While a note on adjustable voltage regulator ? 64.

## MODULE-2.

3a) Simplify using 10-map F(AIB, CIDIE) = Em(0,1,4,5,13,15-20,21,22,23,24,26,28,30,31) 9 10M.

b) While sop + pos der F(AIBICID) = Em(0,2,3,4,8,10,11,15)

C) Apply MEV method F(AIB,C) = &m(0,1,3,5,6) 4M.

Ha) Define essential prime implicant with example ? 64.

b) bolve cesing patricles method F(a,b,c,d) = &m(0,3,4,5,7,9,11,1B) ? 14M.

50) Enplain Hazards 4 its covers? SM.

b) Emplain timing diagram for accent with delay ? 64.

C) Replize 32:1 Mux living 4:1 Mux +2:1 Mux ? 6M.

6a) Explain Aypes of PLD's. 26M.

b) Reelize F(a,b,c) = &m(1,2,3,5,6) Usi7 PLA ?64.

C) Derign a priority enlode the teelt table of which is shown in tig, the order of priority for there slps in X1>X2>X3. However, if the enloder is not enabled by Sor all the slps are inactive the olp AB=00 ? 8M.

Fa) Writ a VHOL code tol multiplene by considering appropriate example ? 6H. b) Wilt the help of timing diagram. Emplain SR Maslei Slave 47 9 8M. C) Deduce the characleristic ey for JK flip flop? 6M.

8a) Wili a VHOL Code for

A DOF G

b) Euplain gated D Lelich ? 6 M. c) Euplain edge liggend D-flip tlop? SM.

## MODULE-5

90) Explain 8-61+ SISO Shift Register? 64.

6) Euplain Sequence cheeker + charges generator ? 611.

C) Draw mealy model for seval adder ? 84.

10 a) Design Decade Counti Uring ER Hip Hop? 841. b) Diffuenciali b/h synchronous + asynchesunous

Courle 96M.

C) Draw mooke state diagram for sequential partly Cheelere? 6M.