GENERAL

The versioning number could be read from the base address @1 = x"80000000":

- @1 + 0(d): ASCII codes

Bits	Name	Description	Access	Default value at startup
[31:24]	Ascii_Code_01	1st ASCII code ('T')	r	x"54"
[23:16]	Ascii_Code_02	2nd ASCII code ('K')	r	x"4B"
[16:8]	Ascii_Code_03	3rd ASCII code ('sp')	r	x"20"
[7:0]	Ascii_Code_04	4th ASCII code ('sp')	r	x"20"

- @1 + 1(d) : ASCII codes

Bits	Name	Description	Access	Default value at startup
[31:24]	Ascii_Code_05	5th ASCII code ('D')	r	x"44"
[23:16]	Ascii_Code_06	6th ASCII code ('A')	r	x"41"
[16:8]	Ascii_Code_07	7th ASCII code ('Q')	r	x"51"
[7:0]	Ascii_Code_08	8th ASCII code ('sp')	r	x"20"

- @1 + 2(d): User Firmware/Architecture Version – Binary Format

Bits	Name	Description	Access	Default value at startup
[31:25]	Fw_ver_year	Firmware version year	r	
[24:21]	Fw_ver_month	Firmware's version month	r	
[20:16]	Fw_ver_day	Firmware's version day	r	
[15:8]	Archi_ver_nb	Archi version number (incremental)	r	
[7:0]	Fw_ver_nb	Firmware version number (incremental)	r	

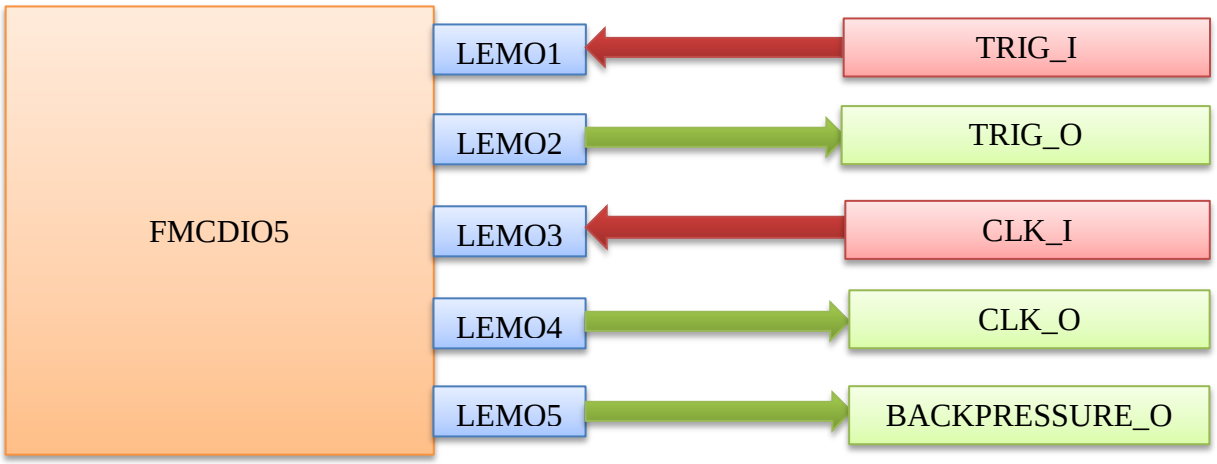
Archi_ver_nb & Fw_ver_nb
x"01_01" … x"01_FF": Architecture with 1x2CBC2 onto the connector FMC1 (J2) – Format DESY
x"02_01" … x"02_FF": Architecture with 1x8CBC2 onto the connector FMC1 (J2) – Format DESY

FMCDIO5 Card

Geographical position

The FMCDIO5 card has to be plugged onto the connector FMC2 (J1) from the GLIB3 to authorize its I2C control (notably to adjust the threshold level of each input). Indeed, the I2C signals controlling the FMCDIO5 are coming from the shared I2C bus with the FMC connector and not from individual signals. Only the FMC2 (J1) connector from the GLIB3 is capable to drive this shared I2C bus. A part of the GLIB VHDL code (system-level) provided by the CERN had been modified to accept the I2C control.

Signals configuration



The output signals TRIG_O and CLK_O are representative of their respective input signals TRIG_I and CLK_I. They are re-transmitted by the FPGA after their reception. They could be inspected by a scope to verify that:

- the transmission and the cabling of their respective input signals TRIG_I and CLK_I are correct
- the signal really handled by the FPGA is alright and does not have glitches or oscillations (this case is true only if the threshold is well adjusted in function as the LOW LEVEL/HIGH LEVEL of the input signal)

Inputs signals – Voltage Level

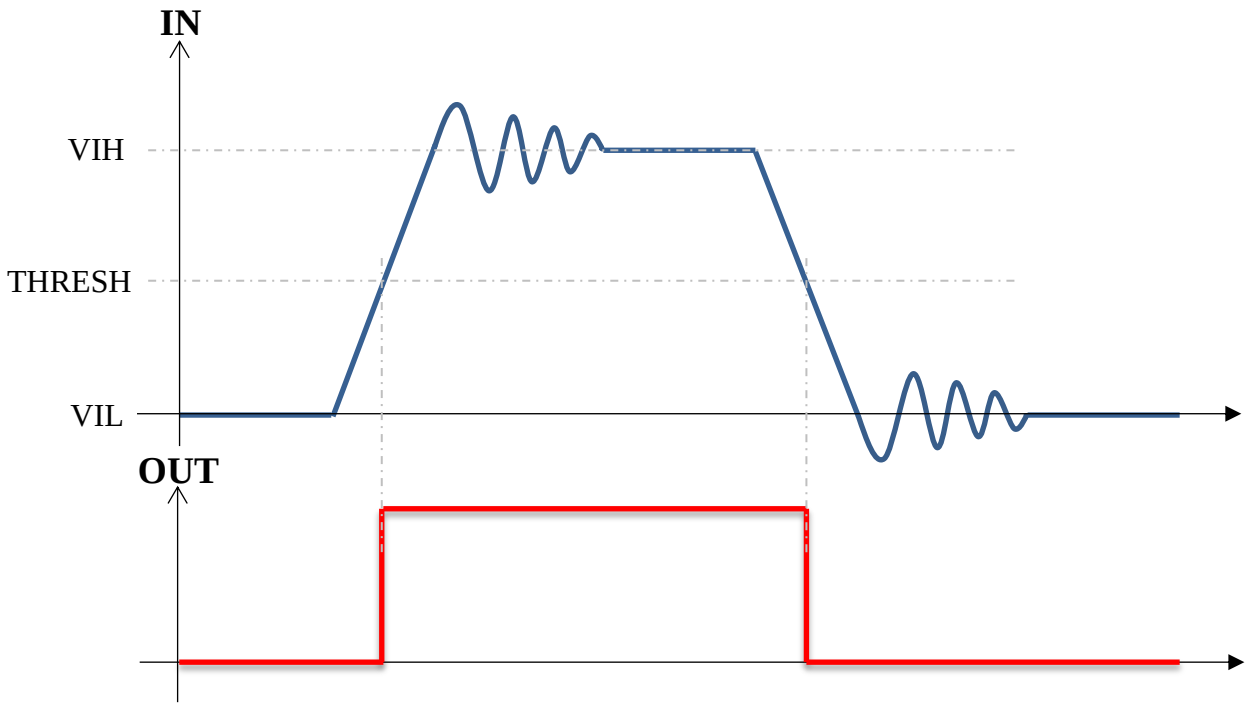
The card accepts any single logic standard between [1V-5V]. The threshold level to well detect the input signal should be adjusted as your needing.

Threshold adjustment

The threshold level is adjustable between [0-3.3V]. The equation is described as follows:

$$\text{Thresh(Volts)} = \frac{Thresh(Decimal)}{256} \times 3.3$$

The threshold level should be adjusted in function as the characteristics of the input signal.



Requirements:

$$+1\text{V} \leq \text{VIH} \leq +5\text{V}$$

$$+1\text{V} \leq \text{VIH} - \text{VIL} \leq +5\text{V}$$

$$\text{Thresh} = \frac{VIH - VIL}{2} = \frac{Thresh(Decimal)}{256} \times 3.3$$

$$\text{Thresh(Decimal)} = \frac{VIH - VIL}{2} \times \frac{256}{3.3}$$

NB:

A transmission of a 40-MHz clock could be critical. So, to achieve the best transmission, it is suitable to add the internal 50Ω termination resistor at each input (configuration by default). Don't forget that a 50Ω termination resistor causes the input signal to be divided by a factor two.
For the outputs, it is not necessary to add the internal 50Ω termination resistor. The 50Ω termination resistor from the scope should be used.

Registers Mapping for FMCDIO5

All the parameters allowing the control of the FMCDIO5 from the GLIB3 through GbE/IPBUS are stored from the base address @2 = x"80000180":

- @2 + 20(d)

Bits	Name	Description	Access	Default value at startup
[7:0]	fmcdio5_threshold_trig_in	Decimal number comprised between [0:255]	r/w	128(d)
[15:8]	fmcdio5_threshold_clk_in	Decimal number comprised between [0:255]	r/w	128(d)
[16]	fmcdio5_trig_in_50ohms	Programmable 50Ω termination for LEMO1 input '1': TERM(50Ω) enabled	r/w	'1'
[17]	fmcdio5_trig_out_50ohms	Programmable 50Ω termination for LEMO2 output '1': TERM(50Ω) enabled	r/w	'0'
[18]	fmcdio5_clk_in_50ohms	Programmable 50Ω termination for LEMO3 input '1': TERM(50Ω) enabled	r/w	'1'
[19]	fmcdio5_clk_out_50ohms	Programmable 50Ω termination for LEMO4 output '1': TERM(50Ω) enabled	r/w	'0'
[20]	fmcdio5_backpressure_out_50ohms	Programmable 50Ω termination for LEMO5 output '1': TERM(50Ω) enabled	r/w	'0'
[21]	fmcdio5_trig_in_edge	Active edge from the input trigger to detect '0': rising edge '1': falling edge	r/w	'0'
[22]	clk_mux_sel	Selection of the DAQ clocking '0': internal clock '1': fmcdio5_clk_in	r/w	'0'
[23]	fmcdio5_backpressure_out_polar	Selection of the polarity of the backpressure output '0': positive (high level when active) '0': negative (low level when active)	r/w	'0'
[24]	fmcdio5_lemo2_sig_sel	Signal selection for LEMO2 output '0': fmcdio5_trig_in '1': L1A pulse generated from fmcdio5_trig_in (Duration = 1/f = 25 ns)	r/w	'0'

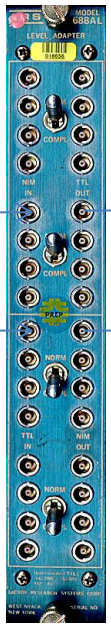
GbEthernet/IPBUS
Data Readout
Slow Ctrl (Trigger and Clock selection)

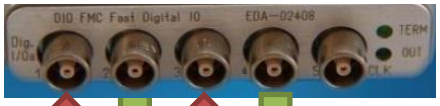
Gigabit Link Interface Board (GLIB)

FMC link (J1, AMC side)

FMCDIO5 card

NIM/TTL Level adapter





External
CLK & TRIG

TRIG_I

CLK_I

Scope
50Ω termination