Software Requirements Specification for Analog Module of Engine Data Acquisition Unit of Airbus Helicopters Generic Vehicle Monitoring System (GVMS)

Document Number: H398-002-001-ANA

Version No: 2.12

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**1 Amendment Record**

*Table 1: Amendment Record*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Version No.** | **Description of Amendment** | **Change Request No.** | **Changed By** | **Release Date** |
| 1.1 | Initial Release | NA | Sayed Bellary | 17-Dec-2021 |
| 1.2 | Updated to address review comments  • Spell check is performed throughout the document and corrected all spelling mistakes  • Verification method is added all functional and derived requirements  • Section 2 overview updated  • Section 4 updated to remove unused acronyms and missing acronyms were added  • Section 6 references updated  • Updated requirement H398-SRS-ANA-DRQ-18 to change the priority for system tick and pend interrupts.  • Updated H398-SRS-ANA-DRQ-24, H398-SRS-ANA-FNC-35, H398-SRS-ANA-FNC-36, H398-SRS-ANA-FNC-62, H398-SRS-ANA-FNC-66 for better readability  • Updated H398-SRS-ANA-FNC-51 to add missing doc IDs and also to change description column  • Updated H398-SRS-ANA-FNC-52 to address include missing DOC IDs  • Updated H398-SRS-ANA-DRQ-68 to add missing rationale for derived requirement.  • Updated H398-SRS-ANA-FNC-32 to change MOPS field from No to Yes  • Updated H398-SRS-ANA-FNC-42, H398-SRS-ANA-FNC-46 and H398-SRS-ANA-FNC-47 to change the DOC Id from 49160 to 49162 | 100010 | Sayed Bellary | 11-Jan-2022 |
| 1.3 | Updated based on Self-Review and QA review comments   * Updated Figure 2 to include DLU with in CMU * Section 4 Acronyms, Terms and Definitions is updated to add missing acronyms and delete unused acronyms * Updated H398-SRS-ANA-FNC-34 to specify external ADC bank information * Updated H398-SRS-ANA-FNC-42 to change server ID column for NSC\_RESET command * Updated H398-SRS-ANA-FNC-43 and H398-SRS-ANA-FNC-44 to add information to explain excitation current * Updated H398-SRS-ANA-DRQ-48 to specify the reset the analog board only when if the request from gateway module. * Updated H398-SRS-ANA-DRQ-54 to add a note that some of the parameters defined in MCD used by calibration software. * Updated H398-SRS-ANA-DRQ-55 to add note for reference MCD values * Updated H398-SRS-ANA-DRQ-54 and H398-SRS-ANA-DRQ-55 to remove CRC field which is no longer part of MCD. * Updated H398-SRS-ANA-DRQ-54 to modify the size of bytes of MCD fields * Corrected spelling mistakes. * Updated H398-SRS-ANA-FNC-51 to maintain consistent font format | 100010 | Vijay Bhaskar | 15-Jan-2022 |
| 1.4 | The following requirements are modified to address DER audit observations:  1. In H398-SRS-ANA-FNC-32 accuracy and filtering related information is removed.  2. H398-SRS-ANA-FNC-52 is split and create two new requirements (H398-SRS-ANA-FNC-77 and H398-SRS-ANA-FNC-78)  The following Requirements are modified due to Self-review:  H398-SRS-ANA-FNC-42  H398-SRS-ANA-DRQ-54  H398-SRS-ANA-FNC-41  H398-SRS-ANA-FNC-50 | 100043 | Vijaya Bhaskar | 28-Feb-2022 |
| 1.5 | The following requirements have been modified due to Rev 3 to Rev4 spec changes:  H398-SRS-ANA-FNC-32  The following requirements have been modified due to Self-review:  Functional requirements modified:  H398-SRS-ANA-DRQ-18  H398-SRS-ANA-DRQ-23  H398-SRS-ANA-DRQ-24  H398-SRS-ANA-FNC-35  H398-SRS-ANA-FNC-41  H398-SRS-ANA-FNC-42  H398-SRS-ANA-FNC-50  H398-SRS-ANA-FNC-51  H398-SRS-ANA-FNC-52  H398-SRS-ANA-DRQ-54  H398-SRS-ANA-FNC-58  H398-SRS-ANA-DRQ-59  H398-SRS-ANA-FNC-62  H398-SRS-ANA-FNC-66  H398-SRS-ANA-DRQ-76  Requirements deleted:  H398-SRS-ANA-FNC-77  H398-SRS-ANA-DRQ-46  H398-SRS-ANA-DRQ-47  General requirements:  6 References | 100058 | Vijaya Bhaskar | 23-Mar-2022 |
| 1.6 | Updated to address QA findings and self review  Following requirements are updated  H398-SRS-ANA-DRQ-18,  H398-SRS-ANA-FNC-32,  H398-SRS-ANA-FNC-62,  H398-SRS-ANA-FNC-35,  H398-SRS-ANA-DRQ-20 | 100058 | Vijaya Bhaskar | 06-Apr-2022 |
| 1.7 | Updated to address DER SOI#2 action and self review  Following requirement is updated  H398-SRS-ANA-FNC-63  Below requirements are added  H398-SRS-ANA-DRQ-80  H398-SRS-ANA-DRQ-81 | 100080 | Vijaya Bhaskar | 12-Apr-2022 |
| 1.8 | Updated to Address HSIT observations  Following requirement is updated  H398-SRS-ANA-FNC-58 | 100106 | Divya R | 29-Nov-2022 |
| 2.0 | The following requiremnts are modified:  H398-SRS-ANA-FNC-32.  H398-SRS-ANA-DRQ-76  The following Sections are modified:  Section 2 Overview  Section 3 Objectives  Section 4 Acronyms, Terms and Definitions  Section 6 References | PR100169 | Prajwal R | 31-01-2024 |
| 2.1 | The following sections are Updated to address review comments:  Section 6 References  Section 15 output Documents updated as per self review | PR100169 | Prajwal R | 10-02-2024 |
| 2.2 | The following sections are Updated to address QA comments:  3 Objectives  10 Approvals  13 Responsibilities  14 Input Documents  The requirement is Updated as per self review  H398-SRS-ANA-FNC-32 | PR100169 | Prajwal R | 13-02-2024 |
| 2.3 | The followings requirements are added as per self-review:  H398-SRS-ANA-DRQ-82  The following requirements are modified as per self-review:  H398-SRS-ANA-FNC-51  H398-SRS-ANA-FNC-52  H398-SRS-ANA-FNC-32  H398-SRS-ANA-DRQ-18 | PR100213 | Prajwal R | 09-05-2024 |
| 2.4 | The following requirements are modified as per review comments:  H398-SRS-ANA-FNC-32  H398-SRS-ANA-FNC-51  H398-SRS-ANA-DRQ-54  H398-SRS-ANA-DRQ-55  H398-SRS-ANA-FNC-62  H398-SRS-ANA-DRQ-75  H398-SRS-ANA-DRQ-70  The following sections got modified as per review comments:  Section:2 Overview  Section:6 References | PR100213 | Prajwal R | 08-07-2024 |
| 2.5 | The following sections are Updated to address QA comments:  Front Page  Section:6 References  Section:10 Approvals | PR100213 | Prajwal R | 10-07-2024 |
| 2.6 | The below requirements are added  H398-SRS-ANA-FNC-83  H398-SRS-ANA-FNC-84  H398-SRS-ANA-FNC-85 | PR100243 | Prajwal R | 06-08-2024 |
| 2.7 | The below requirements are updated as per review comments:  H398-SRS-ANA-FNC-83 | PR100243 | Prajwal R | 13-08-2024 |
| 2.8 | Removed watermarks as per QA comments  Updated table of contens as per self review | PR100243 | Prajwal R | 17-08-2024 |
| 2.9 | The below requirement is updated as per self review  H398-SRS-ANA-DRQ-54 – Table 9: DAC Sensor  H398-SRS-ANA-FNC-32 | PR100281 | Prajwal R | 29-08-2024 |
| 2.10 | The below requirements are updated as per review comments  H398-SRS-ANA-DRQ-54  Table 8 : Tach Sensor  Table 9 : DAC Sensor  Table 12 : Cold Juntion Sensor  H398-SRS-ANA-FNC-32 | PR100324 | Prajwal R | 10-10-2024 |
| 2.11 | The below requirement is updated as per QA review comments  H398-SRS-ANA-FNC-32 | PR100324 | Prajwal R | 15-10-2024 |
| 2.12 | The below requirement added:  H398-SRS-ANA-FNC-86  H398-SRS-ANA-FNC-87 | PR100358 | Sruthi D | 20-06-2025 |

**2 Overview**

The EIS consist of Display Unit (DU), Engine Data Acquisition Unit (EDAU), Configuration Management Unit plus NVM (CMU+) and Data Logging Unit (DLU). It will be complemented by pilot input devices and interconnecting harness. The EIS will interface with the Airbus AS532U2engine sensors and other applicable aircraft systems.

Figure: Functional block diagram - Engine Instrument System describes the functional blocks of Engine Instrument System (EIS).



*Figure 1: Functional block diagram - Engine Instrument System*

**Engine Data Acquisition Unit (EDAU)**

The EDAU shall function to process airframe and engine data and transmit this information to be graphically presented on a cockpit display. The EDAU will process analog and discrete inputs, apply user defined logic to those inputs, and may generate aural and visual Caution and Warning alerts.

The EDAU is utilized to perform the following functions:

1. Provide analog to digital conversion of aircraft and engine systems
2. Provide discrete bit information via A429 for Crew Alerts (CAS)
3. Provide field loadable software update via maintenance port
4. Process data
5. Filter analog and digital signal data
6. Receive/Transmit data
7. Provide discrete strapping for multiple aircraft and engine configurations

To increase the reliability of the system, EDAU will have two Data Acquisition Units (DAU) packed together. Both the Data Acquisition Units (DAU) will run the data acquisition application software, process the same inputs and produce same outputs independently at the same time.

The primary function of the DAU will be acquiring analog engine parameters, discrete inputs, and other aircraft system information for processing and converting to a digital format for display via ARINC 429 to four Display Units (DU).

Each DAU will contain three Boards/Modules, each with its own CPU: The Gateway Board (BH35112) for digital buses, the Analog Board (BH35113) for analog inputs and the Discrete Board (BH35114) for discrete I/O and chip detection. Inter-board communication and communication with CMU+ / DLU will be on CAN bus based on ARINC 825 protocol.

**Configuration Module Unit Plus NVM (CMU+)**

The CMU+ stores Aircraft Configuration Data (ACD). The ACD includes options related to the engine parameters, sensor interface, and airframe configurations. The DAU accesses CMU+ on system initialization to determine the current configuration and active interfaces.

The CMU+ is utilized to perform the following functions:

1. Provide configuration data to each DAU utilizing separate, isolated hardware for each DAU
2. Support the DAU system configuration so that a replacement DAU will function the same as

the DAU being replaced after installation and initialization

c. The EDAU shall provide the capability to support different engine and aircraft configurations.

d. The CMU+ shall store item configuration data for entire EIS

e. The CMU+ shall contain system NVM

The CMU+ is internally redundant with two separate configuration sections packaged into one enclosure (separate power supplies). One section CMU+ #1 is connected to DAU#1 through ARINC825 (CAN #1), and the other section CMU+ #2 is connected to DAU#2 through ARINC825 (CAN #1). Internally CMU+ #1 and CMU+ #2 are connected through an independent ARINC825 (CAN #2).

The CMU+ installed in position #1 will have a USB device interface for programming/accessing configuration information in Maintenance Mode.

Figure: EDAU - decomposition illustrates the decomposition of the DAU into its various internal modules:

A429

Input

Discrete Input

RS232

Input

Analog Module

Discrete Module

Analog Input

Discrete Input

28V

power Input

Discrete Input

28V

Power Input

Discrete Output

Gateway Module

A429

Output

RS232

Output

CMU

+ Module /

DLU

Module

USB

Input/Output

ARINC825

28V

Power Input

ARINC825

EDAU

*Figure 2: EDAU - decomposition*

**Analog Module:**

The Software for the Analog Module follows a cyclic model with interrupts enabled. The main functionality performed by the Analog Module is to read Analog Inputs. The Analog Module uses the CAN bus to communicate with the Gateway Module. Whenever a CAN message is received, it triggers an interrupt. The handler routine copies the received message to a temporary buffer. It then identifies the Logical Communication Channel (LCC) to which the received message belongs to. The LCCs supported are:

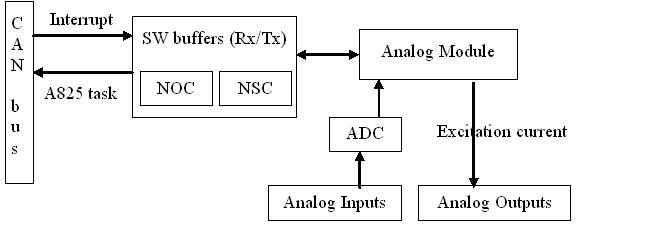
1. Check Node Service Channel (NSC) and Respond.
2. Check Normal Operational Channel (NOC) and Respond.

For each category of LCC, there are separate queues. The handler then inserts the received message in the respective buffer. It now parses the payload, performs the required action and transmits the appropriate response.

The main tasks performed by the Analog Software are:

1. Check Node Service Channel (NSC) and Respond: Check if there are any messages received on this channel. If any valid messages are received then depending on the payload, the Analog Module, will switch on or off the excitation. It then transmits a response to Gateway.
2. Check Normal Operational Channel (NOC) and Respond: Check if there are any messages received on this channel. If a valid ACQUIRE message is received then the Analog Module will read the inputs, scale them and then transmit them to Gateway.

Figure: Analog Module – block diagram depicts the block diagram for the Analog Module.

****

*Figure 3: Analog Module – block diagram*

**Can bus communication:**

The Analog Module uses a CAN bus to communicate with the Gateway Module. Whenever a CAN message is received an interrupt is triggered. The handler routine copies the received message to a temporary buffer. It then identifies the Logical Communication Channel (LCC) of the received message. For each category of LCC, there are separate queues. The handler inserts the received message in the respective buffer. It then parses the payload, performs the required action and transmits the appropriate response.

**Scheduler**

The Application Software uses a kernel to create and schedule jobs. The kernel has a fixed priority pre-emptive scheduler. The scheduler ensures that at any given time, the processor executes the highest priority task of all those tasks that are currently ready to execute. The pre-emptive scheduler has a clock interrupt task that provides the scheduler with an option to switch after the task has had a given period to execute—the time slice.

The kernel uses semaphores to synchronize the tasks. Three operations can be performed on a semaphore: Creation, Pending, and Posting. Each task has to run periodically. A unique semaphore is created for every task. A task desiring to run will perform a PEND on its corresponding semaphore. The scheduler is responsible for releasing the semaphores at correct intervals so that the tasks execute at the required frequency. The scheduler releases the semaphore for a task by doing a POST on the semaphore. Once the semaphore is released, the task is made to run. The task then executes its set of instructions and makes the next PEND. It then waits for a POST from the scheduler. This process goes indefinitely.

**3 Objectives**

The objective of this document is to specify the Software High Level Requirements for the Analog Module of the Engine Data Acquisition Unit (EDAU) for Airbus Helicopter model AS532U2 aircraft.

**4 Acronyms, Terms and Definitions**

The list of Acronyms used in this document are described in Table: Acronyms and Definitions.

*Table 2: List of Acronyms and Definitions*

|  |  |
| --- | --- |
| **Term** | **Definition** |
| A825 | ARINC Specification 825 |
| ACD | Aircraft Configuration Data |
| ADC | Analog to Digital Convertor |
| ANA | Analog |
| ARINC | Aeronautical Radio, Incorporated |
| BIT | Built-In Test |
| CAN | Controller Area Network |
| CAS | Crew Alert System |
| CBIT | Continuous BIT |
| CMU+ | Configuration Management Unit Plus NVM |
| CPU | Central processing unit |
| CRC | Cyclic redundancy check |
| DAU | Data Acquisition Unit |
| DC | Direct Current |
| DLC | Data Length Count |
| DMA | Direct Memory Access |
| DOC | Data Object Code |
| DRQ | Derived Requirements |
| EDAU | Engine Data Acquisition Unit |
| EIS | Engine Instrument System |
| EOP | Engine Oil Pressure |
| EOT | Engine Oil Temperature |
| FIFO | First In First Out |
| FSMC | Flexible Static Memory Controller |
| FTP | File Transfer Protocol |
| GPIO | General Purpose Input and Output |
| HFP | Hydraulic Fluid Pressure |
| HFT | Hydraulic Fluid Temperature |
| Hz | Hertz (unit for frequency) |
| ITT | Inlet Turbine Temperature |
| LCC | Logical Communication Channel |
| LCL | Local Bit |
| LED | Light-emitting diode |
| MCD | Module Configuration Data |
| MOPS | Minimum Operational Performance Standards |
| mV | milli Volts |
| NA | Not Applicable |
| NOC | Normal Operation Channel |
| NSC | Node Service Channel |
| NVIC | Nested Vectored Interrupt Controller |
| NVM | Non-Volatile Memory |
| PBIT | Power-On BIT |
| PVT | Private Bit |
| QA | Quality Assurance |
| RCI | Redundancy Code Identifiers |
| RE | Range Error |
| RSD | Reserved Bit |
| RTCA | Radio Technical Commission for Aeronautics |
| Rx | Receive |
| SFC | Service Function Code |
| SMT | Service Message Type |
| SRS | Software Requirement Specifications |
| SVN | SubVersion |
| Tx | Transmit |
| VDC | Volts Direct Current |
| XADC | External Analog to digital converter |

**5 Scope**

The Scope of this document is limited to specifying the Software High Level Requirements of the Analog Module Application software of the EDAU.

**6 References**

The Table: References provides the Reference documents used for Software High Level Requirements of the Analog Module of the EDAU of Airbus AS532U2 Engine Instrument System.

*Table 3: References*

|  |  |  |
| --- | --- | --- |
| **Source** | **Document No.** | **Title** |
| RTCA | DO-178B | Software Considerations in Airborne Systems and Equipment Certification |
| Howell | SYS2160SRS | Aircraft Helicopter AS532U2 Retrofit Engine Instrument System Requirements Specification |
| Howell Instruments, Inc. | HE0398AHA | Hardware Architecture of Analog Board |
| Howell Instruments, Inc. | BH35186 | PCB Assembly of DAU Analog Board |
| Aeronautical Radio, Inc. | ARINC SPECIFICATION 825-2 | GENERAL STANDARDIZATION OF CAN (CONTROLLER AREA NETWORK) BUS PROTOCOL FOR AIRBORNE USE |
| ALTEN Global Technologies Private Limited | H398-001-002 | Software Development Plan |
| ALTEN Global Technologies Private Limited | H398-001-006 | Software Requirement Standards |

**7 Assumptions**

None

**8 Outstanding Issues**

None

**9 Document Control**

This document is under change control. After baseline, any changes to this document shall be carried out in accordance with H398-001-004 (Software Configuration Management Plan).

**10 Approvals**

The document will be reviewed to meet the objectives of DO-178B level A and approved by ALTEN GT QA.

**11 Distribution**

This document will be distributed over a secure FTP server to Howell Instruments, Inc.

**12 Traceability**

Traceability to SES (System Equipment Specification) is provided in H398-002-002-ANA.

**13 Responsibilities**

1. Software Development Lead shall write the Software High Level Requirements in ReMa.
2. Reviewers shall review the requirements based on the DO-178B SRS check points provided as attributes in ReMa. Developers to respond to these comments and then change the status to <Looked Into> in ReMa.
3. Once all the comments from Reviewer are made to 'Looked Into' and the requirement status is Closed in ReMa.
4. Project Leader is responsible for baselining the document to SVN through ReMa as well as checking in the exported document into the path

http://192.168.1.230/svn/A21HOWBLDAU/V2\_H398/ACCORD/SW/Trunk/Documents/SRS

**14 Input Documents**

* SYS2160SRS
* Software Development Plan (H398-001-002)
* Software Requirements Standards (H398-001-006)

**15 Output Documents**

The Output documents are as mentioned below

* Software Requirements Specification for Analog Module of Engine Data Acquisition Unit of Airbus EDAU (H398-002-001-ANA)
* Traceability Matrix (H398-002-002-ANA)

**16 High Level requirements**

This section explains the Software High Level Requirements of Analog module of the EDAU unit.

**16.1 Initialization**

This section specifies the Software High Level Requirements for the initialization of the following components of Analog Module after Power On.

1. Processor
2. Watchdog timer
3. System Timer
4. On-chip CAN peripheral
5. Nested Vector Interrupt Controller
6. Internal ADC
7. External ADC
8. Internal Flexible Static Memory Controller (FSMC)

16.1.1 Processor

Requirement ID: H398-SRS-ANA-DRQ-18

MOPS: No

Safety Requirement: No

Rationale: The Processor initialization required to execute the software is derived from hardware architecture document HE0398AHA and to execute the application software in normal mode

Verification Method: Testing

The Analog Module shall initialize the processor as follows:

1. Enable HSE (high speed external clock).
2. Enable power interface clock
3. Configure power regulator voltage scale 1
4. Set CPU clock as System Clock
5. Set PCLK1 = CPU clock / 4
6. Set PCLK2 = HCLK clock/ 2
7. Set 5 wait states as the latency period on Flash
8. Enable instruction cache
9. Enable data cache
10. Enable flash prefetch buffer
11. Set PLLCLK = ((25MHz / PLL\_M) \* PPL\_N) / PLL\_P = 168 MHz.
12. Enable PLL.
13. Select PLL as system clock source.
14. Initialize the interrupt vector table in RAM.
15. Set the Vector Table base address at RAM
16. Configure the group priority equal sixteen and sub-priority is zero
17. Set the priority of the system tick interrupt as 15
18. Set the priority of the PendSV interrupt as 14
19. Enable CRC peripheral clock
20. Initializing the FPU context save not to be in lazy mode
21. Enable floating point coprocessor
22. Enable Memory Management Fault, Bus Fault and Usage Fault exceptions in SHCSR register.
23. Enable Usage Fault in Configuration Control Register.
24. Enable FSMC Clock.
25. Enable system configuration clock.
26. Enable GPIOA and GPIOB clock.
27. Configure GPIO Pin 2, Pin 9, Pin 10, Pin 11, Pin 12 of Port B for Heartbeat LED,DAC Selection,Decoder1,Decoder2 and Decoder3 respectively (speed = 50Mhz, mode = output mode, pull-up/pull-down as pull-up, output type as output push pull).
28. Enable GPIOC clock.
29. Configure GPIO Pin 0 of Port C for ADC input (speed = 50Mhz, mode = Analog mode, pull-up/pull-down as no pull-up/pull down).
30. Configure GPIO Pin 10 (reference control), 11 (External ADC conversion start) and 2 (mux select 0), 3 (mux select 1), 4 (mux select 2), 5 (mux select 3) of Port C (mode = output mode, pull-up/pull-down as no pull-up/pull down, output type as output push pull).
31. Enable GPIOD clock.
32. Configure GPIO pins 0, 1, 8, 9, 10, 14 and 15 of port D as FSMC alternate function output pins for data bus bits 2, 3, 13, 14, 15, 0 and 1 respectively (mode = alternate function mode, pull-up/pull-down as no pull-up/pull down, output type as output push pull)
33. GPIO pins 4, 5 and 7 of port D as FSMC OE, FSMC WE FSMC and FSMC NE1 alternate function output pins respectively (speed = 50Mhz, mode = alternate function mode, pull-up/pull-down as no pull-up/pull down, output type as output push pull)
34. Enable GPIOE clock.
35. Configure GPIO pins 7, 8, 9, 10, 11, 12, 13, 14 and 15 of port E as FSMC alternate function output pins for data bus bits 4, 5, 6, 7, 8, 9, 10, 11 and 12 respectively (speed = 50Mhz, mode = alternate function mode, pull-up/pull-down as no pull-up/pull down, output type as output push pull).

16.1.2 Watchdog timer

Requirement ID: H398-SRS-ANA-DRQ-19

MOPS: No

Safety Requirement: No

Rationale: The Watchdog Timer initialization is required to monitor the processor idle state

Verification Method: Testing

The Analog module shall initialize the Watchdog timer to 1 second.

16.1.3 System Timer

Requirement ID: H398-SRS-ANA-DRQ-20

MOPS: No

Safety Requirement: No

Rationale: The System Timer initialization is required to perform periodic scheduling of tasks

Verification Method: Testing

The Analog module shall initialize the System Timer to generate 10000 interrupts every second.

16.1.4 CAN peripheral

Requirement ID: H398-SRS-ANA-DRQ-21

MOPS: No

Safety Requirement: No

Rationale: The initialization of CAN peripheral is required to communicate to Gateway

Verification Method: Testing

The Analog module shall initialize the CAN peripheral as follows:

1. Connect Port A GPIO Pins #11 (Alternate Function 9, No-Pull) and #12 (Alternate Function 9, Push-Pull, No-Pull)

2. Configure mode, speed, output type and pull-up/pull-down type of GPIO Pins #11 and #12 as Alternate Function mode, fast speed, Output push-pull, and pull-up respectively

3. Disable the triggered communication mode, automatic wake-up mode, non-automatic retransmission mode, Receive FIFO Locked mode and Transmit FIFO priority

4. Enable Bus-Off recovery

5. Set Baud rate to 1Mbps.

6. Set up filter #0 to allow all messages and attach the filter to FIFO #0.

16.1.5 Nested Vector Interrupt Controller

Requirement ID: H398-SRS-ANA-DRQ-22

MOPS: No

Safety Requirement: No

Rationale: The initialization of Nested Vector Interrupt Controller required to execute the software

Verification Method: Testing

The Analog module shall initialize the nested vectored interrupt controller to respond to CAN receive and transmit interrupts as follows:

1. Rx Interrupt: Enable NVIC channel#20 and set its Pre-emption priority and Sub Priority to 0

2. Tx Interrupt: Enable NVIC channel#19 and set its Pre-emption priority and Sub Priority to 0

16.1.6 Internal ADC

Requirement ID: H398-SRS-ANA-DRQ-23

MOPS: No

Safety Requirement: No

Rationale: The initialization of Internal ADC is required to process the cold junction temperature for typeK thermo couple inputs

Verification Method: Testing

The Analog module shall initialize Internal ADC module #1 with 12-bit resolution, DMA mode using DMA2 Stream #0 for Cold junction temperature measurement.

16.1.7 External ADC

Requirement ID: H398-SRS-ANA-DRQ-24

MOPS: No

Safety Requirement: No

Rationale: The initialization of external ADC is required to process the analog inputs

Verification Method: Testing

The Analog module shall initialize External ADC hardware with Port C, GPIO Pin #11 is used to end the ADC sample and start conversion on the captured sample i.e

PC11 is set low - initiates conversion on external ADC

PC11 is set high - converted values can be read

16.1.8 Internal Flexible Static Memory Controller (FSMC)

Requirement ID: H398-SRS-ANA-DRQ-25

MOPS: No

Safety Requirement: No

Rationale: The Initialisation of FSMC is required to access external memory address space

Verification Method: Testing

The Analog module shall initialize Internal Flexible Static Memory Controller (FSMC) to access external ADC.

16.1.9 SPI peripheral

Requirement ID: H398-SRS-ANA-DRQ-82

MOPS: No

Safety Requirement: No

Rationale: The SPI peripheral initialization required to interface with Analog to digital converters for reading the analog inputs.

Verification Method: Testing

The Analog Module shall initialize the SPI2 peripheral as follows:

1. Enable SPI2 peripheral clock

2. Set GPIO Pins #13 and #15 for SCK and MOSI as Alternate Function mode

3. Set GPIO Pin #14 for MISO as Alternate Function mode

4. Configure the SPI2 global interrupt

5. Configure SPI2 peripheral as Direction is Full Duplex, SPI mode is Master mode, Data size is 16 bits, Clock Polarity as Low, Clock phase as Edge1, Slave as soft. Baud rate pre scalar to 16, first bit transmission is MSB

6. Set up SPI2 interrupt

7. Enable SPI2 peripheral.

**16.2 Modes of Operation**

This section specifies the Software High Level Requirements for the operational modes of the Analog Module.

16.2.1 Operational Modes

The Analog Module operates in different mode to perform its various responsibilities. The different modes are

1. Power-On BIT mode

2. Normal Mode

3. Error Mode

16.2.1.1 PBIT Mode

Requirement ID: H398-SRS-ANA-DRQ-28

MOPS: No

Safety Requirement: No

Rationale: This is required to identify the PBIT mode of application software

Verification Method: Testing

The Analog Module shall perform a power-up built-in test during PBIT mode.

16.2.1.2 Normal Mode

Requirement ID: H398-SRS-ANA-DRQ-29

MOPS: No

Safety Requirement: No

Rationale: This is required to identify the normal mode of application software

Verification Method: Testing

The Analog Module shall perform the following activities in Normal mode:

1. Read Analog Sensor Inputs and apply the required scaling to Sensor readings.

2. Set Excitation Outputs

3. Perform A825 communication with the Gateway Module.

4. Toggle the Heartbeat LED and reload the watch dog counter every 500ms.

16.2.1.3 Error Mode

Requirement ID: H398-SRS-ANA-DRQ-30

MOPS: No

Safety Requirement: No

Rationale: This is required to identify the error mode of application software

Verification Method: Testing

In Error mode, the Analog Module shall perform the following

1. cease all current activities

2. switch the Heartbeat LED as steady on.

**16.3 Inputs/Outputs**

This section specifies the Software High Level Requirements for Analog Inputs and Outputs.

16.3.1 Analog Inputs

Requirement ID: H398-SRS-ANA-FNC-32

MOPS: Yes

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall read the all the Analog Sensor Inputs depicted in Table: Analog Inputs in every 100ms:

*Table 4: Analog Inputs*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Signal Name** | **Signal Type** | **Channel Name** | **Sensor Type** | **Input Signal Range** | **Tolerance** | **Number of Instances per channel** | **Conversion Method** |
| Engine Gas Generator Speed (NG) | FR175m | TACH\_1  TACH\_2 | High Frequency Signal | 0% to 125% | ±0.1% | 2 – NG1, NG2 | As per SYS2160SRS |
| Differential NG (ΔNG) | PWC100 | Duty Cycle | Pulse Width Measurement | 10 % to 90% | ±0.8% to ±1.6% | 2 - ΔNG1, ΔNG2 | As per SYS2160SRS |
| Exhaust gas output temperature  (T4) | TCK | LL\_1,  LL\_2 | K Type Thermocouple | -200°C to 1294°C | ±5°C | 2 – TOT1, TOT2 | As per HE0398AHA |
| TOT\_R | RS1000 | RTD\_6  RTD\_7 | Resistance Temp. Device | 0 Ω to 1160.5 Ω | ±8.4 Ω | 2 – TOT1\_R, TOT2\_R | As per HE0398AHA |
| Torque  (TRQ) | VD12 | HL\_1,  HL\_2 | Differential DC Voltage | -12.207V to 12.207V | ±80mV | 2- TRQ1, TRQ2 | As per HE0398AHA |
| Engine Oil Temperature  (EOT) | RS300 | RTD\_1,  RTD\_2 | Resistance Temp. Device | 0.00Ω to 313.63Ω | ±1.8 to ±3.2 Ω | 2 – EOT1, EOT2 | As per HE0398AHA |
| Main Gear Box Oil Temperature  (MGBT) | RS1k | RTD\_9 | Resistance measurement | 0.0Ω to 1160.5Ω | ±8.4 Ω | 1 - MGBT | As per HE0398AHA |
| Engine Oil Pressure  (EOP) | VDS300m | LL\_3,  LL\_4, | Differential DC Voltage | -318.16mV to 318.16mV | ±1.5mV to ±2.5mV | 2 – EOP1, EOP2 | As per HE0398AHA |
| Engine Oil Pressure Reference  (EOP REF) | VD12 | HL\_RMS\_01,  HL\_RMS\_03 | Differential DC Voltage | -12.207V to 12.207V | ±0.5V | 2 – EOP1 REF, EOP2 REF | As per HE0398AHA |
| Main Gear Box Oil Pressure  (MGBOP) | VD12 | HL\_RMS\_14 | Differential DC Voltage | -12.207V to 12.207V | ±80mV | 1 – MGBOP | As per HE0398AHA |
| Main Gear Box Oil Pressure Reference  (MGBOP REF) | VD12 | HL\_RMS\_13 | Differential DC Voltage | -12.207V to 12.207V | ±0.5V | 1 – MGBOP REF | As per HE0398AHA |
| Fuel pressure  (FP) | VD12 | HL\_RMS\_06  HL\_RMS\_08 | Differential DC Voltage | -12.207V to 12.207V | ±80mV | 2 – FP1, FP2 | As per HE0398AHA |
| Fuel pressure Reference  (FP REF) | VD12 | HL\_RMS\_05  HL\_RMS\_07 | Differential DC Voltage | -12.207V to 12.207V | ±0.5V | 2 – FP1 REF, FP2 REF | As per HE0398AHA |
| Left hand side Hydraulic Pressure  (LHP) | VD12 | HL\_RMS\_10 | Differential DC Voltage | -12.207V to 12.207V | ±80mV | 1 - LHP | As per HE0398AHA |
| Left hand side Hydraulic Pressure Reference  (LHP REF) | VD12 | HL\_RMS\_09 | Differential DC Voltage | -12.207V to 12.207V | ±0.5V | 1 – LHP\_REF | As per HE0398AHA |
| Right hand side Hydraulic Pressure  (RHP) | VD12 | HL\_RMS\_12 | Differential DC Voltage | -12.207V to 12.207V | ±80mV | 1 - RHP | As per HE0398AHA |
| Right hand side Hydraulic Pressure Reference  (RHP REF) | VD12 | HL\_RMS\_11 | Differential DC Voltage | -12.207V to 12.207V | ±0.5V | 1 – RHP REF | As per HE0398AHA |
| Turbine Outlet Temperature Output  (TOT Output) | VDO5 | DAC4  DAC5 | DC Voltage | -5.250V to 5.250V | ±30mV to ±45 mV | 2 – TOT1 OUT, TOT2 OUT | As per HE0398AHA |
| Main Gear Box Temperature Output  (MGBT Output) | VDO5 | DAC6 | DC Voltage | -5.250V to 5.250V | ±60mV | 1 – MGBT OUT | As per HE0398AHA |
| Main Gear Box Oil Pressure Output  (MGBOP Output) | VDO5 | DAC7 | DC Voltage | -5.250V to 5.250V | ±80mV | 1 – MGBOP OUT | As per HE0398AHA |

Note: To meet the tolerance mentioned above, Stored Calibration offset and gain will be applied to the sensor reading values. Calibration offset and gain will be determined by maintenance operator and stored during maintenance mode.

#### 16.3.1.1 Parameter sensors

Requirement ID: H398-SRS-ANA-FNC-85

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog module shall read the electrical signals from the engines and vehicle parameter sensors shown in H398-SRS-ANA-FNC-32.

16.3.2 Status of Input Signals

Requirement ID: H398-SRS-ANA-FNC-33

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall set status of all input signals to one of the following status:

1. CHANNEL ERROR

2. RANGE ERROR

3. OK

16.3.3 CHANNEL ERROR

Requirement ID: H398-SRS-ANA-FNC-34

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

If a range error is detected on the BIT channel of XADC Bank which measures an input signal, then Analog Module shall set the status of input signal to CHANNEL ERROR and assign the Scaled Reading to the Default value of the signal.

BIT Channel Min Voltage: -2.5V

BIT Channel Max Voltage: 2.5V

16.3.4 RANGE ERROR

Requirement ID: H398-SRS-ANA-FNC-35

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

If the Scaled Reading of an input signal is outside its Range then Analog Module shall set the status of input signal to RANGE ERROR and if default attribute of the input signal is disabled, assign the Scaled Reading to the value of the nearest endpoint of the Range, otherwise Scaled Reading is assigned with default value defined in the module configuration data.

Note: Refer H398-SRS-ANA-FNC-32 for range of the input signals.

16.3.5 OK status

Requirement ID: H398-SRS-ANA-FNC-36

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall set the status of an input signal to OK if neither CHANNEL ERROR nor RANGE ERROR is detected for the signal.

16.3.6 AFCS Engine 1 T4 value

Requirement ID: H398-SRS-ANA-FNC-83

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall set the "AFCS Engine 1 T4 value" as follow:

if Engine 1 T4 validity is valid then

AFCS Engine 1 T4 Value (V) = Engine 1 T4 Value (°C) / 180

else

AFCS Engine 1 T4 Value (V) = 0

16.3.7 AFCS Engine 2 T4 value

Requirement ID: H398-SRS-ANA-FNC-84

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog module shall set the "AFCS Engine 2 T4 value" as follow:

if Engine 2 T4 validity is valid then

AFCS Engine 2 T4 Value (V) = Engine 2 T4 Value (°C) / 180

else

AFCS Engine 2 T4 Value (V) = 0

16.3.8 Engine 1 T4 value

Requirement ID: H398-SRS-ANA-FNC-86

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog module shall set the “Engine 1 T4 value” for each engine as follows:

1. If Engine 1 T4 validity is valid:

* Engine 1 T4 Value (°C) = Engine 1 T4 raw value (°C) x (A x (Engine 1 T4 corrective value)2 + B x Engine 1 T4 corrective value + C)

1. If Engine 1 T4 validity is not valid:
   * Engine 1 T4 Value (°C) = 0

With

A = 1.70166347 E-07

B = -5.05615343 E-04

C = 1.07

16.3.9 Engine 2 T4 value

Requirement ID: H398-SRS-ANA-FNC-87

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog module shall set the “Engine 2 T4 value” for each engine as follows:

1. If Engine 2 T4 validity is valid:

* Engine 2 T4 Value (°C) = Engine 2 T4 raw value (°C) x (A x (Engine 2 T4 corrective value)2 + B x Engine 2 T4 corrective value + C)

1. If Engine 2 T4 validity is not valid:

* Engine 2 T4 Value (°C) = 0

With

A = 1.70166347 E-07

B = -5.05615343 E-04

C = 1.07

**16.4 A825 communication**

This section specifies the Software High Level Requirements for the A825 communication.

Note: Refer ARINC SPECIFICATION 825-2 for A825 communication protocol.

16.4.1 Logical Communication Channel

Requirement ID: H398-SRS-ANA-FNC-38

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall use the following Logical Communication Channels to communicate over the A825 bus with the Gateway Module.

1. Node Service Channel (NSC)

2. Normal Operation Channel (NOC)

16.4.2 Invalid A825 message

Requirement ID: H398-SRS-ANA-FNC-39

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall ignore an A825 message if it is invalid.

Note: an invalid message is one which does not satisfy the specified NSC/NOC message formats.

16.4.3 NSC channel

This section specifies the Software High Level Requirements for messages sent over NSC channel.

16.4.3.1 NSC message format

Requirement ID: H398-SRS-ANA-FNC-41

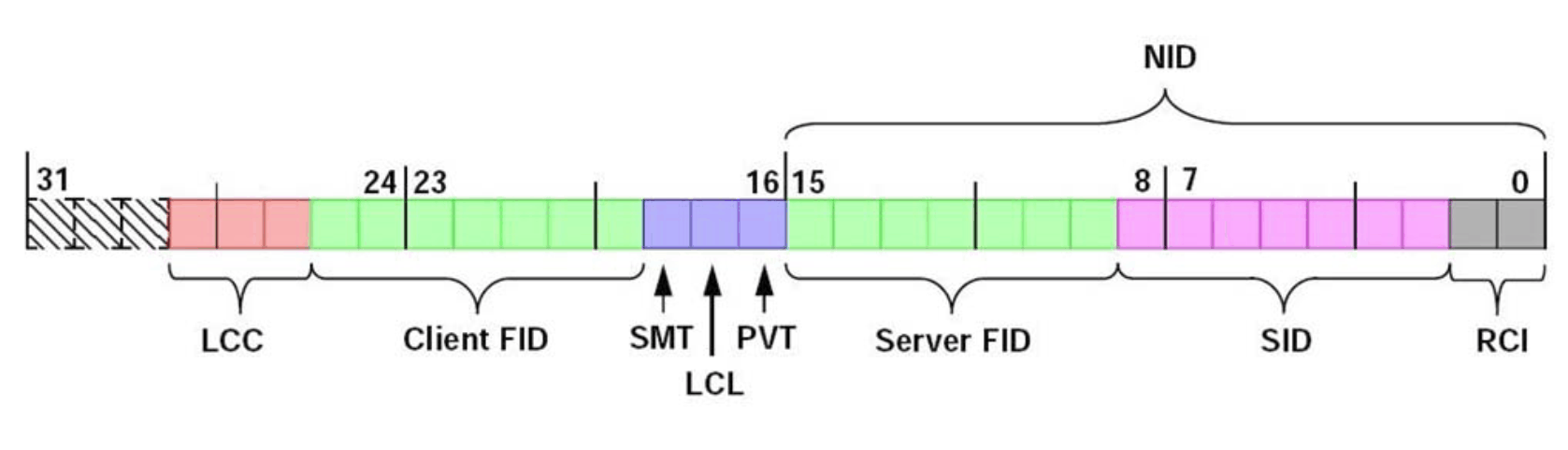
MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall use the message structure as depicted in Figure: Message Structure - NSC channel while using the NSC channel.



*Figure 4: Message Structure - NSC channel*

Note:

i. LCC - Indicates the Logical Communication Channel

ii. Client FID - always HOWELL\_DAU\_FID (42)

iii. SMT - Indicates whether message is Request (1) or Response (0)

iv. LCL - messages is designated only for the network the transmitting node resides in - always 1

v. PVT - messages which have no meaning to nodes other than those which are specifically programmed to use them - always 1

vi. Server FID - Always HOWELL\_DAU\_FID (42)

vii. Server ID - Specifies the recipient node for the message

viii. RCI - Redundancy Channel Identifier.

16.4.3.2 NSC messages

Requirement ID: H398-SRS-ANA-FNC-42

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall use the following Service Function Codes in its A825 communication over the Node Service Channel.

*Table 5: Service Function Codes - NSC*

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **SFC** | **Client FID** | **SMT** | **LCL** | **PVT** | **Server FID** | **Server ID** | **Rx/Tx** | **RCI** | **DLC** | **Description** | **Payload** |
| NSC\_SET\_RCI(49152) | HOWELL\_DAU\_FID(42) | 1 | 1 | 1 | HOWELL\_DAU\_FID(42) | MULITCAST\_SID(0) or ANALOG\_SID(2) | Rx | 3 | 3 | Command to the Analog Module to adopt the specified RCI | The first two bytes of the payload contain the SFC 'NSC\_SET\_RCI'. The next byte contains the desired RCI. Once this data has been received, each data acquisition node will use this RCI for ARINC 825 communication |
| NSC\_EXCITE\_SWITCH(49156) | HOWELL\_DAU\_FID(42) | 1 | 1 | 1 | HOWELL\_DAU\_FID(42) | MULITCAST\_SID(0) or ANALOG\_SID(2) | Rx | 0 | 3 | Command to Analog Module to switch on/off its excitation outputs | The first two bytes of the payload contain the SFC 'NSC\_EXCITE\_SWITCH'. The third byte is (OFF = 0, ON = 1). |
| NSC\_RESET(44544) | HOWELL\_DAU\_FID(42) | 1 | 1 | 1 | HOWELL\_DAU\_FID(42) | ANALOG\_SID(2) | Rx | 0 | 3 | Command to Analog Module to reset the Analog CPU. | The first two bytes of the payload contain the SFC ‘NSC\_RESET'. |

Note:

1. Rx/Tx - Indicates whether Analog Module Receives (Rx) or Transmits (Tx) the message.

2. DLC - Data Length Count - size of the payload in bytes.

16.4.3.3 Enable Excitation

Requirement ID: H398-SRS-ANA-FNC-43

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

For any NSC message with SFC = NSC\_EXCITE\_SWITCH (49156), the Analog Module shall enable its excitation outputs if the payload contains 1.

Note:

Analog Module turns on the excitation current of 0.5mA once it receives the command from gateway module.

16.4.3.4 Disable Excitation

Requirement ID: H398-SRS-ANA-FNC-44

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

For any NSC message with SFC = NSC\_EXCITE\_SWITCH (49156), the Analog Module shall disable its excitation outputs if the payload contains 0.

Note:

Analog board turns off the excitation current of 0.5mA once it receives the command from the gateway module.

16.4.3.5 Setting RCI value

Requirement ID: H398-SRS-ANA-FNC-45

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall set its RCI to the value received from Gateway via A825 message (LCC = NSC and SFC = NSC\_SET\_RCI (49152).

16.4.3.6 Reset Analog CPU

Requirement ID: H398-SRS-ANA-DRQ-48

MOPS: No

Safety Requirement: No

Rationale: Resetting the analog board is required to support software verification activities

Verification Method: Testing

For any NSC message with SFC = NSC\_RESET (44544), the Analog Module shall reset the Analog Module CPU, if the server ID matches with the analog server ID.

Note: For analog server ID, refer H398-SRS-ANA-FNC-42.

16.4.4 NOC channel

This section specifies the Software High Level Requirements for messages sent over NOC channel.

16.4.4.1 NOC message format

Requirement ID: H398-SRS-ANA-FNC-50

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall use the message structure depicted in Figure: Message Structure - NOC channel while using the NOC channel.



*Figure 5: Message Structure - NOC channel*

Note:

i. LCC - Indicates the Logical Communication Channel

ii. Source FID - always HOWELL\_DAU\_FID (42)

iii. RSD - Reserved - always 0

iv. LCL - messages is designated only for the network the transmitting node resides in - always 1

v. PVT - messages which have no meaning to nodes other than those which are specifically programmed to use them - always 1

vi. DOC - Data Object Code

vii. RCI - Redundancy Channel Identifier.

16.4.4.2 NOC messages

Requirement ID: H398-SRS-ANA-FNC-51

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall use the Data Object Codes in its A825 communication over the Normal Operation Channel depicted in the Table : Document Object Codes - NOC .

*Table 6: Document Object Codes - NOC*

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **DOC** | **Source FID** | **RSD** | **LCL** | **PVT** | **RCI** | **Rx/Tx** | **DLC** | **Description** | **Payload** |
| 0 | 42 | 0 | 1 | 1 | Refer note 3 | Rx | 0 | Gateway to trigger for Analog Module to send its Scaled Inputs and Status of Inputs | NA |
| 2700 | 42 | 0 | 1 | 1 | Refer note 3 | Rx | 0 | Gateway to trigger Analog Module to transmit Part number and CRCs of Application and configuration | NA |
| 500 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels   1. BIT\_1 with resolution of 0.01 volts 2. L\_SENSE\_1 (SPARE\_1) 3. L\_SENSE\_2 (SPARE\_2) 4. LL\_1 (TOT1) with resolution of 0.1ºC | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 501 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels   1. LL\_2 (TOT2) with resolution of 0.1ºC 2. LL\_3 (EOP1) with resolution of 0.01mV 3. LL\_4 (EOP2) with resolution of 0.01mV 4. RTD\_1 (EOT1) with 0.01ohms | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 502 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A. BIT\_2 with resolution of 0.01 volts  B. RTD\_2 (EOT2) with 0.01ohms  C. RTD\_3 (SPARE\_3)  D. RTD\_4 (SPARE\_4) | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 503 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels.  A. RTD\_5 (SPARE\_5)  B. RTD\_6 (TOT\_R1) with 0.1ohms  C. RTD\_7 (TOT\_R2) with 0.1ohms  D. RTD\_8 (SPARE\_8) | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 504 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.BIT\_3 with resolution of 0.01 volts  B.RTD\_9 (MGBT) with 0.1ohms  C. HL\_1 (TRQ1) with resolution of 0.001 volts  D.HL\_2 (TRQ2) with resolution of 0.001 volts | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 505 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.HL\_RMS\_01 (EOP1 REF) with resolution of 0.001 volts  B.HL\_RMS\_02 (SPARE\_9)  C.HL\_RMS\_03 (EOP2 REF) with resolution of 0.001 volts  D.HL\_RMS\_04 (SPARE\_10) | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 506 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A. BIT\_4 with resolution of 0.01 volt  B.HL\_RMS\_05 (FP1 REF) with resolution of 0.001 volts  C.HL\_RMS\_06 (FP1) with resolution of 0.001 volts  D.HL\_RMS\_07 (FP2 REF) with resolution of 0.001 volts | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 507 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.HL\_RMS\_08 (FP2) with resolution of 0.01 volts  B.HL\_RMS\_09 (LHP\_REF) with resolution of 0.001 volts  C.HL\_RMS\_10 (LHP) with resolution of 0.001 volts  D.HL\_RMS\_11 (RHP\_REF) with resolution of 0.001 volts | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 508 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.BIT\_5 with resolution of 0.01 volt  B.HL\_RMS\_12 (RHP) with resolution of 0.001 volts  C.HL\_RMS\_13 (MGBOP\_REF) with resolution of 0.001 volts  D.HL\_RMS\_14 (MGBOP) with resolution of 0.001 volts | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 509 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.HL\_RMS\_15 (SPARE\_11)  B.HL\_RMS\_16 (SPARE\_12)  C.HL\_RMS\_17 (SPARE\_13)  D.HL\_RMS\_18 (SPARE\_14) | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 510 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.SPARE  B.DELTA NG1 (Duty Cycle)  C.DELTA NG2 (Duty Cycle)  D.TACH\_1(NG1) | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 511 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.TACH\_2(NG2)  B.TACH\_3(SPARE)  C.TACH\_4(SPARE)  D.TACH\_5(SPARE) | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 512 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Scaled values of the following Analog channels  A.TACH\_6(SPARE)  B.  C.  D. | Each input is reported as 2 bytes of the payload. Analog channel A appears as the first two bytes of the payload. Analog channel B appears as the third and fourth byte, and so on. |
| 600 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Status of Analog input Parameters from 1 to 32.  (Channels 1 – 8 of Bank #1 to Channels 1 – 8 of Bank #4 | Two bits of status for each channel  Value 00 represents Channel OK, Value 01 represents Range Error, Value 10 represents Channel Error and Value 11 has no meaning. |
| 601 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Status of Analog input Parameters from 33.  (Channels 1 – 8 of Bank #5, DeltaNG1, DeltaNG2, Channels 1 – 6 for TACH) | Two bits of status for each channel  Value 00 represents Channel OK, Value 01 represents Range Error, Value 10 represents Channel Error and Value 11 has no meaning. |
| 2743 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Bootloader Part number bytes 0-7 | Analog Bootloader Part number bytes 0-7 stored in bootloader memory section |
| 2744 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Bootloader Part number bytes 8-15 | Analog Bootloader Part number bytes 8-15 stored in bootloader memory section |
| 2745 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Bootloader 32- bit CRC  Byte 0 to 3: CRC  Byte 4 to 7: 0 | Analog Bootloader 32- bit CRC is embedded in  Byte 0 is LS Byte 3 is MS Byte. |
| 2746 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Flight Application Part number bytes 0-7 | Analog Flight Application Part number bytes 0-7 stored in Analog Driver Application memory section |
| 2747 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Flight Application Part number bytes 8-15 | Analog Flight Application Part number bytes 8-15 stored in Analog Driver Application memory section |
| 2748 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Flight Application 32- bit CRC  Byte 0 to 3: CRC  Byte 4 to 7: 0 | Analog Flight Application 32- bit CRC is embedded in  Byte 0 is LS Byte 3 is MS Byte. |
| 2749 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Flight Configuration Part number bytes 0-7 | Analog Flight Configuration Part number bytes 0-7 stored in Analog Driver Configuration memory section |
| 2750 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Flight Configuration Part number bytes 8-15 | Analog Flight Configuration Part number bytes 8-15 stored in Analog Driver Configuration memory section |
| 2751 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Flight Configuration 32- bit CRC  Byte 0 to 3: CRC  Byte 4 to 7: 0 | Analog Flight Configuration 32- bit CRC is embedded in  Byte 0 is LS Byte 3 is MS Byte. |
| 2752 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Boot Configuration Part number bytes 0-7 | Analog Boot Configuration Part number bytes 0-7 stored in Analog Driver Configuration memory section |
| 2753 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Boot Configuration Part number bytes 8-15 | Analog Boot Configuration Part number bytes 8-15 stored in Analog Driver Configuration memory section |
| 2754 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Boot Configuration 32- bit CRC  Byte 0 to 3: CRC  Byte 4 to 7: 0 | Analog Boot Configuration 32- bit CRC is embedded in  Byte 0 is LS Byte 3 is MS Byte. |
| 2758 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Software Loader Part number bytes 0-7 | Analog Software Loader Part number bytes 0-7 stored in Analog Driver Configuration memory section |
| 2759 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Software Loader Part number bytes 8-15 | Analog Software Loader Part number bytes 8-15 stored in Analog Driver Configuration memory section |
| 2760 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Software Loader 32- bit CRC  Byte 0 to 3: CRC  Byte 4 to 7: 0 | Analog Software Loader 32- bit CRC is embedded in  Byte 0 is LS Byte 3 is MS Byte. |
| 2761 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Calibration Software Part number bytes 0-7 | Analog Calibration Software Part number bytes 0-7 stored in Analog Driver Configuration memory section |
| 2762 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Calibration Software Part number bytes 8-15 | Analog Calibration Software Part number bytes 8-15 stored in Analog Driver Configuration memory section |
| 2763 | 42 | 0 | 1 | 1 | Refer note 3 | Tx | 8 | Analog Calibration Software 32- bit CRC  Byte 0 to 3: CRC  Byte 4 to 7: 0 | Analog Calibration Software 32- bit CRC is embedded in  Byte 0 is LS Byte 3 is MS Byte. |

Note:

1. Rx/Tx - Indicates whether Analog module Receives (Rx) or Transmits (Tx) the message

2. DLC - Data Length Count - size of the payload in bytes

3. When SFC 'NSC\_SET\_RCI' in First two bytes and RCI in Third byte is received from Gateway module, Analog module will use this RCI for ARINC 825 communication otherwise RCI is considered as 3.

16.4.4.3 NOC message reply (Analog inputs)

Requirement ID: H398-SRS-ANA-FNC-52

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

When the Analog Module receives an A825 message from Gateway Module with LCC = NOC and DOC = 0 then it shall perform as follows:

1. Scale all Input readings
2. Transmit these Scaled Input readings to Gateway via A825 bus using LCC = NOC and DOC = {500 to 512, 600, 601} by applying the resolution as mentioned in H398-SRS-ANA-FNC-51.

16.4.4.4 NOC message reply (Part number and CRC)

Requirement ID: H398-SRS-ANA-FNC-78

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

When the Analog Module receives an A825 message from Gateway Module with LCC = NOC and DOC = 2700 then it shall perform as follows:

1. Transmit Part number of Analog Boot Module via A825 bus using LCC = NOC and DOC = {2743, 2744}
2. Transmit CRC of Analog Boot Module via A825 bus using LCC = NOC and DOC = {2745}
3. Transmit Part number of Analog Boot Config via A825 bus using LCC = NOC and DOC = {2752, 2753}
4. Transmit CRC of Analog Boot Config via A825 bus using LCC = NOC and DOC = {2754}
5. Transmit Part number of Analog Flight Application via A825 bus using LCC = NOC and DOC = {2746, 2747}
6. Transmit CRC of Analog Flight Application via A825 bus using LCC = NOC and DOC = {2748}
7. Transmit Part number of Analog Flight Config via A825 bus using LCC = NOC and DOC = {2749, 2750}
8. Transmit CRC of Analog Flight Config via A825 bus using LCC = NOC and DOC = {2751}
9. Transmit Part number of Software Loader via A825 bus using LCC = NOC and DOC = {2758, 2759}
10. Transmit CRC of Software Loader via A825 bus using LCC = NOC and DOC = {2760}
11. Transmit Part number of Calibration Software via A825 bus using LCC = NOC and DOC = {2761, 2762}
12. Transmit CRC of Calibration Software via A825 bus using LCC = NOC and DOC = {2763}

**16.5 Module Configuration Data**

This section specifies the Software High Level Requirements of Module Configuration Data for the Analog Module.

16.5.1 Module Configuration Data - Definition

Requirement ID: H398-SRS-ANA-DRQ-54

MOPS: No

Safety Requirement: No

Rationale: Required to define the various sections of Module Configuration Data used to make the software configurable.

Verification Method: Testing

The Analog Module shall have Module Configuration Data.

1. Module Configuration Data consists of Part Number of config Data, Configuration Attributes of the External ADC, Internal ADC Channels and 32-bit CRC of the Config data. Refer the Table : *Module Configuration Data*

*Table 7: Module Configuration Data*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Attribute** | **Description** | **Value** | **Field length (bytes)** | **Remarks** |
| PART Number | Config data Part number | Configurable as per need.  Refer H398-SRS-ANA-DRQ-76 for part number format. | 16 | For entire Config Data |
| Channel Status | Specifies the ADC channel is Enable or Disable | Enable: 1  Disable : 0 | 4 | Each Channel |
| Default Value Status | Specifies whether the default value can be set for the ADC channel or not. | Enable: 1  Disable: 0 | 4 | Each Channel |
| Default Value | Specifies the default value of the ADC channel | 0 | 2 | Each Channel |
| Calibrate | Specifies the ADC channel is Calibrate | TRUE: 1  FALSE: 0 | 1 | Each Channel |
| Low Calibrate Point | Specifies the ADC count for Calibrating low point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| High Calibrate Point | Specifies the ADC count for Calibrating high point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| ADC Channel Sensor Type | Specifies the type of the ADC channel | 0: CAL\_DIS\_MV, mVDC  1: CAL\_DIS\_V, VDC  2: CAL\_DIS\_TEMPC, TCK °C  3: CAL\_DIS\_TEMPF, °F  4: CAL\_DIS\_OHM, Ohms | 4 | Each Channel |
| Low Calibrate Value | Specifies the value for Calibrating low point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| High Calibrate Value | Specifies the value for Calibrating high point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| Resolution | Specifies the resolution value | 0 to 1000 | 2 | Each Channel |
| Excitation | Specifies Excitation required for the channel. | TRUE: 1  FALSE: 0 | 1 | Each Channel |
| Sensor Table (ADC reading in voltage) | Specifies the pointer to the table for the voltage reading of the ADC channel. | Valid reference to Lookup table for voltage reading of the ADC channel. | 4 | Each Channel |
| Sensor Table (Sensor unit) | Specifies the pointer to the table of the Sensor units for the corresponding voltage reading of the ADC channel. | Valid reference to Lookup table for Sensor units for the corresponding voltage reading of the ADC channel. | 4 | Each Channel |
| Minimum Value | Specifies the minimum limit of the Scaled Reading. | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| Maximum Value | Specifies the maximum limit of the Scaled Reading. | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |

Note: The CRC field is filled during build process.

Table : Tach Sensor

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Attribute | Description | Value | Field length  (bytes) | Remarks |
| PART Number | Config data Part number | Configurable as per need.  Refer H398-SRS-ANA-DRQ-76 for part number format. | 16 | For entire Config Data |
| Channel State | Specifies the ADC channel is Enable or Disable | Enable: 1  Disable: 0 | 4 | Each Channel |
| Default State | Specifies whether the default value can be set for the ADC channel or not. | Enable: 1  Disable: 0 | 4 | Each Channel |
| Default Value | Specifies the default value of the ADC channel | 0 | 2 | Each Channel |
| Reference Frequency | Specifies the reference frequency for the read signal | Configurable as per need, range is from 70.0f to 7785.0f | 4 | Each Channel |
| Scaled reading | Specifies the scaling value for the reference frequency of the signal | 1000 | 2 | Each Channel |
| Minimum Range | Specifies the minimum limit of the Scaled Reading. | range is from 0 to 65535 | 2 | Each Channel |
| Maximum Range | Specifies the maximum limit of the Scaled Reading. | range is from 0 to 65535 | 2 | Each Channel |
| Resolution | Specifies the resolution value.  Note: This parameter can be used Calibration software only. | range is from 0 to 10 | 2 | Each Channel |

Table : DAC Sensor

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Attribute** | **Description** | **Value** | **Field length (bytes)** | **Remarks** |
| PART Number | Config data Part number | Configurable as per need.  Refer H398-SRS-ANA-DRQ-76 for part number format. | 16 | For entire Config Data |
| Channel Status | Specifies the ADC channel is Enable or Disable | Enable: 1  Disable: 0 | 4 | Each Channel |
| Default State | Specifies whether the default value can be set for the ADC channel or not. | Enable: 1  Disable: 0 | 4 | Each Channel |
| Default Value | Specifies the default value of the ADC channel | 0 | 2 | Each Channel |
| Calibrate | Specifies the ADC channel is Calibrate | Yes: TRUE  No: FALSE | 1 | Each Channel |
| Low Calibrate Point | Specifies the ADC count for Calibrating low point | range is from -2147483648 to 2147483647 | 4 | Each Channel |
| High Calibrate Point | Specifies the ADC count for Calibrating high point | range is from -2147483648 to 2147483647 | 4 | Each Channel |
| C type | Specifies the type of the ADC channel | 0: CAL\_DIS\_MV, mVDC  1: CAL\_DIS\_V, VDC  2: CAL\_DIS\_TEMPC, TCK °C  3: CAL\_DIS\_TEMPF, °F  4: CAL\_DIS\_OHM, Ohms | 4 | Each Channel |
| Low Calibrate Value | Specifies the value for Calibrating low point | range is from -32768 to 32767 | 2 | Each Channel |
| High Calibrate Value | Specifies the value for Calibrating high point | range is from -32768 to 32767 | 2 | Each Channel |
| Resolution | Specifies the resolution value | range is from 1 to 10 | 2 | Each Channel |
| Excitation | Specifies Excitation required for the channel. | range is from Yes: TRUE  No: FALSE | 1 | Each Channel |
| Sensor Table (ADC reading in voltage) | Specifies the pointer to the table for the voltage reading of the ADC channel. | Valid reference to Lookup table for voltage reading of the ADC channel. | 4 | Each Channel |
| Sensor Table (Sensor unit) | Specifies the pointer to the table of the Sensor units for the corresponding voltage reading of the ADC channel. | Valid reference to Lookup table for Sensor units for the corresponding voltage reading of the ADC channel. | 4 | Each Channel |
| Minimum Value | Specifies the minimum limit of the Scaled Reading. | range is from -32768 to 32767 | 2 | Each Channel |
| Maximum Value | Specifies the maximum limit of the Scaled Reading. | range is from -32768 to 32767 | 2 | Each Channel |

Table 10: Cold Junction Sensor

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Attribute** | **Description** | **Value** | **Field length (bytes)** | **Remarks** |
| PART Number | Config data Part number | Configurable as per need.  Refer H398-SRS-ANA-DRQ-76 for part number format. | 16 | For entire Config Data |
| Channel Status | Specifies the ADC channel is Enable or Disable | Enable: 1  Disable : 0 | 4 | Each Channel |
| Default Value Status | Specifies whether the default value can be set for the ADC channel or not. | Enable: 1  Disable: 0 | 4 | Each Channel |
| Default Value | Specifies the default value of the ADC channel | 0 | 2 | Each Channel |
| Calibrate | Specifies the ADC channel is Calibrate | TRUE: 1  FALSE: 0 | 1 | Each Channel |
| Low Calibrate Point | Specifies the ADC count for Calibrating low point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| High Calibrate Point | Specifies the ADC count for Calibrating high point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| ADC Channel Sensor Type | Specifies the type of the ADC channel | 0: CAL\_DIS\_MV, mVDC  1: CAL\_DIS\_V, VDC  2: CAL\_DIS\_TEMPC, TCK °C  3: CAL\_DIS\_TEMPF, °F  4: CAL\_DIS\_OHM, Ohms | 4 | Each Channel |
| Low Calibrate Value | Specifies the value for Calibrating low point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| High Calibrate Value | Specifies the value for Calibrating high point | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| Resolution | Specifies the resolution value | 1 | 2 | Each Channel |
| Excitation | Specifies Excitation required for the channel. | TRUE: 1  FALSE: 0 | 1 | Each Channel |
| Sensor Table (ADC reading in voltage) | Specifies the pointer to the table for the voltage reading of the ADC channel. | Valid reference to Lookup table for voltage reading of the ADC channel. | 4 | Each Channel |
| Sensor Table (Sensor unit) | Specifies the pointer to the table of the Sensor units for the corresponding voltage reading of the ADC channel. | Valid reference to Lookup table for Sensor units for the corresponding voltage reading of the ADC channel. | 4 | Each Channel |
| Minimum Value | Specifies the minimum limit of the Scaled Reading. | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |
| Maximum Value | Specifies the maximum limit of the Scaled Reading. | Configurable as per need, range is from -32768 to 32767 | 2 | Each Channel |

16.5.2 Module Configuration Data Format

Requirement ID: H398-SRS-ANA-DRQ-55

MOPS: No

Safety Requirement: No

Rationale: Required to define the format of Module Configuration Data

Verification Method: Testing

The Module Configuration Data for the Analog Module ADC channels shall have the format provided in Table : Format of Analog MCD.

*Table 11: Format of Analog MCD*

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input Signal** | **Channel State** | **Default State** | **Default Value** | **Calibrate** | **Low Calibrate Point** | **High Calibrate Point** | **ADC Channel Sensor Type** | **Low Calibrate Value** | **High Calibrate Value** | **Resolution** | **Excitation** | **Min Value** | **Max Value** | **Sensor Table <Member 1>** | **Sensor Table <Member 2>** |
| Part Number Config Data | 16 Bytes Part number of the Config Data | | | | | | | | | | | | | | |
| External ADC Signal 1 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| External ADC Signal 2 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| External ADC Signal 3 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| …..  …..  …. | …..  …..  …. | …..  …..  …. | …..  …..  …. |  |  |  |  |  |  |  |  |  |  | …..  …..  …. | …..  …..  …. |
| External ADC Signal 39 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| External ADC Signal 40 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| Internal ADC Signal | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| Input Signal | Channel State | Default State | Default Value | Reference frequency | Scaled Reading | Minimum Reading | Maximum Reading | Resolution | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| TACH Signal 1 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| TACH Signal 2 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| ….. | ….. | ….. | ….. |  |  |  |  |  |  |  |  |  |  | ….. | ….. |
| ….. | ….. | ….. | ….. |  |  |  |  |  |  |  |  |  |  | ….. | ….. |
| TACH Signal 9 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| TACH Signal 10 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| **Input Signal** | **Channel State** | **Default State** | **Default Value** | **Calibrate** | **Low Calibrate Point** | **High Calibrate Point** | **ADC Channel Sensor Type** | **Low Calibrate Value** | **High Calibrate Value** | **Resolution** | **Excitation** | **Min Value** | **Max Value** | **Sensor Table <Member 1>** | **Sensor Table <Member 2>** |
| DAC Signal 1 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| DAC Signal 2 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| ….. | ….. | ….. | ….. |  |  |  |  |  |  |  |  |  |  | ….. | ….. |
| DAC Signal 7 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |
| DAC Signal 8 | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> | <value> |

Note: 1) The first row and first column will not be part of the table. It is illustrated here to identify the table

entries.

2) For value refer H398-SRS-ANA-DRQ-54.

**16.6 BIT**

This Section describes the Software High Level Requirements for the following Built in Tests performed by the Analog Module.

1.PBIT

2.CBIT

16.6.1 PBIT

Requirement ID: H398-SRS-ANA-FNC-57

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall perform PBIT within 5 Sec after the power-on using the following steps:

i. Perform CRC test on Code Section.

ii. Perform test on Module Configuration Data

iii. Perform the CPU Test.

iv. Perform the RAM Test.

16.6.1.1 CRC Test

Requirement ID: H398-SRS-ANA-FNC-58

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall perform the CRC test as follows:

1. Calculate the CRC over the required memory region. (CRC polynomial is X^32+X^26+X^23+X^22+X^16+X^12+X^11+X^10+X^8+X^7+X^5+X^4+X^2+X^1+X^0)

2. Compare the calculated CRC with the CRC present in the memory (Refer note 2)

3. If both values match, then CRC test is PASS else FAIL

Note:

1. Analog Module shall perform the CRC test on Module configuration data region, Application Software region and calibration data region.

2. Module configuration data CRC is present at 0x80BFFFC, Application Software CRC is present at 0x803FFFC and Calibration Data CRC is present at 0x800BFFC.

16.6.1.2 Module Configuration Data - Validity Test

Requirement ID: H398-SRS-ANA-DRQ-59

MOPS: No

Safety Requirement: No

Rationale: Derived to define the validity check of the Module Configuration Data

Verification Method: Testing

The Analog Module shall verify the parameters of the Module Configuration Data are within the ranges mentioned in H398-SRS-ANA-DRQ-54 during PBIT.

16.6.1.3 CPU Test

Requirement ID: H398-SRS-ANA-FNC-60

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall perform a CPU test as follows:

1. Perform the following operations with known operands

Arithmetic Operators - addition, subtraction, multiplication, division

Logical Operators - AND, OR, XOR

2. If the obtained result matches with the known result, then the test is pass else it is fail.

Note: Flags - Carry, Overflow, zero flags are also tested while performing the above operations.

16.6.1.4 RAM Test

Requirement ID: H398-SRS-ANA-FNC-61

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall perform a RAM check as follows:

1. Write the pattern 0xA5A5 to a test buffer

2. Read back the values from the test buffer

3. Write the pattern 0x5A5A to the same test buffer

4. Read back the values from the test buffer

5. If all the values read in Steps #2 and #4 match with the values written in the previous check then the check is a pass else check is failed.

Note: The test buffer is 16byte buffer marked in the external memory for this specific test.

16.6.2 CBIT

Requirement ID: H398-SRS-ANA-FNC-62

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

As part of CBIT, the Analog Module shall perform Stack Test for the following tasks:

* Init Task
* Application Task
* ARINC 825 comm task.
* CBIT Task
* Idle task
* DAC Task

Note: CBIT task is executed at the rate specified in H398-SRS-ANA-DRQ-70

16.6.2.1 Stack Test

Requirement ID: H398-SRS-ANA-FNC-63

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog module shall perform the Stack test as follows:

1. Read the location at 70% of the stack length

2. If the value read is not equal to 0xDEADDEAD then the test is failed else it is passed

Note: Stack is initially filled with 0xDEADDEAD

16.6.3 BIT-Fault indication

This Section describes the Software High Level Requirements for the fault indication for the following Built in Tests performed by the Analog Module.

1.PBIT fault indication

2.CBIT fault indication

16.6.3.1 PBIT fault indication

Requirement ID: H398-SRS-ANA-FNC-65

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

For any failure detected in PBIT, the Analog Module shall enter into Error Mode.

16.6.3.2 CBIT fault indication

Requirement ID: H398-SRS-ANA-FNC-66

MOPS: No

Safety Requirement: No

Rationale: NA

Verification Method: Testing

The Analog Module shall enter into error mode for any one of the following during CBIT:

1. Stack test failure
2. Detection of NonMaskable interrupt, HardFault interrupt, MemManage interrupt, BusFault interrupt, SpuriousInterrupt interrupt and UsageFault interrupt.

**16.7 Kernel and Scheduler**

This section specifies the Software High Level Requirements for the Kernel and Scheduler used in the Analog Module.

16.7.1 Kernel/Scheduler - Initializations

Requirement ID: H398-SRS-ANA-DRQ-68

MOPS: No

Safety Requirement: No

Rationale: This requirement has been derived to ensure proper initialisation so that all tasks are functioning correctly

Verification Method: Testing

The Analog Module shall initialize the data structures used by the Kernel and Scheduler after PBIT.

16.7.2 Scheduler - Algorithm

Requirement ID: H398-SRS-ANA-DRQ-69

MOPS: No

Safety Requirement: No

Rationale: This requirement has been derived to ensure that all tasks are functioning correctly

Verification Method: Testing

The Analog Module shall use a priority based pre-emptive Scheduler.

16.7.3 Tasks

Requirement ID: H398-SRS-ANA-DRQ-70

MOPS: No

Safety Requirement: No

Rationale: This requirement has been derived to differentiate the activities that are to be performed by different tasks

Verification Method: Testing

The Analog Module shall create the tasks as described in Table: Analog Module - Tasks during initialization.

*Table 12: Analog Module - Tasks*

|  |  |  |  |
| --- | --- | --- | --- |
| **Tasks** | **Frequency** | **Priority** | **Description** |
| Application Task | 100ms | 5 | This is the main task of the Analog Module. It performs all the communication and calculation related activities of the Analog board. |
| A825 Task | 10ms | 6 | This task is to communicate over A825 CAN bus. |
| Init Task | 500ms | 8 | This task initializes the peripherals, scheduler, kernel and creates other tasks. |
| Cbit Task | 100ms | 9 | This task is performed during the operational mode of the application module. It initializes the stack and creates Task to implement Continuous Built-In-Test |
| Idle Task | - | 63 | It is executed when there are no other Ready tasks. |
| DAC Task | 100ms | 7 | This task is to create the application task and updates outputs of different values on DAC channels |

16.7.4 Semaphores

Requirement ID: H398-SRS-ANA-DRQ-71

MOPS: No

Safety Requirement: No

Rationale: This requirement has been derived to specify the mechanism used for task activation

Verification Method: Testing

The Analog Module shall use a separate binary semaphore for each task to activate the task.

16.7.5 Task activation by semaphore

Requirement ID: H398-SRS-ANA-DRQ-72

MOPS: No

Safety Requirement: No

Rationale: This requirement has been derived to specify the mechanism used for task activation

Verification Method: Testing

The Analog Module shall use the System Timer interrupt to release the semaphore for tasks as per the timing mentioned in H398-SRS-ANA-DRQ-70.

16.7.6 Task structure

Requirement ID: H398-SRS-ANA-DRQ-73

MOPS: No

Safety Requirement: No

Rationale: This has been derived to ensure that all tasks have a common structure for executing their defined activities

Verification Method: Testing

The Analog Module shall behave as per the following steps to execute the tasks mentioned in H398-SRS-ANA-DRQ-70:

1. Wait for the semaphore

2. On semaphore release, perform the task activity once

3. Infinitely repeat Steps#1 and #2.

Note: The Idle task is an exception. It is activated when there are no other tasks which are ready.

**16.8 Software Part Number**

The Analog Module consists of two binaries. Each binary has a unique part number to identify itself.

16.8.1 Software Part Number - Application Software

Requirement ID: H398-SRS-ANA-DRQ-75

MOPS: No

Safety Requirement: No

Rationale: Derived to define the Software Part Number to identify the Application Software

Verification Method: Testing

The Analog Module shall define a 16-character string at a prefixed location in memory (0x0803FFEC) to identify its Software Part Number.

Format: <H108E-810><space><-><x><.><yy><space>

where,

x is major release number

yy is minor release number

16.8.2 Software Part Number - Module Configuration Data Binary

Requirement ID: H398-SRS-ANA-DRQ-76

MOPS: No

Safety Requirement: No

Rationale: Derived to define the Software Part Number to identify the Module Configuration Data

Verification Method: Testing

The Analog Module shall define a 16-character string at a prefixed location in memory (0x080A0000) to identify its Module Configuration Data (MCD) Software Part Number.

Format:

<H108E-674><space><-><x><.><yy><space>

where,

x is major release number

yy is minor release number

## 16.9 Resource Utilization

This section specifies the Software High Level Requirements for the resource utilization of the Analog Module.

### 16.9.1 Memory Usage

Requirement ID: H398-SRS-ANA-DRQ-80

MOPS: No

Safety Requirement: No

Rationale: This margin is required for future enhancements

Verification Method: Analysis

The Analog Module software shall not utilise more than 80% of the available FLASH and RAM memory for the initial certification of the product.

### 16.9.2 Throughput Usage

Requirement ID: H398-SRS-ANA-DRQ-81

MOPS: No

Safety Requirement: No

Rationale: This margin is required for future enhancements

Verification Method: Analysis

The Analog Module software shall not utilise more than 80% of the available processor throughput for the initial certification of the product.