#### Report Submission

# CON101- Introduction to Computer Science and Engineering Indian Institute of Technology Delhi

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#### 1 Introduction

When only one program access a particular memory space, we can safely say that what is the value stored at any particular instance of time.

But when more than one program access and modify the same memory space, then it depends on the sequence i.e when the value is changed and by which program. Thus to ensure the memory consistency, we define the notion of sequential consistency. And TSO, PSO, and RMO are the memory models related to sequential consistency.

#### 2 Sequential Consistency(SC)

- The output should be the same as in a time sharing processor.
- Threads issue commands of memory in program order.
- It does not proceed to assigning next memory block and waits until the previous ongoing operation terminates.
- A read is said to be complete only when the value is returned to read.

#### 3 Total Store Ordering(TSO)

Consider the following example where two threads are running simultaneously on same memory block. Here, instead of waiting for the commands to execute, we could instead place it into a store buffer. Since the buffer is in core memory, it is pretty fast to access. When the processor is free, it will unhide the commands present in this store buffer. Thereby, we hide the delay which is necessary for one command to be executed.

Store buffering preserves single-threaded behavior.

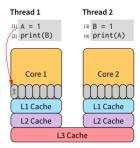


Figure 1: Two threads running on same memory block.

#### 4 Partial Store Ordering(PSO)

- Partial Store Ordering (PSO) is a more relaxed memory consistency model compare to the Total Store Ordering (TSO).
- PSO includes all the features of TSO and an extra relaxation in terms of consistency i.e PSO only guarantees writes to the same location is in order whereas writes to different memory location may not be in order at all.
- In this case, the processor may shuffle the writes in a way that does not match the original order.
- It become very inefficient when number of threads is very large. So, we have to come up with various levels of relaxation in consistency.

### 5 Relaxed Memory Ordering(RMO)

- Relaxed Memory Ordering(RMO) is a more relaxed memory consistency model compare to the Partial Store Ordering(PSO).
- The ordering of reading and writing may be shuffled.
- Weak Ordering Model
- $\bullet$ Release Consistency Model (RCsc / RCpc)
- Digital Alpha, Sparc V9 RMO, IBM Power PC. Except Alpha, rest all allows shuffling of the two reads at the same block.
- RCpc and PowerPC allow a read to return the value of another processors to write early.

## 6 References

- 1. https://plv.mpi-sws.org/trns/paper.pdf
- 2. https://www.cis.upenn.edu/ devietti/classes/cis601-spring2016/sc $_tso.pdf$
- $3. \ http://www.inf.ed.ac.uk/teaching/courses/pa/Notes/lecture07-sc.pdf$