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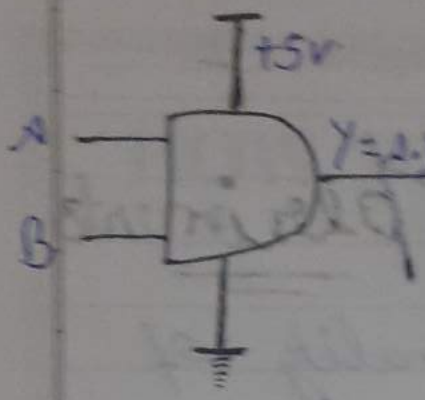
Expt. No. Page No. 1

List Of Experiments

1. Verification of the functionality of all logic gates.
2. Implementing Half ADDER, FULL ADDER using basic logic gates
3. Implementing Binary - to - Gray, Gray-to - Binary code conversions.
4. Implementing 3-8 line Decoder
5. Implementing 4X1 and 8X1 MULTIPLEXERS
6. Verify the excitation tables of various FLIP-FLOPS
7. Design of an 8-bit Input/output System with four 8-bit Internal Registers.
8. Design of an 8-bit ARITHMETIC LOGIC UNIT.
9. Design the data path of a computer from its register transfer language description.
10. Implement a simple instruction set computer with a control unit and a data path.

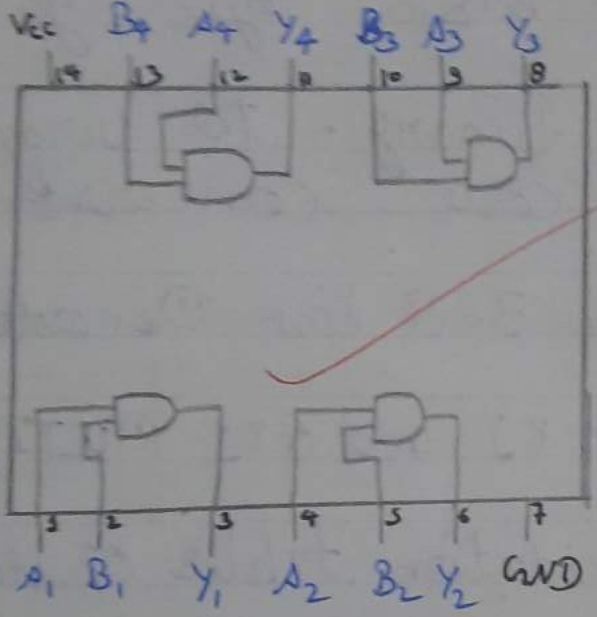
Teacher's Signature :

AND Gate (IC 7408)



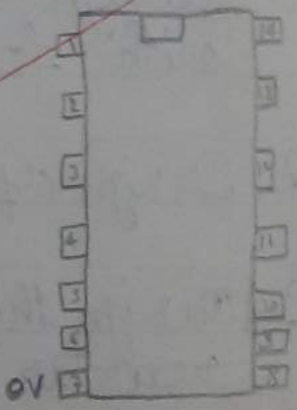
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

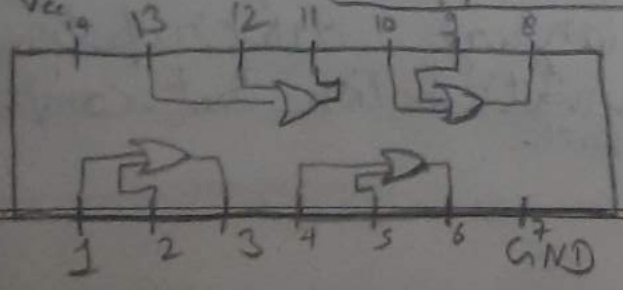
(AND Gate)



OR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1





Experiment → 1

Date

Expt. No. 1 Page No. 2

⊙ **Aim:-** Verify operation of all the logic gates.

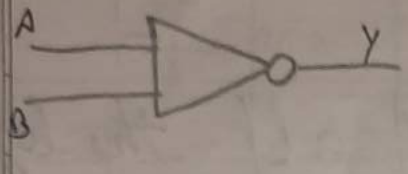
- **Equipments:-** Bread Board, connecting wires, LED, power supply,
  IC 7408 (Quad 2 input AND gates)
  IC 7432 (Quad 2 input OR gates).
  IC 7402 (Quad 2 input NOR gates),
  IC 7400 (Quad 2 input NAND gates),
  IC 7404 (Hex 1 input NOT gates)
  IC 7486 (Quad 2 input XOR gates).

- **Theory:-**

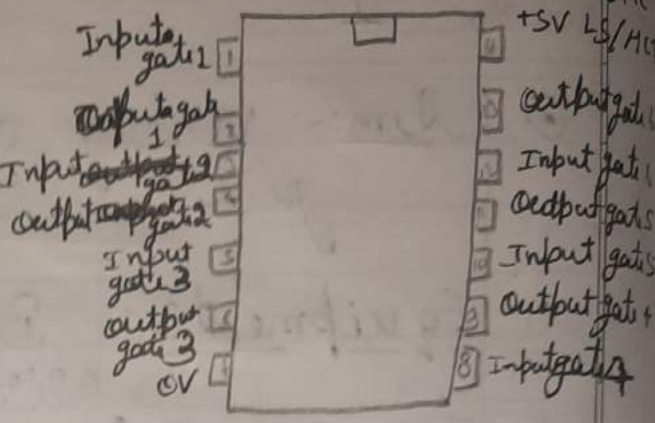
* **Logic gates:-** A logic gate is a circuit that has one or more input signal but only one output signal. Truth Table for a logic gate is tabular listing of all possible combination of input and resultant output for each combination.

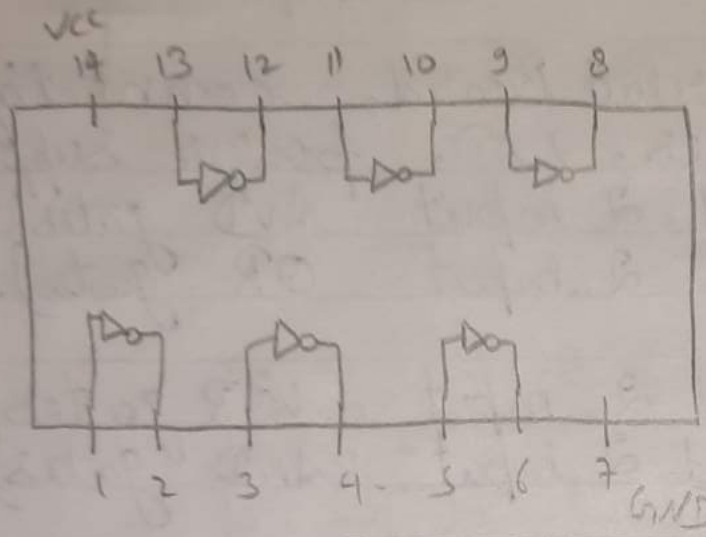
Teacher's Signature :

Not gate



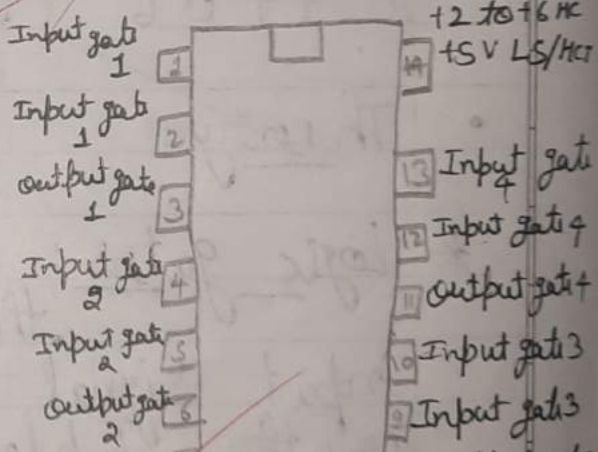
A	Y
0	1
1	0

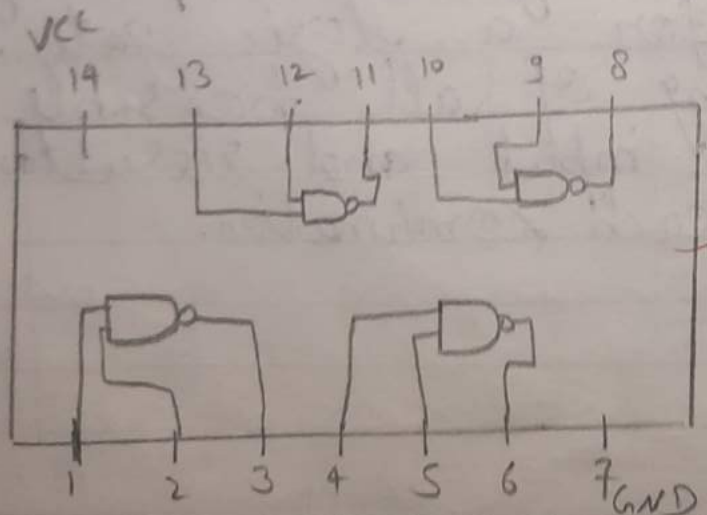




NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0





Date

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* **OR gate (IC 7432):-** IC7432 is used as OR gate which has two or more inputs and one output. In OR gate the output is low only when no input is high. Output is high which one or all inputes are high.

* **NOT gate (IC7404):-**

IC7404 is used as NOT gate which has two or more inputs and one output In Not gate the output is low when input is high. Output is high when input is low.

* **IC7400 (Quad 2 input NAND gate):-**

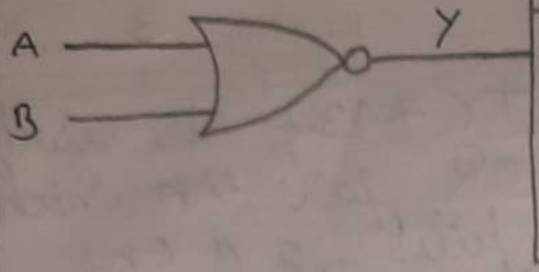
IC7400 is used as NAND gate which has two or more input and one output.

* **IC7402 (QUAD 2 input NOR gate):-**

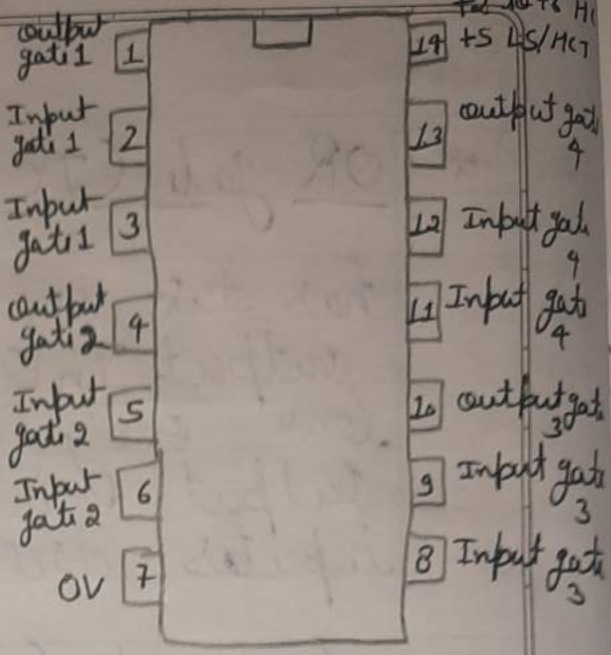
IC7402 is used as NOR gate which has two or more input and one output.

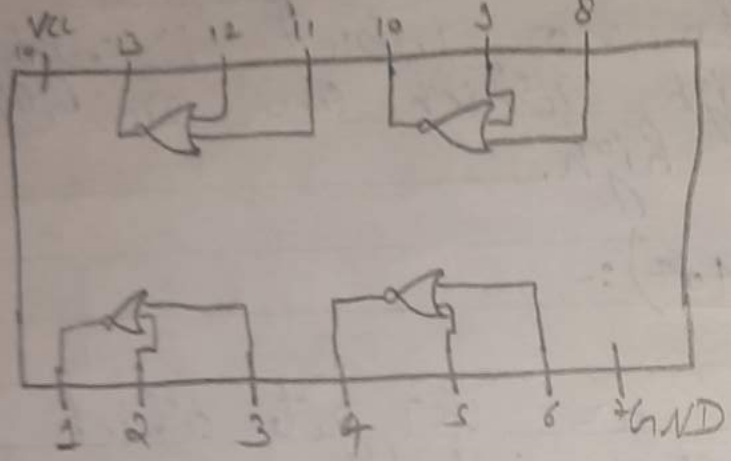
Teacher's Signature :

NOR gate



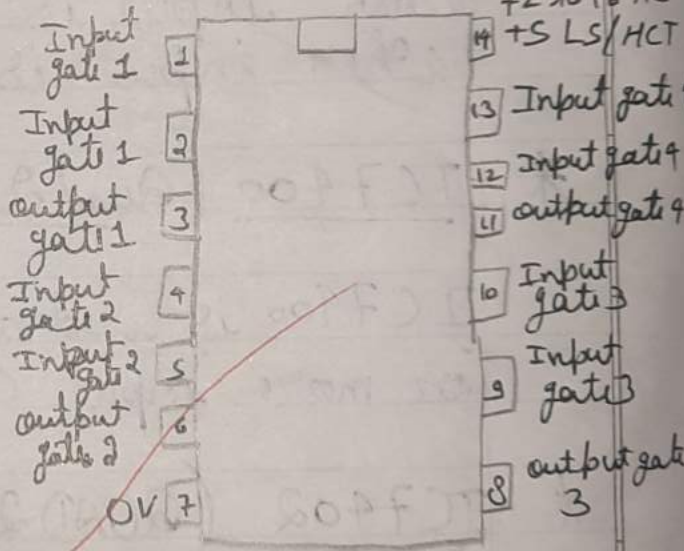
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

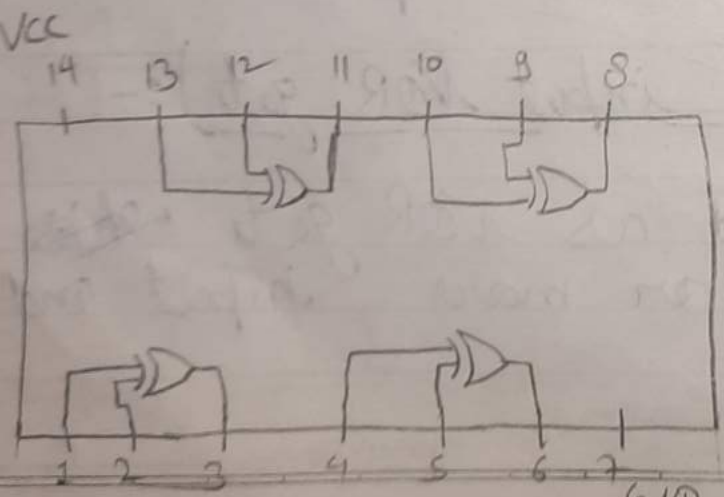




XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0





Date

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* IC7486 (QUAD 2 input XOR gate):-

IC7486 is used as XOR gate which has two or more inputs and one input. In XOR gate the output is high if either of one input is high. Output is Low when both input are same. To the gate enable when one ~~to~~ odd no. of input appear.

⊙ Procedure:-

1. Identify the pin configuration of ICs and make the connection.

2. Connect the supply of +5V ground to IC.

3. Supply Input according to the truth and verify the output.

⊙ Result:-

1. Make sure that logic level inputs are proper with LED display.

Teacher's Signature :

Date

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2). Beware of loose connections.

3). Check the connection properly before supplying power.

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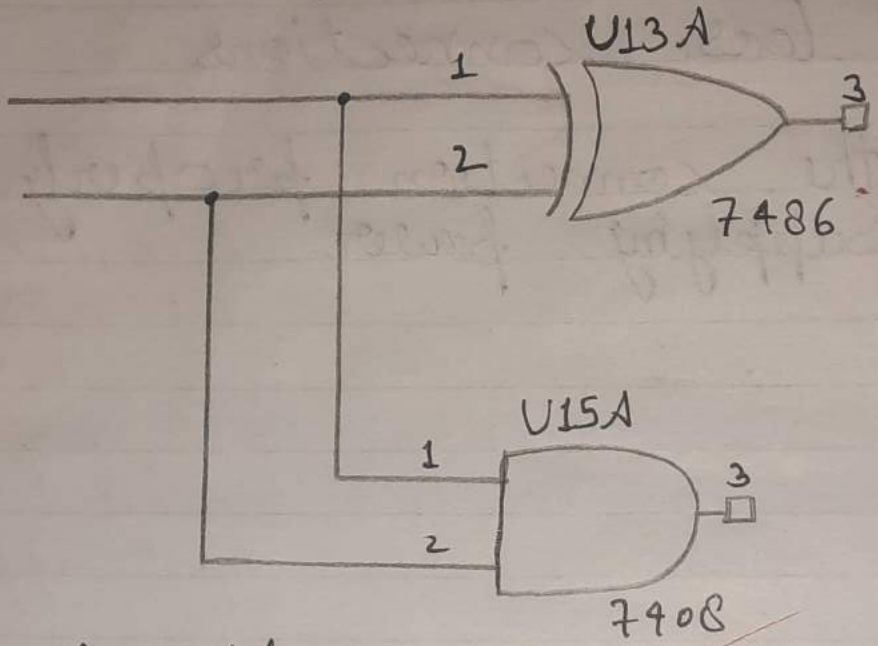
Teacher's Signature :

Circuit Diagram Of Half adder:



$S = A \oplus B$

$C = AB$

Truth Table:

(1). For half adder:

Input		output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Experiment - 2

Date

Expt. No. 2 Page No. 6

Aim: To implement Half Adder, Full Adder using basic logic gates.

Equipements Required:

S.No.	Apparatus	Specification	Quantity
1	IC	7486	1
2	IC	7408	1
3	Digital Trainer Kit	-	1
4	Connection Wires	-	As required

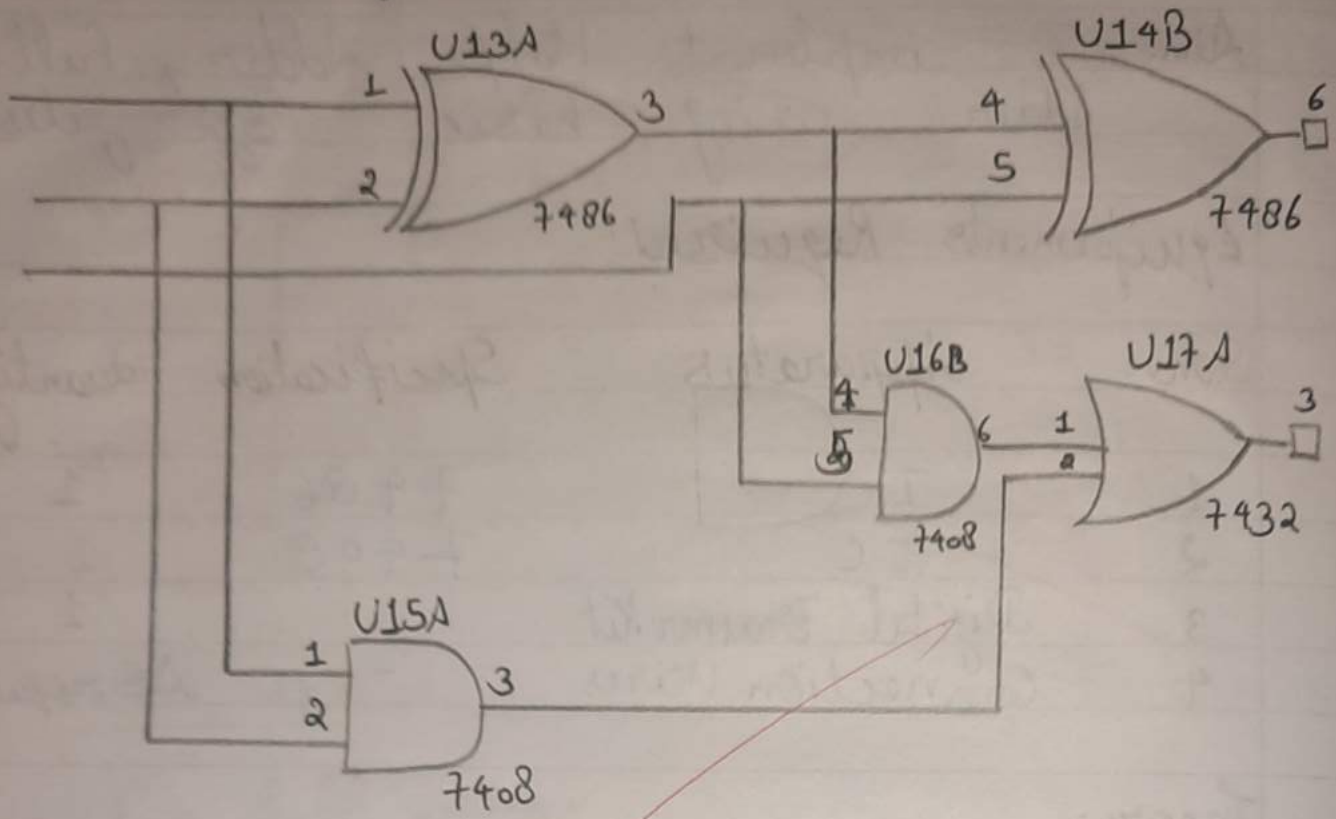
Theory:

Half Adder:

Half Adder can add two bits. It needs two inputs A, B and Sum and carry are two binary operations. The applications of half adder are very limited because it can't accept a carry from a previous addition. When we add two binary numbers, we start with the least-Significant column. That is by adding the A_0 and B_0 bits of the two numbers. This means that we have to add two bits with the possibility of a carry. The circuit used for this is called half-adder.

Teacher's Signature :

Circuit Diagram of Full Adder:



Truth table

(2). For Full adder:

Input			output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder:

A full adder has the provision to add two bits along with a carry coming from lower order bits when binary addition on multi bit numbers is to be performed. It need two inputs A, B and carry from lowest bits C_{in}. The output is Sum and C_{in} are two binary operations. For addition of higherorder columns (other than last significant one), we have to use full-adder, a logic circuit that can add three bits at a time. The third bit is the carry from the lower column. Full adder, therefore, is a logic circuit with three inputs and two outputs. The truth tables for full-adder is shown in table

Exercise: Show that the output at SUM can be written as

$SUM = (A \oplus B) \oplus C$.

Teacher's Signature :

Date

Expt. No. Page No. 8

Procedure:

(1) Identify the pin configuration
(2) Connect the circuit as per the circuit diagram.
(3) Connect the all V_{cc} to +5V and ground.

Result:-

The truth table of half adder and full adder is being verified.

Precaution:

(1) Verify the reading properly.
(2) All the connections should be tight.
(3) Take out the IC carefully from the breadboard.
(4) Supply should not exceed +5V.

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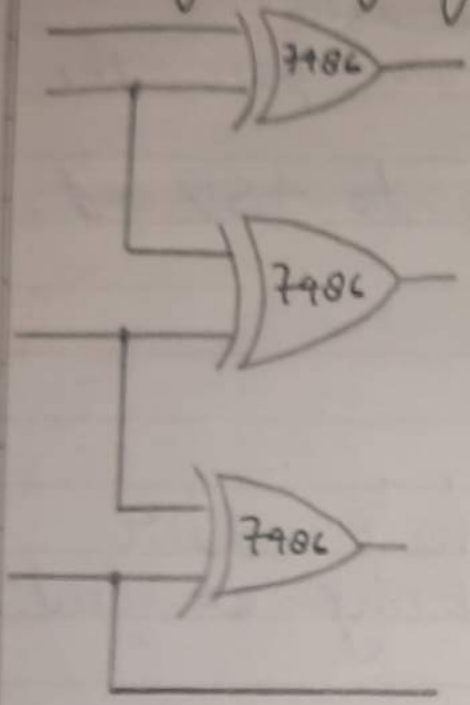
Teacher's Signature :

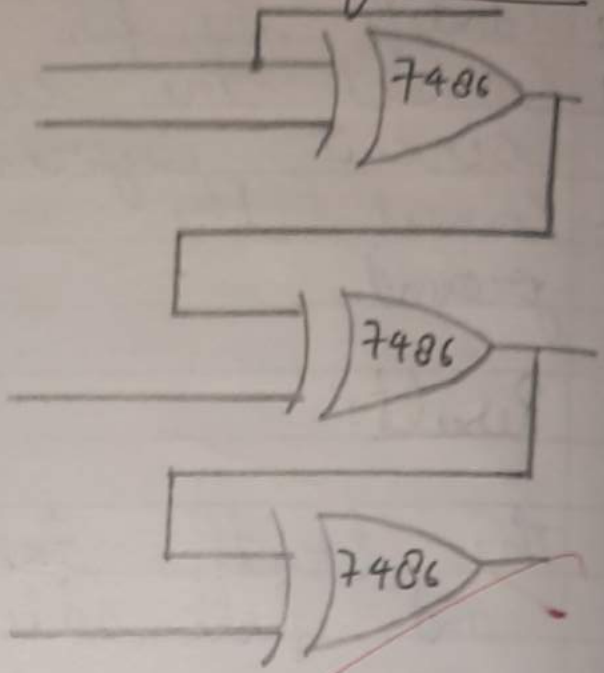
Circuit Diagram

Binary to gray



Using
Ex OR gates

Gray to Binary



Using
EX-OR gates

Experiment No 3

Date

Expt. No. 3 Page No. 9

Aim: Implementing Binary - to - Gray, Gray - to - Binary code conversions.

Equipments Required:

S.No.	Apparatus	Specification	Quantity
1	IC	7486	1
2	Digital Trainer Kit	—	1
3	Connection Wires	—	As required

Theory:

Binary to gray code conversion

Binary to gray code conversion is a very simple process. There are several steps to do these types of conversions. Steps given below elaborate on the idea on this type of conversion.

(1). The M.S.B. of the gray code will be exactly equal to the first bit of the given binary number.

Teacher's Signature :

Truth Table For Both :-

Inputs				Outputs			
B3	B2	B1	B0	G3(V)	G2(V)	G1(V)	G0(V)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

(2). Now the second bit of the code will be exclusive-or of the first and second bit of the given binary number, i.e. if both the bits are same the result will be 0 and if they are different the result will be 1.

(3). The third bit of gray code will be equal to the exclusive-or of the second and third bit of the given binary number. Thus the Binary to gray code conversion goes on.

Gray code to binary conversion

Gray code to binary conversion is again very simple and easy process. Following steps can make your idea clear on this type of conversions.

(1). The M.S.B. of the binary number will be equal to the M.S.B. of the given gray code.

(2). Now if the second gray bit is 0 the second binary bit will be same as the previous or the first bit. If the gray bit is 1

Teacher's Signature : _____

the second binary bit will alter. If it was 1 it will be 0 and if it was 0 it will be 1.

(3). This step is continued for all the bits to do Gray code to binary conversion.

Procedure:

(1). The circuit connections are made as shown in fig..

(2). Pin(14) is ~~con~~ connected to $+V_{cc}$ and Pin(7) to ground.

(3). In the case of binary to gray conversion, the inputs B0, B1, B2 and B3 are given at respective pins and outputs B0, B1, B2 and B3 are taken for all the 16 combinations of inputs.

(4). The values of the outputs are tabulated.

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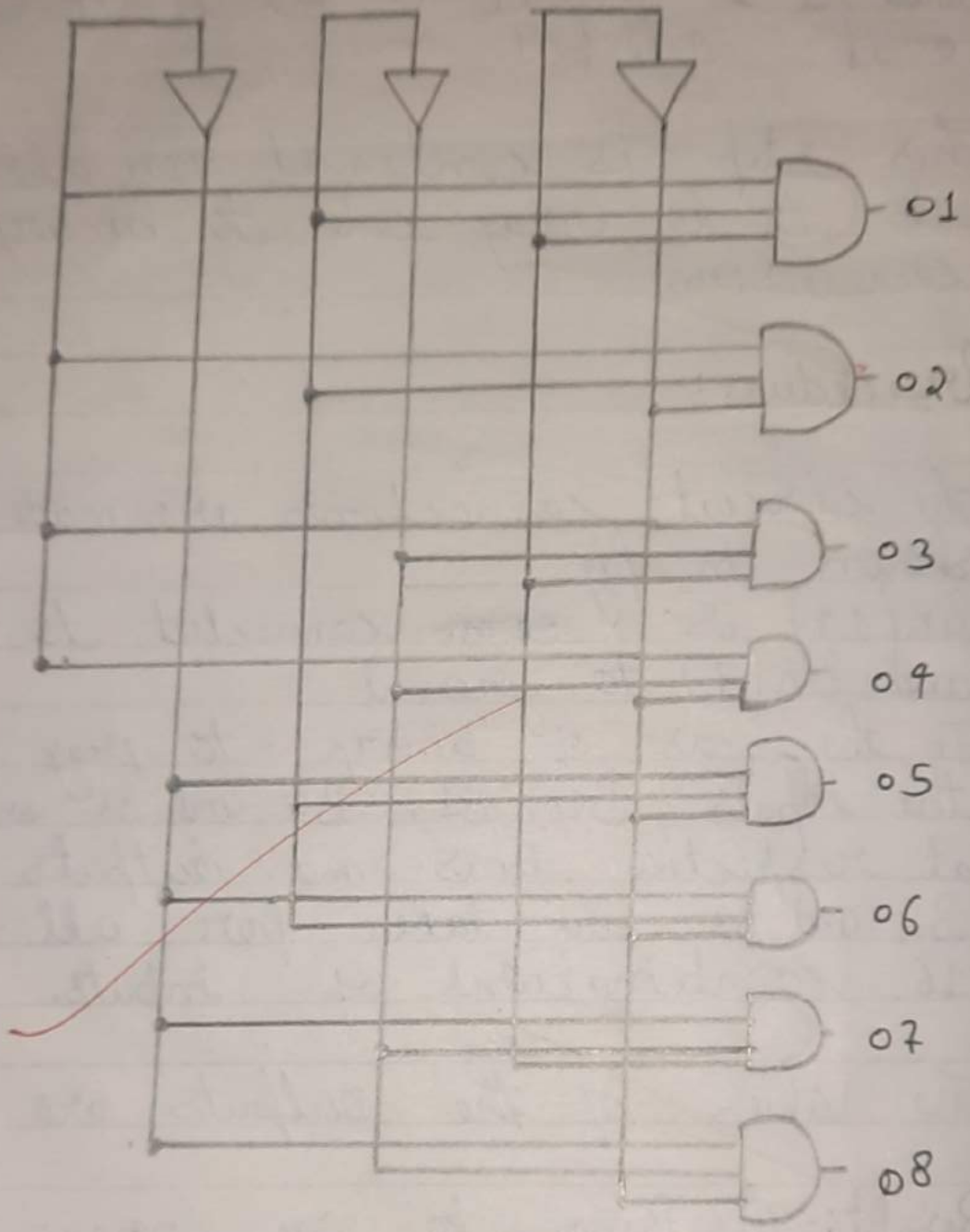
Result:- The Binary-to-Gray, Gray-to-Binary code conversions has been done and verified.

Teacher's Signature :

Logic diagram

Decoder: 3 to 8 line



Date

Expt. No. 04

Page No. 12

Aim: Implementing 3-8 line DECODER and Implementing 4x1 and 8x1 MULTIPLEXERS.

Apparatus required:

S.No.	Component	Specification	QTY.
1	IC	74139	1
2	IC	74153	1
3	Digital trainer kit	—	1
4	Patch cards & connections wire	—	As req.

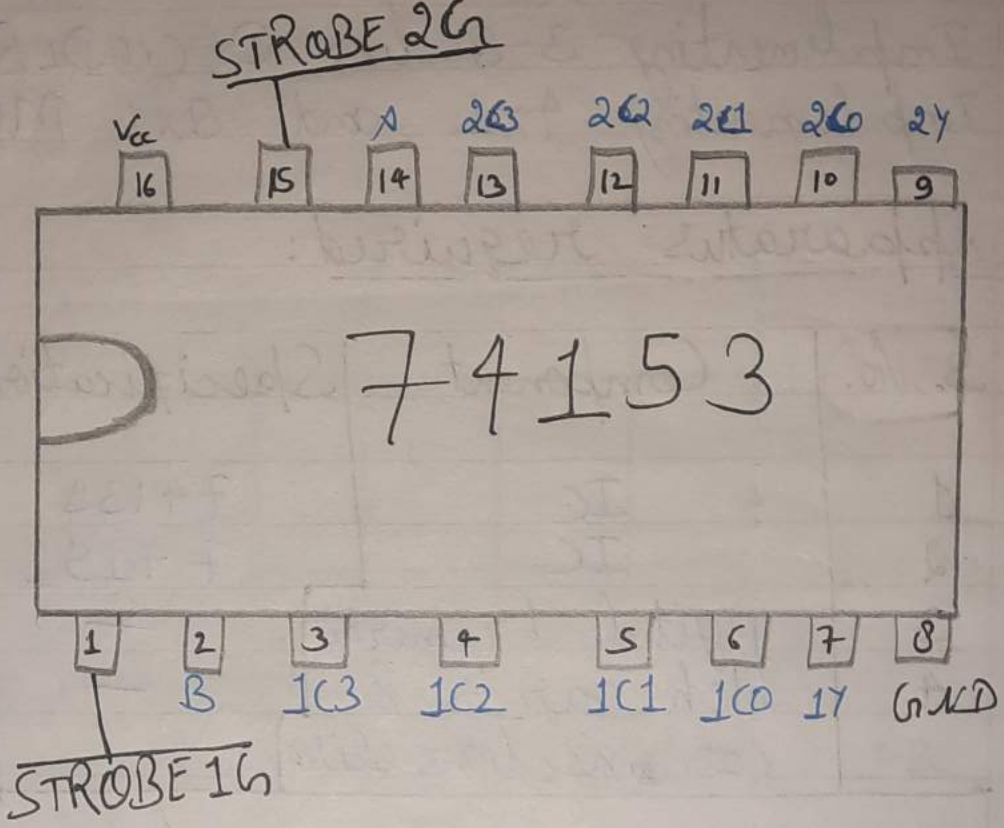
Theory:

Decoder:

A decoder is a device which does the reverse operations of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines.

Teacher's Signature :

Pin diagram IC74153 (4x1 multiplexer)



Inputs			Outputs							
a	b	c	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1
Output functions			$\bar{a}\bar{b}\bar{c}$	$\bar{a}\bar{b}c$	$\bar{a}b\bar{c}$	$\bar{a}bc$	$a\bar{b}\bar{c}$	$a\bar{b}c$	$ab\bar{c}$	abc

Date

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Multiplexer:

Multiplexer generally means many into one. A multiplexer is a circuit with many Inputs but only one output. By applying control signals we can steer any input to the output. The fig. (1) shows the general idea. The ckt. has n-input signal, control signal & one output signal. where $2n = m$. One of the popular multiplexer is the 16 to 1 multiplexer, which has 16 input bits, 4 control bits & 1 output bit.

Procedure:

(1). Identify the pin configuration.

(2). Give the connection in the breadboard as per the circuit diagram.

(3). Connect V_{cc} (+5V) and ground of the IC.

(4). The values of the output are tabulated.

Teacher's Signature :

Truth Table of multiplexer (4x1) IC 74153

A	B	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Date

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Result:

verify the truth table of decoder and multiplexer for various inputs.

Precautions:

1). Make the connections according to the IC Pin diagram.

2). The connections should be tight.

3). The V_{cc} and ground should be applied carefully at the specified pin only.

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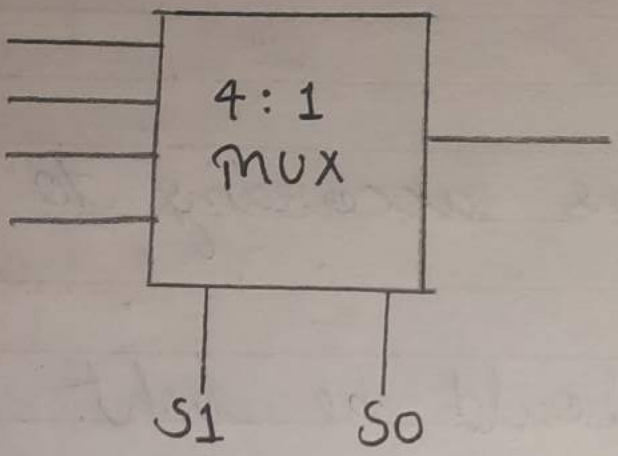
Teacher's Signature :



S_1	S_0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Experiment No - 5

Date

Expt. No. 05

Page No. 15

AIM :-

Implementation of 4*1 and 8*1 multiplexer using logic gates.

Equipment :-

(1). Bread board
(2). Connecting wires
(3). LED
(4). Power supply
(5). Two IC 7408 (Quad 2 input AND gates)
(6). One IC 7432 (Quad 2 input OR gates)
(7). One IC 7404 (Hex 1 input NOT gate)

Theory :-

A Multiplexer is a combinational logic circuit which selects one of the information from many input lines and transmits it to the output line. The selection of input is controlled by a set of selection lines for 2^n inputs the no. of selection lines required is n.

Teacher's Signature :

Date

Expt. No. Page No. 16

Procedure :-

(1). Identify the pin configuration of ICs according to circuit given below.

(2). Connect the supply of +5V ground to IC's

(3). Supply input according to the truth table and verify the output.

Result :-

Operation of multiplexer is verified.

Precaution :-

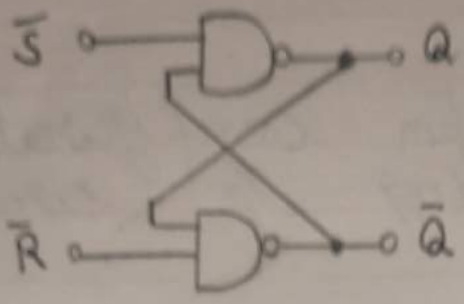
(1). Make sure that logic level inputs are proper with LED display.

(2). Beware of loose connection.

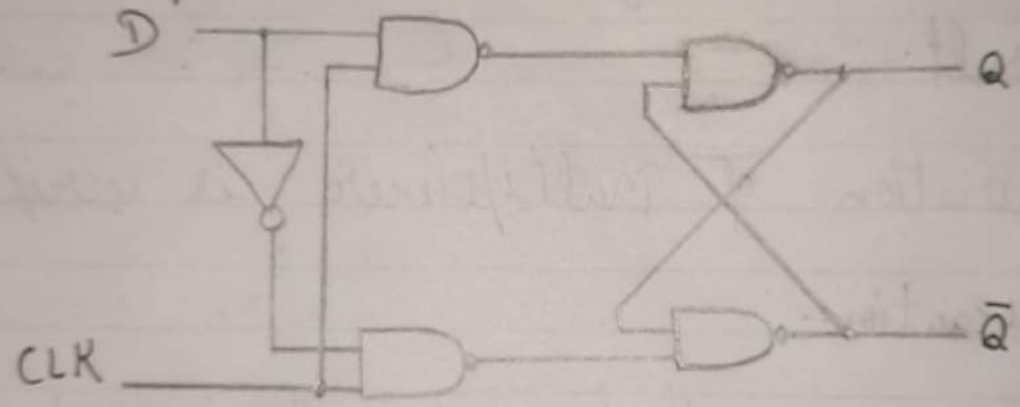
(3). Check the connection properly before supplying power.

Teacher's Signature :

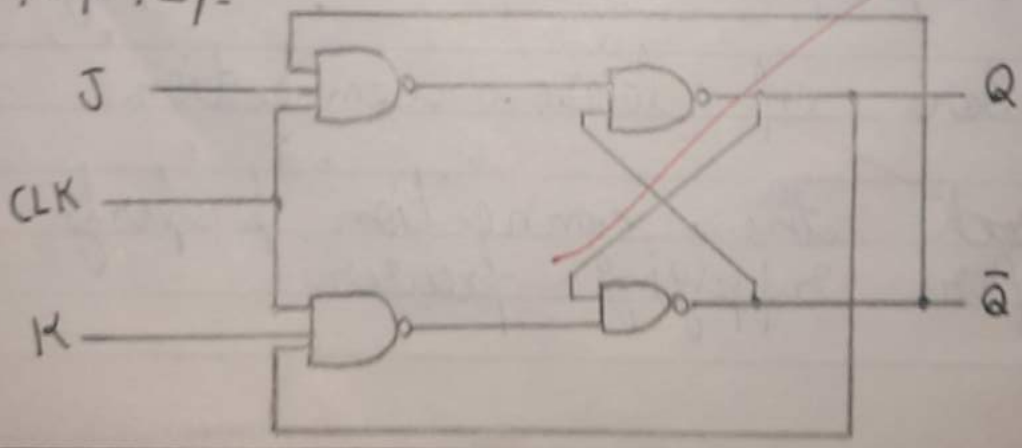
SR Flip flop



D flip flop



JK flip flop



Experiment No. 6

Date _____

Expt. No. 6 Page No. 17

Aim:- Verify the excitation tables of various FLIP-FLOPS.

Apparatus required:-

S. No.	Component	Specification	Qty.
1.	IC	7400	1
2.	IC	7404	1
3.	Digital trainer kit	—	1
4.	Patch cords & connecting wire	—	As req.

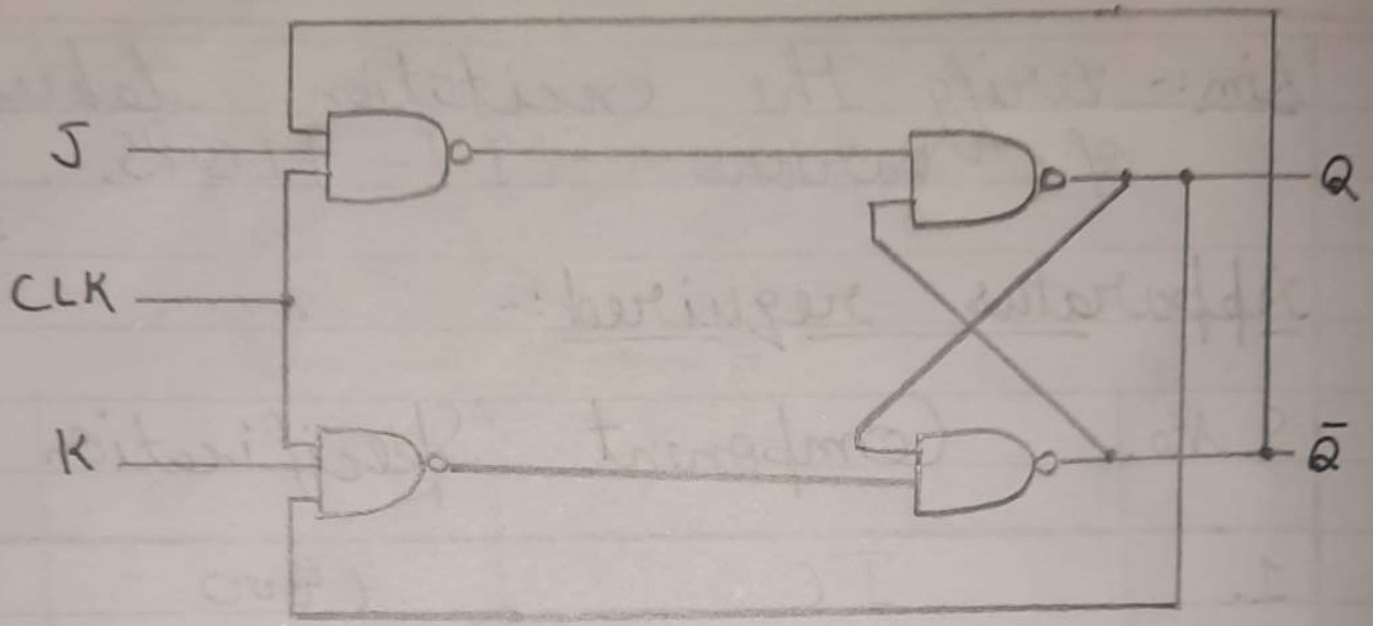
Theory

Flip-flop

A flip-flop is a circuit which exists in one of two states and so can store information. A simple flip-flop can be defined in term of two NAND logic gates.

Teacher's Signature : _____

T- flip flop



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Flip flops are nonlinear circuits, meaning the output from one of its gates is fed 'back' to be processed with the input signal.

RS FLIP FLOP:-

There are two inputs to the flip-flop defined as R and S. When I/P's R=0 and S=0 the O/P remains unchanged. When I/P's R=0 and S=1 the flip flop is switches to the stable state O/P is 1 i.e. SET. The I/P condition is R=1 and S=0 the flip flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R=1 and S=1 the flip flop is switched to the stable state where O/P is forbidden.

JK FLIP FLOP:-

For purpose of counting, the JK Flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip-flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disable and Q retains its last value.

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D flip flop :-

This kind of flip flop prevents the value of D ~~from~~ from reaching the Q output until clock pulses occurs when the clock is low, both AND gates are disabled D can change value without affecting the value of Q. On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. A D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

T Flip-flop :-

The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary ~~for~~ Counters.

Teacher's Signature :

D flip flop Truth Table

S.No.	INPUT	OUTPUT
1	0	0
1	1	1

JK flip flop Truth Table

clock	J	K	Q_{n+1}
1	0	0	No change
1	0	1	0
1	1	0	1
1	1	1	Q_n

T flip flop T

clock	T	Q(N+1)
1	0	No change
1	1	change

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Procedure:

(1). Connect the circuit shown in figure.

(2). Apply V_{cc} and Ground signal to every IC.

(3). Observation the input output according to the truth table.

SR Flip flop Truth Table

Clock	S	R	Q_{n+1}
1	0	0	No change
1	0	1	0
1	1	0	1
1	1	1	—

Precautions:-

(1). Make the connections according to the IC pin diagram.
(2). The connections should be tight.
(3). The V_{cc} and ground should be applied carefully at the specified pin only.

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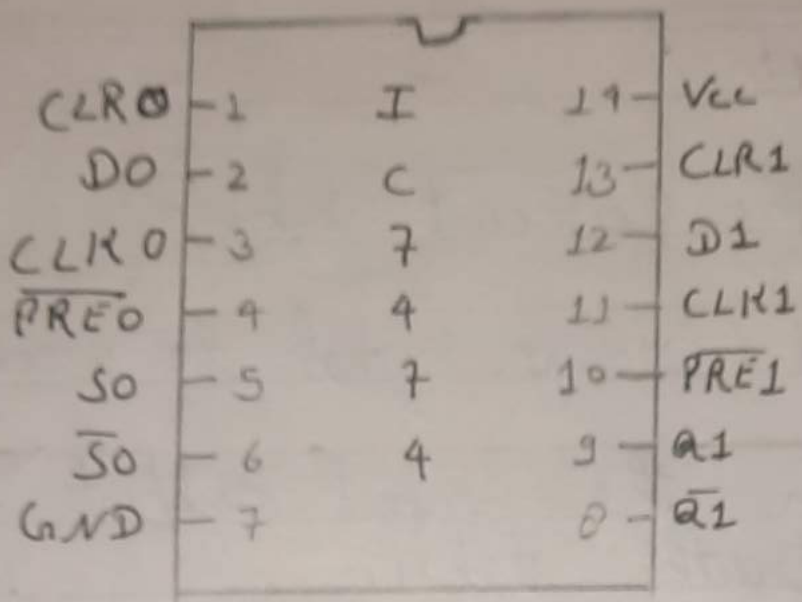
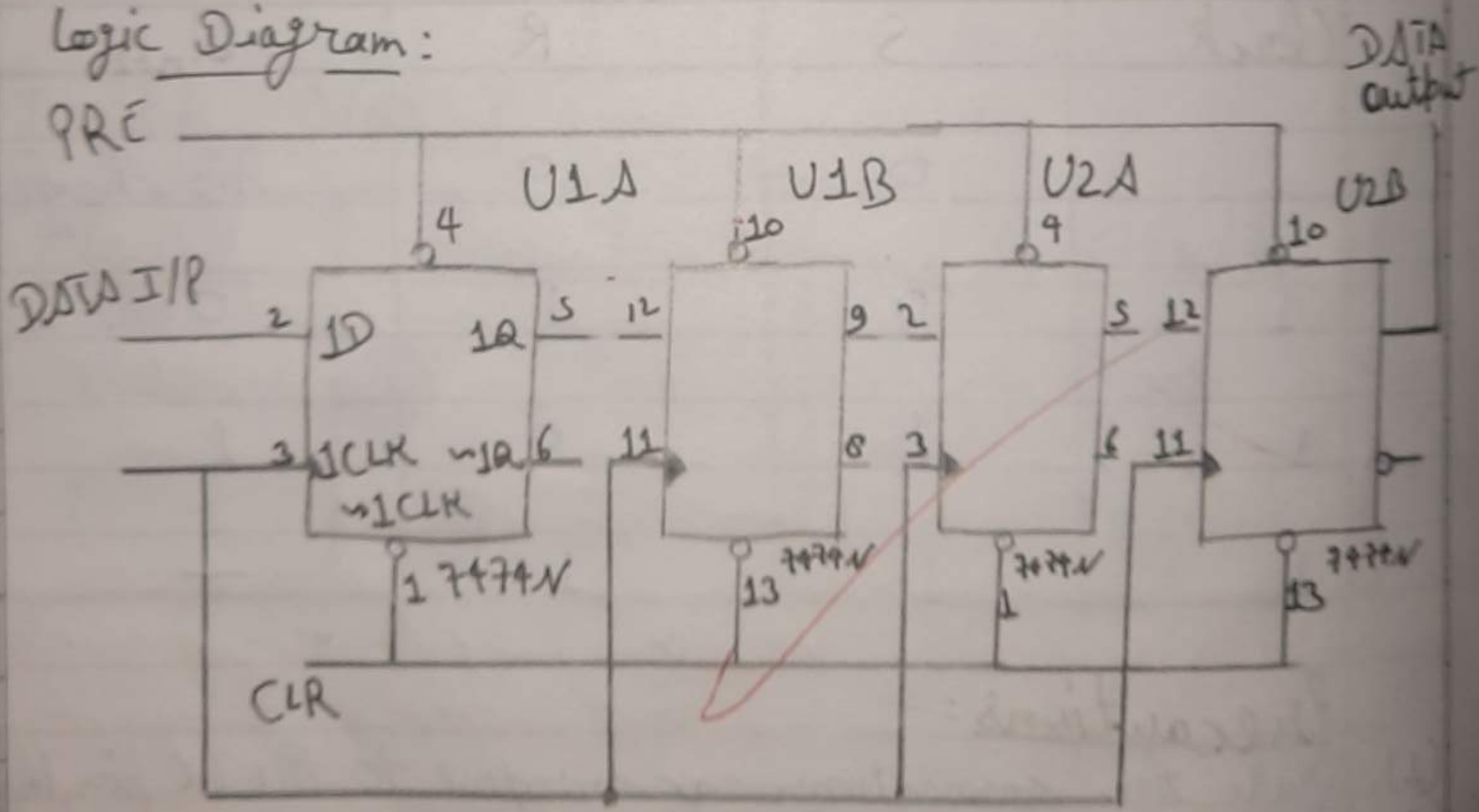


Logic Diagram:



Experiment No. 07 (a)

Date _____

Expt. No. 7 (a) Page No. 21

Aim:- Implementation of a 3-bit SIPO and SISO shift registers using flip-flops.

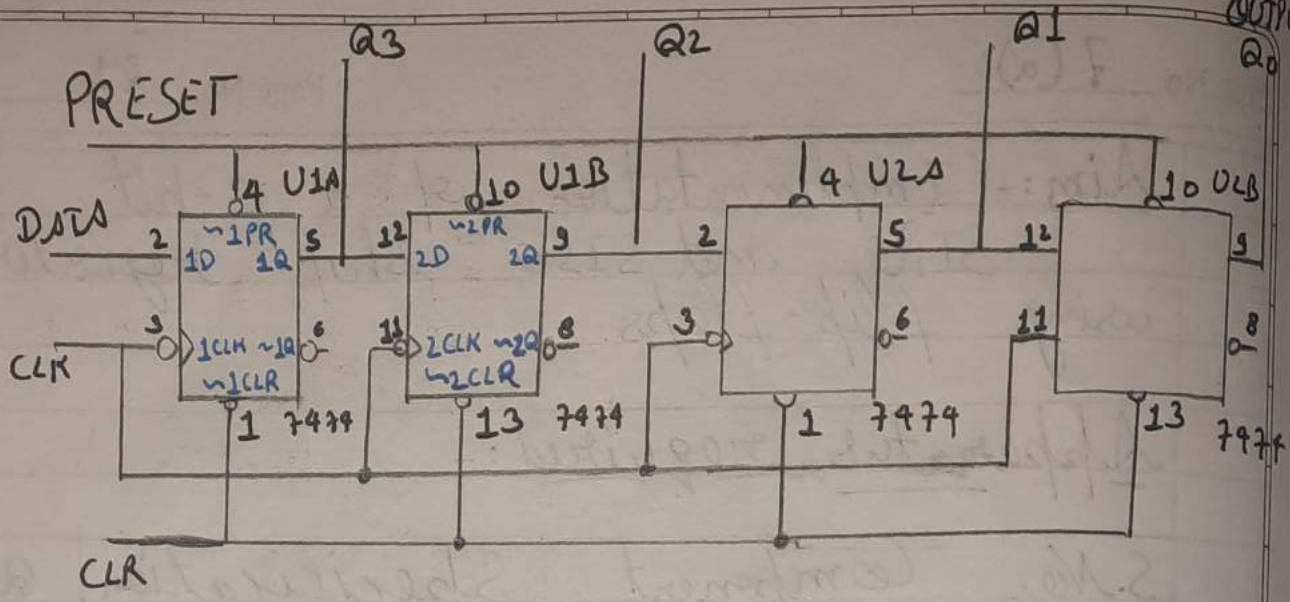
Apparatus required:-

S.No.	Component	Specification	Qty.
1.	D Flip flop	IC 7474	2
2.	OR Gate	IC 7432	1
3.	IC Trainer Kit	–	1
4.	Patch Cords	–	35

Theory:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flop receive common clock pulses which causes the shift in the output of the flip flop. The simplest possible shift register is one that uses only flip flop.

Teacher's Signature : _____



Result: 3-bit SIPO and SISO shift registers using flip-flops has been designed and verified.

Date

Expt. No. Serial in serial out: Page No. 22

Truth table:

CLK	Serial in	Serial out
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

Serial in Parallel out:

Truth table:

		OUTPUT			
CLK	DATA	Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	1
4	1	1	0	0	1

Procedure: (1). Connections are given as per circuit diagram.

(2). Logical inputs are given as per circuit diagram.

(3). Observe the output and verify the truth table.

Teacher's Signature :

Experiment No. 7(b)

Date

Expt. No. 7(b) Page No. 23

Aim: Implementation of a 3-bit PIPO and PISO shift registers using flip-flops.

Apparatus required:

S.No.	Component	Specification	Qty.
1	D Flip flop	IC 7474	2
2	OR Gate	IC 7432	1
3	IC Trainer Kit	—	1
4	Patch Cords	—	35

Theory:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-flip flop cascaded with output of one flip flop connected to input of next flip flop. The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register.

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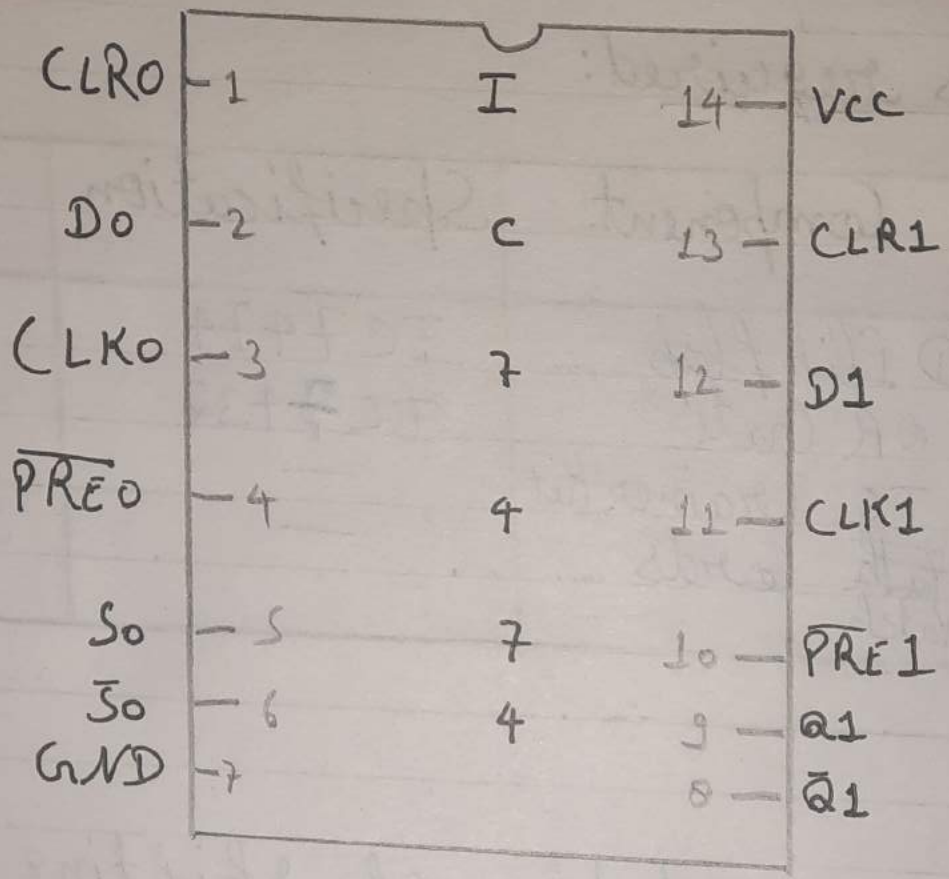
CLR0
1
I
14
VCC
D0
2
C
13
CLR1
CLK0
3
7
12
D1
PRE0
4
4
11
CLK1
S0
5
7
10
PRE1
S0
6
4
9
Q1
GND
7
8
Q1

Date _____

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Truth table:

CLK	Q_3	Q_2	Q_1	Q_0	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

Truth table:

	DATA INPUT				OUTPUT			
CLK	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

Procedure: (1). Connections are given as per circuit diagram.
(2). Logical inputs are given as per circuit diagram.
(3). Observe the output and verify the truth table.

Result:- 3-bit PIPO and PISO shift registers using flip-flop has been designed and verified.

Teacher's Signature : _____

Experiment No. 08

Date _____

Expt. No. 08 Page No. 25

Aim: Design of an ARITHMETIC LOGIC UNIT.

Apparatus required:

S. No.	Component	Specification	Qty.
1	4-to-1 MUXs	IC 74153	1
2	AND Gate	IC 7408	1
3	OR Gate	IC 7432	1
4	XOR Gate	IC 7486	1
5	NOT Gate	IC 7404	1
6	Logic Trainer	–	1
7	Patch Cords & Connecting wire	–	As req.

ALU logic circuit:

The ALU, logic circuit performs the basic logic micro operations: NOT, AND, OR and XOR. From these four micro operations all known logic micro operations can be derived. Fig. 5-2 shows the logic diagram for one stage of logic circuit. The four gates generate the four logic operations and the multiplexer select the desired operation.

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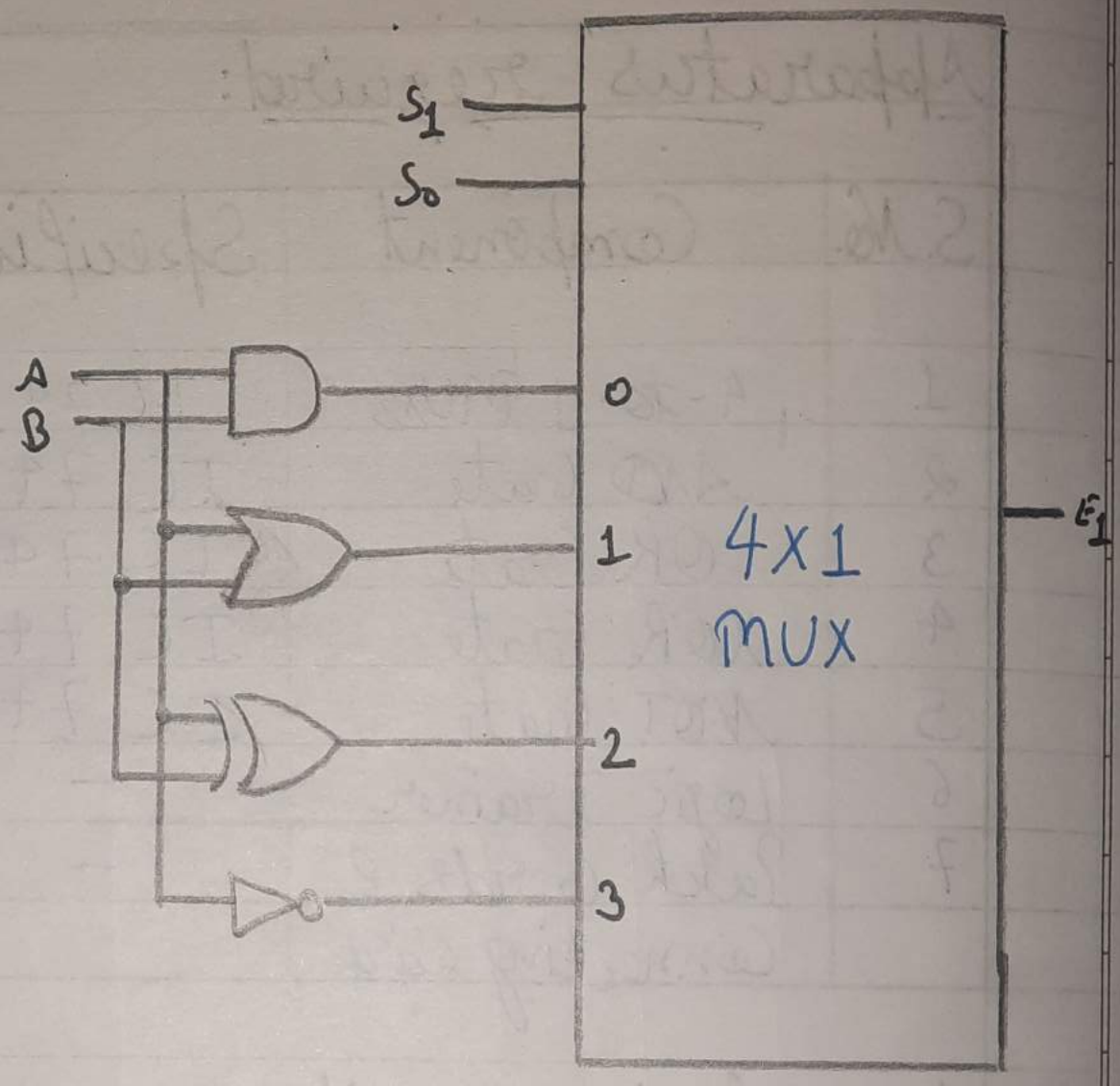

Circuit diagram of the 2-bit logic circuit..

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Function table of the 2-bit logic circuit

S_1	S_0	output	Operation
0	0	AB	AND
0	1	$A+B$	OR
1	0	$A \oplus B$	XOR
1	1	A'	Complement

Procedures:

1. Bring all IC chips necessary to build the circuit from the IC Cabinet.
2. Drive the wiring diagram for the logic diagram.
3. Insure that the power switch of the IC trainer is turned off.
4. Plug the IC chips into the proper sockets.

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Date

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5. Connect the voltage supply and ground lines to the chips.

6. Use the connection leads to connect the circuit according to the derived wiring diagram.

7. Once all connections have been done, turn on the power switch of the IC trainer.

8. Verify the circuit function.

Result: The Arithmetic Logic Unit has been designed and verified.

Precaution:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.
4. After finishing the experiment, turn off the power switch, disconnect the wires, and take out the IC chips from the trainer.

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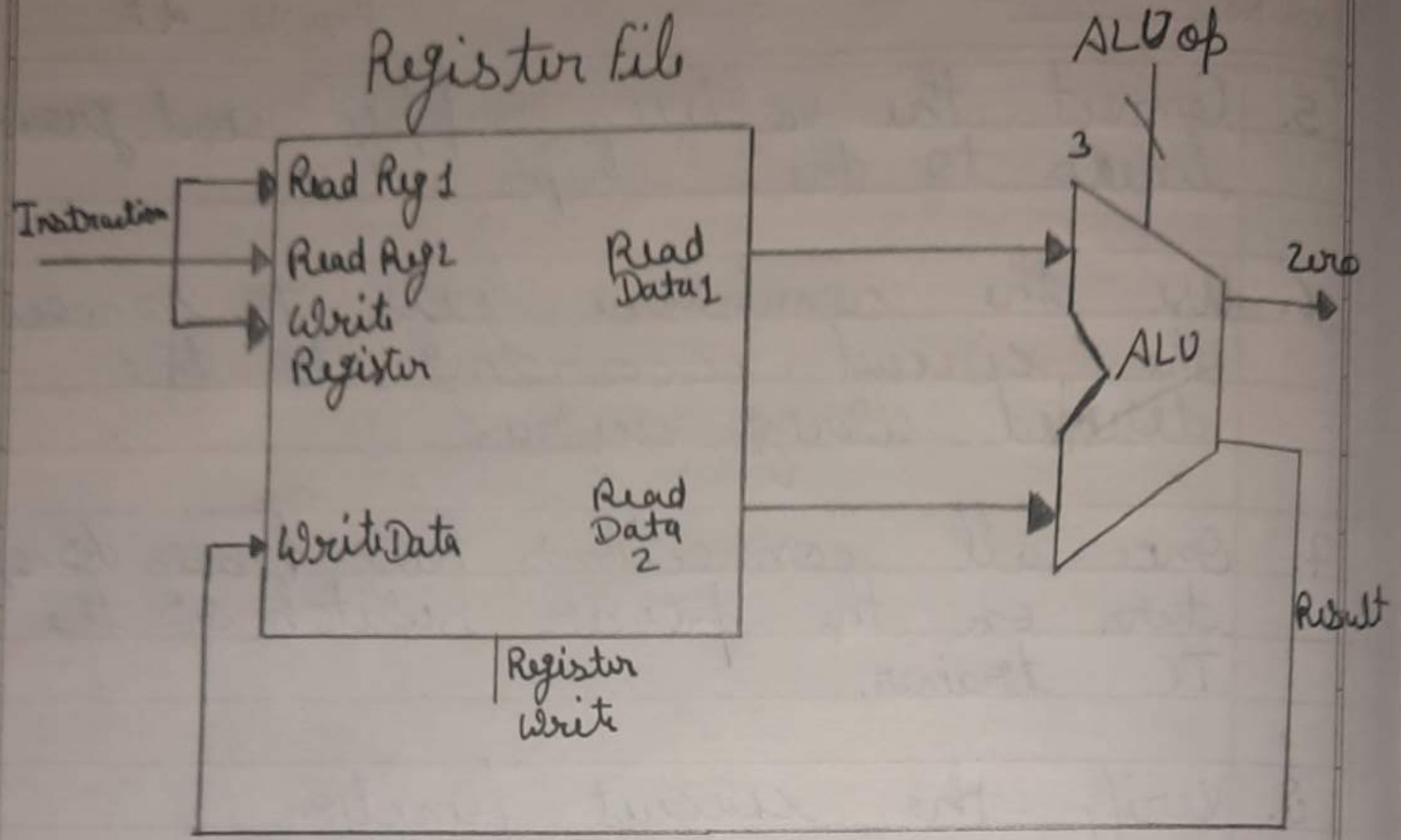

Schematic diagram R-format instruction datapath :

Experiment No. 09

Date

Expt. No. 09 Page No. 28

Aim: Design the data path of a computer from its register transfer language description.

(1). R-format Datapath :-

Implementation of the datapath for R-format instructions is fairly straightforward - the register file and the ALU are all that is required. The ALU accepts its input from the DataRead ports of the register file, and the register file is written to by the ALU result output of the ALU, in combination with the Reg Write signal.

- Format: opcode r1, r2, r3

(2). Load/Store Datapath :-

The Load/Store datapath uses instructions such as lw $t1, offset($t2), where offset denotes a memory address offset applied to the base address in register $t2. The lw instruction reads from

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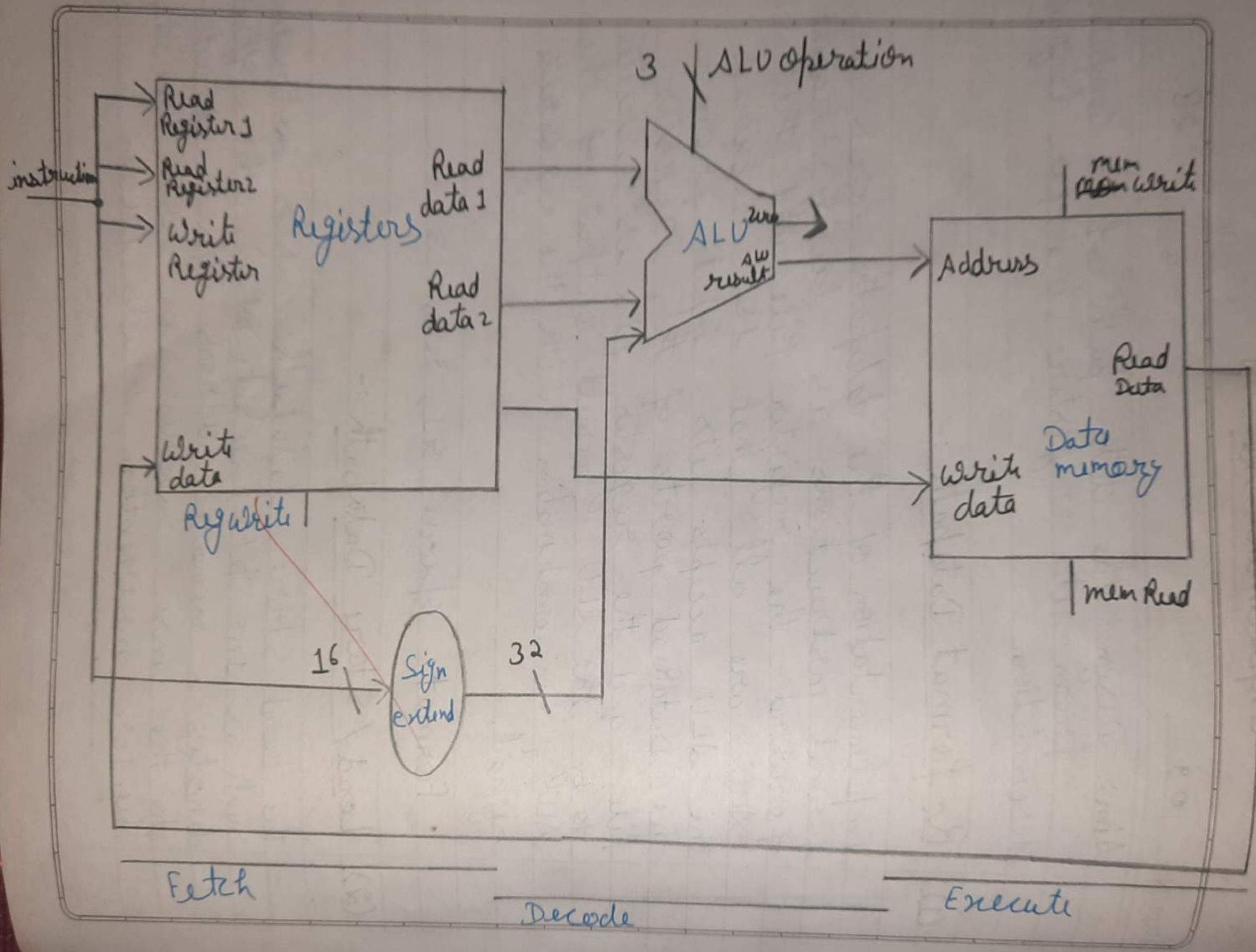
3
ALU operation
Read Register 1
Read Register 2
Write Register
Registers
Read data 1
Read data 2
Write data
RegWrite
instruction
ALU
zero
ALU result
Address
Read Data
Data memory
Write data
MemWrite
MemRead
16
Sign extend
32
Fetch
Decode
Execute

memory and writes into register $t1

The load/store datapath is illustrated and performs the following actions in the order given:

(1). Register Access takes input from the register file, to implement the instruction, data or address fetch step of the fetch-decode-execute cycle.

(2). Memory Address Calculation decodes the base address. This step uses the sign extender and ALU.

Read/Write from Memory takes data or instructions from the data memory, and implements the first part of the execute step of the fetch/decode/execute cycle.

Write into Register File puts data or instructions into the data memory, implementing the second part of the execute step of the fetch/decode/execute cycle.

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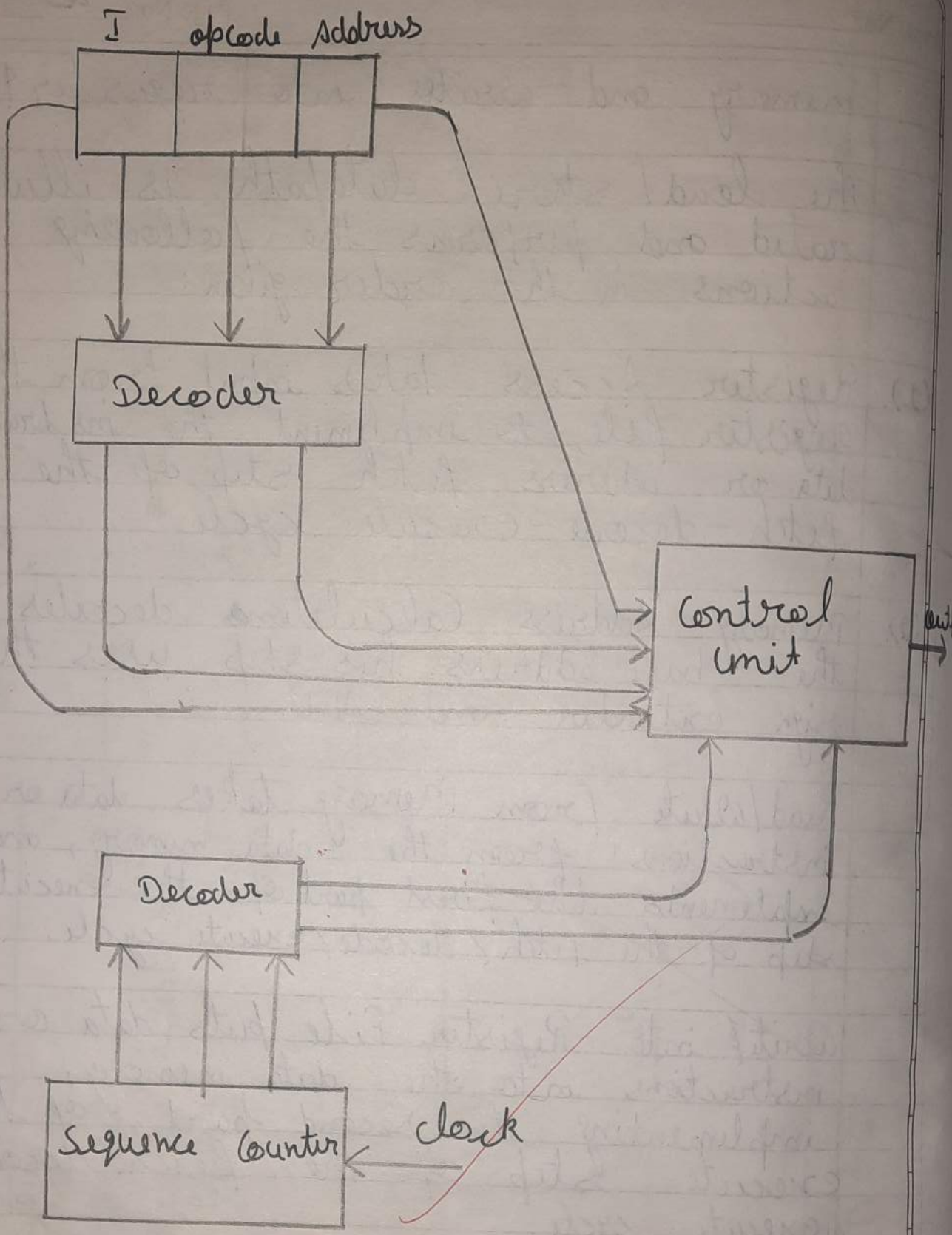
I
opcode
address
Decoder
Control unit
Decoder
Sequence Counter
clock

Experiment No. 10

Date

Expt. No. 10 Page No. 30

Aim:- Design the control unit of a computer using either hardwiring or microprogramming based on its register transfer language description.

Design of Control Unit

Control unit generates timing and control signals for the operations of the computer. The control unit communicates with ALU and main memory. It also controls the transmission between processor, memory and various peripherals. It also instructs the ALU which operations has to be performed on data.

Control unit can be designed by two methods which are given below:

Control
Hardware Unit

It is implemented with the help of gates, flip flops, decoders etc. in the hardware. The inputs to control unit are the instruction register, flags, timing signals etc. This organization can be very complicated if we have to make the control unit large.

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Difference between Hardwired Control and Microprogrammed Control

	Hardwired Control	Microprogrammed Control
(i).	Technology is circuit based.	(i). Technology is software based.
(ii).	It is implemented through flip-flops, gates, decoders etc.	(ii). Microinstructions generate signals to control the execution of instruction.
(iii).	Fixed instruction format.	(iii). Variable instruction format (16-64 bits per instruction).
(iv).	Instructions are register based.	(iv). Instructions are not register based.
(v).	ROM is not used.	(v). ROM is used.
(vi).	It is used in RISC.	(vi). It is used in CISC.
(vii).	Faster decoding.	(vii). Slower decoding.
(viii).	Difficult to modify.	(viii). Easily modified.
(ix).	Chip area is less	(ix). Chip area is large.

Date

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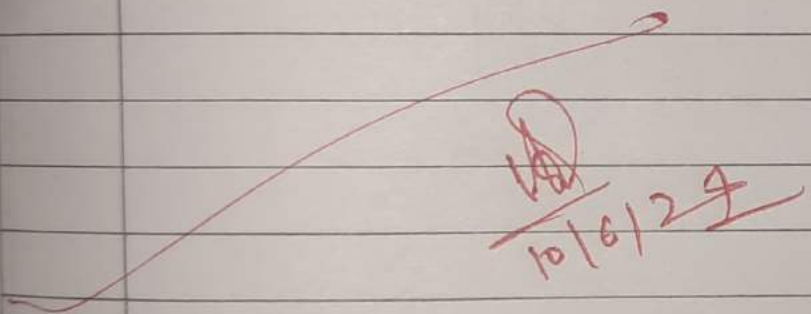
Microprogrammed Control Unit

It is implemented by using programming approach. A sequence of micro operations is carried out by executing a program consisting of micro-instructions. In this organization any modifications or changes can be done by updating the micro program in the control memory by the programmer.



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