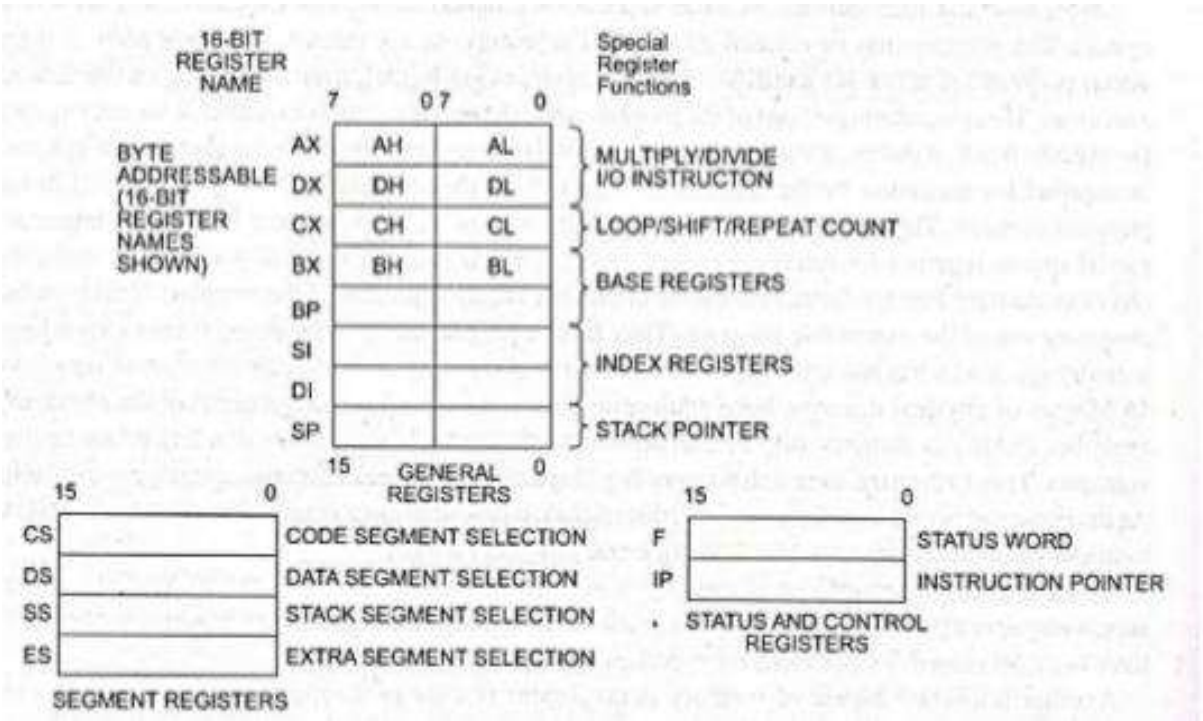
UNIT VII – Advanced Microprocessors

80286 Microprocessor

- The **Intel 80286** is a high-performance 16-bit microprocessor introduced in 1982.
- It has been specially designed for multiuser and multitasking systems.
- 80286 is upwardly compatible with 8086 in terms of instruction set. (That is the 8086,8088,80186,80286 CPU family all contain the same instruction set)
- It has **24 address lines** and **16 data lines**.
- There are two operating modes for 80286
  - The **real** address mode
  - The **protected** virtual memory address mode
- In **real** address mode the processor can address upto **1 MB** of physical memory.
- The **virtual** address mode is for multiuser/multitasking system. In this mode the processor can address upto **1 GB** of virtual memory.

80286 Register Set



The 80286 CPU contains almost the same set of registers, as in 8086.

a) Eight 16-bit general purpose registers.
b) Four 16-bit segment registers.
c) Status and control register
d) Instruction Register.

- The flag register bits are modified according to the result of the execution of logical and arithmetical instructions. These are called status flag bits.

80286 Block Diagram

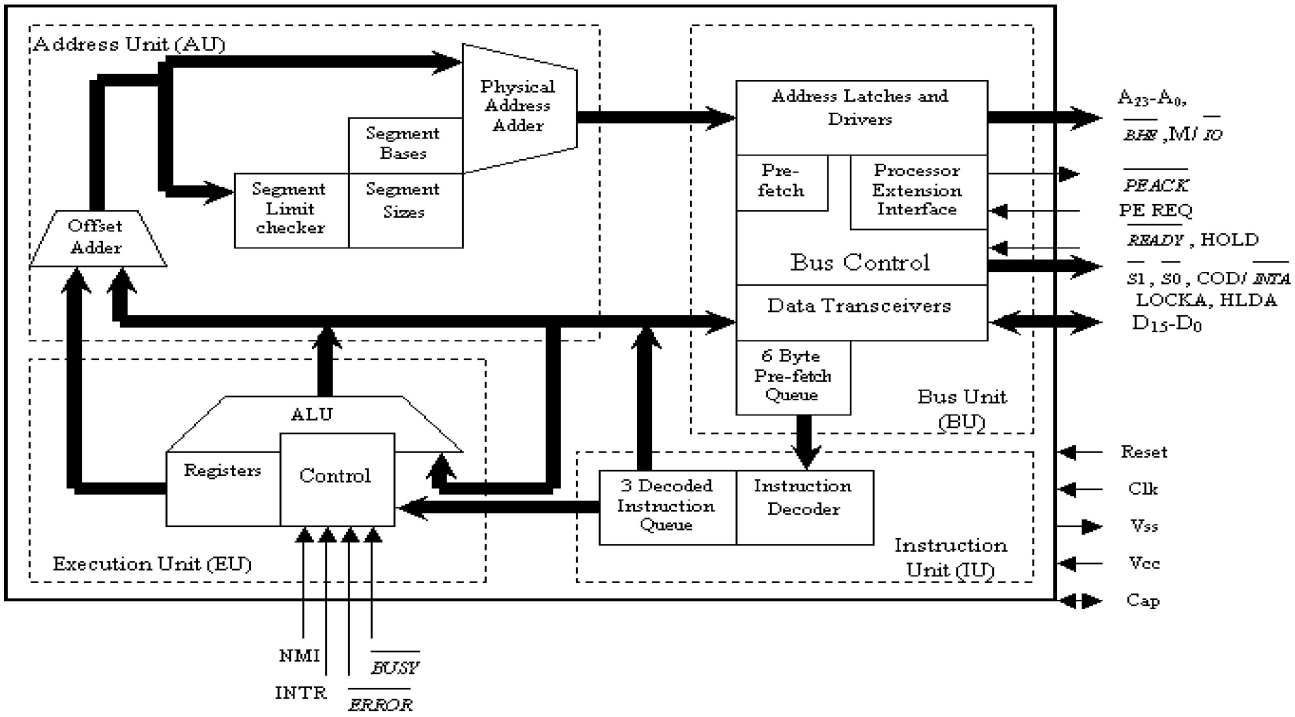


Fig: Block Diagram of 80386

Block diagram of 80286 contain **four** functional parts:

a) Address Unit (AU)
b) Bus Unit (BU)
c) Instruction Set Unit (IU)
d) Execution Unit (EU)

- The **Address Unit (AU)** is responsible for calculating the physical address of instructions and data that CPU wants to access.

- The physical address computed by the address unit is handed over to the **BUS Unit (BU)** of the CPU.
- One of the major function of the bus unit is to fetch instruction bytes from the memory.

- The **Instruction Unit (IU)** accepts instructions from the prefetch queue and an instruction decoder decodes them one by one.

- The **Execution Unit (EU)** is responsible for instructions received from the decoded instruction queue, which sends the data part of the instruction over the data bus. It is responsible for the execution of the decoded instruction.

Operating Modes of 80286

1) Real Address Mode

- 80286 just act as a faster version of 8086.
- And program for 8086 can be executed without modification in 80286.
- In **real** address mode the processor can address upto **1 MB** of physical memory.

2) Protected Virtual Address Mode

- 80286 supports multitasking
- Able to run several program at the same time
- Able to protect memory space for another program
- In this mode the processor can address upto 16 MB of physical memory whereas 8086 can address only 1 MB.
- In this mode the processor can address upto **1 GB** of virtual memory.
- 80286 can treat external storage as it were physical memory and execute programs that are too large to be contained in physical memory.

Flag Register of 80286

Flag register is similar to 8086 which contains 6 conditional/status flags and 3 control flags.

Conditional/Status Flags

- Carry, Auxiliary Carry, Sign, Parity, Zero & Overflow.

Control Flags

- TRAP, Interrupt & Direction Flag.

The **direction flag** is a **flag** that controls the left-to-right or right-to-left **direction** of string processing, stored in the **FLAGS** register.

Interrupt in 80286

Interrupts of 80286 may be divided into three categories,

a) External or Hardware interrupts
b) INT instruction or software interrupts
c) Interrupts generated internally by exceptions (TRAP)

Maskable Interrupt INTR

- This is a maskable interrupt which is to be provided by an external circuit like an interrupt controller.

Non-maskable Interrupt

- NMI has higher priority than the INTR interrupt.
- Once the CPU responds to a NMI request, it does not serve any other interrupt request.

80286 Addressing Modes

(Similar to 8086)

1) Register Addressing Mode
2) Immediate Addressing Mode
3) Direct Addressing Mode
4) Register Indirect Addressing Mode
5) Based Index Addressing Mode
6) Based Addressing Mode
7) Indexed Addressing Mode
8) Input Output Addressing Mode

(Give same example as 8086, because all registers are same & it uses same instruction set).

80286 Memory Management Scheme

Memory is organized into logical segments. Segment size can be anywhere between 1 Byte to 16 KB. All 24 address pins are active and 16 MB of physical memory is available.

Descriptor Cache

- It is 8-byte quantity. Each segment has a descriptor. There are two main types of descriptor -

- Segment Descriptor
- System control Descriptor

- Descriptors are contained in a descriptor table. There are two categories of descriptor table - global and local.
- A system has only one **global descriptor table or GDT**.
- A **local descriptor table or LDT** is set up in the system for each task or closely related group of tasks. Each task can have its own descriptor table and memory area defined by the descriptors in it.

Accessing Segments

- The 80286 microprocessor keeps the base address and limits for the descriptor tables currently in use in internal registers.
- These registers are load descriptor table register (LDTR) and global descriptor table register (GDTR).
- Descriptor in memory is addressed by adding segment selector to these registers.
- The descriptors contain the base address of segments, which when added with the offset in the virtual address points to the required memory location.

Accessing Segments of Higher Privilege Level

- Tasks operate at the lowest privilege level. Usually, segments at a lower privilege level are not allowed to access segments at a higher privilege level directly.
- However, a lower level segment can access a higher level segment indirectly by a Gate Descriptor. The details of a gate descriptor are given herewith.

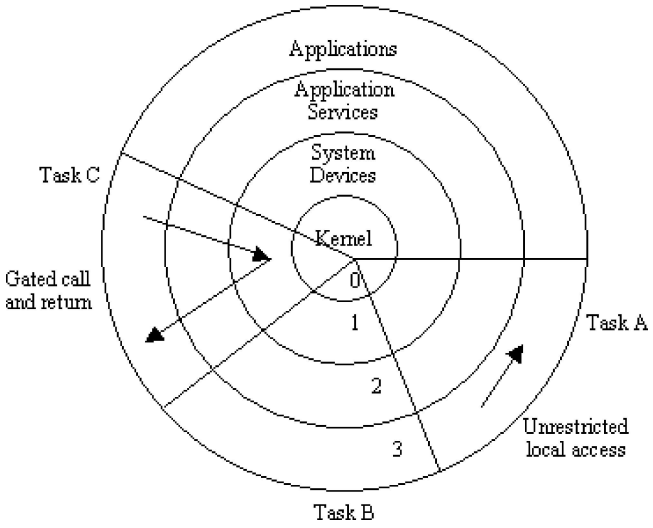


Fig: Privilige Levels

80386 Microprocessor

- 80386 is a **32bit** processor that supports, **8bit/32bit data operands**.
- The **80386 instruction** set is upward compatible with all its predecessors.
- The 80386 can run 8086 applications under protected mode in its virtual 8086 mode of operation.
- With **the 32 bit address bus**, the 80386 can address upto 4Gbytes of physical memory. The physical memory is organised in terms of segments of 4Gbytes at maximum.
- The 80386 CPU supports 16K number of segments and thus the total virtual space of 4Gbytes * 16K = 64 Terrabytes.
- The memory management section of 80386 supports the virtual memory, paging and four levels of protection, maintaining full compatibility with 80286.
- The 80386 offers a set of 8 debug registers DR 0-DR 7 for hardware debugging and control.
- The concept of paging is introduced in 80386 that enables it to organise the available physical memory in terms of pages of size 4Kbytes each, under the segmented memory.

Two versions of 80386 are commonly available:

1) 80386DX

- 32 bit address bus
- 32 bit data bus
- Packaged in 132 pin grid array (PGA)
- Address 4 GB of memory

2) 80386SX

- 24 bit address bus
- 16 bit data bus
- 100 pin flat package
- 16 MB of memory

Block Diagram of 80386 Microprocessor

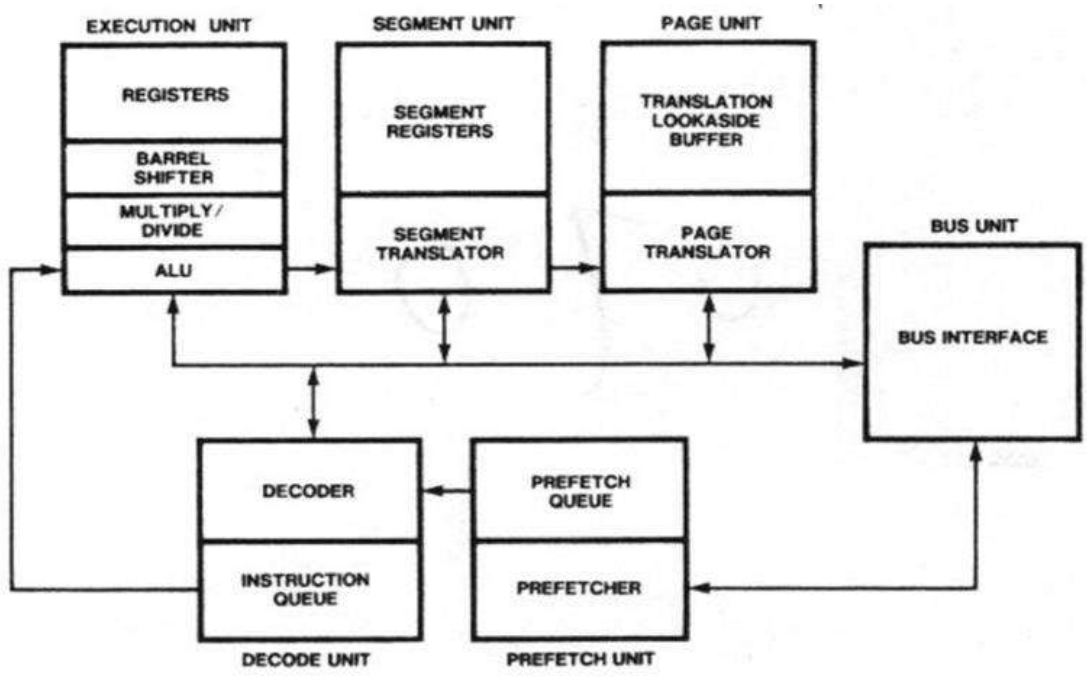


Fig: Block Diagram of 80386 Microprocessor

The Internal Architecture of 80386 is divided into 3 sections.

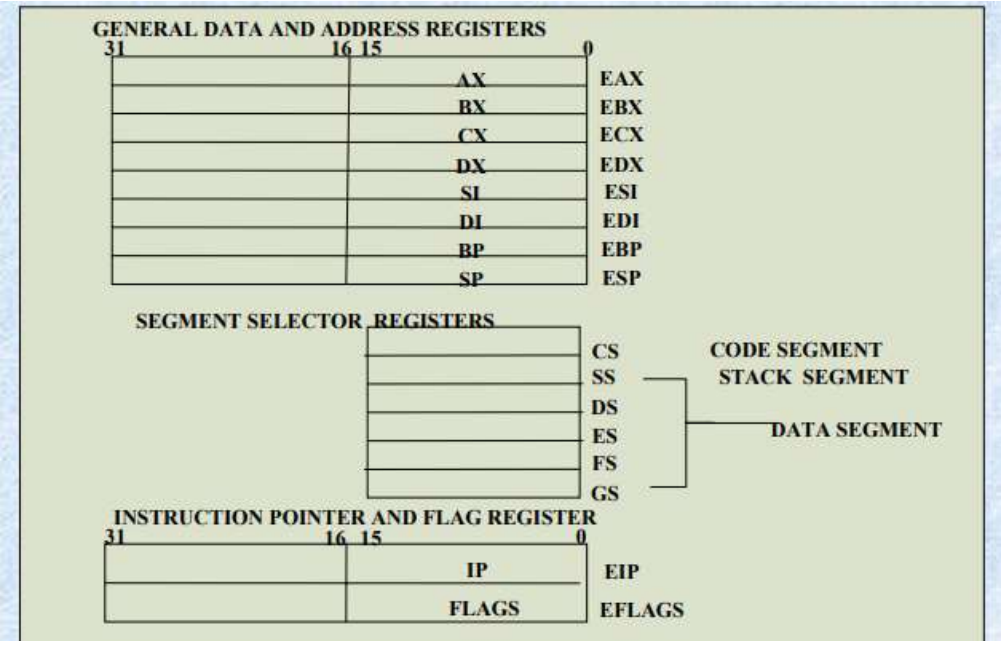
- Central processing unit
- Memory management unit
- Bus interface unit

- Central processing unit is further divided into **Execution unit and Instruction unit**.
- **Execution unit** has 8 General purpose and 8 Special purpose registers which are either used for handling data or calculating offset addresses.
- **The Instruction unit** decodes the opcode bytes received from the 16-byte instruction code queue and arranges them in a 3- instruction decoded instruction queue.

- The **Memory management unit** consists of a **Segmentation unit** and a **Paging unit.**
- **Segmentation unit** allows the use of two address components, viz. segment and offset for relocability and sharing of code and data.
- Segmentation unit allows segments of size 4Gbytes at max.
- The **Paging unit** organizes the physical memory in terms of pages of 4kbytes size each.
- Paging unit works under the control of the segmentation unit, i.e. each segment is further divided into pages. The virtual memory is also organizes in terms of segments and pages by the memory management unit.

- The **Bus control unit** has a prioritizer to resolve the priority of the various bus requests. This controls the access of the bus. The address driver drives the bus enable and address signal A0 – A31.

80386 Register Organization



- The 80386 has eight 32 - bit general purpose registers which may be used as either 8 bit or 16 bit registers.
- A 32 - bit register known as an extended register, is represented by the register name with prefix E.
- Example: A 32-bit register corresponding to AX is EAX, similarly BX is EBX etc.
- The 16 bit registers BP, SP, SI and DI in 8086 are now available with their extended size of 32 bit and are names as EBP, ESP, ESI and EDI.
- AX represents the lower 16 bit of the 32-bit register EAX.
- BP, SP, SI, DI represents the lower 16 bit of their 32 bit counterparts, and can be used as independent 16 bit registers.
- The six **segment registers** available in 80386 are CS, SS, DS, ES, FS and GS.
- The CS and SS are the code and the stack segment registers respectively, while DS, ES, FS, GS are 4 data segment registers.
- A 16-bit **instruction pointer IP** is available along with 32-bit counterpart EIP.
- The **Flag register** of 80386 is a 32-bit register.
- **Control Registers:** The 80386 has three 32-bit control registers CR), CR 2 and CR 3 to hold global machine status independent of the executed task. Load and store instructions are available to access these registers.
- **Debug and Test Registers:** Intel has provided a set of 8 debug registers for hardware debugging.

Protected Mode of 80386

- All the capabilities of 80386 are available for utilization in its protected mode of operation.
- The 80386 in protected mode support all the software written for 80286 and 8086 to be executed under the control of memory management and protection abilities of 80386.
- The protected mode allows the use of additional instruction, addressing modes and capabilities of 80386.

ADDRESSING IN PROTECTED MODE

- In this mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment.

Paging in 80386

- Paging is one of the memory management techniques used for virtual memory multitasking operating system.
- The segmentation scheme may divide the physical memory into a variable size segments but the paging divides the memory into a fixed size pages.
- The pages are just fixed size portions of the program module or data.
- The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time.
- The paging unit is a memory management unit enabled only in protected mode. The paging mechanism allows handling of large segments of memory in terms of pages of 4Kbyte size.

- Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory. Thus the memory requirement of the task is substantially reduced, relinquishing the available memory for other tasks.
- Whenever the other pages of task are required for execution, they may be fetched from the secondary storage.
- The previous page which are executed, need not be available in the memory, and hence the space occupied by them may be relinquished for other tasks.
- Thus paging mechanism provides an effective technique to manage the physical memory for multitasking systems.