# CMOS Bridge Rectifier (CBR) using 28nm Technology

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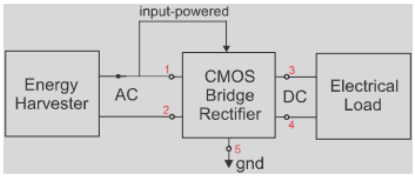
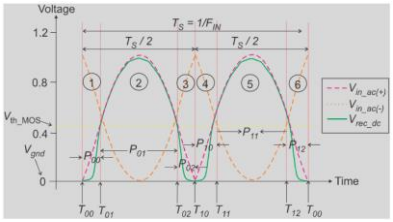
***Abstract*—Generally, CMOS circuits are known for low power supply and great efficiency. The CMOS logic is a collective form of SDG-NMOS and SGS-PMOS.SDG-NMOS refers to drain gate n-channel and SGS-PMOS refers to gate to source p-channel. Full wave bridge rectifier design using CMOS has 11% more efficiency compared to designed with p-n junction. Here we going to implement this circuit at 28nm CMOS technology.**

## I. Reference circuit details

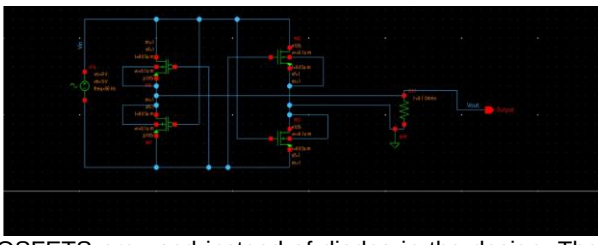
CMOS bridge rectifier is used to reduce the size of the rectifier. It is implemented at 28nm CMOS process technology, powered by its input AC voltage. It has five external connections; two for the input, two for the output, and one connected to the ground (GND). The proposed CBR is targeted for low input AC voltage with an output DC voltage with low voltage drop. The working frequency is set at 50 Hz input with 1.0 V input ac voltage of operation. The proposed CBR functions to convert AC input voltage to a DC output.MOSFETS will be turned on or off based upon the different potential of the gate-source voltage, NMOS will be on only when Vgs>Vth_MOS_NMOS whereas PMOS is turned ON when Vgs<Vth_MOS_PMOS.



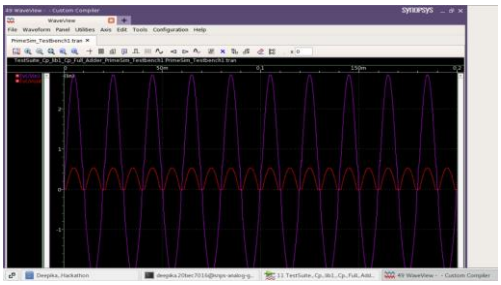

The simulated waveforms of input ac voltages; Vin_ac(+) and Vin_ac(-), together with Vrec_dc and VGND for the CBR circuit. Note that, the period of time from P00 to P02 for the positive cycle of input ac source, while P10 to P12 for the negative cycle of input ac source in CBR circuit. At the initiative of the period t = T00, when Vin_ac(+) = 0 and Vgs of the MOSFETs is zero, thus the MOSFETs P_R1, P_R2, N_R3, and N_R4 in the CBR circuit are turned OFF. When Vin_ac(+) > 0 in state 1, the Vgs of the P_R1 is smaller than Vth_MOS, thus the P_R1 is turned ON. Meanwhile, the N_R4 is turned OFF due to Vgs < Vth_MOS. At t = T01 when Vin_ac(+) > 0, Vgs of the N_R4 is higher than Vth_MOS, thus the N_R4 is turned ON. During the interval, the P_R1 is turned OFF due to Vgs > Vth_MOS. However, the Vin_ac(+) is reduced after reaching the peak voltage at 1.0 V in state 2. Thus, at T = T02 when Vin_ac(+) > 0, Vgs of the N_R4 is smaller than Vth_MOS, causing the N_R4 to turn OFF. Meanwhile, the P_R1 is turned ON due to Vgs < Vth_MOS in state 3. In-state 1, 2, and 3 the MOSFETs P_R2 and N_R3 are turned OFF due to the reverse-biased condition. The operation of the CBR in the second half-cycle is similar to the first half-cycle, except that P_R2 and N_R3 are turning ON. When Vin_ac(-) > 0 in state 4, the Vgs of the P_R2 is smaller than Vth_MOS, thus the P_R2 is turned ON. Meanwhile, the N_R3 is turned OFF due to Vgs < Vth_MOS. At t = T11 when Vin_ac(-) > 0, Vgs of the N_R3 is higher than Vth_MOS, thus the N_R3 is turned ON. During the interval, the P_R2 is turned OFF due to Vgs > Vth_MOS. However, the Vin_ac(-) is reduced after reaching the peak voltage at 1.0 V in state 5. Thus, at T = T12 when Vin_ac(-) > 0, Vgs of the N_R3 is smaller than Vth_MOS, causing the N_R3 to turn OFF. Meanwhile, the P_R2 is turned ON due to Vgs < Vth_MOS in state 6. In-state 4, 5, and 6 the MOSFETs P_R1 and N_R4 are turned OFF due to the reverse-biased condition.

## II. Reference circuit design



MOSFETS are used instead of diodes in the design. These MOSFETs reduce the undesirable power loss during forward bias due to the higher ON-state resistance associated with diodes; a constraint for low input AC voltage of AC-DC converter using CMOS technology. However, the design of an equivalent rectifier based on MOSFET must consider other constraints due to the inherent drawback that includes high leakage, low gate oxide breakdown, and larger area requirements W/L ratio matters a lot with the calculation using the formula the predicted W/L ratio is 750/0.028.

## III. Reference waveforms and area estimation



A full wave rectifier is defined as a type of rectifier that converts both halves of each cycle of an alternating wave (AC signal) into a pulsating DC signal. If such rectifiers rectify both the positive and negative half cycles of an input alternating waveform, the rectifiers are full-wave rectifiers. Thus, by this We can say the efficiency is high.

## IV. Reference papers/Journels


- A. Kempitiya, D.-A. Borca-Tasciuc, and M. M. Hella, "Low Power ASIC for Microwatt Electrostatic Energy Harvesters," IEEE Trans. Ind. Electron., vol. 60, no. 12, pp. 5639–5647, Dec. 2013.
- Design of Analog CMOS Integrated Circuits by Razavi
- M. Stoopman, S. Member, and S. Keyrouz, "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 622–634, 2014.
- https://electronics.stackexchange.com/questions/289755/how-to-design-cmos-bridge-rectifier
- https://ijssst.info/Vol-17/No-41/paper31.pdf