UIT2304 Digital Logic & Computer Organisation

Assignment-2

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IT-A

1.

0 0000 0000 0001 0010

1 0000 0000 0010 0100

2 0000 0000 0100 1000

3 0000 0000 1001 0000

Decimal equivalent = $2^4 + 2^7 = 16 + 128$

$= 144$

2. a) 20

b) M[20] = 40

c) M[M[20]] = M[40] = 60

d) 30

e) M[30] = 50

f) M[M[30]] = M[50] = 70

3.

	Compiler A	Compiler B
rAlpha	$\frac{700 \times 1.2}{3.4 \times 10^9} = 2.47 \times 10^{-6}$	$\frac{500 \times 1.5}{3.4 \times 10^9} = 2.2 \times 10^{-6}$
C86	$\frac{1500 \times 2.2}{2.6 \times 10^9} = 1.26 \times 10^{-6}$	$\frac{1000 \times 40}{2.6 \times 10^9} = 1.53 \times 10^{-6}$

∴ C86 Compiler A is the best option.

4. a) Cycle time = 300 + 400 + 350 + 550 + 100

= 1700 ps

Latency = 1700 ps

Throughput = $1/\text{cycle time} = 1/1700$ inst/ps

b) Cycle time = 200 + 150 + 100 + 190 + 140

= 780 ps

Latency = 780 ps

Throughput = 1/780 inst/ps.

b)

a) Cycle time = 550 + 20 = 570 ps

Latency = 5 x 570 = 2850 ps

Throughput = 1/570 inst/ps

b) Cycle time = 200 + 20 = 220 ps

Latency = 5 x 220 = 1100 ps

Throughput = 1/220 inst/ps

5. a) 1A2BC012

⇒ 0001 1010 0010 1011 1100 0000 0001 0010

Ignore word bits

⇒ 0001 1010 0001 01011

Decimal

⇒ 13579

13579 % 256 = 11

∴ In block 11

b) FFFF00FF

⇒ 1111 1111 1111 1111 0000 0000 1111 1111

⇒ 1111 1111 1111 1111

⇒ 65535

⇒ 65535 % 256 = 255

∴ In block 255

c) 12345678

⇒ 0001 0010 0011 0100 0101 0110 0111 1000

⇒ 0001 0010 0011 0100

⇒ 7456

⇒ 7456 % 256 = 32

∴ In block 32

d) C109D532

=> 1100 0001 0001 1001 1101 0101 0011 0010

=> 1100 0001 0001 1001

=> 49241

=> 49241 % 256 = 105

∴ In Block 105

6. a) 1110000111110000

Left most pg offset

=> 0000111110000

Convert Pg to decimal 7

Page is in frame 7

offset = 0000111110000 - 240

∴ In frame 7, offset 240

b) 0000 0000 0000 0000

Page number 0

offset 0

∴ Page 0, offset 0

7. i) Compulsory misses:

Occurs when a block is accessed for first time.

ii) Capacity misses:

Occurs when cache is not large enough to accomodate all data & some blocks are replaced.

iii) Conflict misses:

Occurs in set associative or direct mapped caches when multiple memory blocks compete

iv) Coherence misses:

Occurs in multicore systems when one core update & memory loc & another core has a stale copy of data in its cache.

8. Level-1:

Fast access to frequently use data

Level-2:

Provide additional space to frequently access data.

Level-3:

Reduces memory access time for multiple users.

Level-4:

Further increase cache size.

9. i) Program Counter (PC):

Keep track of address of next inst to be fetched.

ii) Instruction Register (IR):

Hold the current instruction being executed.

iii) Stack Pointer:

Manages address of top of stack in memory.

iv) Status Register:

Store condition codes flags based on result of operations

v) Memory Address Register:

Holds address where data to be fetched or stored.

10.

RISC	CISC
1. Simple instruction set with reduced instruction	1. Complex instruction set with larger instruction
2. Fixed length instruction	2. Variable length instruction
3. Large no. of registers	3. Small no. of registers
4. Single clock cycle	4. Multiple clock cycles
5. Deeper pipeline	5. Shorter pipelines
6. Store orchitecture	6. Memory operation part of inst
7. Simplified control unit	7. Complex control unit
8. Optimizing compiler software	8. Hardware designed to Handle
9. Smaller code	9. Code can be complex
10. ARM, MIPS	10. Intel, AMD