

The following table lists RISC-V assembler pseudo instructions:

Pesudo-instruction	Expansion	Description
nop	addi zero,zero,0	No operation
li rd, expression	(several expansions)	Load immediate
la rd, symbol	(several expansions)	Load address
mv rd, rs1	addi rd, rs, 0	Copy register
not rd, rs1	xori rd, rs, -1	One's complement
neg rd, rs1	sub rd, x0, rs	Two's complement
negw rd, rs1	subw rd, x0, rs	Two's complement Word
sext.w rd, rs1	addiw rd, rs, 0	Sign extend Word
seqz rd, rs1	sltiu rd, rs, 1	Set if = zero
snez rd, rs1	sltu rd, x0, rs	Set if ≠ zero
sltz rd, rs1	slt rd, rs, x0	Set if < zero
sgtz rd, rs1	slt rd, x0, rs	Set if > zero
fmv.s frd, frs1	fsgnj.s frd, frs, frs	Single-precision move
fabs.s frd, frs1	fsgnjx.s frd, frs, frs	Single-precision absolute value
fneg.s frd, frs1	fsgnjn.s frd, frs, frs	Single-precision negate
fmv.d frd, frs1	fsgnj.d frd, frs, frs	Double-precision move
fabs.d frd, frs1	fsgnjx.d frd, frs, frs	Double-precision absolute value
fneg.d frd, frs1	fsgnjn.d frd, frs, frs	Double-precision negate
beqz rs1, offset	beq rs, x0, offset	Branch if = zero
bnez rs1, offset	bne rs, x0, offset	Branch if ≠ zero
blez rs1, offset	bge x0, rs, offset	Branch if ≤ zero
bgez rs1, offset	bge rs, x0, offset	Branch if ≥ zero
bltz rs1, offset	blt rs, x0, offset	Branch if < zero
bgtz rs1, offset	blt x0, rs, offset	Branch if > zero
bgt rs, rt, offset	blt rt, rs, offset	Branch if >
ble rs, rt, offset	bge rt, rs, offset	Branch if ≤
bgtu rs, rt, offset	bltu rt, rs, offset	Branch if >, unsigned
bleu rs, rt, offset	bltu rt, rs, offset	Branch if ≤, unsigned
j offset	jal x0, offset	Jump
jr offset	jal x1, offset	Jump register
ret	jalr x0, x1, 0	Return from subroutine