

9.38.5 RISC-V Instruction Formats

The RISC-V Instruction Set Manual Volume I: User-Level ISA lists 15 instruction formats where some of the formats have multiple variants. For the ‘.insn’ pseudo directive the assembler recognizes some of the formats. Typically, the most general variant of the instruction format is used by the ‘.insn’ directive.

The following table lists the abbreviations used in the table of instruction formats:

opcode	Unsigned immediate or opcode name for 7-bits opcode.
opcode2	Unsigned immediate or opcode name for 2-bits opcode.
func7	Unsigned immediate for 7-bits function code.
func6	Unsigned immediate for 6-bits function code.
func4	Unsigned immediate for 4-bits function code.
func3	Unsigned immediate for 3-bits function code.
func2	Unsigned immediate for 2-bits function code.
rd	Destination register number for operand x, can be GPR or FPR.
rd’	Destination register number for operand x, only accept s0-s1, a0-a5, fs0-fs1 and fa0-fa5.
rs1	First source register number for operand x, can be GPR or FPR.
rs1’	First source register number for operand x, only accept s0-s1, a0-a5, fs0-fs1 and fa0-fa5.
rs2	Second source register number for operand x, can be GPR or FPR.
rs2’	Second source register number for operand x, only accept s0-s1, a0-a5, fs0-fs1 and fa0-fa5.
simm12	Sign-extended 12-bit immediate for operand x.
simm20	Sign-extended 20-bit immediate for operand x.

simm6	Sign-extended 6-bit immediate for operand x.
uimm5	Unsigned 5-bit immediate for operand x.
uimm6	Unsigned 6-bit immediate for operand x.
uimm8	Unsigned 8-bit immediate for operand x.
symbol	Symbol or lable reference for operand x.

The following table lists all available opcode name:

C0
C1
C2

Opcode space for compressed instructions.

LOAD

Opcode space for load instructions.

LOAD_FP

Opcode space for floating-point load instructions.

STORE

Opcode space for store instructions.

STORE_FP

Opcode space for floating-point store instructions.

AUIPC

Opcode space for auipc instruction.

LUI

Opcode space for lui instruction.

BRANCH

Opcode space for branch instructions.

JAL

Opcode space for jal instruction.

JALR

Opcode space for jalr instruction.

OP

Opcode space for ALU instructions.

OP_32

Opcode space for 32-bits ALU instructions.

OP_IMM

Opcode space for ALU with immediate instructions.

OP_IMM_32

Opcode space for 32-bits ALU with immediate instructions.

OP_FP

Opcode space for floating-point operation instructions.

MADD

Opcode space for madd instruction.

MSUB

Opcode space for msub instruction.

NMADD

Opcode space for nmadd instruction.

NMSUB

Opcode space for msub instruction.

AMO

Opcode space for atomic memory operation instructions.

MISC_MEM

Opcode space for misc instructions.

SYSTEM

Opcode space for system instructions.

CUSTOM_0

CUSTOM_1

CUSTOM_2

CUSTOM_3

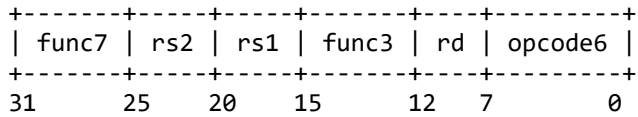
Opcode space for customize instructions.

An instruction is two or four bytes in length and must be aligned on a 2 byte boundary. The first two bits of the instruction specify the length of the instruction, 00, 01 and 10 indicates a two byte instruction, 11 indicates a

four byte instruction.

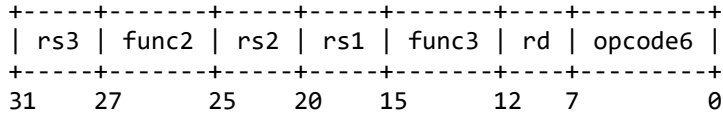
The following table lists the RISC-V instruction formats that are available with the ‘.insn’ pseudo directive:

R type: .insn r opcode6, func3, func7, rd, rs1, rs2



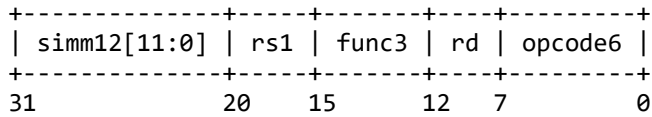
R type with 4 register operands: .insn r opcode6, func3, func2, rd, rs1, rs2, rs3

R4 type: .insn r4 opcode6, func3, func2, rd, rs1, rs2, rs3

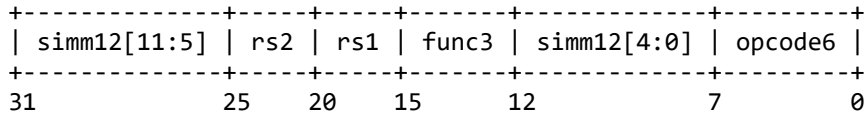


I type: .insn i opcode6, func3, rd, rs1, simm12

I type: .insn i opcode6, func3, rd, simm12(rs1)

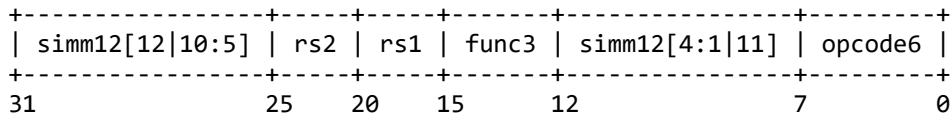


S type: .insn s opcode6, func3, rs2, simm12(rs1)

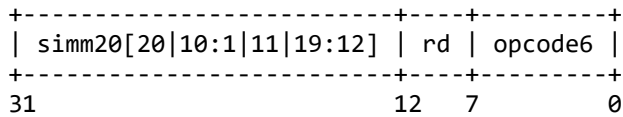


B type: .insn s opcode6, func3, rs1, rs2, symbol

SB type: .insn sb opcode6, func3, rs1, rs2, symbol

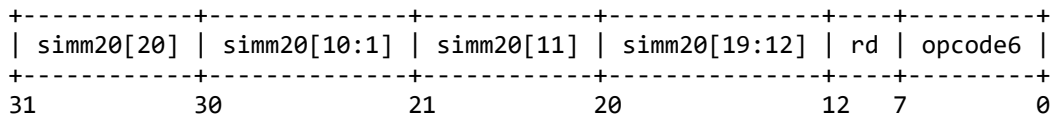


U type: .insn u opcode6, rd, simm20

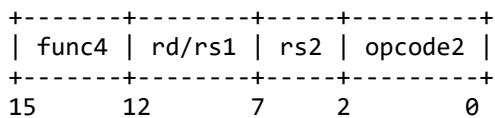


J type: .insn j opcode6, rd, symbol

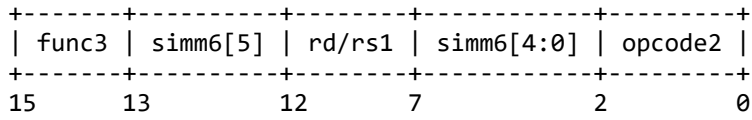
UJ type: .insn uj opcode6, rd, symbol



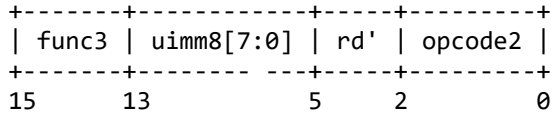
CR type: .insn cr opcode2, func4, rd, rs2



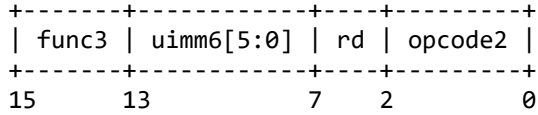
CI type: .insn ci opcode2, func3, rd, simm6



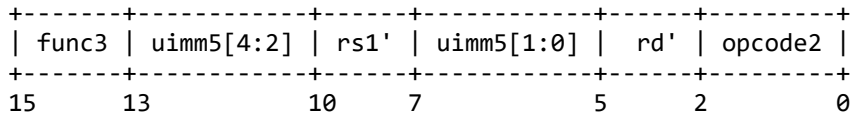
CIW type: .insn ciw opcode2, func3, rd', uimm8



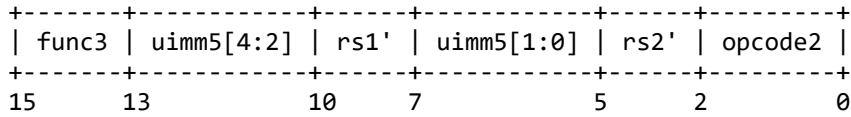
CSS type: .insn css opcode2, func3, rd, uimm6



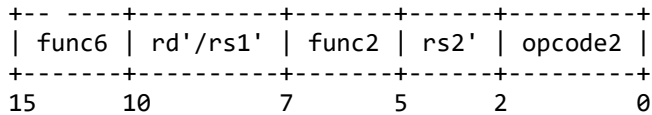
CL type: .insn cl opcode2, func3, rd', uimm5(rs1')



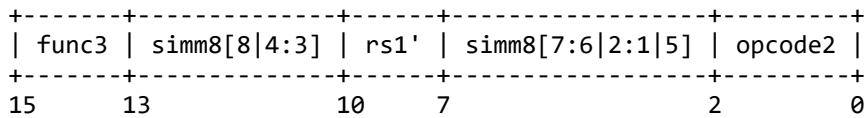
CS type: .insn cs opcode2, func3, rs2', uimm5(rs1')



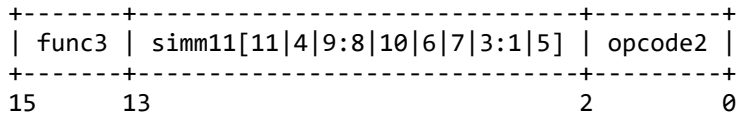
CA type: .insn ca opcode2, func6, func2, rd', rs2'



CB type: .insn cb opcode2, func3, rs1', symbol



CJ type: .insn cj opcode2, symbol



For the complete list of all instruction format variants see The RISC-V Instruction Set Manual Volume I: User-Level ISA.