Experiment No : 5

Aim : To study about Timer Programming .

Procedure:

- Create a square wave of 50% duty cycle (with equal portions high and low) on the P1.5 bit using timer mode 1 with timer 0 to generate the time delay. Display the output using edsim simulator. Use CPL to transition from hi to lo
- Modify TL and TH in question 1 to get the largest pulse width possible. Use SETB and CLR to transition from hi,lo
- Assume that XTAL = 16 MHz. Write A program for timer 0 to create a pulse width of 5 ms on P2.3 in mode 1.
- Create a square wave (with 75%portion high and 25% portion low) on the P1.5 bit using timer mode 1 with timer 0 to generate the time delay. Display the output using edsim simulator. use CPL to transition from hi to lo
- Assume XTAL = 11.0592 MHz, generate a square wave of 50% duty cycle on P1.0 using timer 1 in mode 2
- Assume XTAL = 11.0592 MHz, generate a time delay of 50 counts,200 times, using timer1 mode2. find the total time delay generated

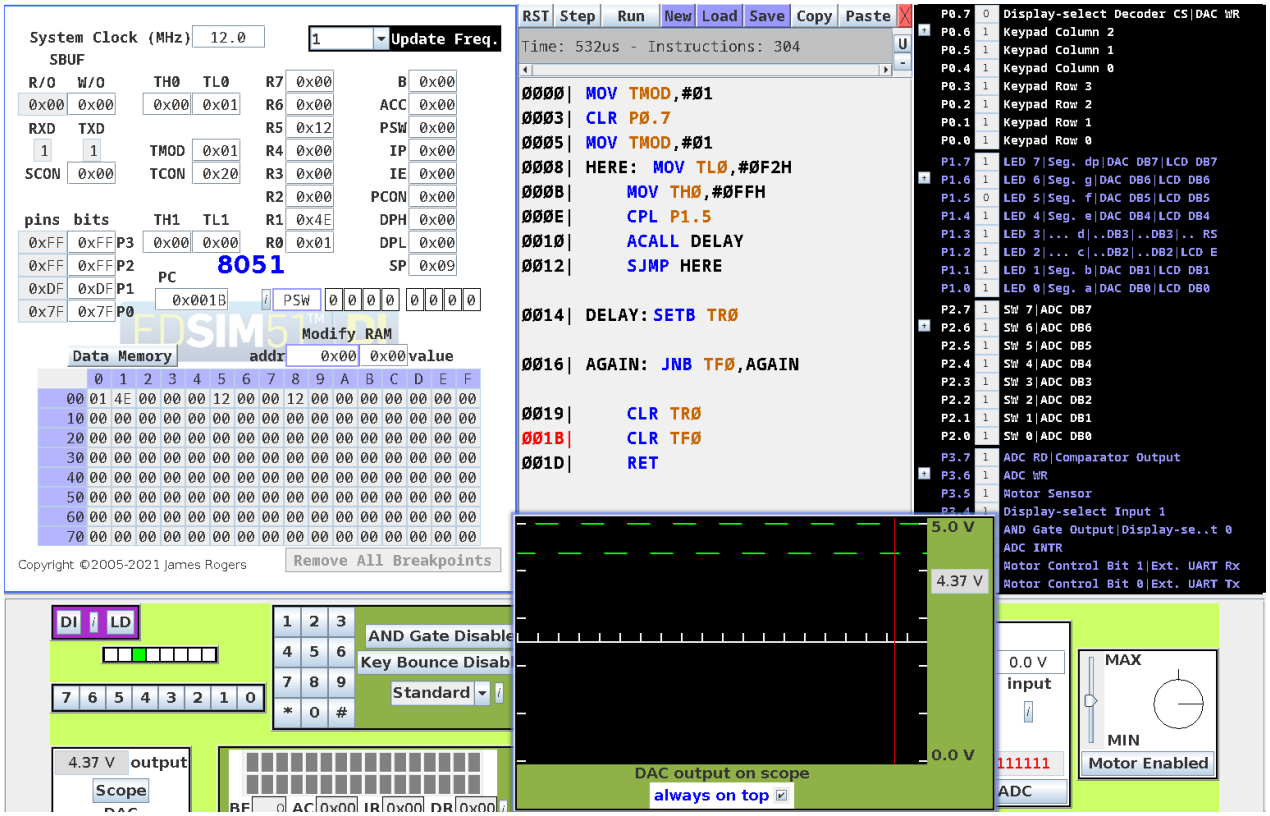
Programs :

- **Program 1**

```
MOV TMOD,#01
CLR P0.7
HERE:   MOV TL0,#0F2H
        MOV TH0,#0FFH
        CPL P1.5
        ACALL DELAY
        SJMP HERE
DELAY: SETB TR0
AGAIN: JNB TF0,AGAIN

        CLR TR0
        CLR TF0
        RET
```

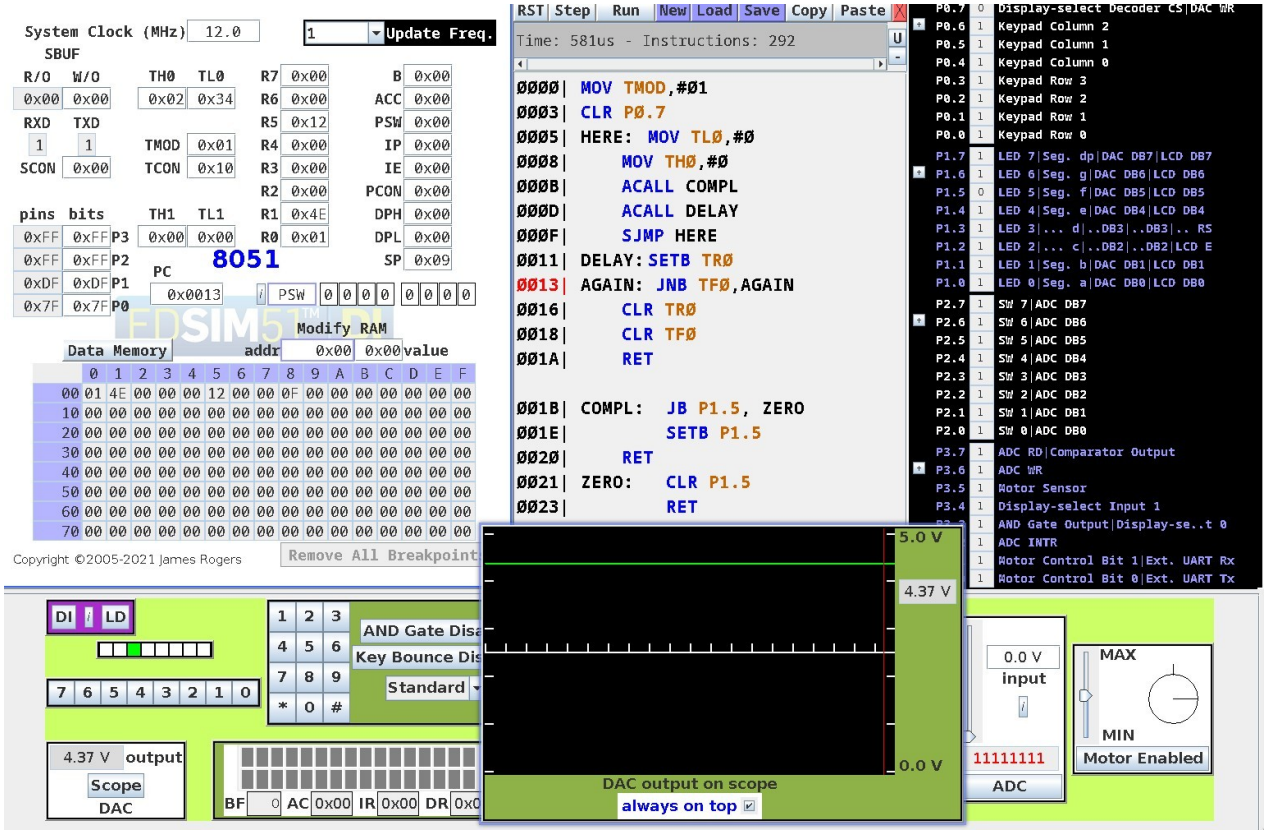
Output :



- **Program 2**

```
 MOV TMOD,#01
 CLR P0.7
HERE:   MOV TL0,#0
        MOV TH0,#0
        ACALL COMPL
        ACALL DELAY
        SJMP HERE
DELAY: SETB TR0
AGAIN: JNB TF0,AGAIN
        CLR TR0
        CLR TF0
        RET
COMPL: JB P1.5, ZERO
        SETB P1.5
        RET
ZERO: CLR P1.5
        RET
```

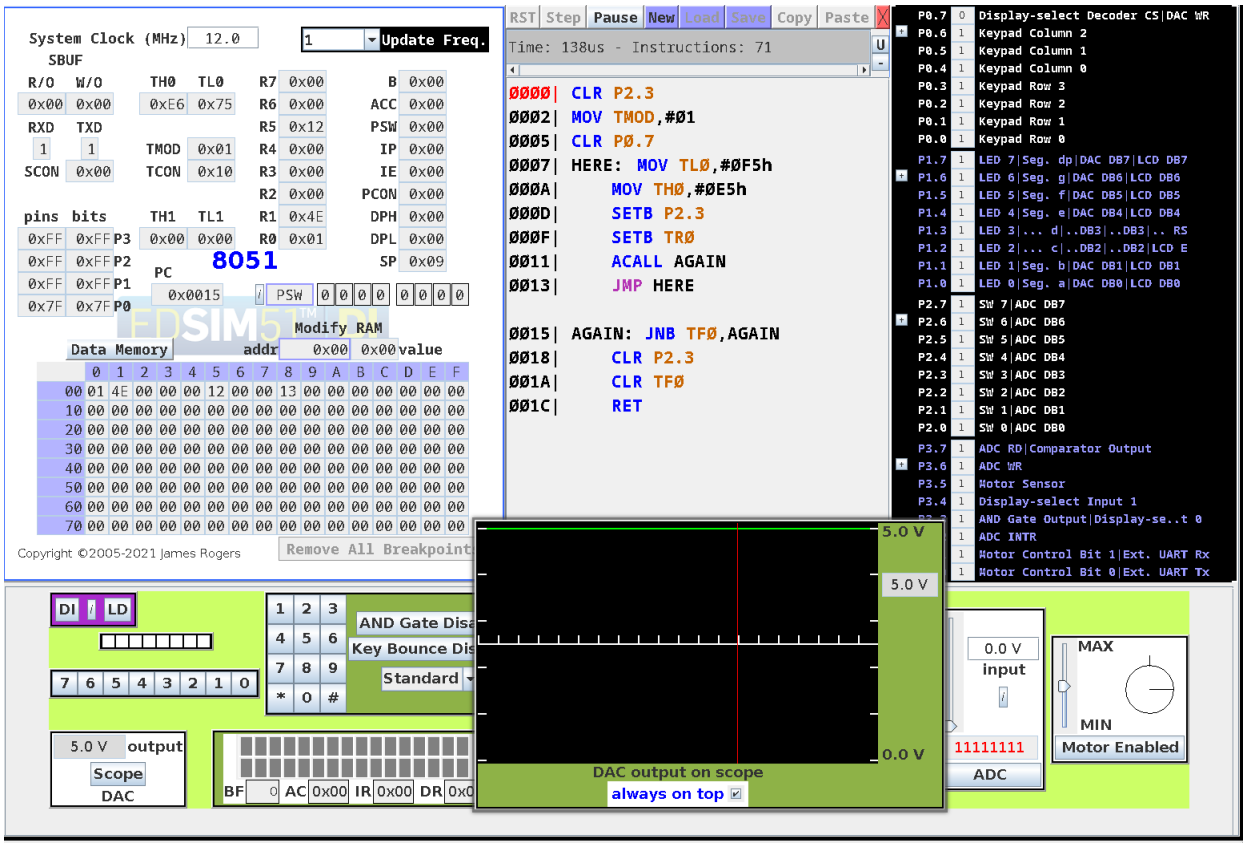
Output :



- **Program 3**

```
CLR P2.3
MOV TMOD,#01
CLR P0.7
HERE:  MOV TL0,#0F5h
                MOV TH0,#0E5h
                SETB P2.3
                SETB TR0
                ACALL AGAIN
                JMP HERE
AGAIN: JNB TF0,AGAIN
                CLR P2.3
                CLR TR0
                CLR TF0
                RET
```

Output :



- **Program 4**

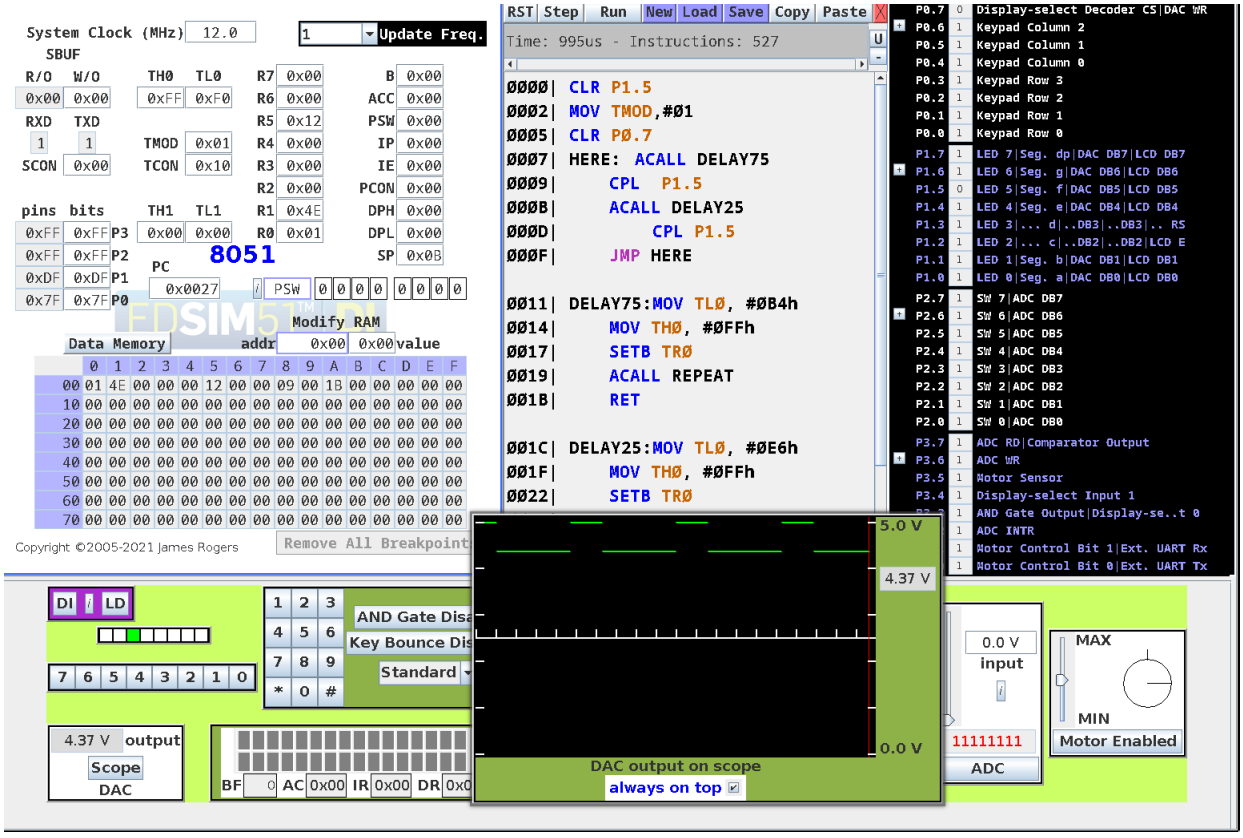
```
CLR P1.5
MOV TMOD,#01
CLR P0.7
HERE:   ACALL DELAY75
                    CPL   P1.5
                    ACALL DELAY25
                    CPL P1.5
                    JMP HERE

DELAY75:MOV TL0, #0B4h
                    MOV TH0, #0FFh
                    SETB TR0
                    ACALL REPEAT
                    RET

DELAY25:MOV TL0, #0E6h
                    MOV TH0, #0FFh
                    SETB TR0
                    ACALL REPEAT
                    RET

REPEAT: JNB TF0, REPEAT
                    CLR TF0
                    CLR TR0
                    RET
```

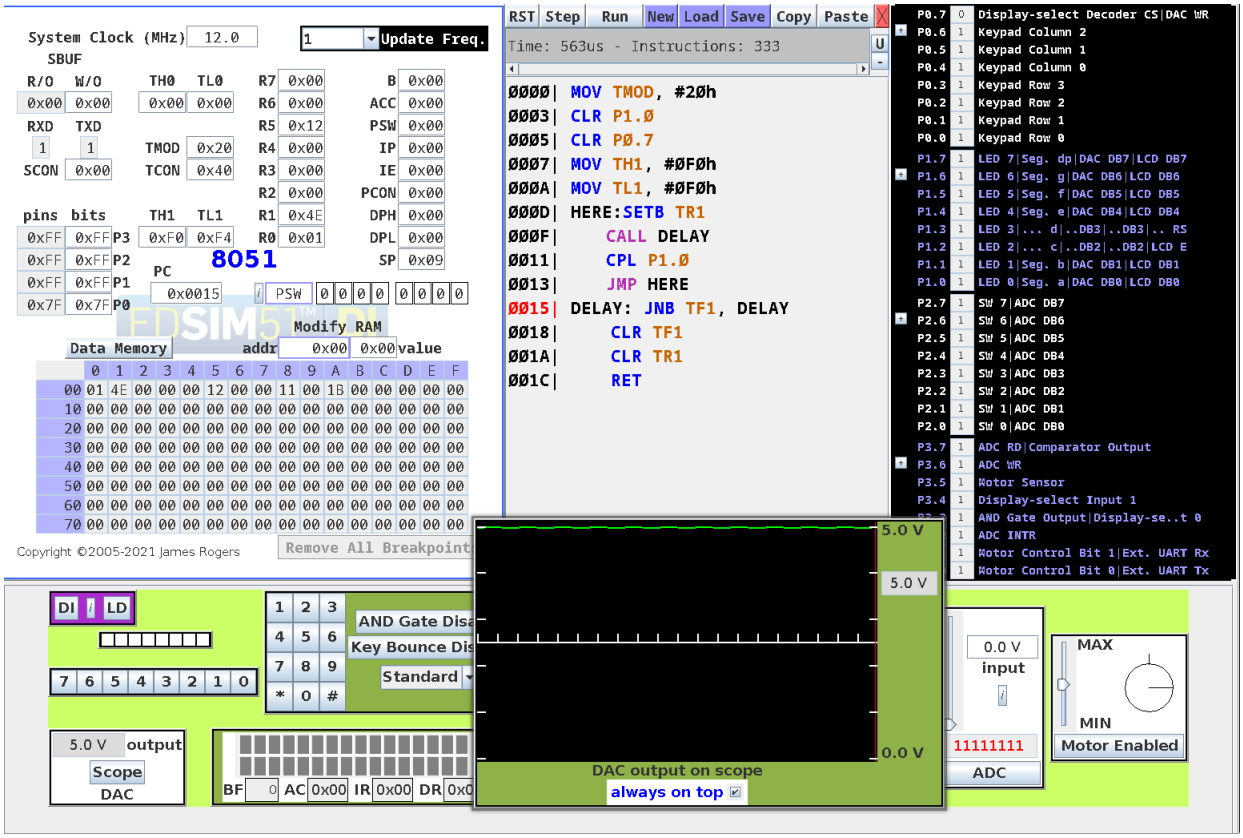
Output :



- **Program 5**

```
MOV TMOD, #20h
CLR P1.0
CLR P0.7
MOV TH1, #0F0h
MOV TL1, #0F0h
HERE:SETB TR1
                CALL DELAY
                CPL P1.0
                JMP HERE
DELAY: JNB TF1, DELAY
                CLR TF1
                CLR TR1
                RET
```

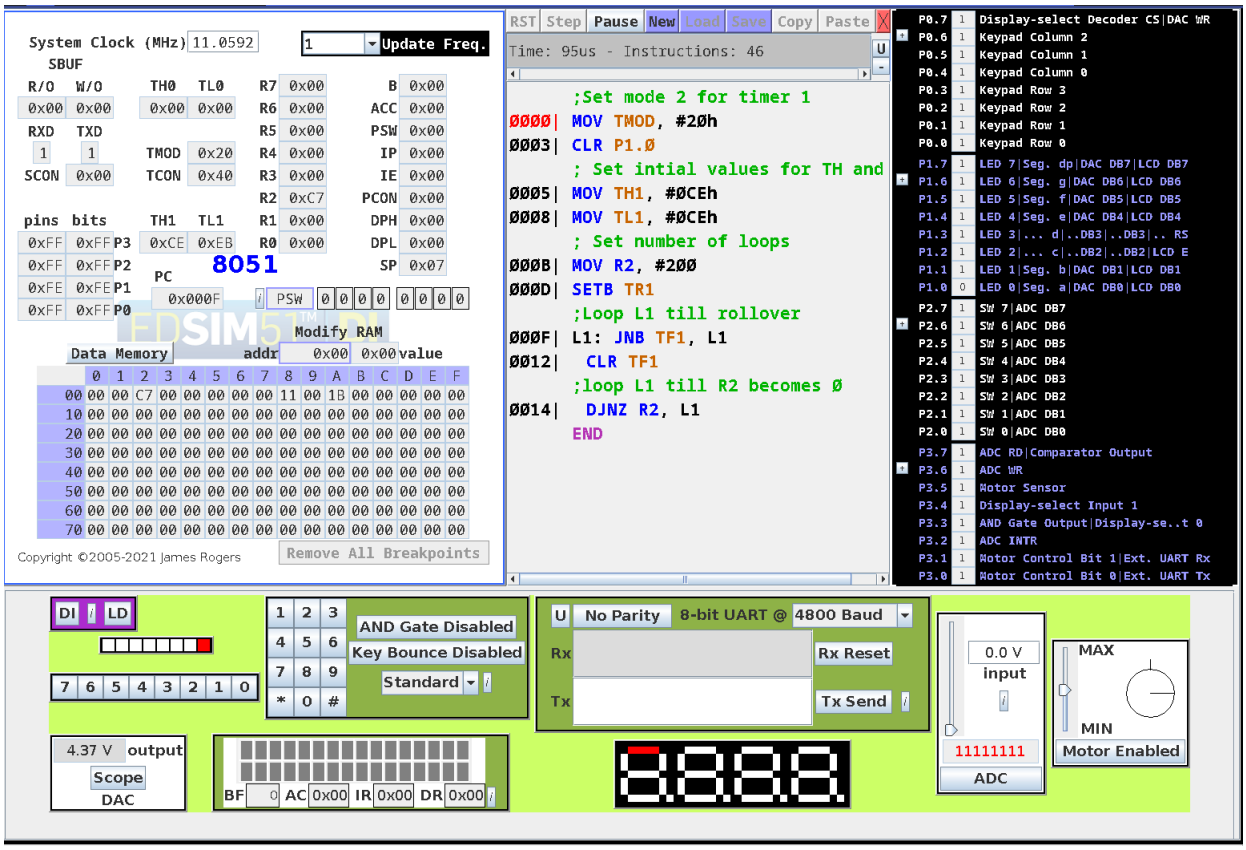
Output :



- **Program 6**

```
;Set mode 2 for timer 1
MOV TMOD, #20h
CLR P1.0
; Set intial values for TH and TL
MOV TH1, #0CEh
MOV TL1, #0CEh
; Set number of loops
MOV R2, #200
SETB TR1
;Loop L1 till rollover
L1: JNB TF1, L1
        CLR TF1
;loop L1 till R2 becomes 0
        DJNZ R2, L1
END
```

Output :



Total time delay generated:

Let frequency of clock pulse be f and the crystal frequency be C; then;

f = C/12

= 11.0592/12

= 921KHz

Let time for one machine cycle be T; then:

T = 1/f

= 1/921

= 1.085μs

Therefore total time delay(D) generated is

D = 50 ∗ 200 ∗ T

= 10.8ms

Conclusion :

Programs to study Timer were successfully implemented.

Deepraj Bhosale

181105016