EL 6463: Advanced Hardware Design 2020

FINAL EXAM (20%) DUE: Thursday, December 24th, 11:55 PM EDT

Instructions

- Read all instructions carefully before starting your exam.
- Complete **all** questions.
- This exam is to be completed **individually.** Collaboration/plagiarism will not be tolerated.
- Please abide by the code of conduct (located at the bottom of this exam). Sign a copy and include it in your submission.
- Clarification questions can be posted on Slack in #finalexam, but do not put any specifics about your own answers in the channel.
- During the exam period, you will not be allowed to receive assistance from the teaching staff regarding the use of the tools or implementation/simulation.

Overview:

In this exam the focus is on testing your knowledge and understanding of High Level Synthesis for digital design. This exam comprises a mix of implementation and analysis which should be submitted as part of a report. When creating your project, select FPGA part XC7A35TLCPG236

Questions

Problem A: Baseline implementation and Analysis (do not modify the C code)

[8 points]

(1) You have been provided with a baseline algorithm implementation in C (please check the spreadsheet for your allocated design/exam variant and then download the corresponding C source from NYU Classes). Understand the C implementation.

(2) Prepare a C-based testbench to simulate the design. Run the simulation and add relevant screenshots (that show that the algorithm works and that you understand the output) to your report. Your simulation should include printing the test inputs and outputs of your testbench. [1 pt]

(3) Synthesize the given baseline design and explain the initial synthesized hardware's resource usage, describing which parts of the C code are mapped to what kind of FPGA resources. State and explain your reasons for the mappings. [2 pts]

(4) Perform C/RTL co-simulation of your design and add screenshot(s) to your report. Explain how co-simulation works and annotate the screenshot to show that the co-simulation works as expected. [2 pts]

(5) What part(s) of the design are dominating the latency? Explain your justifications using screenshots of the scheduling analysis and synthesis report. [1 pt]

(6) Prepare a list of potential structures in the code that provide opportunities for optimization (e.g., what are the loops/datatypes/arrays which you can apply pragmas to). For these structures, list which pragmas are likely to be applicable. Are there any pragmas that do not work? Explain your answer. [2 pt]

Problem B: Optimization and Design Space Exploration (For parts (1) to (3), do not modify the C code, use the directives file to add pragmas for the different solutions)

[8 points]

(1) Given the pragmas you identified in A-(6), identify pragmas/settings that will:
   (a) Increase the latency of the synthesized hardware (compared to the baseline) [0.2 pt]
   (b) Decrease the latency of the synthesized hardware (compared to the baseline) [0.2 pt]
   (c) Increase the resource usage of the synthesized hardware (compared to the baseline) [0.2 pt]
   (d) Decrease the resource utilization of the synthesized hardware (compared to the baseline) [0.2 pt]
   (e) Increase the throughput of the synthesized hardware (compared to the baseline) [0.2 pt]

(2) Implement combinations of pragmas used in the above question. Report the resource usage, latency, timing of every solution generated. Make a graph where x-axis is latency and y-axis is area, and plot every solution to show trade-offs between the solutions. Explain the graph in your own words, what are the tradeoffs and the reasons ? [3 pts]

(3) Add resource constraints to the C design (make sure that the number of resource constraints are lower than reported in the baseline design synthesis report). Add the resulting resource usage and scheduling screenshot to your report. Explain how this impacts synthesis of your baseline design. [2 pts]

(4) Currently, the C implementation is not amenable to pipelining with an II=1, modify the C code to achieve this. For this part of the question, please create a new project with your modified C code. Explain the changes made. [2 pts]

Problem C: Short Answer Questions (Feel free to modify the C design)

[5 points]

(1) If your design has a loop and the loop bound is a variable, does your design synthesize ? Explain in detail. [0.5 pt]

(2) Consider a loop in your design which uses an array. If you map the array to a BRAM and unroll loop fully, what do you observe ? Write the pragmas you used. [0.5 pt]

(3) Synthesize the C design with a variable as ap_start signal. Is it possible to synthesize without the handshake signal ? [0.5 pt]

(4) Compare and contrast the differences between traditional VHDL/Verilog based design and C-based HLS. [0.5 pt]

(5) When you add the loop unroll pragma with increasing unroll factor, would one always expect the resource utilization to increase ? Explain your answer. [0.5 pt]

(6) Consider the loop in your design which uses an array. How does array partitioning impact the resulting latency? [0.5 pt]

(7) Pipelining a loop with II=1 is expected to reduce latency. Does this optimization always result in reduction of latency? [0.5 pt]

(8) Contrast the difference in resource usage and latency, between (a) an array resource mapped as registers and, (b) an array resource mapped as BRAM. State reasons for this difference. [0.5 pt]

(9) Identify 4 c constructs that are not synthesizable. Explain your reasoning. [0.5 pts]

(10) Take 2 constructs from (9) and explain how you can make them synthesizable. Give an example for each [0.5 pts]?

Deliverables:

Submit a zip file with your Vivado HLS solutions and a PDF report containing answers to the short answer questions.

Student Exam Code of Conduct

I certify and affirm that,

1. The work presented is 100% my own, and I have not collaborated with anyone on this test.
2. I have not cheated or misrepresented someone else's work as my own.
3. I have not copied or recorded the content of this test.
4. I will not discuss, nor in any way divulge the content of this test.
5. I understand that my failure to abide by my code of conduct will result in consequences outlined in the university code of conduct.

Name: _____

Signature: _____

Date: _____