PROGRAMMABLE LOGIC DEVICES

Introduction:

- Logic designers have a wide range of standard ICs available to them with numerous logic functions and logic circuit arrangements on a chip.
- Standard ICs (Ex: Multiplexers, Demultiplexers, Decoders, Encoders, Adders, Code converters, comparators, etc.) are also called fixed function ICs because each one of them performs a fixed digital operation.
- However, there are some problems with circuit and system designs that use only standard ICs. Some of the disadvantages of this method are as follows:
    1. Large board space requirements
    2. Large power requirements
    3. Lack of quality
    4. Additional cost, space, power requirements, etc. required to modify the design or to introduce more features.
- To overcome the disadvantageous of fixed function ICs, *Application specific integrated circuits (ASIC)* have been developed.
- The ASICs are designed by the users to meet the specific requirements of a circuit and are produced by an IC manufacturer as per the specifications supplied by the user.
- The advantageous of ASIC are as follows:
    1. Reduced space requirements
    2. Reduced power requirements
    3. Considerable cost reduction if produced in large volumes.
    4. Large reduction in size through the use of high levels on integration.
- The disadvantageous of ASIC are as follows:
    1. Initial development cost may be enormous.
    2. Testing methods may have to be developed which may also increase the cost and effort.
- Another approach which has the advantageous of both the above methods is the use of *PROGRAMMABLE LOGIC DEVICES (PLDs).*
- *A Programmable logic device is an IC that is user configurable and is capable of implementing logic functions.* It is programmed by the user to perform a function required for application.
- A PLD contains a large number of gates, flip-flops, and registers that are interconnected on the chip. The IC is said to be programmable because the specific functions of the IC for a given application is determined by the selective breaking of some of the interconnections while leaving others intact.
- This process is called Programming because it produces the desired circuit pattern interconnecting the gates, flipflops and registers and so on.
- PLDs can be programmed in a few seconds and hence give more flexibility to experiment with designs.
- The advantageous of PLDs over fixed function ICs are as follows:
    1. Low development cost
    2. Less space requirement
    3. Less power requirement
    4. High reliability

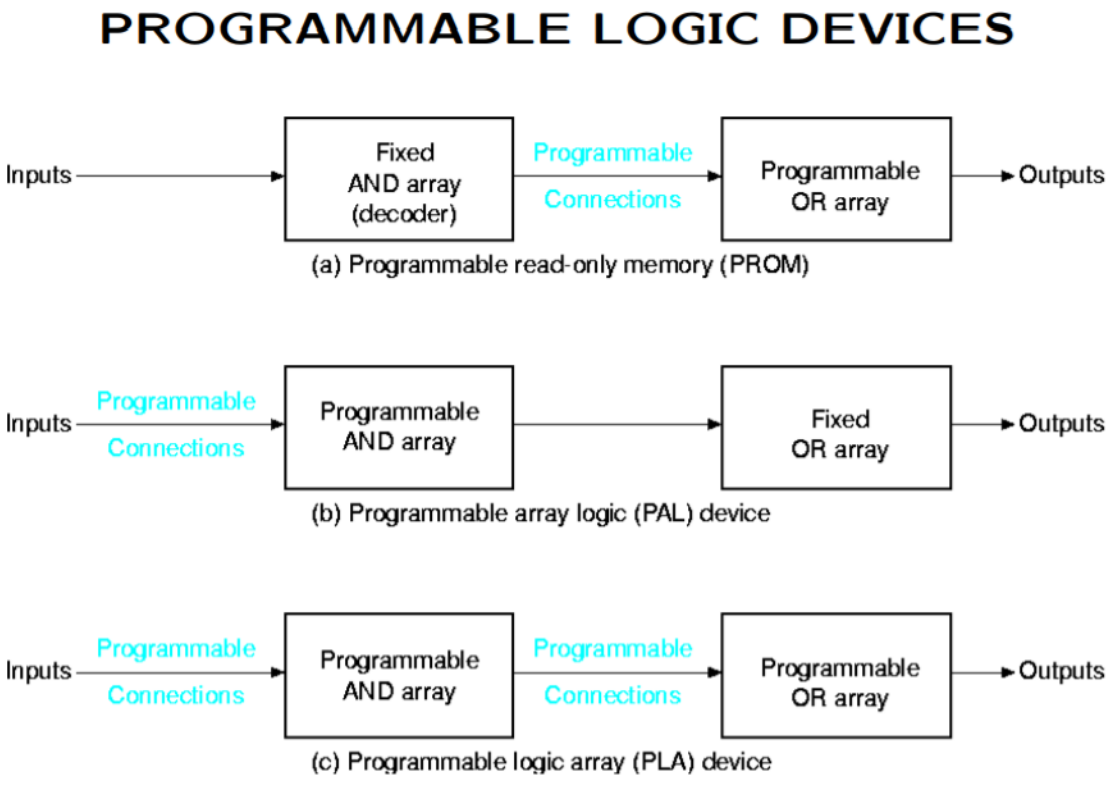
DIVYA SATHI B
Assistant Professor
ECE Department

5. Easy circuit testing.
6. Easy design modification
7. High design security
8. Less design time
9. High switching speed.

- PLDs have many of the advantageous of ASICs as given below:
  1. Higher densities
  2. Lower quantity production costs
  3. Design security
  4. Reduced power requirements
  5. Reduced space requirements.

COMBINATIONAL PROGRAMMABLE LOGIC DEVICES:

- A combinational PLD is an integrated circuit with programmable gates divided into an AND array and an OR array to provide an AND-OR sum of products implementation.
- There are three major types of combinational PLDs and they differ in the placement of the programmable connection in the AND-OR array.
- The various PLDs used are
  1. PALs (Programmable array logics)
  2. PLAs (Programmable logic arrays)
  3. PROMs (Programmable read only memories)
- Figure shows the configuration of the 3 PLDs.

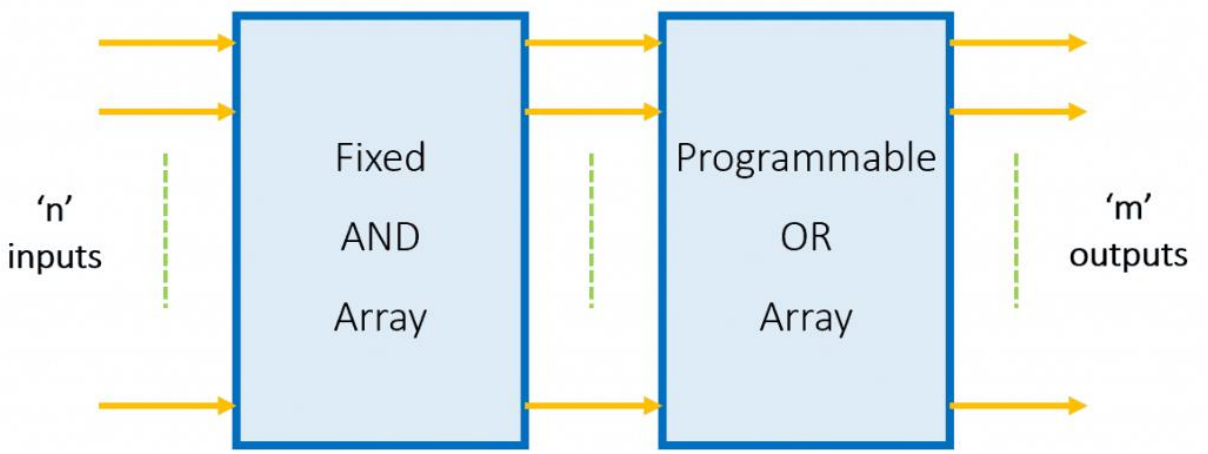


DIVYA SATHI B
Assistant Professor
ECE Department

- The programmable read-only memory (PROM) has a fixed AND array constructed as a decoder and a programmable OR array. The AND gates are programmable to provide the product terms for the Boolean functions, which are logically summed in each OR gate.
- The Programmable array logic (PAL) has programmable AND array a fixed OR array.
- The most flexible PLD is the programmable logic array (PLA) where both the AND and OR arrays can be programmed. The product terms in the AND array may be shared by any OR gate to provide the required sum of products implementation.

PROGRAMMABLE READ ONLY MEMORY (PROM):

- A programmable ROM is a memory device which permanently stores binary information.
- It differs from a normal ROM because it can be programmed electrically once using a PROM programmer.
- This programmable logic device has Fixed AND arrays and Programmable OR arrays.



Block Diagram of PROM

- The inputs of the AND array are not programmable. Thus, we generate 2^n product terms using 2^n AND gates having n inputs each, using n x 2^n decoder.
- This decoder generates '2^n' minterms.
- Unlike the AND array, the OR gates inputs are programmable.
- The output of the AND array are the inputs to this OR array system.
- Thus, the output of PROM will be as a sum of minterms.

DIVYA SATHI B
Assistant Professor
ECE Department

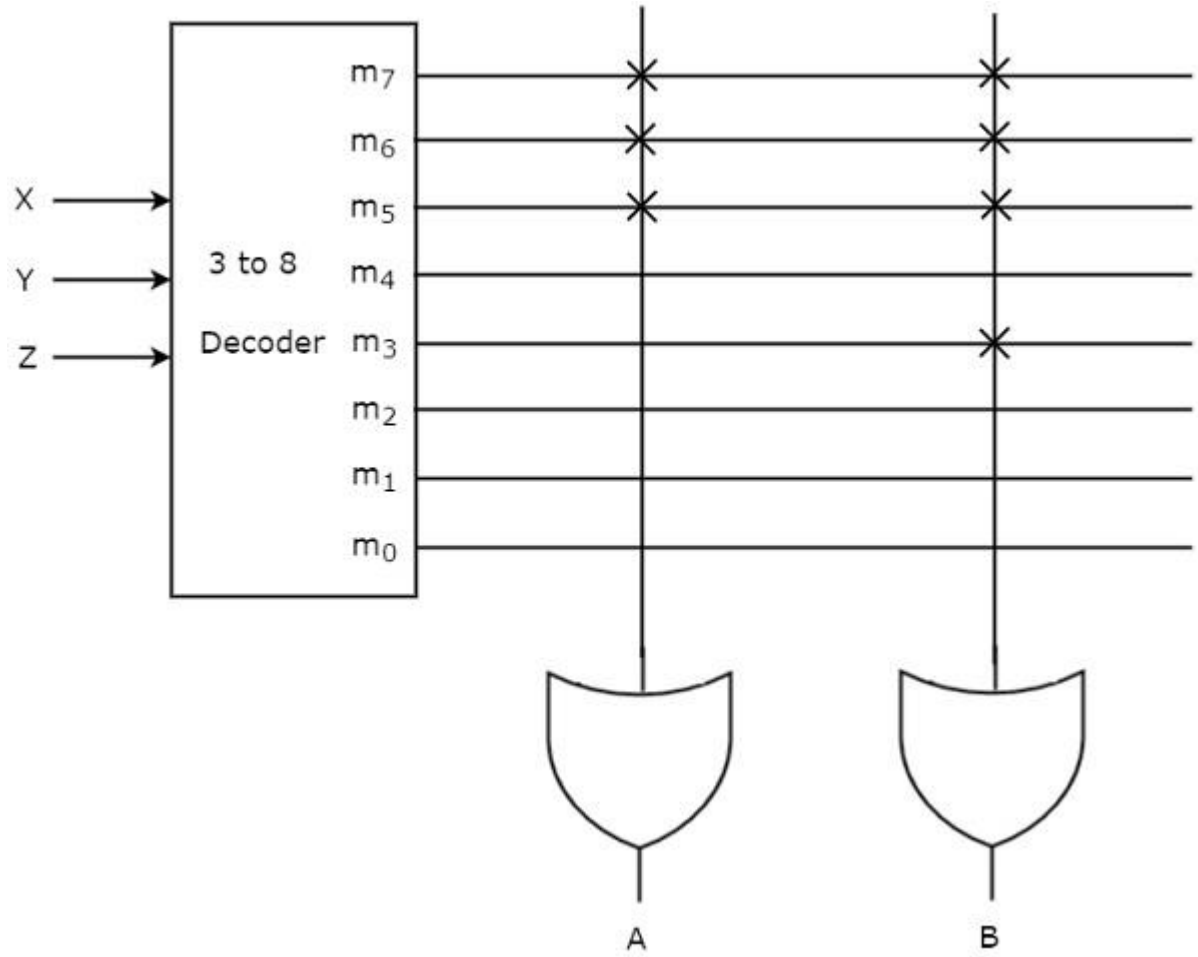
Example

Let us implement the following Boolean functions using PROM.

$$A(X,Y,Z)=\sum m(5,6,7)$$

$$B(X,Y,Z)=\sum m(3,5,6,7)$$

Answer: The given two functions are in sum of min terms form and each function is having three variables X, Y & Z. So, we require a 3 to 8 decoder and two programmable OR gates for producing these two functions. The corresponding PROM is shown in the following figure.

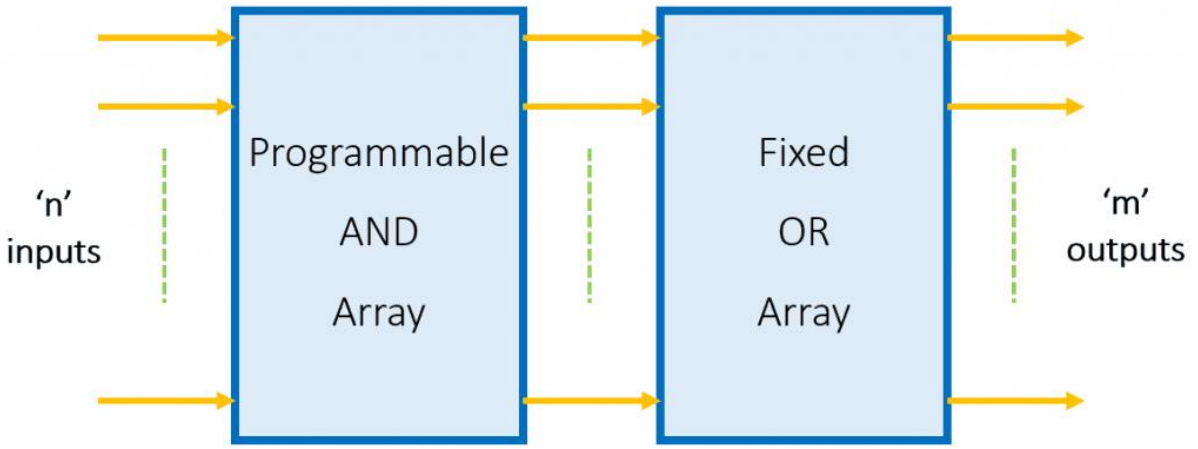


Here, 3 to 8 decoder generates eight min terms. The two programmable OR gates have the access of all these min terms. But, only the required min terms are programmed in order to produce the respective Boolean functions by each OR gate. The symbol 'X' is used for programmable connections.

DIVYA SATHI B
Assistant Professor
ECE Department

PROGRAMMABLE ARRAY LOGIC (PAL):

- PAL is a programmable logic device that has Programmable AND array & fixed OR array.
- The advantage of PAL is that we can generate only the required product terms of Boolean function instead of generating all the min terms by using programmable AND gates.
- The block diagram of PAL is shown in the following figure.



Block Diagram of PAL

- Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required product terms by using these AND gates.
- Here, the inputs of OR gates are not of programmable type. So, the number of inputs to each OR gate will be of fixed type. Hence, apply those required product terms to each OR gate as inputs. Therefore, the outputs of PAL will be in the form of sum of products form.

Example

Let us implement the following Boolean functions using PAL.

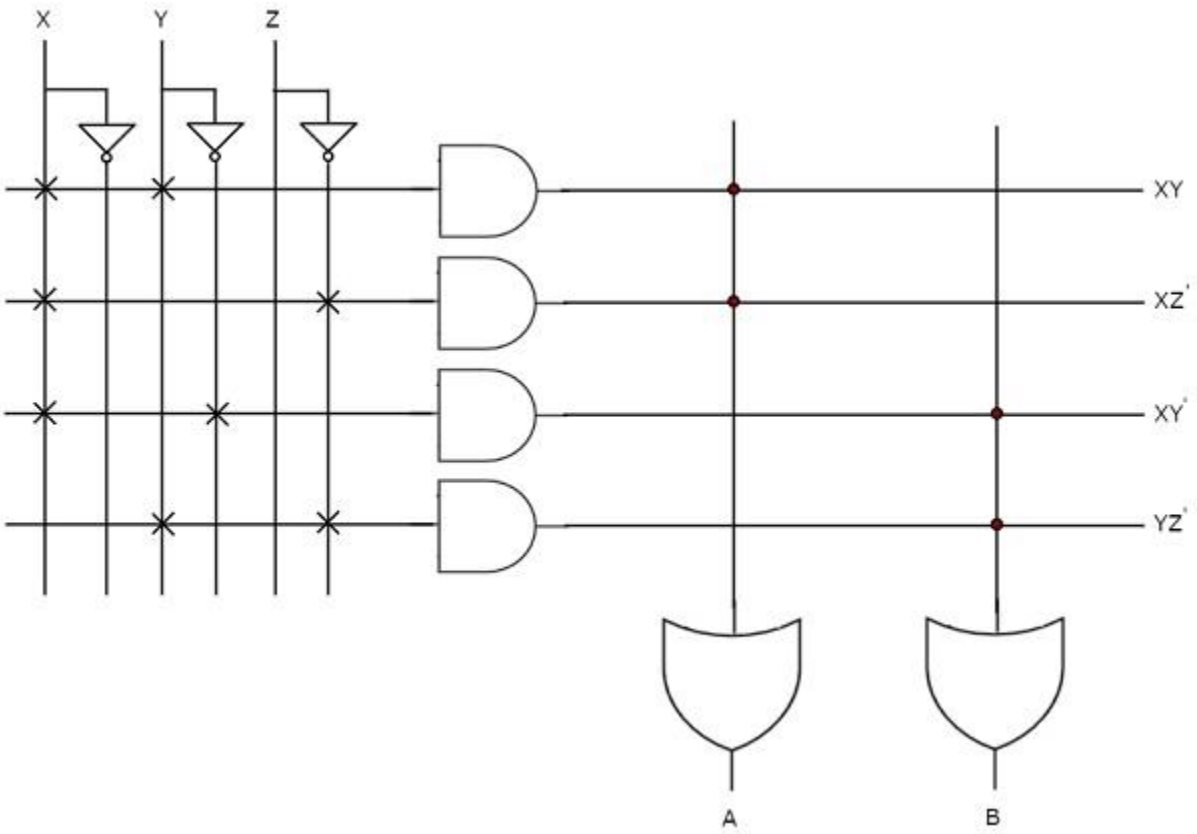
$$A=XY+XZ'$$

$$A=XY'+YZ'$$

Answer:

The given two functions are in sum of products form. There are two product terms present in each Boolean function. So, we require four programmable AND gates & two fixed OR gates for producing those two functions. The corresponding PAL is shown in the following figure.

DIVYA SATHI B
Assistant Professor
ECE Department



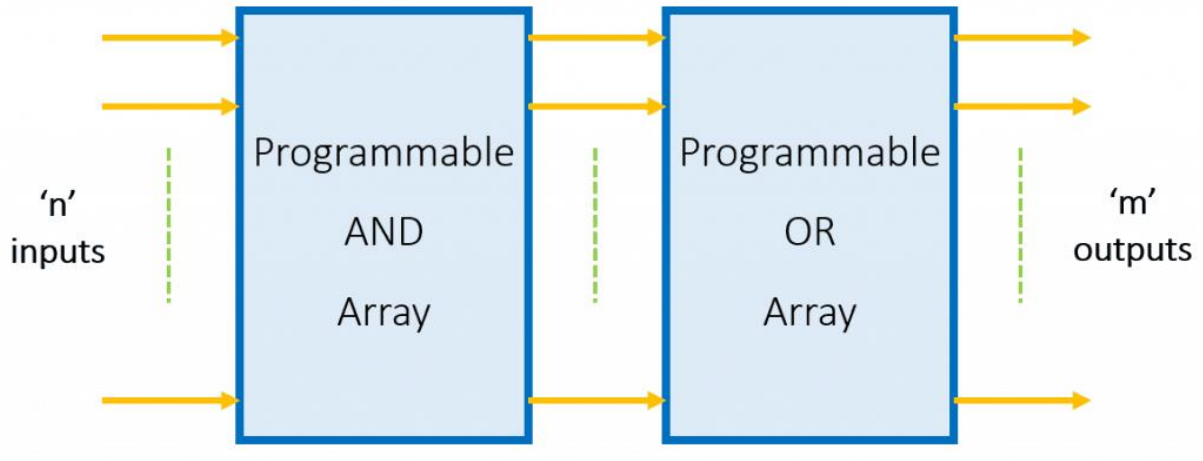
The programmable AND gates have the access of both normal and complemented inputs of variables. In the above figure, the inputs X, X′, Y, Y′, Z & Z′, are available at the inputs of each AND gate. So, program only the required literals in order to generate one product term by each AND gate. The symbol ‘X’ is used for programmable connections.

Here, the inputs of OR gates are of fixed type. So, the necessary product terms are connected to inputs of each OR gate. So that the OR gates produce the respective Boolean functions. The symbol ‘.’ is used for fixed connections.

DIVYA SATHI B
Assistant Professor
ECE Department

PROGRAMMABLE LOGIC ARRAY (PLA):

- The Programmable Logic Array is a PLD that has both sections of the AND and OR Arrays as programmable, i.e. there is a Programmable AND Array and Programmable OR Array as well.
- We call these sections as the AND-plane and the OR-plane.



Block Diagram of PLA

- Here, the inputs of AND gates are programmable. That means each AND gate has both normal and complemented inputs of variables. So, based on the requirement, we can program any of those inputs. So, we can generate only the required product terms by using these AND gates.

- Here, the inputs of OR gates are also programmable. So, we can program any number of required product terms, since all the outputs of AND gates are applied as inputs to each OR gate. Therefore, the outputs of PAL will be in the form of sum of products form.

Example

Let us implement the following Boolean functions using PLA.

$$A=XY+XZ'$$

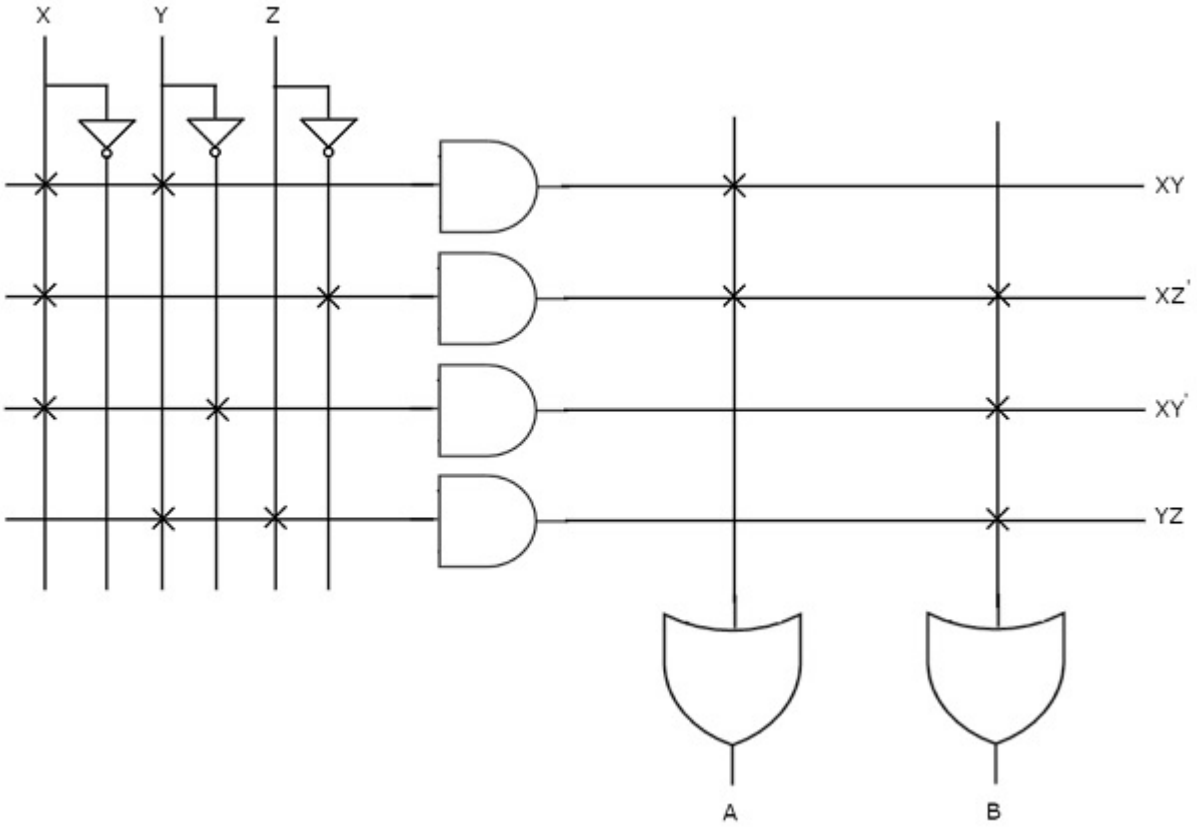
$$B=XY'+YZ+XZ'$$

Answer:

The given two functions are in sum of products form. The number of product terms present in the given Boolean functions A & B are two and three respectively. One product term, Z′X is common in each function.

So, we require four programmable AND gates & two programmable OR gates for producing those two functions. The corresponding PLA is shown in the following figure.

DIVYA SATHI B
Assistant Professor
ECE Department



The **programmable AND gates** have the access of both normal and complemented inputs of variables. In the above figure, the inputs X, X′X′, Y, Y′Y′, Z & Z′Z′, are available at the inputs of each AND gate. So, program only the required literals in order to generate one product term by each AND gate.

All these product terms are available at the inputs of each **programmable OR gate**. But, only program the required product terms in order to produce the respective Boolean functions by each OR gate. The symbol 'X' is used for programmable connections.

Applications:

- PLA is used to provide control over datapath.
- PLA is used as a counter.
- PLA is used as a decoders.
- PLA is used as a BUS interface in programmed I/O.

DIVYA SATHI B
Assistant Professor
ECE Department

COMPARISON AMONG PROM, PLA AND PAL:

S.NO	PROM	PLA	PAL
1.	**AND array** is fixed and **OR array** is programmable.	**Both AND** and **OR arrays** are programmable.	**OR array** is fixed and **AND array** is programmable.
2.	Cheaper and simple to use.	Costliest and more complex than PLAs and PROMs.	Cheaper and simpler.
3.	All minterms are decoded.	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
4.	Only Boolean functions in standard SOP form can be implemented using PROM.	Any Boolean function in SOP form can be implemented using PLA.	Any Boolean function in SOP form can be implemented using PAL.

DIVYA SATHI B
Assistant Professor
ECE Department